INTERNATIONAL TELECOMMUNICATION UNION

CCITT

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

BLUE BOOK

VOLUME VIII – FASCICLE VIII.1

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

SERIES V RECOMMENDATIONS

IXTH PLENARY ASSEMBLY
MELBOURNE, 14-25 NOVEMBER 1988

Geneva 1989

COVERING NOTE

GENERAL SECRETARIAT INTERNATIONAL TELECOMMUNICATION UNION

Subject : ERRATA SHEET FOR BLUE BOOK VERSION
RECOMMENDATION V.42

FASCICLE VIII.1

IXth PLENARY ASSEMBLY OF THE CCITT
MELBOURNE, 1988

Geneva, August 1990

Following the publication of Volume VIII, Fascicle VIII.1 of the *Blue Book*, technical experts in Study Group XVII discovered a number of editorial discrepancies in the text of Recommendation V.42. Some of these would lead to improper implementation if the text were precisely followed. The technical experts have developed and submitted to the CCITT a comprehensive list of the necessary corrections. While these will be reflected in the published text at some future date, printing deadlines did not permit their inclusion in the present version. The reader is kindly requested to take note of the errata noted below while considering the content of Recommendation V.42 (only the technically significant corrections are noted in this document).

Table 8/V.42 (page 317): Within the Supervisory format, second line, change " RR" (above " Receive not Ready") to " RNR" in two places (concerns F/E versions only).

Figure 9/V.42: Decrease all octet numbers by 1 (in the table and throughout the text of the notes).

Section 8.4.3.2 (page 323): In the last paragraph (bottom of page), change the words " and stop timer T401" to " and start timer T401" .

Section 8.4.6, Note 2 (page 326): All of the text beginning with Note 2 and continuing to the heading for § 8.4.7 is part of Note 2 and should be properly indented.

Section 8.5.5 (page 329): Replace the second paragraph with " Upon occurrence of a frame-rejection condition, the error-correcting entity shall initiate re-establishment (see § 8.4.9.2) while an error-corrected condition is established. At other times, the frame causing the condition shall be discarded.

(The following corrections concern English version only.)

Section 8.10.(page 332): Change " T410" to " T401" .

Section A.6.6.1.3 (page 353): Change " data-sequence phase" to " data-sequence space" .

Section A.7.1.5.6 (page 358): Change " all known parameters" to " all unknown parameters" .

Section A.7.2.4 (page 358): In the heading, change " Executive" to " Excessive" .

Section A.7.3 (page 358): In the second paragraph, change " transfer data" to " transfer user data" .

Section A.7.3.5 (page 360): In the first paragraph, change " have been acknowledged" to " have not been acknowledged" . In the last paragraph, change " any unacknowledged LT frames" to " any acknowledged LT frames" .

Section A.7.4.5 (page 361): In the heading, change " LA" to " LNA" .

Section A.7.5.1 (page 362): In the list of definition of terms in the formula, change " L_r" to " L_f" .

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CONTENTS OF THE CCITT BOOK
APPLICABLE AFTER THE NINTH PLENARY ASSEMBLY (1988)

BLUE BOOK

FASCICLE III.6 – Line transmission of non-telephone signals. Transmission of sound-programme and television signals. Series H and J Recommendations (Study Group XV).

FASCICLE III.7 – Integrated Services Digital Network (ISDN) – General structure and service capabilities. Recommendations I.110-I.257 (Study Group XVIII).

FASCICLE III.8 – Integrated Services Digital Network (ISDN) – Overall network aspects and functions, ISDN user-network interfaces. Recommendations I.310-I.470 (Study Group XVIII).

FASCICLE III.9 – Integrated Services Digital Network (ISDN) – Internetwork interfaces and maintenance principles. Recommendations I.500-I.605 (Study Group XVIII).

Volume IV

FASCICLE IV.1 – General maintenance principles: maintenance of international transmission systems and telephone circuits. Recommendations M.10-M.782 (Study Group IV).

FASCICLE IV.2 – Maintenance of international telegraph, phototelegraph and leased circuits. Maintenance of the international public telephone network. Maintenance of maritime satellite and data transmission systems. Recommendations M.800-M.1375 (Study Group IV).

FASCICLE IV.3 – Maintenance of international sound-programme and television transmission circuits. Series N Recommendations (Study Group IV).

FASCICLE IV.4 – Specifications for measuring equipment. Series O Recommendations (Study Group IV).

Volume V – Telephone transmission quality. Series P Recommendations (Study Group XII).

Volume VI

FASCICLE VI.1 – General Recommendations on telephone switching and signalling. Functions and information flows for services in the ISDN. Supplements. Recommendations Q.1-Q.118 *bis* (Study Group XI).

FASCICLE VI.2 – Specifications of Signalling Systems Nos. 4 and 5. Recommendations Q.120-Q.180 (Study Group XI).

FASCICLE VI.3 – Specifications of Signalling System No. 6. Recommendations Q.251-Q.300 (Study Group XI).

FASCICLE VI.4 – Specifications of Signalling Systems R1 and R2. Recommendations Q.310-Q.490 (Study Group XI).

FASCICLE VI.5 – Digital local, transit, combined and international exchanges in integrated digital networks and mixed analogue-digital networks. Supplements. Recommendations Q.500-Q.554 (Study Group XI).

FASCICLE VI.6 – Interworking of signalling systems. Recommendations Q.601-Q.699 (Study Group XI).

FASCICLE VI.7 – Specifications of Signalling System No. 7. Recommendations Q.700-Q.716 (Study Group XI).

FASCICLE VI.8 – Specifications of Signalling System No. 7. Recommendations Q.721-Q.766 (Study Group XI).

FASCICLE VI.9 – Specifications of Signalling System No. 7. Recommendations Q.771-Q.795 (Study Group XI).

FASCICLE VI.10 – Digital subscriber signalling system No. 1 (DSS 1), data link layer. Recommendations Q.920-Q.921 (Study Group XI).

FASCICLE VI.11 – Digital subscriber signalling system No. 1 (DSS 1), network layer, user-network management. Recommendations Q.930-Q.940 (Study Group XI).

FASCICLE VI.12 – Public land mobile network. Interworking with ISDN and PSTN. Recommendations Q.1000-Q.1032 (Study Group XI).

FASCICLE VI.13 – Public land mobile network. Mobile application part and interfaces. Recommendations Q.1051-Q.1063 (Study Group XI).

FASCICLE VI.14 – Interworking with satellite mobile systems. Recommendations Q.1100-Q.1152 (Study Group XI).

Volume VII

FASCICLE VII.1 – Telegraph transmission. Series R Recommendations. Telegraph services terminal equipment. Series S Recommendations (Study Group IX).

FASCICLE VII.2 – Telegraph switching. Series U Recommendations (Study Group IX).

FASCICLE VII.3 – Terminal equipment and protocols for telematic services. Recommendations T.0-T.63 (Study Group VIII).

FASCICLE VII.4 – Conformance testing procedures for the Teletex Recommendations. Recommendation T.64 (Study Group VIII).

FASCICLE VII.5 – Terminal equipment and protocols for telematic services. Recommendations T.65-T.101, T.150-T.390 (Study Group VIII).

FASCICLE VII.6 – Terminal equipment and protocols for telematic services. Recommendations T.400-T.418 (Study Group VIII).

FASCICLE VII.7 – Terminal equipment and protocols for telematic services. Recommendations T.431-T.564 (Study Group VIII).

Volume VIII

FASCICLE VIII.1 – Data communication over the telephone network. Series V Recommendations (Study Group XVII).

FASCICLE VIII.2 – Data communication networks: services and facilities, interfaces. Recommendations X.1-X.32 (Study Group VII).

FASCICLE VIII.3 – Data communication networks: transmission, signalling and switching, network aspects, maintenance and administrative arrangements. Recommendations X.40-X.181 (Study Group VII).

FASCICLE VIII.4 – Data communication networks: Open Systems Interconnection (OSI) – Model and notation, service definition. Recommendations X.200-X.219 (Study Group VII).

FASCICLE VIII.5 – Data communication networks: Open Systems Interconnection (OSI) – Protocol specifications, conformance testing. Recommendations X.220-X.290 (Study Group VII).

FASCICLE VIII.6 – Data communication networks: interworking between networks, mobile data transmission systems, internetwork management. Recommendations X.300-X.370 (Study Group VII).

FASCICLE VIII.7 – Data communication networks: message handling systems. Recommendations X.400-X.420 (Study Group VII).

FASCICLE VIII.8 – Data communication networks: directory. Recommendations X.500-X.521 (Study Group VII).

Volume IX – Protection against interference. Series K Recommendations (Study Group V). Construction, installation and protection of cable and other elements of outside plant. Series L Recommendations (Study Group VI).

Volume X

FASCICLE X.1 – Functional Specification and Description Language (SDL). Criteria for using Formal Description Techniques (FDTs). Recommendation Z.100 and Annexes A, B, C and E, Recommendation Z.110 (Study Group X).

FASCICLE X.2 – Annex D to Recommendation Z.100: SDL user guidelines (Study Group X).

FASCICLE X.3 – Annex F.1 to Recommendation Z.100: SDL formal definition. Introduction (Study Group X).

FASCICLE X.4 – Annex F.2 to Recommendation Z.100: SDL formal definition. Static semantics (Study Group X).

FASCICLE X.5 – Annex F.3 to Recommendation Z.100: SDL formal definition. Dynamic semantics (Study Group X).

FASCICLE X.6 – CCITT High Level Language (CHILL). Recommendation Z.200 (Study Group X).

FASCICLE X.7 – Man-Machine Language (MML). Recommendations Z.301-Z.341 (Study Group X).

CONTENTS OF FASCICLE VIII.1 OF THE BLUE BOOK

Series V Recommendations

Data communication over the telephone network

1 The Questions entrusted to each Study Group for the Study Period 1989-1992 can be found in Contribution No. 1 to that Study Group.

2 In this Volume, the expression "Administration" is used for shortness to indicate both a telecommunication Administration and a recognized private operating agency.

3 The status of annexes and appendices attached to the Series V Recommendations should be interpreted as follows:

- an *annex* to a Recommendation forms an integral part of the Recommendation;
- an *appendix* to a Recommendation does not form part of the Recommendation and only provides some complementary explanation or information specific to that Recommendation.

FASCICLE VIII.1

Series V Recommendations

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

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PRINCIPLES GOVERNING THE COLLABORATION BETWEEN THE CCITT AND OTHER INTERNATIONAL ORGANIZATIONS IN THE STUDY OF DATA COMMUNICATIONS

Recommendation A.20 published in Volume I is reproduced below for the convenience of the reader of the Series V Recommendations.

Recommendation A.20

COLLABORATION WITH OTHER INTERNATIONAL ORGANIZATIONS OVER DATA TRANSMISSION

(Geneva, 1964; amended at Mar del Plata, 1968, and at Geneva, 1972, 1976 and 1980; Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that, according to Article 1 of the agreement between the United Nations and the International Telecommunication Union, the United Nations recognizes the International Telecommunication Union as the specialized agency responsible for taking such action as may be appropriate under its basic instrument for the accomplishment of the purposes set forth therein;

(b) that Article 4 of the International Telecommunication Convention (Nairobi, 1982) states that the purposes of the Union are:

"a) to maintain and extend international cooperation between all Members of the Union for the improvement and rational use of telecommunications of all kinds, as well as to promote and to offer technical assistance to developing countries in the field of telecommunications;

b) to promote the development of technical facilities and their most efficient operation with a view to improving the efficiency of telecommunication services, increasing their usefulness and making them, so far as possible, generally available to the public;

c) to harmonize the actions of nations in the attainment of those ends;"

(c) that Article 40 of the Convention states that, in furtherance of complete international coordination on matters affecting telecommunication, the Union shall cooperate with international organizations having related interests and activities;

(d) that in the study of data transmission the CCITT has to collaborate with the organizations dealing with data processing and office equipment and particularly the International Organization for Standardization (ISO) and the International Electrotechnical Commission (IEC);

(e) that this collaboration has to be organized in a manner that will avoid duplication of work and decisions that would be contrary to the principles set out above;

unanimously declares the view

that international standards for data transmission should be established with the following considerations in mind:

(1) Clearly it will be the responsibility of the CCITT to lay down standards for *transmission channels*, i.e. aspects of data transmission which require a knowledge of telecommunication networks or affect performance of these networks.

(2) The standardization of signal conversion terminal equipment (modems) is the province of the CCITT; the standardization of the junction (interface) between modem and the data terminal equipment is a matter of agreement between the CCITT and the ISO or the IEC.

(3) Devices designed to detect and (or) correct errors must take account of:

- the error rate tolerable to the user;
- the line transmission conditions;
- the code, which has to meet the exigencies of the data alphabet and the requirements of error control (this must be such as to give an output satisfactory to the user) together with the requisite signalling (synchronism, repetition signals, etc.).

Standardization here may not come wholly within the CCITT's province, but the CCITT has very considerable interests at stake.

(4) The alphabet (as defined in Fascicle X.1 – Terms and Definitions) is a "table of correspondence between an agreed set of characters and the signals which represent them".

The CCITT and the ISO reached agreement on an alphabet for general (but not exclusive) use for data and message transmission and have standardized a common alphabet which is known as International Alphabet No. 5 (CCITT Recommendation T.50 and ISO Standard No. 646-1983; ISO 7-bit coded character set for information interchange).

Complementary study of some control characters of the alphabet should be effected cooperatively.

(5) Coding (as defined in Fascicle X.1 – Terms and Definitions) is "a system of rules and conventions according to which the telegraph signals forming a message or the data signals forming a block should be formed, transmitted, received and processed". Hence, it consists of a transformation of the format of the signals in the alphabet for taking account of synchronous methods, and introduction of redundancy in accordance with the error control system. This is not a field in which the CCITT alone may be able to decide; however, no decision should be taken without reference to the Committee, because of the possible restrictions which transmission and switching peculiarities may impose on coding.

When the general switched network is used (telephone or telex) and when the error control devices are subject to restrictions (switching signals – reserved sequences), it is the CCITT which is in fact responsible for any necessary standardization in conjunction with other bodies.

(6) The limits to be observed for transmission performance on the transmission path (modem included) fall within the competence of the CCITT; the limits for the transmission performance of the sending equipment and the margin of terminal data equipment (depending on the terminal apparatus and the transmission path limits) should be fixed by agreement between the ISO and the CCITT.

(7) In all instances, the CCITT alone can lay down manual and automatic operating procedures for the setting-up, holding and clearing of calls for data communications when the general switched networks are used, including type and form of signals to be interchanged at the interface between data terminal equipment and data circuit terminating equipment.

(8) When a public data network is involved, the CCITT has the responsibility to provide the Recommendations which apply. Where these Recommendations have an impact on the basic design and features of data processing systems and office equipment [normally the Data Terminal Equipment (DTE)], they shall be the subject of consultation between CCITT and ISO and in some cases a mutual agreement may be desirable. Likewise when the ISO is developing or changing standards that may affect compatibility with the public data network there shall be consultation with the CCITT.

SECTION 1

GENERAL

Recommendation V.1

EQUIVALENCE BETWEEN BINARY NOTATION SYMBOLS AND THE SIGNIFICANT CONDITIONS OF A TWO-CONDITION CODE

(New Delhi, 1960; amended at Geneva, 1964 and 1972)

Binary numbering expresses numbers by means of two digits normally represented by the symbols 0 and 1. Transmission channels are especially well suited to the transmission of signals by a modulation having two significant conditions (two-condition modulation). These two significant conditions are sometimes called "space" and "mark" or "start" and "stop", or they may be called condition A or condition Z [1].

It is very useful to make the two conditions of a two-condition modulation correspond to the binary digits 0 and 1. Such equivalence will facilitate the transmission of numbers resulting from binary calculation, the conversion of codes for binary numbers and of codes for decimal numbers, maintenance operations and relations between transmission personnel and the personnel in charge of data-processing machines.

At first sight, it does not seem to matter whether the symbol 0 corresponds in transmission to condition A or condition Z, the symbol 1 then corresponding to condition Z or condition A or vice versa.

In telegraphy, however, when a telegraphic communication is set up and the sending of signals is stopped (called the idle condition of the line), the signal sent over the line consists of condition Z throughout the suspension of transmission.

It is logical (and for certain VF telegraph systems also essential) to use the same rule in data transmission. During the "idle periods" of transmission, condition Z should be applied to the circuit input.

Data transmission on a circuit is often controlled by perforated tape. On perforated tapes used for telegraphy, condition Z is represented by perforation. When binary numbers are represented by means of perforations, it is customary to represent the symbol 1 by a perforation. It is therefore logical to make this symbol 1 correspond to condition Z.

For these reasons, the CCITT

unanimously declares the following view:

1 In transmitting data by two-condition code, in which the digits are formed using binary notation, the symbol 1 of the binary notation will be equivalent to condition Z of the modulation, and the symbol 0 of the binary notation will be equivalent to condition A of the modulation.

2 During periods when there is no signal sent to the input of the circuit, the circuit input condition is condition Z.

3 If perforation is used, one perforation corresponds to one unit interval under condition Z.

4 In accordance with Recommendation R.31, the sending of symbol 1 (condition Z) corresponds to the tone being sent on a channel using amplitude modulation.

5 In accordance with Recommendation R.35, when frequency modulation is used, the sending of symbol 0 corresponds to the higher frequency, while the sending of symbol 1 corresponds to the lower frequency.

6 a) For phase modulation with reference phase:
the symbol 1 corresponds to a phase equal to the reference phase;
the symbol 0 corresponds to a phase opposed to the reference phase.

b) For differential two-phase modulation where the alternative phase changes are 0 degree or 180 degrees:
the symbol 1 corresponds to a phase inversion from the previous element;
the symbol 0 corresponds to a no-phase inversion from the previous element.

7 A summary of equivalence is shown in Table 1/V.1.

TABLE 1/V.1

Summary of equivalence (see Note 1)

	Digit 0 "Start" signal in start-stop code Line available condition in telex switching "Space" element of start-stop code Condition A	Digit 1 "Stop" signal in start-stop code Line idle condition in telex switching (Note 2) "Mark" element of start-stop code Condition Z
Amplitude modulation	Tone-off	Tone-on
Frequency modulation	High frequency	Low frequency
Phase modulation with reference phase	Opposite phase to the reference phase	Reference phase
Differential two-phase modulation where the alternative phase changes are 0 degree or 180 degrees	No phase inversion	Inversion of the phase
Perforations	No perforation	Perforation

Note 1 – The standardization described in this Recommendation is general, whether over telegraph-type circuits or over circuits of the telephone type, making use of electromechanical or electronic devices.

Note 2 – It primarily applies to anisochronous use.

Reference

[1] CCITT Definition: *Position A; position Z*, Vol. X, (Terms and Definitions).

Recommendation V.2 [1]

POWER LEVELS FOR DATA TRANSMISSION OVER TELEPHONE LINES

(New Delhi, 1960; amended at Geneva, 1964 and 1980)

The objectives in specifying data signal levels are as follows:

a) To ensure satisfactory transmission and to permit coordination with devices such as signalling receivers or echo suppressors, the data signal levels on international circuits should be controlled as closely as possible,

b) To ensure correct performance of multichannel carrier systems from the point of view of loading and noise, the mean power of data circuits should not differ much from the conventional value of channel loading (−15 dBm0 for each direction of transmission: see Note below). This conventional value makes allowance for a reasonable proportion P (dependent on the transmission systems and probably less than 50%; the value will have to be specified in subsequent studies) of the channels in a multichannel system being used for nonspeech applications at fixed power levels at about −13 dBm0 for each direction of transmission.

   If the proportion of nonspeech applications (including data) does not exceed the above value P, the mean power of −13 dBm0 for each direction of transmission would be allowable for data transmission also.

   However, assuming that the proportion of nonspeech circuits is appreciably higher than P (due to the development of data transmission) on international carrier systems, a reduction of this power by 2 dB might be reasonable (these values require further study).

   Note – The distribution of long-term mean power among the channels in a multichannel carrier telephone system (conventional mean value of −15 dBm0), probably has a standard deviation in the neighbourhood of 4 dB (see [2]).

c) It is probable that Administrations will wish to fix specific values for the signal power level of data modulators either at the subscriber's line terminals or at the local exchanges. The relation between these values and the power levels on international circuits depends on the particular national transmission plan; in any case, a wide range of losses among the possible connections between the subscriber and the input to international circuits must be expected.

d) Considerations a) to c) suggest that specification of the maximum data signal level only is not the most useful form. One alternative proposal would be to specify the nominal power at the input to the international circuit. The nominal power would be the statistically estimated mean power obtained from measurement on many data transmission circuits.

For these reasons, the CCITT

unanimously declares the following view:

1 Data transmission over leased telephone circuits (private wires) set up on carrier systems

1.1 The maximum power output of the subscriber's equipment into the line shall not exceed 1 mW at any frequency.

1.2 For systems transmitting tones continuously, e.g., frequency-modulation systems, the maximum power level at the zero relative level point shall be −13 dBm0. When transmission of data is discontinued for any appreciable time, the power level should preferably be reduced to −20 dBm0 or lower.

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[1] Recommendation V.2 corresponds to Recommendation H.15 [1].

1.3 For systems not transmitting tones continuously, e.g., amplitude-modulation systems, the signal characteristics should meet all of the following requirements:

i) The maximum value of the 1-minute mean power shall not exceed −13 dBm0.

ii) Provisionally, the maximum value of the instantaneous power shall not exceed a level corresponding to that of a 0 dBm0 sine wave signal. This limit should be confirmed or amended after further study.

iii) Provisionally, the maximum signal power determined for a 10-Hz bandwidth centred at any frequency shall not exceed −10 dBm0. This limit should be confirmed or amended after further study.

Note 1 – It is estimated that the proportion of international circuits which are carrying data transmissions is approximately 20%. If the proportion should reach a high level (approximately 50% or even less in the case of high-usage systems), the limits now proposed would need to be reconsidered.

Note 2 – Supplement No. 16 [3] of the Yellow Book, Volume III, gives information on the out-of-band power of signals applied to leased telephone-type circuits.

2 Data transmission over the switched telephone system

2.1 The maximum power output of the subscriber's equipment into the line shall not exceed 1 mW at any frequency.

2.2 For systems transmitting tones continuously, such as frequency- or phase-modulation systems, the power level of the subscriber's equipment should be fixed at the time of installation to allow for loss between his equipment and the point of entry to an international circuit, so that the corresponding nominal level of the signal at the international circuit input shall not exceed −13 dBm0.

2.3 For systems not transmitting tones continously, e.g. amplitude-modulation systems, the signal characteristics should meet all of the following requirements (see also Note 1 to § 1.3):

i) The maximum value of the 1-minute mean power shall not exceed −13 dBm0.

ii) Provisionally, the maximum value of the instantaneous power shall not exceed a level corresponding to that of a 0 dBm0 sine wave signal. This limit should be confirmed or amended after further study.

iii) Provisionally, the maximum signal power determined for a 10 Hz bandwidth centred at any frequency shall not exceed −10 dBm0. This limit should be confirmed or amended after further study.

Note 1 – In practice, it is no easy matter to assess the loss between a subscriber's equipment and the international circuit, so that § 2 of the present Recommendation should be taken as providing general planning guidance.

Note 2 – In switched connections, the loss between subscribers' telephones may be high: 30 to 40 dB. The level of the signals received will then be very low, and these signals may suffer disturbance from the dialling pulses sent over other circuits.

If there is likely to be a heavy demand for international connections for data transmission over the switched network, some Administrations might want to provide special 4-wire subscriber lines. If so, the levels to be used might be those proposed for leased circuits.

References

[1] CCITT Recommendation *Power levels for data transmission over telephone lines*, Vol. III, Rec. H.51.

[2] *Measurement of the load of telephone circuits*, Green Book, Vol. III-2, Supplement No. 5, ITU, Geneva, 1973.

[3] *Out-of-band characteristics of signals applied to leased telephone-type circuits*, Vol. III, Supplement No. 16.

GENERAL STRUCTURE OF SIGNALS OF INTERNATIONAL ALPHABET No. 5 CODE FOR CHARACTER ORIENTED DATA TRANSMISSION OVER PUBLIC TELEPHONE NETWORKS[1)]

(Mar del Plata, 1968; amended at Geneva, 1976 and 1980, and at Melbourne, 1988)

The CCITT,

I. *considering, firstly,*

the agreement between the International Organization for Standardization (ISO) and the CCITT on the main characteristics of a seven-unit alphabet [International Alphabet No. 5 (IA5)] to be used for data transmission and for telecommunications requirements that cannot be met by the existing five-unit International Telegraph Alphabet No. 2 (ITA2);

the interest, both to the users and to the telecommunication services, of an agreement concerning the chronological order of transmission of bits in serial working;

declares the view

that the agreed rank number of the unit in the alphabetical table of combinations should correspond to the chronological order of transmission in serial working on telecommunication circuits;

that, when this rank in the combination represents the order of the bit in binary numbering, the bits should be transmitted in serial working with the low order bit first;

that the numerical meaning corresponding to each information unit considered in isolation is that of the digit:

0 for a unit corresponding to condition A (travail = space), and

1 for a unit corresponding to condition Z (repos = mark),

in accordance with the definitions of these conditions for a two-condition transmission system;

II. *considering, moreover,*

that it is often desirable, in character oriented data transmission, to add an extra "parity" unit to allow for the detection of errors in received signals;

the possibility offered by this addition for the detection of faults in data terminal equipment;

the need to reserve the possibility of making this addition during the transmission itself, after the seven information units proper have been sent;

declares the view

that signals of the International Alphabet No. 5 code for data transmission should, in general, include an additional "parity" unit;

that the rank of this unit and, hence, the chronological order of the transmission in serial working should be the eighth of the combination thus completed;

III. *considering*

that, in start-stop systems working with electromechanical equipment, the margin of such equipment and the reliability of the connection are considerably increased by the use of a stop element corresponding to the duration of two unit intervals of the modulation;

that for transmissions over telephone circuits via modems installed on the user's premises, the latter must be able to use the connections at the highest possible practical rate in characters per second, and that in such a case a single-unit stop element leads to a gain of about 10% as regards this practical rate;

[1)] See Recommendation X.4 [1] for data transmission over public data networks.

that, however, it does not appear that the production of electronic devices capable of working at will with start-stop signals having a stop element equal to one or two unit intervals should lead to costly complications and that such an arrangement can have the advantage of appreciably limiting the error rate without greatly reducing the practical efficiency of the connection;

declares the view

that in start-stop systems using combinations of the seven-unit alphabet normally followed by a parity unit, the first information unit of the transmitted combination should be preceded by a start element corresponding to condition A (space);

that the duration of this start element should be a one-unit interval for the modulation rate under consideration, at transmitter output;

that the combination of seven information units, normally completed by its parity unit, should be followed by a stop element corresponding to condition Z (mark);

that for start-stop systems using the seven-unit code on switched telephone networks, a two-unit stop element should be used with electromechanical data terminal equipments operating at modulation rates up to and including 200 bauds. In other cases, the use of a one-unit stop element is preferable. However, this is subject to a mutual agreement between Administrations concerned;

that similar situations when a one-unit stop element can be used may apply to leased circuits;

that the start-stop receivers should be capable of correctly receiving start-stop signals comprising a single-unit stop element, whose duration will be reduced by a time interval equal to the deviation corresponding to the degree of gross start-stop distortion permitted at receiver input. However, for electromechanical equipment which must use a two-unit stop element (eleven-unit code signal) with a modulation rate of 200 bauds or less, receivers should be capable of correctly receiving signals with a stop element reduced to one unit;

IV. *considering, finally,*

that the direction of the parity unit can only be that of the even parity on the perforated tapes, particularly owing to the possibility of deletion (combination 7/15 of the alphabet) which causes a hole to appear in all tracks;

that, on the other hand, the odd parity is considered essential in the equipment which depends on transitions in the signals to maintain synchronism [in cases where combination 1/6 (SYNC) of the alphabet does not permit of an economical solution];

declares the view

that the parity unit of the signal should correspond to the even parity in links or connections operated on the principle of the start-stop system;

that this parity should be odd on links or connections using end-to-end character oriented synchronous operation;

that arrangements should be made when necessary to reverse the direction of the parity unit at the input and output of the synchronous equipment connected either to apparatus working on the start-stop principle or receiving characters on perforated tape;

that the detection of a character out-of-parity may be represented by:

a) reverse question mark (ʔ) graphic character or a representation of the capital letters SB (see ISO 2047) provided that these letters occupy a single character position on the screen or printer, and could have been entered by a single key stroke, recognizing it may be difficult to achieve a legible "SB" character from some matrix printers or displays where the characters are printed; or

b) a recording of the 1/10 (SUB) character on the tape or other storage medium, where provided

and that, where a SUB character occurs in a received transmission, or is presented to a DTE via a storage medium, e.g. paper tape, then the reaction should be as in a) and b) above.

Reference

[1] CCITT Recommendation *General structure of signals of International Alphabet No. 5 code for character oriented data transmission over public data networks*, Vol. VIII, Rec. X.4.

Recommendation V.5

STANDARDIZATION OF DATA SIGNALLING RATES FOR SYNCHRONOUS DATA TRANSMISSION IN THE GENERAL SWITCHED TELEPHONE NETWORK

(former Recommendation V.22, Geneva, 1964; amended at Mar del Plata, 1968, at Geneva, 1972 and 1976, at Malaga-Torremolinos, 1984 and at Melbourne, 1988)

1 Data transmission by international communications carried on the general switched telephone network using a synchronous transmission procedure will be done with a specific mode of modulation, two- or multi-condition, and serial transmission (see Note 1). For synchronous data transmission on leased telephone-type circuits see Recommendation V.6.

2 The data signalling rates for synchronous transmission in the general switched telephone network will be:

600, 1200, 2400, 4800 and 9600 bits (see Note 2).

The users will choose among these rates, in accordance with their needs and the facilities afforded by the connection.

3 Data signalling rates should in no case deviate from the nominal value by more than ± 0.01%.

Note 1 – The application of parallel data transmission is a subject of other Recommendations.

Note 2 – Modems for use in the general switched telephone network at these data signalling rates; see Recommendations V.23, V.26 *bis* and V.27 *ter* respectively for a half-duplex mode of operation, and V.22, V.22 *bis*, V.26 *ter* and V.32, respectively, for a duplex-mode of operation.

Note 3 – For asynchronous data transmission at 300 bit/s, see Recommendation V.21.

Recommendation V.6

STANDARDIZATION OF DATA SIGNALLING RATES FOR SYNCHRONOUS DATA TRANSMISSION ON LEASED TELEPHONE-TYPE CIRCUITS

(former Recommendation V.22 bis, Geneva, 1972; amended at Geneva, 1976, at Malaga-Torremolinos, 1984 and at Melbourne, 1988)

1 Data transmission by international communications carried on leased telephone-type circuits (either normal quality or special quality circuits) using a synchronous transmission procedure will be done with a specific mode of modulation, two- or multi-condition, and serial transmission (see Note 1). For synchronous data transmission in the general switched telephone network see Recommendation V.5.

2 It is recommended that for synchronous transmission the data signalling rates should be divided into two distinct classes to be known as "preferred" and "supplementary", both of which are included in the "permitted" data signalling rates.

a) *Preferred range of data signalling rates (bits per second)*

600 (see Note 2)	4 800 (see Note 2)
1 200 (see Note 2)	9 600 (see Note 2)
2 400 (see Note 2)	14 400 (see Note 2)

b) *Supplementary range of data signalling rates (bits per second)*

3 000 (see Note 3)	7 200 (see Note 2)
6 000 (see Note 3)	12 000 (see Note 3)

c) *Permitted range of data signalling rates (bits per second)*

The range is defined as 600 times "N" bits per second where $1 \leqslant N \leqslant 24$; N: a positive integer.

In determining the permitted range, the CCITT has in mind the need to restrict the number of data signalling rates (and hence modem design required), yet at the same time to allow the best use to be made of technical progress in both modem development and improvement in the telephone plant. It is considered that a geometric progression in standard rates provides the most satisfactory basis of development.

3 Data signalling rates should in no case deviate from the nominal value by more than ± 0.01%.

Note 1 – The application of parallel data transmission is a subject of other Recommendations.

Note 2 – Modems for use on leased telephone-type circuits at these data signalling rates; see Recommendations V.22, V.22 *bis*, V.23, V.26, V.26 *ter*, V.27, V.27 *bis*, V.29, V.32 and V.33.

Note 3 – It is recognized that there is a usage of these data signalling rates for the connection of DTEs to circuit switched public data networks. Addition of other data signalling rates for this purpose is under consideration.

Note 4 – Modems for use on leased telephone-type circuits at these signalling rates are under study.

Recommendation V.7

DEFINITIONS OF TERMS CONCERNING DATA COMMUNICATION OVER THE TELEPHONE NETWORK

(Geneva, 1980; amended at Malaga-Torremolinos, 1984 and at Melbourne, 1988)

Note – This Recommendation contains only new and amended definitions of terms concerning data communication over the telephone network which were elaborated by Study Group XVII since 1977 and approved by the VIIth and VIIIth Plenary Assemblies of the CCITT.

It should be noted that there exist a large number of relevant definitions in force which have been published in the *List of definitions of essential telecommunication terms*, Part I (including its two Supplements), *Green Book*, Volume VIII and *Orange Book*, Volume VIII.2.

1 effective data transfer rate

F: débit effectif du transfert des données

S: velocidad real de transferencia de datos

The average number of bits, characters, or blocks per unit time transferred from a data source to a data sink and accepted as valid. It is expressed in bits, characters, or blocks per second, minute, or hour.

2 error control

F: contrôle des erreurs

S: control de errores (protección contra errores)

That part of a protocol controlling the detection and possibly the correction of transmission errors.

3 data concentrator

F: concentrateur de données

S: concentrador de datos

Equipment that permits a common transmission medium to serve more *data sources* than there are data channels currently available within the transmission medium.

4 simple multipoint circuit

F: circuit multipoint simple

S: circuito multipunto simple

A multipoint circuit that does not contain more than two DCEs in series and that provides for centralized multipoint operation.

5 inband signalling

F: signalisation dans la bande

S: señalización dentro de banda

The exchange of control signals between interconnected DCEs using the DCE line signal band with which data in the forward channel are transmitted. The transmission of DTE data, if any, is disrupted.

6 out-of-band signalling

F: signalisation hors bande

S: señalización fuera de banda

The exchange of control signals between interconnected DCEs using signals other than those for the transmission of data in the forward channel. The transmission of DTE data is not disrupted.

7 coded inband signalling

F: signalisation dans la bande avec codage

S: señalización codificada dentro de banda

Inband signalling by which control signals are exchanged via data in the forward channel.

8 half-duplex operation

F: exploitation en semi-duplex

S: explotación (o funcionamiento) semidúplex

The exchange of data in either direction, one direction at a time.

9 interface rate

F: débit à l'interface

S: velocidad de interfaz

The transfer rate of the bit stream found on the physical interchange circuits.

10 information rate

F: débit d'information

S: velocidad de información

The transfer of information bits (the equivalent of the bit rate of circuit 103 or 104 on a V.24 interface).

11 control signalling rate

F: débit de la signalisation de commande

S: velocidad de señalización de control

The transfer rate of the encoded and multiplexed control signalling (the equivalent of V.24 and V.25 interchange circuits, except the data and timing circuits, insofar as required for an application, with the possibility of adding other signalling).

12 parallel automatic calling

F: appel automatique en parallèle

S: llamada automática paralelo; llamada automática en modo paralelo

A procedure by which a DTE, by use of the 200 series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in parallel form on interchange circuits 206 to 209.

13 serial automatic calling

F: appel automatique en série

S: llamada automática serie; llamada automática en modo serie

A procedure by which a DTE, by use of the 100 series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission from DTE to DCE, of each digit to be dialled, is achieved in serial form on interchange circuit 103.

14 start-stop transmission

F: transmission arythmique

S: transmisión arrítmica

A form of anisochronous transmission in which each group of contiguous data units is preceded by a start signal and is terminated by a stop signal.

SECTION 2

INTERFACES AND VOICE-BAND MODEMS

Recommendation V.10

ELECTRICAL CHARACTERISTICS FOR UNBALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR GENERAL USE WITH INTEGRATED CIRCUIT EQUIPMENT IN THE FIELD OF DATA COMMUNICATIONS [1]

(Geneva, 1976; amended at Geneva, 1980 and at Melbourne, 1988)

1 Introduction

This Recommendation deals with the electrical characteristics of the generator, receiver and interconnecting leads of an unbalanced interchange circuit employing a differential receiver.

In the context of this Recommendation an unbalanced interchange circuit is defined as consisting of an unbalanced generator connected to a receiver by an interconnecting lead and a common return lead.

Annexes and Appendices are provided to give guidance on a number of application aspects as follows:

Annex A Compatibility with other interfaces

Annex B Considerations for coaxial cable applications – V.10 COAXIAL

Appendix I Waveshaping

Appendix II Cable guidelines

Note – Generator and load devices meeting the electrical characteristics of this Recommendation need not operate over the entire data signalling rate range specified. They may be designed to operate over narrower ranges to satisfy specific requirements more economically, particularly at lower data signalling rates.

The interconnecting cable is normally not terminated, but the matter of terminating coaxial interconnecting cable is dealt with in Annex B. Where the interchange circuit incorporates the special provisions for coaxial applications with cable termination this shall be referred to as "complying with Recommendation V.10 (COAXIAL)".

Reference measurements are described which may be used to verify certain of the recommended parameters but it is a matter for individual manufacturers to decide what tests are necessary to ensure compliance with the Recommendation.

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[1] This Recommendation is also designated as X.26 in the Series X Recommendations.

2 Field of application

The electrical characteristics specified in this Recommendation apply to interchange circuits operating with data signalling rates up to 100 kbit/s[2)], and are intended to be used primarily in Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE) implemented in integrated circuit technology.

This Recommendation is not intended to apply to equipment implemented in discrete component technology, for which the electrical characteristics covered by Recommendation V.28 are more appropriate.

Typical points of application are illustrated in Figure 1/V.10.

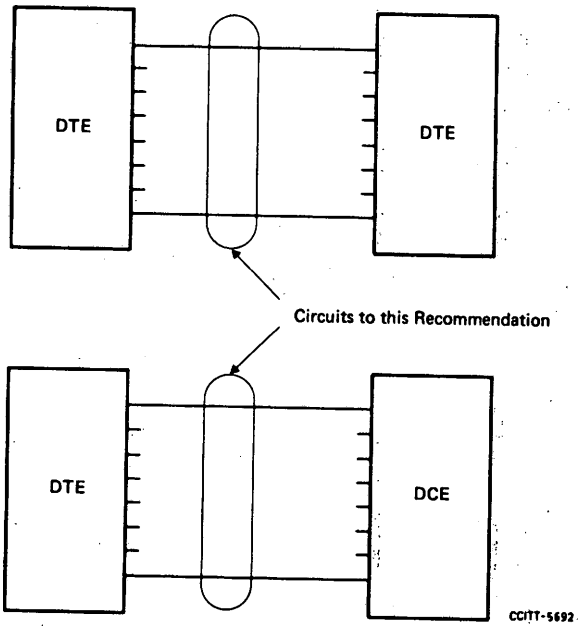


FIGURE 1/V.10

Typical applications of unbalanced interchange circuits

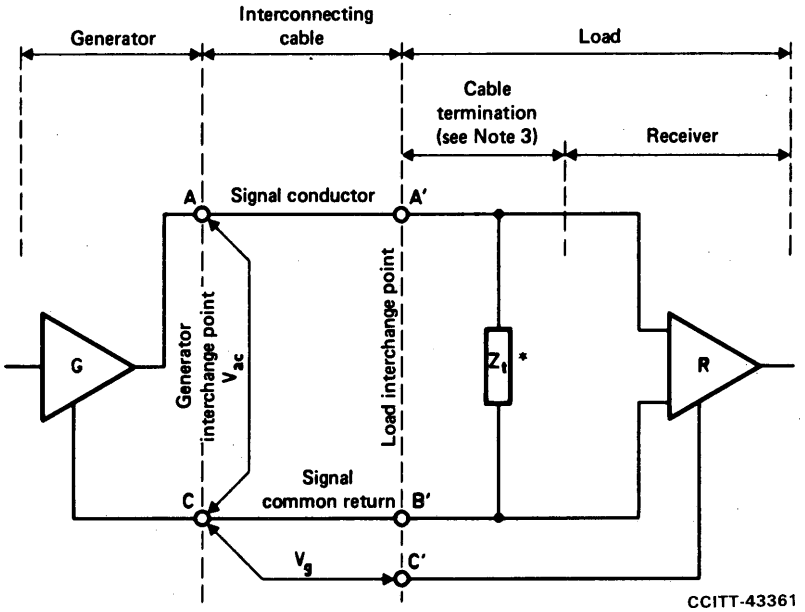
Whilst the unbalanced interchange circuit is primarily intended for use at the lower data signalling rates, its use should be avoided in the following cases:

1) where the interconnecting cable is too long for proper unbalanced circuit operation;
2) where extraneous noise sources make unbalanced circuit operation impossible;
3) where it is necessary to minimize interference with other signals.

Whilst a restriction on maximum cable length is not specified, guidelines are given with respect to conservative operating distance as a function of data signalling rates (see Appendix II).

[2)] Signalling rates above the suggested 100 kbit/s may also be employed, but the maximum suggested operating distances should be shortened accordingly (see Figure II-1/V.10).

3 Symbolic representation of an interchange circuit (Figure 2/V.10)



V_{ac} = generator output voltage
V_g = ground potential difference
A = generator active interchange point
C = generator common return point
A' = load active interchange point
B' = load common return point
C' = receiver zero reference point

* This terminating resistor is only used with "V.10-COAXIAL", see Annex B

Note 1 – Two interchange points are shown. The output characteristics of the generator, excluding any interconnecting cable, are defined at the "generator interchange point". The electrical characteristics to which the receiver must respond are defined at the "load interchange point".

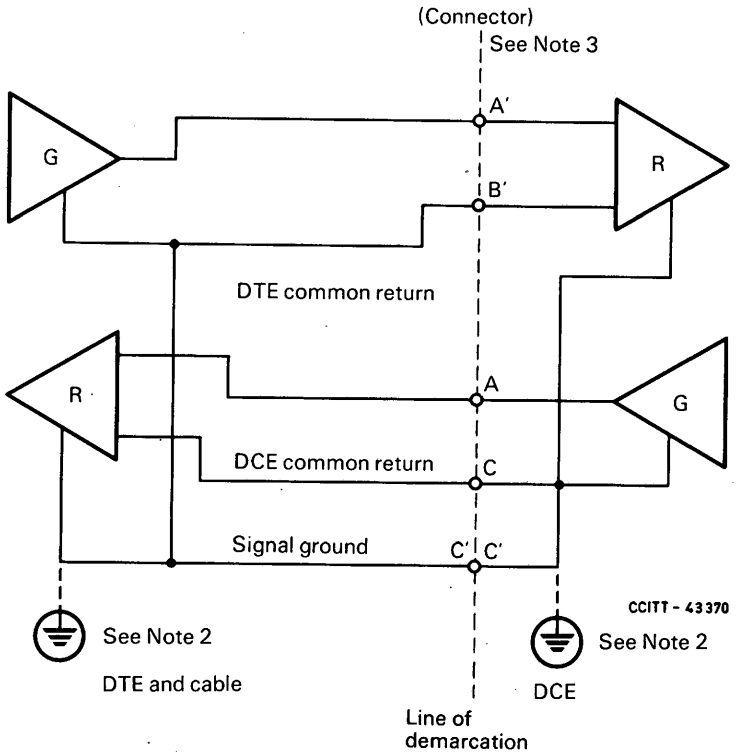
Note 2 – The connection of the signal common return is dealt with in § 10 below. Points C and C′ may be connected to protective ground if required by national regulations.

Note 3 – The interconnecting cable is normally not terminated. The termination of coaxial interconnecting cable is dealt with in Annex B.

FIGURE 2/V.10

Symbolic representation of an unbalanced interchange circuit

For data transmission applications, it is commonly accepted that the interface cabling is provided by the DTE. This introduces the line of demarcation between the DTE plus cable and the DCE. This line is also called the interchange point and physically implemented in the form of a connector. The applications also require interchange circuits in both directions. This leads to an illustration as shown in Figure 3/V.10.



Note 1 – The zero volt reference interchange points C′ may be interconnected via the signal ground conductor.

Note 2 – Signal ground may be further connected to external protective ground if national regulations require.

Note 3 – The type of connector with this electrical characteristic specification depends on the application. ISO specifies, for data transmission over telephone type facilities, a 37-pin connector in ISO 4902.

FIGURE 3/V.10

Practical representation of the interface

4 Generator polarities and receiver significant levels

4.1 *Generator*

The signal conditions for the generator are specified in terms of the voltage between output points A and C shown in Figure 2/V.10.

When the signal condition 0 (space) for data circuits, or ON for control and timing circuits, is transmitted the output point A is positive with respect to point C. When the signal condition 1 (mark) for data circuits, or OFF for control and timing circuits, is transmitted the output point A is negative with respect to point C.

4.2 *Receiver*

The receiver significant levels are shown in Table 1/V.10, where $V_{A'}$ and $V_{B'}$ are respectively the voltage at points A′ and B′ relative to point C′.

TABLE 1/V.10

Receiver significant levels

	$V_{A'} - V_{B'} \leqslant -0.3$ V	$V_{A'} - V_{B'} \geqslant +0.3$ V
Data circuits	1	0
Control and timing circuits	OFF	ON

5 Generator[3)]

5.1 *Output impedance*

The total dynamic output impedance of the generator shall be equal to or less than 50 ohms.

5.2 *Static reference measurements*

The generator characteristics are specified in accordance with measurements illustrated in Figure 4/V.10 and described in §§ 5.2.1 to 5.2.4 below.

5.2.1 *Open circuit measurement* [Figure 4a)/V.10]

The open circuit voltage measurement is made with a 3900-ohm resistor connected between points A and C. In both binary states, the magnitude of the signal voltage (V_0) shall be equal to or greater than 4.0 volts but not greater than 6.0 volts.

5.2.2 *Test termination measurement* [Figure 4b)/V.10]

With a test load of 450 ohms connected between output points A and C, the magnitude of the output voltage (V_t) in both binary states shall be equal to or greater than 0.9 of the magnitude of V_0.

5.2.3 *Short-circuit measurement* [Figure 4c)/V.10]

With the output points A and C short-circuited the current (I_s) flowing through point A in both binary states shall not exceed 150 milliamperes.

5.2.4 *Power-off measurements* [Figure 4d)/V.10]

Under power-off condition, with a voltage ranging between +0.25 volt and −0.25 volt applied between the output point A and point C, the magnitude of the output leakage current (I_x) shall not exceed 100 micro-amperes.

[3)] For test purposes other than specified in this Recommendation (e.g. signal quality measurement), a transmitter test load of 450 ohms may be used.

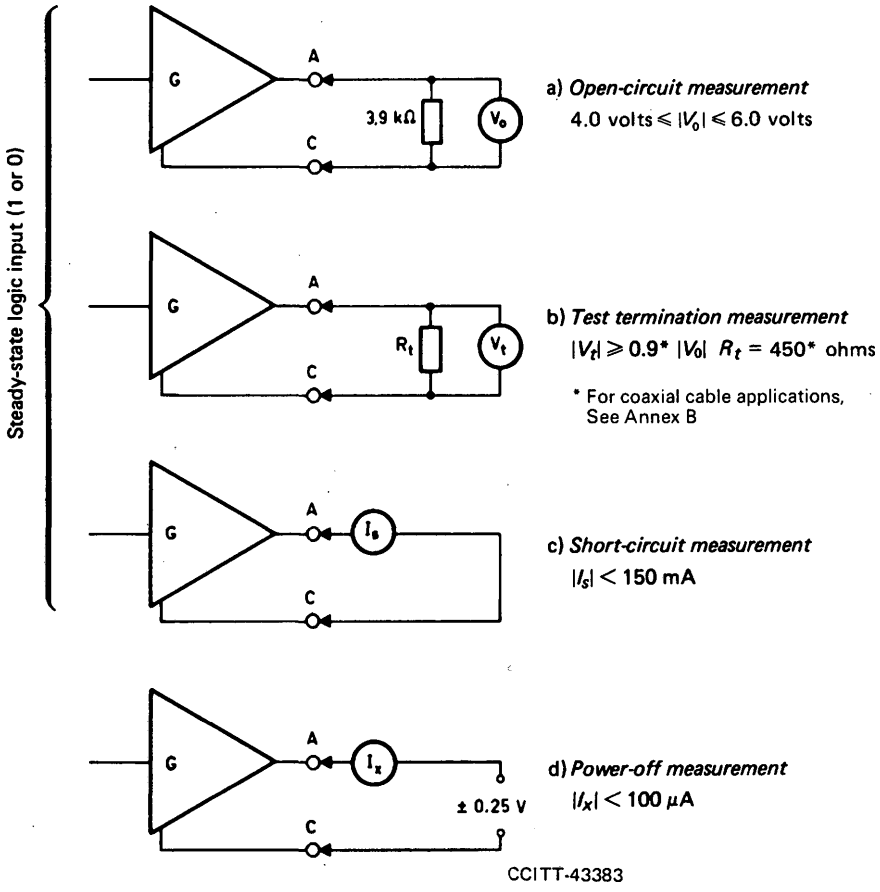


FIGURE 4/V.10

Generator parameter reference measurements

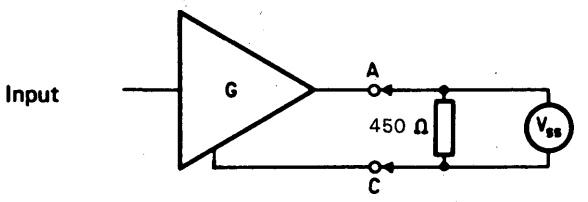
5.3 *Generator output rise-time measurement* (Figure 5/V.10)

5.3.1 *Waveform*

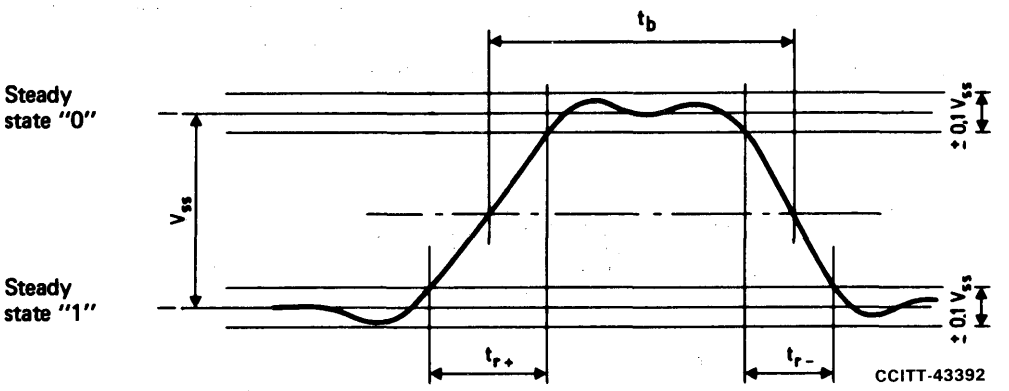
The measurement will be made with a resistor of 450 ohms connected between points A and C. A test signal, with a nominal signal element duration t_b and composed of alternate ones and zeros, shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 of V_{ss}.

5.3.2 *Waveshaping*

Waveshaping of the generator output signal shall be employed to control the level of interference (near-end crosstalk) which may be coupled to adjacent circuits in an interconnection. The rise time (t_r) of the output signal shall be controlled to ensure the signal reaches 0.9 V_{ss} between 0.1 and 0.3 of the duration of the unit interval (t_b) at signalling rates greater than 1 kbit/s, and between 100 and 300 microseconds at signalling rates of 1 kbit/s or less. The method of waveshaping is not specified but examples are given in Appendix I.



V_{ss} = Voltage difference between steady state signal conditions



t_b = nominal duration of the test signal element
$100\ \mu s \leqslant t_r \leqslant 300\ \mu s$ when $t_b \geqslant 1$ ms
$0.1\ t_b \leqslant t_r \leqslant 0.3\ t_b$ when $t_b < 1$ ms

FIGURE 5/V.10

Generator output rise-time measurement

6 Load

6.1 *Characteristics*

The load consists of a receiver (R) as shown in Figure 2/V.10. The electrical characteristics of the receiver are specified in terms of the measurements illustrated in Figures 6/V.10, 7/V.10 and 8/V.10 and described in §§ 6.2, 6.3 and 6.4 below. A circuit meeting these requirements results in a differential receiver having a high input impedance, a small input threshold transition region between −0.3 and +0.3 volts differential, and allowance for an internal bias voltage not to exceed 3 volts in magnitude.

The receiver is electrically identical to that specified for the balanced receiver in Recommendation V.11.

6.2 *Receiver input voltage – current measurements* (Figure 6/V.10)

With the voltage V_{ia} (or V_{ib}) ranging between −10 volts and +10 volts, while V_{ib} (or V_{ia}) is held at 0 volt, the resultant input current I_{ia} (or I_{ib}) shall remain within the shaded range shown in Figure 6/V.10. These measurements apply with the power supply of the receiver in both the power-on and power-off conditions.

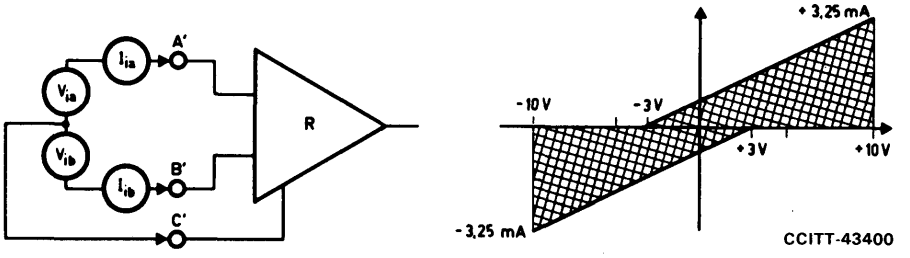
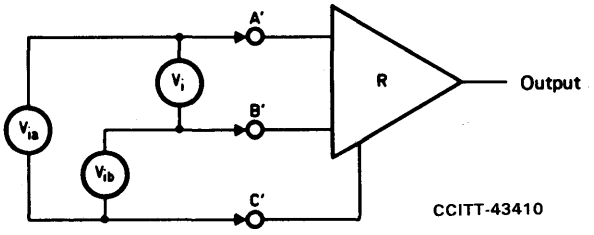


FIGURE 6/V.10

Receiver input voltage-current measurements

6.3 *DC input sensitivity measurements* (Figure 7/V.10)

Over the entire common-mode voltage (V_{cm}) range of +7 volts to −7 volts, the receiver shall not require a differential input voltage (V_i) of more than 300 millivolts to assume correctly the intended binary state. Reversing the polarity of V_i shall cause the receiver to assume the opposite binary state.



Applied voltages		Resulting input voltage	Output binary state	Purpose of measurement
V_{ia}	V_{ib}	V_i		
−12 V	0 V	−12 V	(not specified)	To ensure no damage to receiver inputs
0 V	−12 V	+12 V		
+12 V	0 V	+12 V		
0 V	+12 V	−12 V		
+10 V	+ 4 V	+ 6 V	0	To guarantee correct operation at V_i = 6 V (maintain correct logic state)
+ 4 V	+10 V	− 6 V	1	
−10 V	− 4 V	− 6 V	1	
− 4 V	−10 V	+ 6 V	0	
				300 mV threshold measurement
+0.30 V	0 V	+0.3 V	0	} V_{cm} = 0 V
0 V	+0.30 V	−0.3 V	1	
+7.15 V	+6.85 V	+0.3 V	0	} V_{cm} = +7 V
+6.85 V	+7.15 V	−0.3 V	1	
−7.15 V	−6.85 V	−0.3 V	1	} V_{cm} = −7 V
−6.85 V	−7.15 V	+0.3 V	0	

FIGURE 7/V.10

Receiver input sensitivity measurement

The maximum voltage (signal plus common-mode) present between either receiver input and receiver ground shall not exceed 10 volts nor cause the receiver to malfunction. The receiver shall tolerate a maximum differential voltage of 12 volts applied across its input terminals without being damaged.

In the presence of the combinations of input voltages V_{ia} and V_{ib} specified in Figure 7/V.10, the receiver shall maintain the specified output binary state and shall not be damaged.

Note – Designers of equipment should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiving equipment; therefore, appropriate techniques should be implemented to prevent such behaviour. For example, adequate hysteresis may be incorporated in the receiver to prevent such conditions.

6.4 *Input balance test* (Figure 8/V.10)

The balance of the receiver input resistances and internal bias voltages shall be such that the receiver shall remain in the intended binary state under the conditions shown in Figure 8/V.10 and described as follows:

a) with $V_i = +720$ millivolts and V_{cm} varied between -7 and $+7$ volts;

b) with $V_i = -720$ millivolts and V_{cm} varied between -7 and $+7$ volts;

c) with $V_i = +300$ millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study);

d) with $V_i = -300$ millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study).

Note – The values of V_i are provisional and are the subject of further study.

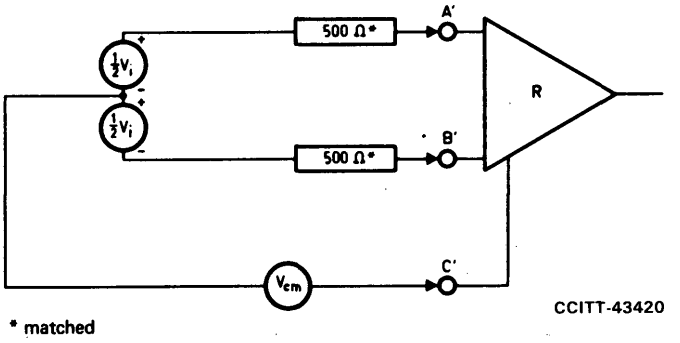


FIGURE 8/V.10

Receiver input balance test

7 Environmental constraints

In order to operate an unbalanced interchange circuit at data signalling rates ranging between 0 and 100 kbit/s, the following conditions apply:

1) The total peak differential noise measured between the points A′ and B′ at the load interchange point (with the generator interchange point connected to a 50-ohm resistor substituted for the generator) shall not exceed the expected amplitude of the received signal minus 0.3 volts (provisional value).

2) The worst-case combination of generator-receiver ground potential difference (V_g, Figure 2/V.10) and longitudinally induced peak random noise voltage measured between the receiver points A′ or B′ and C′ with the generator ends of the cable A and C joined together shall not exceed 4 volts.

8 Circuit protection

Unbalanced generator and load devices complying with this Recommendation shall not be damaged under the following conditions:

1) generator open circuit;

2) short-circuit between the conductors of the interconnecting cable;

3) short-circuit between the conductors and Point C or C′.

The above faults 2) and 3) might cause power dissipation in the interchange circuit devices to approach the maximum power dissipation that may be tolerated by a typical integrated circuit (IC) package. The user is therefore cautioned that where multiple generators and receivers are implemented in a single IC package, only one such fault per package might be tolerable at any one time without damage occurring.

The user is also cautioned that the generator and receiver devices complying with this Recommendation might be damaged by spurious voltages applied between their input or output points and points C and C′ (Figure 2/V.10). In those applications where the interconnecting cable may be inadvertently connected to other circuits or where it may be exposed to a severe electromagnetic environment, protection should be employed.

9 Category 1 and category 2 receivers

In order to provide flexibility in the choice of generator (V.10 or V.11), two categories of receiver are defined as follows:

Category 1 – Receivers shall have both input terminals A′ and B′ connected to individual terminals at the load interchange point, independent of all other receivers, as shown in Figure 9/V.10, and as applied in Annex A, Figure A-1/V.10.

Category 2 – Receivers shall have one terminal connection for each A′ input terminal at the load interchange point, and all B′ input terminals shall be connected together within the DCE or DTE and shall be brought to one common B′ input terminal as shown in Figure 10/V.10.

The specification of the category to be used in any application is part of the appropriate DCE Recommendation, using this type of interface electrical characteristics.

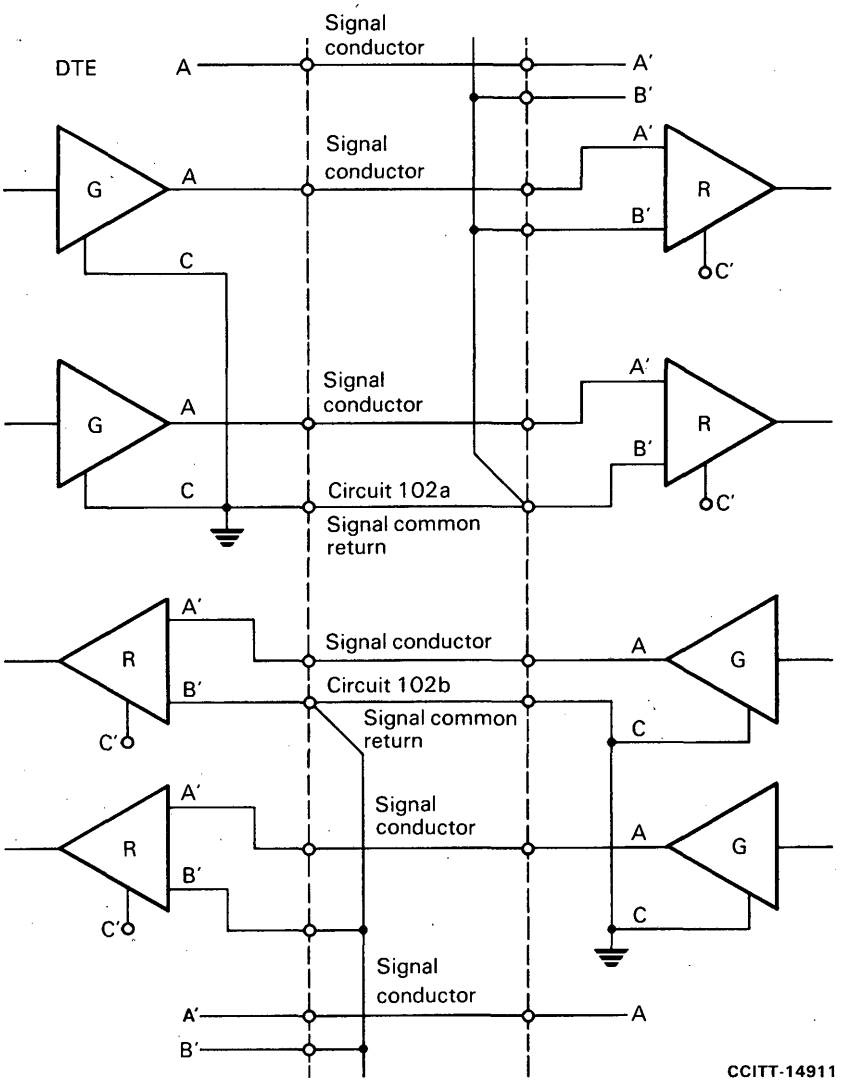


FIGURE 9/V.10

Interconnection of signal common return for category 1 receivers

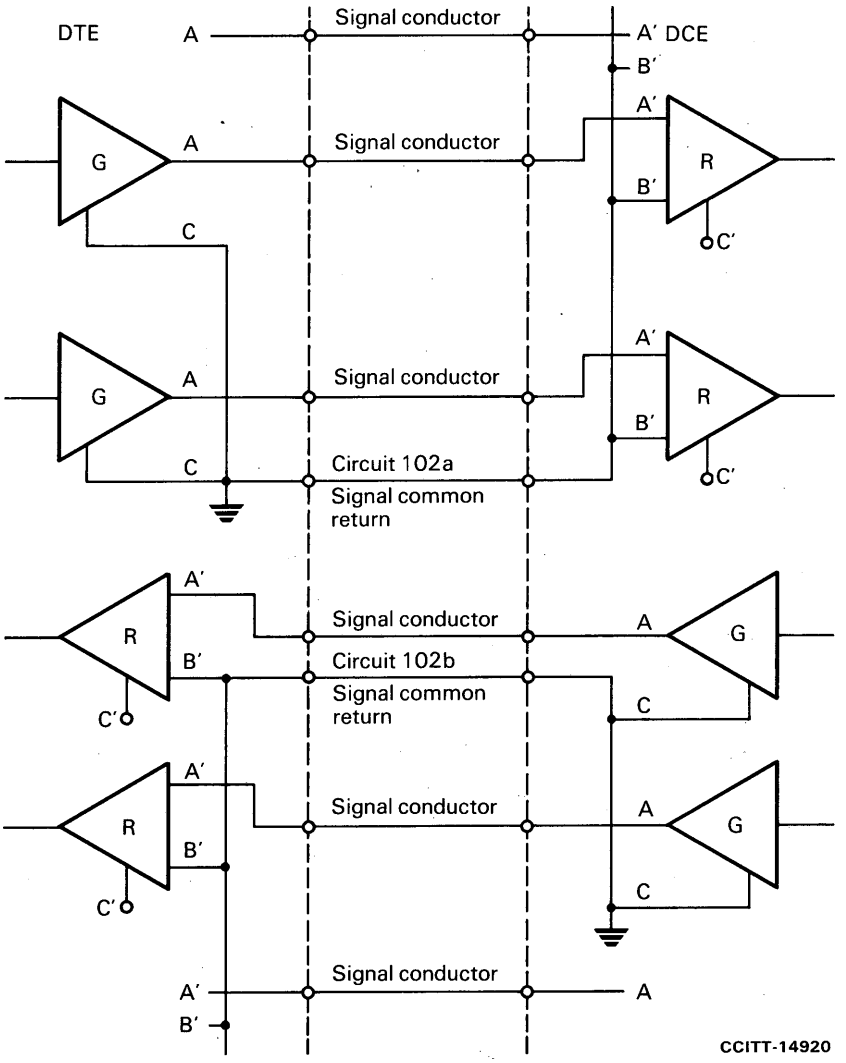


FIGURE 10/V.10

Interconnection of signal common return for category 2 receivers

10 Signal common return

The interconnection between the generator and the load interchange points in Figure 2/V.10 shall consist of a signal conductor for each circuit and one signal common return for each direction as shown in Figures 9/V.10 and 10/V.10. Signal common return may be implemented by more than one lead, where required to accomplish interworking, as described in § A.2 and as shown in Figure A-1/V.10.

To minimize the effects of ground potential difference V_g and longitudinally-coupled noise on the signal at the load interchange point, the signal common return shall be connected to ground only at the C terminal of the generator interchange point. For example, the B′ terminal of all the receivers in DTE which interconnect with unbalanced generators in DCE shall connect to signal common return circuit 102b, which is connected to ground only in DCE. Signal common return circuit 102a is used to interconnect terminal B′ of the receivers in DCE with the grounded terminal C of the unbalanced generators in DTE, as in Figures 9/V.10 and 10/V.10.

11 Detection of generator power-off or circuit failure

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator power-off condition;
2) receiver not interconnected with a generator;
3) open-circuited interconnecting cable;
4) short-circuited interconnecting cable;
5) input signal to the load remaining within the transition region (± 300 millivolts) for an abnormal period of time.

When detection of one or more fault conditions is required by specific applications, additional provisions are required in the load and the following items must be determined:

a) which interchange circuits require fault detection;
b) what faults must be detected;
c) what action must be taken when a fault is detected, e.g. which binary state must the receiver assume?

The interpretation of a fault condition by a receiver (or load) is application dependent. Each application may use a combination of the following classification:

Type 0 – No interpretation. A receiver or load does not have fault detection capability.

Type 1 – Data circuits assume a binary 1 state. Control and timing circuits assume an OFF condition.

Type 2 – Data circuits assume binary 0 state. Control and timing circuits assume an ON condition.

Type 3 – Special interpretation. The receiver or load provides a special indication for interpreting a fault condition. This special indication requires further study.

The association of the circuit failure detection to particular interchange circuits in accordance with the above types is a matter of the functional and procedural characteristics specification of the interface.

The interchange circuits monitoring circuit fault conditions in the general telephone network interfaces are indicated in Recommendation V.24.

The interchange circuits monitoring circuit fault conditions in data network interfaces are indicated in Recommendation X.24 [1].

The receiver fault detection type required is specified in the relevant DCE Recommendations.

12 Measurements at the physical interchange point

The following information provides guidance for measurements when maintenance persons examine the interface for proper operation at the interchange point.

12.1 *Listing of essential measurements*

- open-circuit measurements;
- test-termination measurement;
- short-circuit measurement;
- generator output rise time;
- d.c. input sensitivity measurements.

12.2 *Listing of optional measurements*

- the total generator resistance between points A and C shall be equal to or less than 50 ohms;
- power-off measurements;
- receiver input voltage espace-espace current measurements;
- input balance test;
- check of the required circuit fault detection (§ 11).

The parameters defined in this Recommendation are not necessarily measurable at the physical interchange point. This is for further study.

ANNEX A

(to Recommendation V.10)

Compatibility with other interfaces

A.1 *Compatibility of Recommendation V.10 and Recommendation V.11 interchange circuits in the same interface*

The electrical characteristics of Recommendation V.10 are designed to allow the use of balanced (see Recommendation V.11) and unbalanced circuits within the same interface. For example, the balanced circuits may be used for data and timing whilst the unbalanced circuits may be used for associated control circuit functions.

A.2 *Recommendation V.10 interworking with Recommendation V.11*

The differential receiver specifications of Recommendations V.10 and V.11 are electrically identical. It is therefore possible to interconnect an equipment using Recommendation V.10 receivers and generators on one side of the interface with an equipment using Recommendation V.11 generators and receivers on the other side of the interface. Such interconnection would result in interchange circuits according to Recommendation V.11 in one direction and interchange circuits according to Recommendation V.10 in the other direction. Where such interworking is contemplated, the following technical considerations must be taken into account.

A.2.1 Interconnecting cable lengths are limited by performance of the circuits working to the Recommendation V.10 side of the interface.

A.2.2 The optional cable termination resistance (Z_t), if implemented, in the equipment using Recommendation V.11 must be removed.

A.2.3 V.10-type receivers shall be of category 1 (see Figure A-1/V.10).

A.3 *Recommendation V.10 interworking with Recommendation V.28*

The unbalanced electrical characteristics of Recommendation V.10 have also been designed to permit limited interworking, under certain conditions, with generators and receivers to Recommendation V.28. Where such interworking is contemplated, the following technical limitations must be considered:

A.3.1 Separate DTE and DCE signal return paths will not be available at the Recommendation V.28 side of the interface.

A.3.2 Data signalling-rate limitations according to Recommendation V.28 shall apply.

A.3.3 Interconnecting cable lengths are limited by the Recommendation V.28 performance restrictions.

A.3.4 Probability of satisfactory operation will be enhanced by providing the maximum generator voltage possible on the Recommendation V.10 side of the interface within the limitations stipulated in Recommendation V.10.

A.3.5 Whilst Recommendation V.28 type generators may use potentials in excess of 12 volts, many existing equipments are designed to operate with power supplies of 12 volts or less. Where this is the case, no further protection of Recommendation V.10 receivers is required; however, in the general case, protection against excessively high voltages from Recommendation V.28 generators must be provided for the Recommendation V.10 receivers.

A.3.6 Power-off detectors in Recommendation V.28 receivers may not necessarily work with Recommendation V.10 generators.

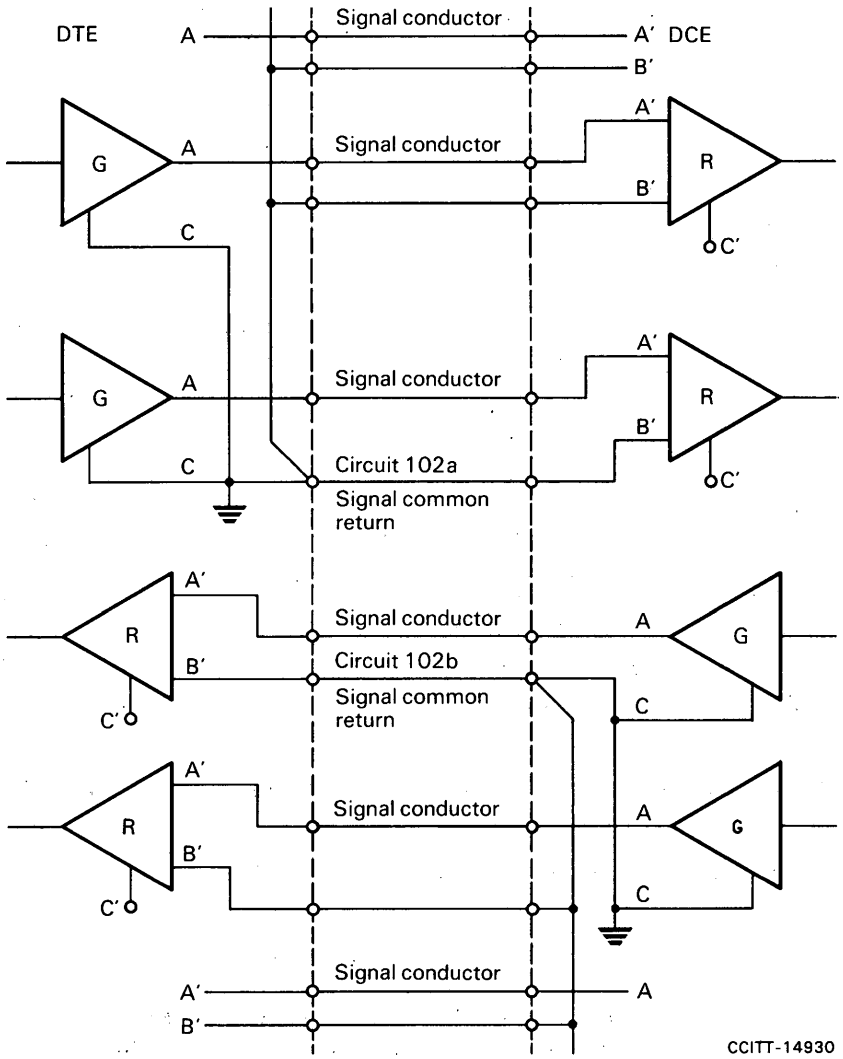


FIGURE A-1/V.10

Interconnection of signal common return by more than one conductor in order to accomplish interoperation of V.10 generators with category 1 receivers

ANNEX B

(to Recommendation V.10)

Considerations for coaxial cable applications – V.10 COAXIAL[4)]

It is recognized that where coaxial cables are used for interconnecting purposes it may be desirable to include a terminating resistance at the receiver end of the cable. This is considered to be a special case for which special generator characteristics are required. The terminating resistance shall in no case be less than 50 ohms and the reference measurements under §§ 5.2.2 and 5.3 shall be made with a 50-ohm test termination[5)]. Use of this special application will require appropriate agreement with the proper authority.

---

4) All the electrical characteristics specified in Recommendation V.10 other than those set down in this Annex are applicable to the coaxial cable case with a cable case with a cable termination.

5) For test purposes other than specified in this Recommendation (e.g. signal quality measurement), a transmitter test load of 50 ohms may be used.

The alternative set of electrical characteristics applied in the coaxial cable case is the following:

5.2.2 *bis* *Test termination measurement* [Figure 4b)/V.10]

With a test load (R_t) of 50 ohms connected between output points A and C, the magnitude of the output voltage (V_t) shall be equal to or greater than 0.5 of the magnitude of V_0.

5.3.1 *bis* *Waveform* (Figure 5/V.10)

The measurement will be made with a resistor of 50 ohms connected between points A and C. A test signal, with a nominal signal element duration t_b and composed of alternate ones and zeros, shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 of V_{ss}.

5.3.2 *bis* *Waveshaping*

Waveshaping is not normally required for coaxial cable applications.

10 *bis* *Signal common return*

In applications where coaxial cables are used, the screen of the coaxial cable shall be connected to ground only at point C at the generator end as shown in Figure B-1/V.10.

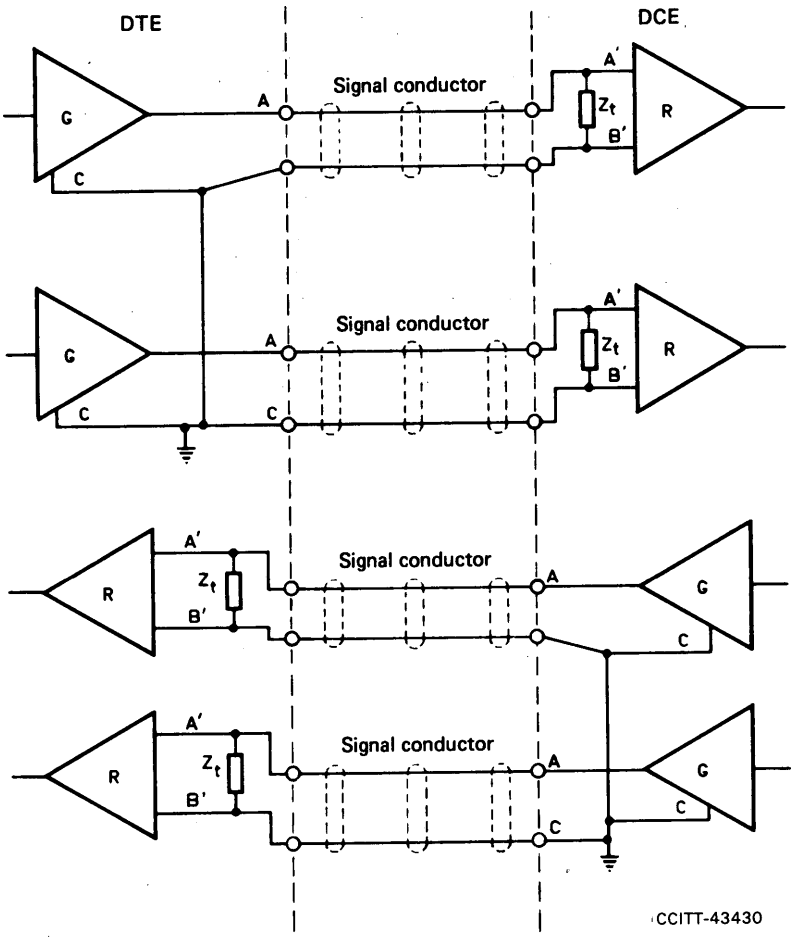


FIGURE B-1/V.10

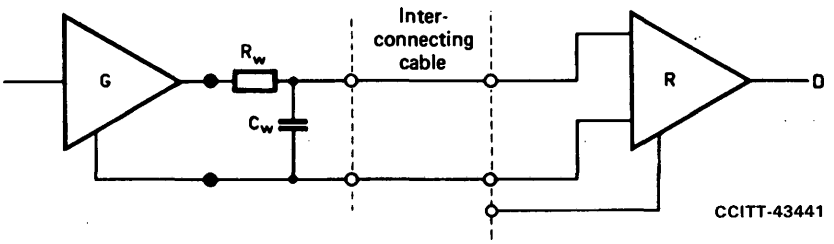
Interconnection with coaxial cable

APPENDIX I

(to Recommendation V.10)

Waveshaping

The required waveshaping may be accomplished either by providing a slew-rate control in the generator or by inserting an RC filter at the generator interchange point. A combination of these methods may also be employed. An example of the RC filter method is shown in Figure I-1/V.10. Typical values of capacitance C_w, with the value of R_w selected so that $R_w + R_d$ is approximately 50 ohms, are given for typical cable with an interconductor shunt capacitance of approximately 0.05 microfarads per kilometre.



R_d = generator internal resistance
R_w = 50 ohms – R_d

C_w (microfarads)	Data signalling rate range (kbit/s)
1.0	0 - 2.5
0.47	2.5 - 5.0
0.22	5.0 - 10
0.1	10 - 25
0.047	25 - 50
0.022	50 - 100

FIGURE I-1/V.10

Example method of waveshaping

APPENDIX II

(to Recommendation V.10)

Cable Guidelines

No electrical characteristics of the interconnection cable are specified in this Recommendation. However, guidance is given herein concerning operational constraints imposed by cable length and near-end crosstalk.

The maximum operating distance for the unbalanced interchange circuit is primarily a function of the amount of interference (near-end crosstalk) coupled to adjacent circuits in the equipment interconnection. Additionally the unbalanced circuit is susceptible to exposure to differential noise resulting from any imbalance between the signal conductor and signal common return at the load interchange point. Increasing the physical separation and interconnection cable length between the generator and load interchange points might increase the exposure to common-mode noise and the degree of near-end crosstalk. Accordingly, users are advised to restrict the cable length to a minimum consistent with the generator-load physical separation requirements.

The curve of cable length versus data signalling rate given in Figure II-1/V.10 may be used as a conservative guide. This curve is based upon calculations and empirical data using twisted-pair telephone cable with a shunt capacitance of 0.052 microfarads per kilometre, a 50-ohm source impedance, a 6-volt source signal and maximum near-end crosstalk of 1-volt peak. The rise time (t_r) of the source signal at signalling rates below 1000 bit/s is 100 microseconds and above 1000 bit/s is 0.1 t_b (see Figure 5/V.10).

The user is cautioned that the curve given in Figure II-1/V.10 does not account for common-mode noise or near-end crosstalk levels beyond the limits specified, that may be introduced between the generator and load by exceptionally long cables. On the other hand operation within the signalling-rate and distance bounds of Figure II-1/V.10 will usually ensure that the distortion of the signal appearing at the receiver input will be acceptable. Many applications, however, can tolerate greater levels of signal distortion, and correspondingly greater cable lengths can be employed. The generation of near-end crosstalk can be reduced by increasing the amount of waveshaping employed.

Experience has shown that in most practical cases the operating distance at the lower data signalling rates may be extended to several kilometres.

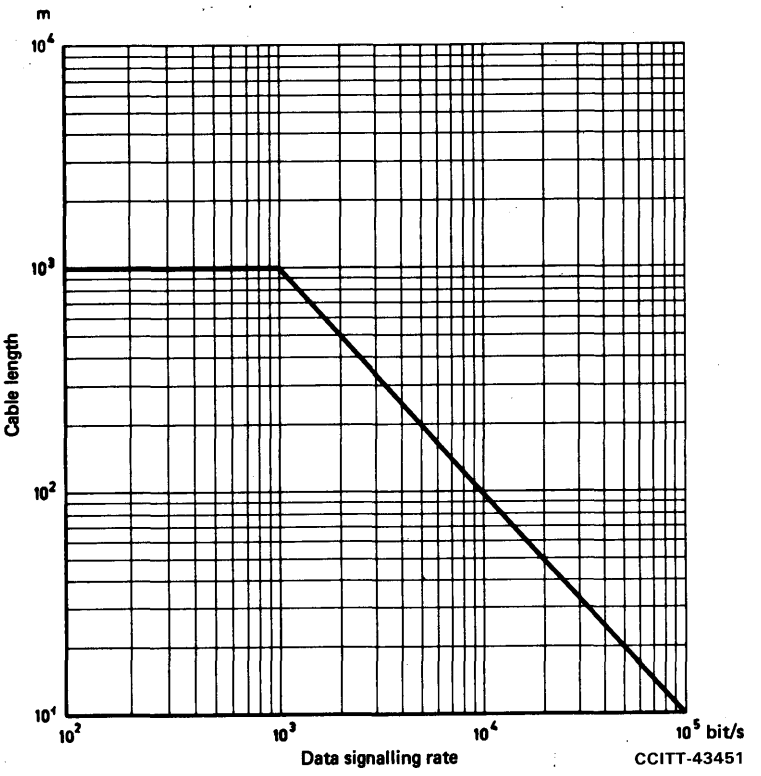


FIGURE II-1/V.10

Data signalling rate vs cable length for unbalanced interchange circuit

Reference

[1] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks*, Vol. VIII, Rec. X.24.

ELECTRICAL CHARACTERISTICS FOR BALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR GENERAL USE WITH INTEGRATED CIRCUIT EQUIPMENT IN THE FIELD OF DATA COMMUNICATIONS[1)]

(Geneva, 1976; amended Geneva, 1980 and at Melbourne, 1988)

1 Introduction

This Recommendation deals with the electrical characteristics of the generator, receiver and interconnecting leads of a differential signalling (balanced) interchange circuit with an optional d.c. offset voltage.

The balanced generator and load components are designed to cause minimum mutual interference with adjacent balanced or unbalanced interchange circuits (see Recommendation V.10) provided that waveshaping is employed on the unbalanced circuits.

In the context of this Recommendation, a balanced interchange circuit is defined as consisting of a balanced generator connected by a balanced interconnecting pair to a balanced receiver. For a balanced generator the algebraic sum of both the outlet potentials, with respect to earth, shall be constant for all signals transmitted; the impedances of the outlets with respect to earth shall be equal. The degree of balance and other essential parameters of the interconnecting pair is a matter for further study.

An Annex and two Appendices are provided to give guidance on a number of application aspects as follows:

Annex A Compatibility with other interfaces.

Appendix I Cable and termination.

Appendix II Multipoint operation.

Note – Generator and load devices meeting the electrical characteristics of this Recommendation need not operate over the entire data signalling rate range specified. They may be designed to operate over narrower ranges to satisfy requirements more economically, particularly at lower data signalling rates.

Reference measurements are described which may be used to verify certain of the recommended parameters but it is a matter for individual manufacturers to decide what tests are necessary to ensure compliance with the Recommendation.

2 Field of application

The electrical characteristics specified in this Recommendation apply to interchange circuits operating with data signalling rates up to 10 Mbit/s, and are intended to be used primarily in Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE) implemented in integrated-circuit technology.

This Recommendation is not intended to apply to equipment implemented in discrete component technology, for which the electrical characteristics covered by Recommendation V.28 are more appropriate.

Typical points of application are illustrated in Figure 1/V.11.

Whilst the balanced interchange circuit is primarily intended for use at the higher data signalling rates, its use at the lower rates may be necessary in the following cases:

1) where the interconnecting cable is too long for proper unbalanced circuit operation;
2) where extraneous noise sources make unbalanced circuit operation impossible;
3) where it is necessary to minimize interference with other signals.

[1)] This Recommendation is also designated as X.27 in the Series X Recommendations.

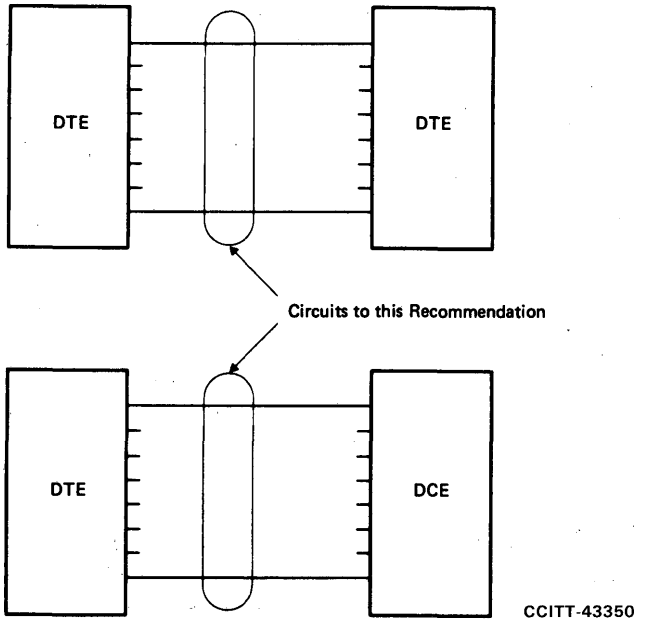
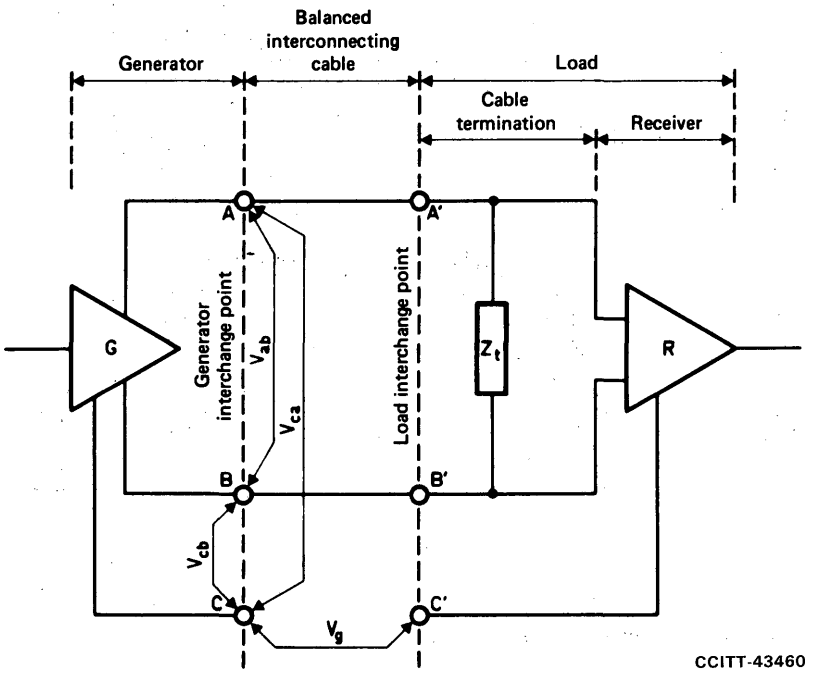


FIGURE 1/V.11

Typical applications of balanced interchange circuits

3 Symbolic representation of interchange circuit (Figure 2/V.11)



V_{ab} = generator output voltage between points A and B
V_{ca} = generator voltage between points C and A
V_{cb} = generator voltage between points C and B
Z_t = cable termination impedance
V_g = ground potential difference
A, B and A', B' = interchange points
C, C' = zero volt reference interchange points

Note 1 – Two interchange points are shown. The output characteristics of the generator, excluding any interconnecting cable, are defined at the "generator interchange point". The electrical characteristics to which the receiver must respond are defined at the "load interchange point".

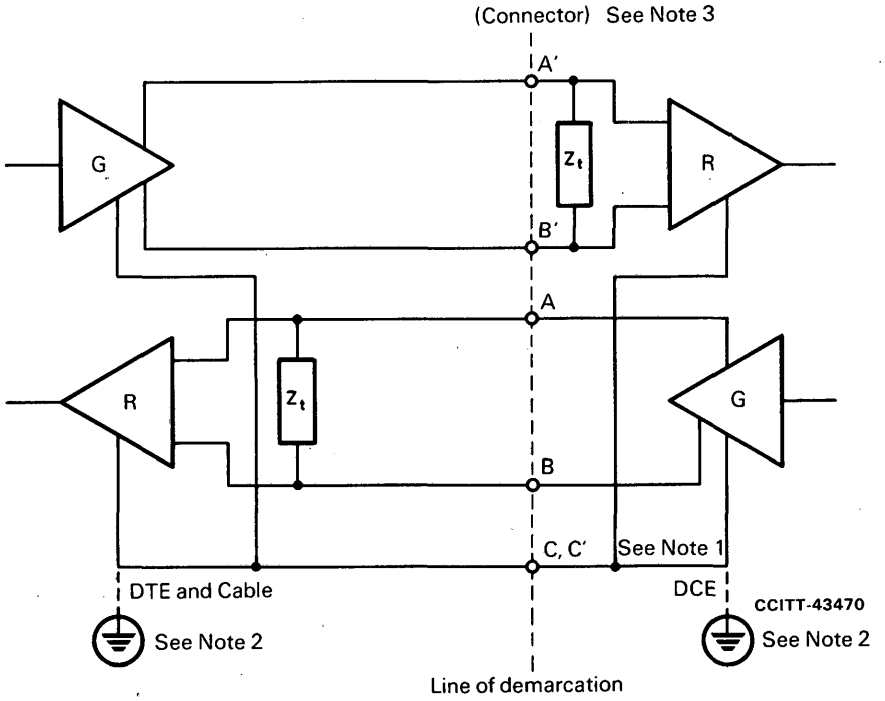
Note 2 – Points C and C' may be interconnected and further connected to protective ground if required by national regulations.

FIGURE 2/V.11

Symbolic representation of a balanced interchange circuit

The equipment at both sides of the interface may implement generators as well as receivers in any combination. Consequently, the symbolic representation of the interchange circuit, Figure 2/V.11 above, defines a generator interchange point as well as a load interchange point.

For data transmission applications, it is commonly accepted that the interface cabling will be provided by the DTE. This introduces the line of demarcation between the DTE plus cable and the DCE. This line is also called the interchange point and physically implemented in the form of a connector. The applications also require interchange circuits in both directions. This leads to an illustration as shown in Figure 3/V.11.



Note 1 – The zero volt reference interchange point C, C′ may be interconnected via the signal ground conductor.

Note 2 – Signal ground may be further connected to external protective ground if national regulations require.

Note 3 – The type of connector with this electrical characteristic specification depends on the application. ISO specifies, for data transmission over telephone type facilities, a 37-pin connector in ISO 4902 and, for data transmission over data network facilities, a 15-pin connector in ISO 4903.

FIGURE 3/V.11

Practical representation of the interface

4 Generator polarities and receiver significant levels

4.1 *Generator*

The signal conditions for the generator are specified in terms of the voltage between output points A and B shown in Figure 2/V.11.

When the signal condition 0 (space) for data circuits or ON for control and timing circuits is transmitted, the output point A is positive with respect to point B. When the signal condition 1 (mark) for data circuits or OFF for control and timing circuits is transmitted, the output point A is negative with respect to point B.

4.2 *Receiver*

The receiver differential significant levels are shown in Table 1/V.11, where $V_{A'}$ and $V_{B'}$ are respectively the voltages at points A′ and B′ relative to point C′.

TABLE 1/V.11

Receiver differential significant levels

	$V_{A'} - V_{B'} \leqslant -0.3$ V	$V_{A'} - V_{B'} \geqslant +0.3$ V
Data circuits	1	0
Control and timing circuits	OFF	ON

5 Generator[2)]

5.1 *Resistance and d.c. offset voltage*

5.1.1 The total generator resistance between points A and B shall be in the range of 50 to 100 ohms and adequately balanced with respect to point C. (It is left for further study as to the degree of balance required both statically and dynamically.)

Note 1 – It is assumed that the value of the dynamic source impedance is in the same range.

Note 2 – There may be integrated circuits in the field which do not comply with the requirement of 50 ohms as a minimum. If this causes problems in certain applications (e.g. reflections), additional series resistors of approximately 33 ohms at each of the generator output leads would correct these problems, if the use of a cable termination is not possible (e.g. for V.10 compatibility).

5.1.2 The magnitude of the generator d.c. offset voltage (see § 5.2.2 below) shall not exceed 3 V under all operating conditions.

5.2 *Static reference measurements*

The generator characteristics are specified in accordance with measurements illustrated in Figure 4/V.11 and described in §§ 5.2.1 to 5.2.4 below.

5.2.1 *Open-circuit measurement* [Figure 4a)/V.11]

The open-circuit voltage measurement is made with a 3900-ohm resistor connected between points A and B. In both binary states, the magnitude of the differential voltage (V_0) shall not be more than 6.0 volts, nor shall the magnitude of V_{0a} and V_{0b} be more than 6.0 volts.

5.2.2 *Test-termination measurement* [Figure 4b)/V.11]

With a test load of two resistors, each 50 ohms, connected in series between the output points A and B, the differential voltage (V_t) shall not be less than 2.0 volts or 50% of the magnitude of V_0, whichever is greater. For the opposite binary state the polarity of V_t shall be reversed ($-V_t$). The difference in the magnitudes of V_t and $-V_t$ shall be less than 0.4 volt. The magnitude of the generator offset voltage V_{0s} measured between the centre of the test load and point C shall not be greater than 3.0 volts. The magnitude of the difference in the values of V_{0s} for one binary state and the opposite binary state shall be less than 0.4 volt.

Note – Under some conditions this measurement does not determine the degree of balance of the internal generator impedances to point C. It is left for further study whether additional measurements are necessary to ensure adequate balance in generator output impedances.

5.2.3 *Short-circuit measurement* [Figure 4c)/V.11]

With the output points A and B short-circuited to point C, the current flowing through each of the output points A or B in both binary states shall not exceed 150 milliamperes.

[2)] For test purposes other than specified in this Recommendation (e.g. signal quality measurement), a transmitter test load of 100 ohms may be used.

5.2.4 *Power-off measurements* [Figure 4d)/V.11]

Under power-off condition with voltages ranging between +0.25 volt and −0.25 volt applied between each output point and point C, as indicated in Figure 4d)/V.11, the magnitude of the output leakage currents (I_{xa} and I_{xb}) shall not exceed 100 microamperes.

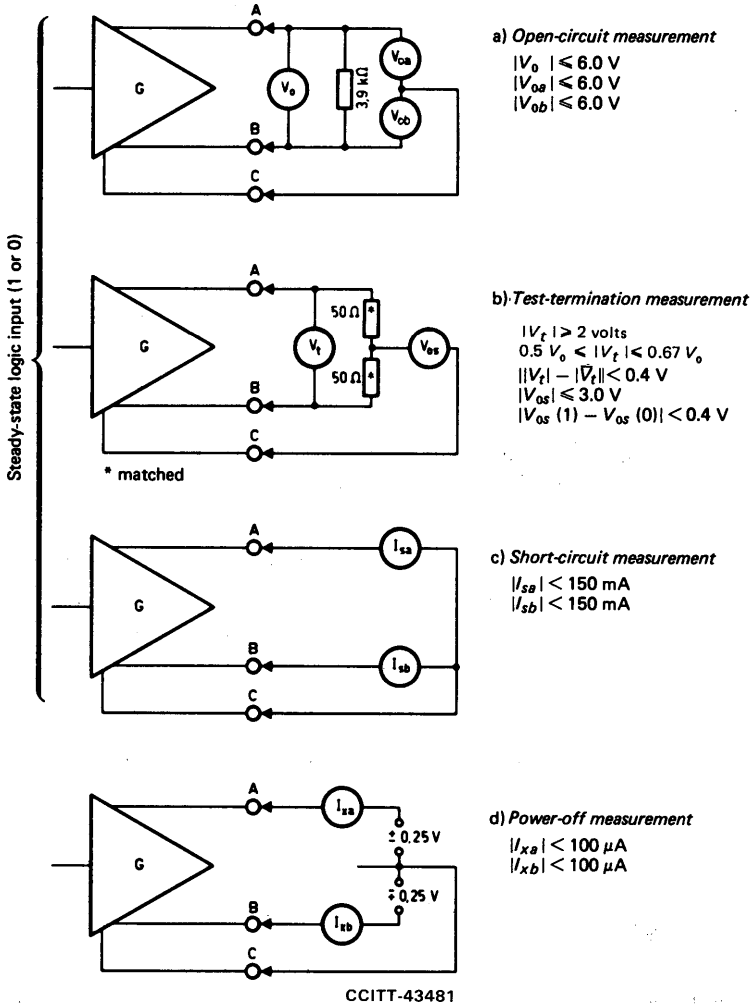


FIGURE 4/V.11

Generator-parameter reference measurements

5.3 *Dynamic voltage balance and rise time measurements* (Figure 5/V.11)

With the measurement configuration shown in Figure 5/V.11, a test signal with a nominal signal element duration t_b and composed of alternate ones and zeros, shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 V_{ss} within 0.1 of t_b or 20 nanoseconds, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{ss} from the steady state value.

The resultant voltage due to imbalance (V_E) shall not exceed 0.4 V peak-to-peak.

6 Load

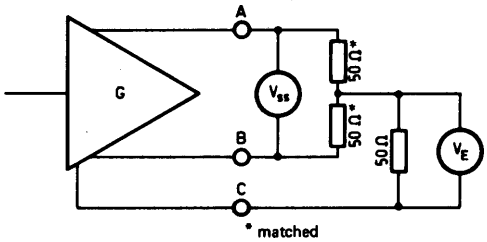
6.1 *Characteristics*

The load consists of a receiver (R) and an optional cable termination resistance (Z_t) as shown in Figure 2/V.11. The electrical characteristics of the receiver are specified in terms of the measurements illustrated in Figures 6/V.11, 7/V.11 and 8/V.11 and described in §§ 6.2, 6.3 and 6.4 below. A circuit meeting these requirements results in a differential receiver having a high input impedance, a small input threshold transition region between −0.3 and +0.3 volts differential, and allowance for an internal bias voltage not to exceed 3 volts in magnitude.

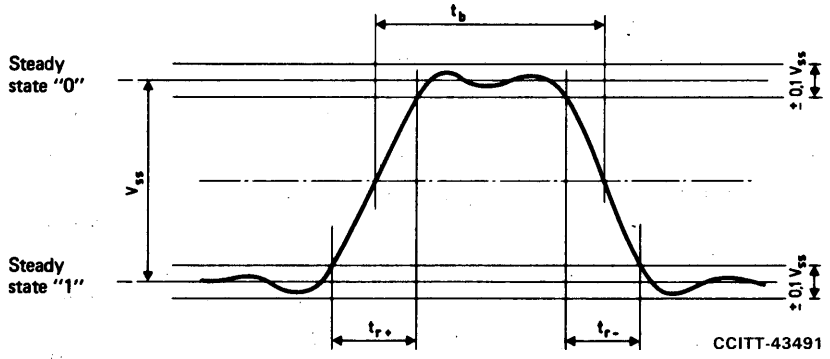
The receiver is electrically identical to that specified for the unbalanced receiver in Recommendation V.10.

6.2 *Receiver input voltage – current measurements* (Figure 6/V.11)

With the voltage V_{ia} (or V_{ib}) ranging between -10 volts and $+10$ volts, while V_{ib} (or V_{ia}) is held at 0 volt, the resultant input current I_{ia} (or I_{ib}) shall remain within the shaded range shown in Figure 6/V.11. These measurements apply with the power supply of the receiver in both the power-on and power-off conditions.



V_E < 0.4 V peak-to-peak (provisional)
V_{ss} = Voltage difference between steady-state signal conditions



t_b = nominal duration of the test signal element
for $t_b \geq 200$ ns, $t_r \leq 0.1\ t_b$
for $t_b < 200$ ns, $t_r \leq 20$ ns

FIGURE 5/V.11

Generator dynamic balance and rise-time measurements

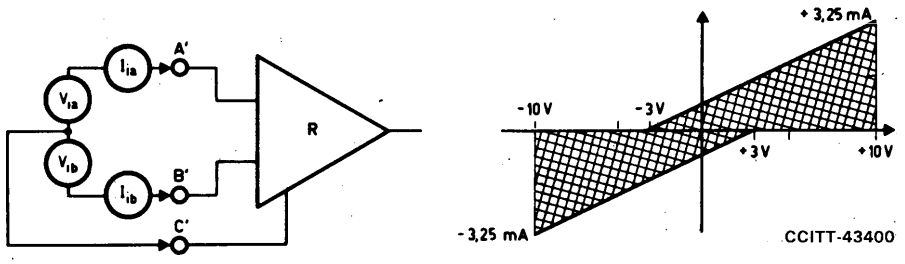


FIGURE 6/V.11

Receiver input voltage-current measurements

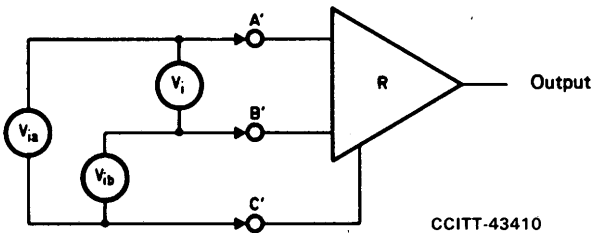
6.3 *D.c. input sensitivity measurements* (Figure 7/V.11)

Over the entire common mode voltage (V_{cm}) range of +7 volts to −7 volts, the receiver shall not require a differential input voltage (V_i) of more than 300 millivolts to assume correctly the intended binary state. Reversing the polarity of V_i shall cause the receiver to assume the opposite binary state.

The maximum voltage (signal plus common mode) present between either receiver input and receiver ground shall not exceed 10 volts nor cause the receiver to malfunction. The receiver shall tolerate a maximum differential voltage of 12 volts applied across its input terminals without being damaged.

In the presence of the combination of input voltages V_{ia} and V_{ib} specified in Figure 7/V.11, the receiver shall maintain the specified output binary state and shall not be damaged.

Note – Designers of equipment should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiving equipment; therefore, appropriate techniques should be implemented to prevent such behaviour. For example, adequate hysteresis may be incorporated in the receiver to prevent such conditions.



Applied voltages		Resulting input voltage V_i	Output binary state	Purpose of measurement
V_{ia}	V_{ib}			
−12 V	0 V	−12 V	(not specified)	To ensure no damage to receiver inputs
0 V	−12 V	+12 V		
+12 V	0 V	+12 V		
0 V	+12 V	−12 V		
+10 V	+ 4 V	+ 6 V	0	To guarantee correct operation at V_i = 6 V (maintain correct logic state)
+ 4 V	+10 V	− 6 V	1	
−10 V	− 4 V	− 6 V	1	
− 4 V	−10 V	+ 6 V	0	
				300 mV threshold measurement
+0.30 V	0 V	+0.3 V	0	V_{cm} = 0 V
0 V	+0.30 V	−0.3 V	1	
+7.15 V	+6.85 V	+0.3 V	0	V_{cm} = +7 V
+6.85 V	+7.15 V	−0.3 V	1	
−7.15 V	−6.85 V	−0.3 V	1	V_{cm} = −7 V
−6.85 V	−7.15 V	+0.3 V	0	

FIGURE 7/V.11

Receiver input sensitivity measurement

6.4 *Input balance test* (Figure 8/V.11)

The balance of the receiver input resistance and internal bias voltages shall be such that the receiver shall remain in the intended binary state under the conditions shown in Figure 8/V.11 and described as follows:

a) with $V_i = +720$ millivolts and V_{cm} varied between -7 and $+7$ volts;

b) with $V_i = -720$ millivolts and V_{cm} varied between -7 and $+7$ volts;

c) with $V_i = +300$ millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study);

d) with $V_i = -300$ millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study).

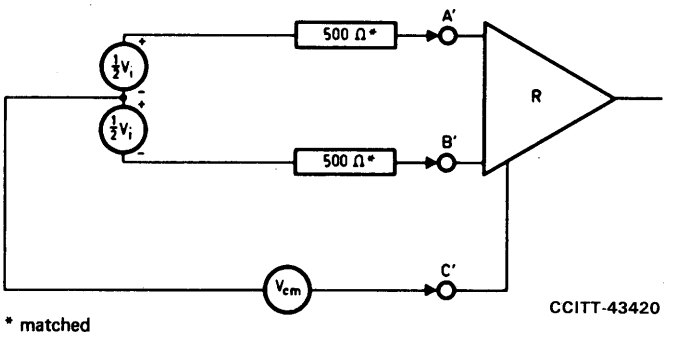


FIGURE 8/V.11

Receiver input balance test

6.5 *Terminator*

The use of a cable terminating impedance (Z_t) is optional depending upon the specific environment in which the interchange circuit is employed (see Appendix I). In no case shall the total load resistance be less than 100 ohms.

7 Environmental constraints

In order to operate a balanced interchange circuit at data signalling rates ranging between 0 and 10 Mbit/s, the following conditions apply:

1) For each interchange circuit a balanced interconnecting pair is required.

2) Each interchange circuit must be appropriately terminated (see Appendix I).

3) The total common-mode voltage at the receiver must be less than 7 volts peak.

The common mode voltage at the receiver is the worst case combination of:

a) generator-receiver ground-potential difference (V_g, Figure 2/V.11);

b) longitudinally induced random noise voltage measured between the receiver points A′ or B′ and C′ with the generator ends of the cable A, B and C joined together; and

c) generator d.c. offset voltage, if any.

Unless the generator is of a type which generates no d.c. offset voltage, the sum of a) and b) above, which is the element of the common mode voltage due to the environment of the interchange circuit, must be less than 4 volts peak.

8 Circuit protection

Balanced generator and load devices complying with this Recommendation shall not be damaged under the following conditions:

1) generator open circuit;
2) short-circuit between the conductors of the interconnecting cable;
3) short-circuit between either or both conductors and point C or C'.

The above faults 2) and 3) might cause power dissipation in the interchange circuit devices to approach the maximum power dissipation that may be tolerable by a typical integrated circuit (IC) package. The user is therefore cautioned that where multiple generators and receivers are implemented in a single IC package, only one such fault per package might be tolerable at any one time without damage occurring.

The user is also cautioned that the generator and receiver devices complying with this Recommendation might be damaged by spurious voltages applied between their input or output points and points C or C' (Figure 2/V.11). In those applications where the interconnecting cable may be inadvertently connected to other circuits, or where it may be exposed to a severe electromagnetic environment, protection should be employed.

9 Detection of generator power-off or circuit failure

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator power-off condition;
2) receiver not interconnected with a generator;
3) open-circuited interconnecting cable;
4) short-circuited interconnecting cable;
5) input signal to the load remaining within the transition region (± 300 millivolts) for an abnormal period of time.

When detection of one or more fault conditions is required by specific applications, additional provisions are required in the load and the following items must be determined:

a) which interchange circuits require fault detection;
b) what faults must be detected;
c) what action must be taken when a fault is detected, e.g. which binary state must the receiver assume?

The interpretation of a fault condition by a receiver (or load) is application dependent. Each application may use a combination of the following classification:

Type 0 – No interpretation. A receiver or load does not have fault detection capability.

Type 1 – Data circuits assume a binary 1 state. Control and timing circuits assume an OFF condition.

Type 2 – Data circuits assume binary 0 state. Control and timing circuits assume an ON condition.

Type 3 – Special interpretation. The receiver or load provides a special indication for interpreting a fault condition. This special indication requires further study.

The association of the circuit failure detection to particular interchange circuits in accordance with the above types is a matter of the functional and procedural characteristics specification of the interface.

The interchange circuits monitoring circuit fault conditions in the general telephone network interfaces are indicated in Recommendation V.24.

The interchange circuits monitoring circuit fault conditions in public data network interfaces are indicated in Recommendation X.24 [1].

The receiver fault detection type required is specified in the relevant DCE Recommendations.

10 Measurements at the physical interchange point

The following information provides guidance for measurements when maintenance persons examine the interface for proper operation at the interchange point.

10.1 *Listing of essential measurements*

- the magnitude of the generator d.c. offset voltage under all operating conditions;
- open-circuit measurements;
- test-termination measurement;
- short-circuit measurement;
- dynamic voltage balance and rise time;
- d.c. input sensitivity measurements.

10.2 *Listing of optional measurements*

- The total generator resistance between points A and B shall be equal to or less than 100 ohms and adequately balanced with respect to point C. (It is left for further study as to the degree of balance required both statically and dynamically);
- power-off measurements;
- receiver input voltage-current measurements;
- input balance test;
- check of the required circuit fault detection (§ 9).

The parameters defined in this Recommendation are not necessarily measurable at the physical interchange point. This is for further study.

ANNEX A

(to Recommendation V.11)

Compatibility with other interfaces

A.1 *Compatibility of Recommendation V.10 and Recommendation V.11 interchange circuits in the same interface*

The electrical characteristics of Recommendation V.11 are designed to allow the use of unbalanced (see Recommendation V.10) and balanced circuits within the same interface. For example, the balanced circuits may be used for data and timing whilst the unbalanced circuits may be used for associated control circuit functions.

A.2 *Recommendation V.11 interworking with Recommendation V.10*

The differential receiver specifications of Recommendations V.10 and V.11 are electrically identical. It is therefore possible to interconnect an equipment using Recommendation V.10 receivers and generators on one side of the interface with an equipment using Recommendation V.11 generators and receivers on the other side of the interface. Such interconnection would result in the interchange circuits according to Recommendation V.11 in one direction and interchange circuits according to Recommendation V.10 in the other direction. Where such interworking is contemplated, the following technical considerations must be taken into account.

A.2.1 Interconnecting cable lengths are limited by performance of the circuits working to the Recommendation V.10 side of the interface.

A.2.2 The optional cable termination resistance (Z_t), if implemented, in the equipment using Recommendation V.11 must be removed.

A.2.3 V.10-type receivers shall be of category 1.

A.3 *Recommendation V.11 interworking with Recommendation V.35*

Equipment having interchange circuits according to Recommendation V.11 is expected to interoperate with practical implementations of the electrical characteristics defined in Recommendation V.35, Appendix II. Interoperation between a V.35 transmitter and a V.11 receiver will result in shorter cable length than those indicated in Figure I-1/V.11. This is due to the fact that the output voltage from the V.35 transmitter loaded by a 100 ohms resistor has a minimum value of 0.44 volts peak/peak, which represents about 1/5 of the voltage of the V.11 transmitter (2 volts), as per Figure 7/V.11.

APPENDIX I

(to Recommendation V.11)

Cable and termination

No electrical characteristics of the interconnecting cable are specified in this Recommendation. Guidance is given herein concerning operational constraints imposed by the length, balance and terminating resistance of the cable.

I.1 *Cable*

Over the length of the cable, the two conductors should have essentially the same values of:

1) capacitance to ground;
2) longitudinal resistance and inductance;
3) coupling to adjacent cables and circuits.

I.2 *Cable length*

The maximum permissible length of cable separating the generator and the load in a point-to-point application is a function of the data signalling rate. It is further influenced by the tolerable signal distortion and the environmental constraints such as ground potential difference and longitudinal noise. Increasing the distance between generator and load might increase the exposure to ground potential difference.

As an illustration of the above conditions, the curves of cable length versus data signalling rate in Figure I-1/V.11 may be used for guidance.

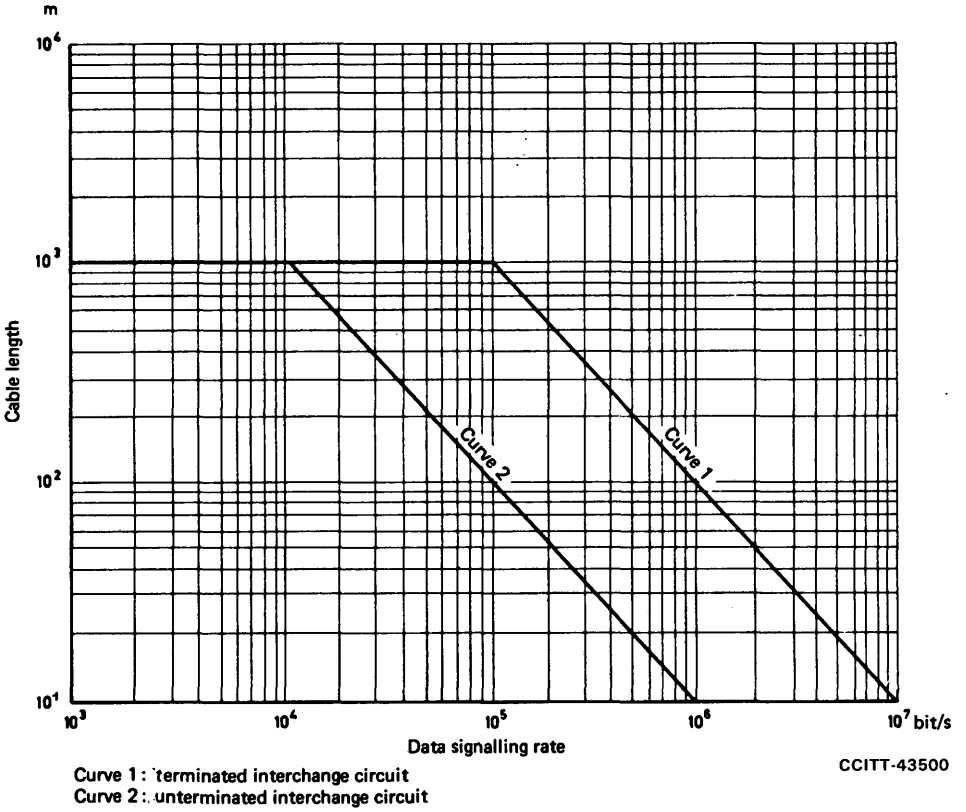


FIGURE I-1/V.11

Data signalling rate vs cable length for balanced interchange circuit

These curves are based upon empirical data using twisted pair telephone cable (0.51-mm wire diameter) both unterminated and terminated in a 100-ohm resistive load. The cable length restrictions shown by the curves are based upon the following assumed signal quality requirements at the load:

1) signal rise and fall time equal to, or less than, one-half the duration of the signal element;

2) a maximum voltage loss between generator and load of 6 dB.

At the higher data signalling rates (see Figure I-1/V.11) the sloping portion of the curves shows the cable length limitation established by the assumed signal rise and fall time requirements. The cable length has been arbitrarily limited to 1000 metres by the assumed maximum allowable loss of 6 dB.

These curves assume that the environmental limits specified in this Recommendation have been achieved. At the higher data signalling rates these conditions are more difficult to attain due to cable imperfections and common-mode noise. Operation within the data signalling rate and distance bounds of Figure I-1/V.11 will usually ensure that distortion of the signal appearing at the receiver input will be acceptable. Many applications, however, can tolerate much greater levels of signal distortion and in these cases correspondingly greater cable lengths may be employed.

Experience has shown that in many practical cases the operating distance at lower signalling rates may extend to several kilometres.

For synchronous transmission where the data and signal element timing are transmitted in opposite directions, the phase relationship between the two may need to be adjusted to ensure conformity with the relevant requirements of signal quality at the interchange point.

I.3 *Cable termination*

The use of a cable termination resistance (Z_t) is optional and dependent on the specific application. At the higher data signalling rates (above 200 kbit/s) or at any data signalling rate where the cable propagation delay is of the order of half the signal element duration a termination should be used to preserve the signal rise time and minimize reflections. The terminating impedance should match as closely as possible the cable characteristic impedance in the signal spectrum.

Generally, a resistance in the range of 100 to 150 ohms will be satisfactory, the higher values leading to lower power dissipation.

At the lower data signalling rates, where distortion and rise-time are not critical, it may be desirable to omit the termination in order to minimize power dissipation in the generator.

APPENDIX II

(to Recommendation V.11)

Multipoint operation

For further study. A specification for multipoint operation including the version ISO 8482 is under study.

Reference

[1] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks*, Vol. VIII, Rec. X.24.

SIMULATED CARRIER CONTROL

(Melbourne, 1988)

The CCITT,

considering

(a) that there is a wide variety of duplex data systems available;

(b) that some data terminal equipment (DTE) operate 2-way alternate over these systems.

recommends

that the following procedure be employed for simulated circuit 105 to circuit 109 operation, when specifically called for in a CCITT Recommendation.

1 Scope

This Recommendation applies wherever a requirement for control of a remote circuit 109 by a local circuit 105 exists, and where switching OFF and ON of a modem carrier is impossible or impractical. Examples of such environments are:

- sub-channels of modems containing multiplex facilities;
- modems with long equalizer/echo canceller training sequences;
- high efficiency multiplexers containing no control channels;
- PCM channels used for 64 bit/s data transmission.

2 Location of the simulation function

Within this Recommendation the function is described as though it were located between the DTE and the remaining part of the data circuit-terminating equipment (DCE). Location with respect to the loop device as defined in Recommendation V.54 is for further study.

3 Operation

When circuit 105 is OFF the DCE will transmit a pattern of bits (idle pattern) produced by scrambling a binary 1 with the polynominal $1 + x^{-3} + x^{-7}$, in lieu of data bits for that port. No particular starting state is specified for the scrambler. When circuit 105 turns ON, the DCE will immediately transmit a pattern of 8 bits (ON pattern) produced by scambling a binary 0 with the polynomial $1 + x^{-3} + x^{-7}$, after which data bits are sent (Note 1). Circuit 106 may be turned ON within 8 bit intervals after circuit 105 turns ON, and the first bit appearing on circuit 103 after circuit 106 turns ON should be sent as the first data bit (Note 2). When circuit 106 is turned ON before transmission of the ON pattern has been completed, data bits appearing on circuit 103 are stored in a data buffer for subsequent transmission.

At the remote DCE circuit 109 is turned OFF whenever a sufficient number of successive bits in the above idle pattern is detected (Note 3). Circuit 109 is turned ON after detecting a pattern of 8 bits produced by scrambling a binary 0 with the polynominal $1 + x^{-3} + x^{-7}$ (Note 4). Circuit 104 (received data) is held at binary 1 when circuit 109 is OFF (see also Notes 5, 6, 7).

Note 1 – The starting state of the scrambler used for scrambling a binary 0 with the polynomial $1 + x^{-3} + x^{-7}$ should be the same as the ending scrambler state after scrambling binary 1.

Note 2 – Additional circuit 106 turn ON delays may be provided as manufacturer's options.

Note 3 – The number of successive bits of the idle pattern required to be detected to turn circuit 109 OFF is recommended to be 48-64. Before circuit 109 turns OFF, the idle pattern may appear on circuit 104.

Note 4 – It is recommended that circuit 109 be turned ON only if the ON pattern is preceded by a sufficient number of consecutive scrambled ones. The protection against failure to recognize the ON pattern when transmission errors occur is subject to further study. The length of the ON pattern required to be detected to turn circuit 109 ON is provisionally fixed to 8.

Note 5 – Following an ON to OFF transition of circuit 105, circuit 105 should be ignored for at least 128 bit intervals so that at least 128 bits produced by scrambling a binary 1 are sent to the remote modem.

Note 6 – When circuit 105 is OFF, precaution should be taken that the output of the scrambler is not continuous 1, but rather is a 127 bit pseudo-random sequence.

Note 7 – Circuit 109 may be erroneously turned ON at the time of receiving the idle pattern, or circuit 109 may remain OFF at the time of receiving the ON pattern, when transmission errors occur. It may also turn OFF due to simulation by user data.

Recommendation V.14

TRANSMISSION OF START-STOP CHARACTERS OVER SYNCHRONOUS BEARER CHANNELS

(Melbourne, 1988)

1 Scope

1.1 This Recommendation describes a method of conveying start-stop characters over synchronous bearer channels using an async-to-sync converter in the data signalling rate range of up to 19 200 bit/s. Start-stop characters at signalling rates below or equal to 300 bit/s can be conveyed over synchronous bearer channels by oversampling at a signalling rate of at least 1200 bit/s.

Note – The conversion method provided here replaces the conversion method applied earlier to Recommendations V.22, V.22 *bis*, V.26 *ter* and V.32.

1.2 This converter may be an intermediate device inserted into the data lines of both circuit 103 in the transmitter and circuit 104 in the receiver inside a synchronous DCE (see Figure A-1/V.14 in Annex A), or a stand-alone unit in certain applications.

2 Data signalling rates

The conversion method shall be limited to signalling rates of up to 19 200 bit/s preferring the standard signalling rates of Recommendation V.5.

The nominal signalling rates for both the start-stop characters and the synchronous DCE shall be the same. The tolerance of the signalling rate of the synchronous transmission shall be ±0.01%.

3 Signalling rate ranges of the start-stop characters at the converter input

The conversion method is capable of tolerating the signalling rates of the DTE in two ranges:

a) basic range: +1% to −2.5%

b) extended range: +2.3% to −2.5%

The use of the basic signalling rate range is preferred since it results in lower distortion. The choice of range shall be made at the time of installation, and shall be the same for both transmitter and receiver. It is not intended to be under customer control.

4 Start-stop character format

It shall be possible to condition the converter to accept the following formats; viz:

a) a one-unit start element, followed by seven data units, and a stop element of the unit in length (9-bit characters);

b) a one-unit start element, followed by eight data units, and a stop element of one unit in length (10-bit characters);

c) a one-unit start element, followed by nine data units, and a stop element of one unit in length (11-bit characters);

The converter may also accept characters consisting of:

d) a one-unit start element, followed by six data units, and a stop element of one unit in length (8-bit characters).

Note that character formats c) and d) do not conform to International Alphabet No. 5.

The character format selected shall be the same for both transmitter and receiver. The characters shall be in accordance with Recommendation V.4 regardless of whether they conform to International Alphabet No. 5. It shall be possible to transmit characters continuously or with any additional continuous stop element of arbitrary length between characters.

Note – In each of the four formats, data units can be replaced by additional stop units. For example, format c) will allow 11-bit characters consisting of a one-unit start element, followed by eight data units and a stop element of two units to be handled.

5 Margin of the converter input

The effective net margin of the converter for transmitting of start-stop characters applied to the input of the converter shall be at least 40%. This figure is a subject for further study.

6 Selection of synchronous or asynchronous modes of operation

Selection for synchronous or asynchronous modes of operation shall be provided by switch (or similar means) enabling the user to perform normal transmission and testing in each mode of operation, respectively.

In synchronous mode of operation the converter is totally bypassed in both directions.

7 Async-to-sync conversion method

The general method to handle the speed differences between the intracharacter signalling rate of the start-stop characters and the data signalling rate of the synchronous bearer channel will be the insertion/deletion of stop elements at the transmitter and reinsertion of deleted stop elements at the receiver. Means are provided to transfer continuous start polarity (break signals) as well.

7.1 *Transmitter*

In the transmit direction the start-stop characters shall be adapted to the signalling rate of the synchronous bearer channel by:

- deleting stop elements in case of overspeed of the start-stop characters;
- insertion of additional stop elements in case of underspeed of the start-stop characters.

7.1.1 *Basic signalling rate range*

No more than one stop element shall be deleted for any eight consecutive characters.

7.1.2 *Extended signalling rate range*

No more than one stop element shall be deleted for any four consecutive characters.

7.2 *Receiver*

The intracharacter signalling rate provided by the converter shall be in the range of the nominal data rate to the limit of the specified overspeed tolerance, i.e. +1% in the basic and +2.3% in the extended data signalling range. The length of the stop element shall not be reduced by more than 12.5% for the basic signalling rate range (or 25% for the optional extended signalling rate range) to allow for overspeed in the transmitting terminal. The nominal length of the start and data elements for all characters shall be the same.

Note – Equipments exists in the field which delete stop elements more frequently than specified in §§ 7.1.1 and 7.1.2. However, in these equipments there will always be at least one additional inserted stop element between deleted stop elements.

7.3 *Break signal*

7.3.1 *Transmitter*

If the converter detects M to 2M + 3 bits all of "start" polarity, where M is the number of bits per character in the selected format, the converter shall transmit 2M + 3 bits of "stop" polarity. If the converter detects more than 2M + 3 bits all of "start" polarity the converter shall transmit all these bits as "start" polarity.

Note – The converter must receive at least 2M bits of "stop" polarity after the "start" polarity break signal in order to ensure that it regains the character synchronism.

7.3.2 *Receiver*

The 2M + 3 or more bits of "start" polarity received from the transmitting modem shall be transferred to the output of the converter, and the character synchronism shall be regained from the following "stop" to "start" transition.

Note – In some earlier implementations an uninitiated NUL character may precede the break signal at the output of the converter when no measures have been taken to prevent this.

7.4 *Tandem operation*

Tandem operation between two ends comprising async-to-sync conversions can be established only by using cascaded synchronous bearer channels.

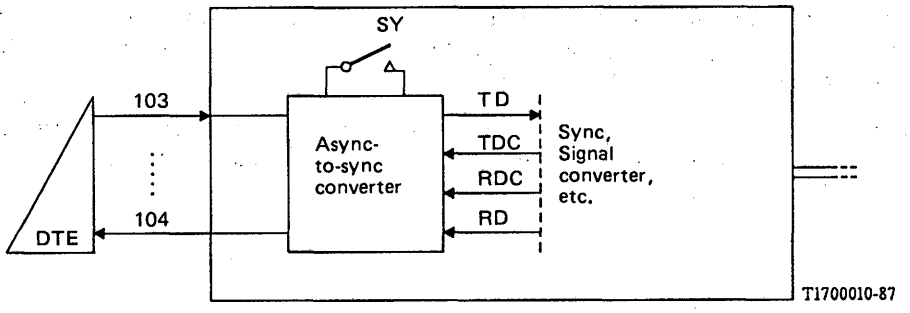
7.5 *Testing facilities*

All the tests recommended in the relevant Recommendations can be performed in asynchronous operation as well, where this converter is used, with the exception of self test end-to-end.

ANNEX A

(to Recommendation V.14)

Inclusion of an async-to-sync converter into a synchronous DCE



103 Transmitted data; data input to the DCE

TD Transmitted data; the synchronous output of the converter following the async-to-sync conversion of start-stop characters to be transmitted

TDC Transmitter signal element timing; internal timing information for the generation of synchronous transmitted data

RDC Receiver signal element timing; internal timing information associated with synchronous received data

RD Received data; the input of the converter for the restoration of start-stop characters

104 Received data; data output from the DCE

SY Synchronous mode; selection of the required mode of operation (asynchronous or synchronous)

FIGURE A-1/V.14

Note – Other interchange circuits which are provided are not involved in the operation of the async-to-sync converter but must comply with the requirements of the relevant DCE Recommendations including the conditions of the timing circuits (i.e. 113, 114 and 115) during both the asynchronous and synchronous modes of operation.

Recommendation V.15

USE OF ACOUSTIC COUPLING FOR DATA TRANSMISSION

(Geneva, 1972; amended at Malaga-Torremolinos, 1984)

Note – Acoustic coupling is a technique used to couple the output of a modem to an analogue telecommunication facility using acoustic energy/power between the device and a telephone instrument. As such, it provides for minimum complexity of attachment as well as excellent galvanic isolation. However, the technique does limit the data signalling rates used and does limit the functionality which can be provided by the associated modem. Since this arrangement will generally be used to communicate with a permanently installed V Series modem at a remote station, the characteristics of the modem will, accordingly, comply with requirements defined elsewhere in these Series V Recommendations, e.g., V.21 or V.23. As far as functionality permits, interfaces with the associated DTE will be as defined in those Recommendations. Because of operator intervention required in manipulating the telephone handset, automatic calling and automatic answering are not normally considered part of the functionality of an acoustically coupled modem. However, an acoustically coupled modem can call a remote station which has automatic answering capability and can observe the protocol defined in Recommendation V.25, § 6, "Manual data station calling automatic answering data station" as modified herein.

The CCITT,

considering

that there is a wide variety of telephone instruments in existence and that the acoustic path involved in the use of any coupling device cannot be accurately prescribed for all cases, and hence it will be difficult to ensure satisfactory transmission in all situations,

recommends

1 that acoustic coupling of data transmission equipment via telephone instruments to the telephone transmission network should not be used for permanent installations.

It is, however, recognized that there may be a need for a means to provide temporary connection of portable data transmission equipment to the network in circumstances where it may not be possible to obtain convenient access to the subscriber's line terminals.

The use of acoustic coupling for temporary communications is subject to the agreement of the Administration in charge of the telephone network to which the equipment will be connected.

If an Administration decides to permit acoustic coupling for temporary data transmission stations, the acoustic coupling equipment conforms to the following:

1) The maximum power output of the subscriber's equipment to the line shall not exceed 1 mW at any frequency.

   The mean permitted telephone line signal power shall not exceed −13 dBm0.

2) If p is the signal power in the frequency band 0-4 kHz, the signal power outside this band shall not exceed the following values when integrated over any period of approximately 3 seconds:

   p – 20 dB in the band 4 to 8 kHz,

   p – 40 dB in the band 8 to 12 kHz,

   p – 60 dB in each 4-kHz band above 12 kHz.

3) The frequencies emitted by the transducer shall be such as not to interfere with national and international telephone signalling systems and pilot signals involved in the telephone connection envisaged.

4) Adequate protection shall be provided in the transducer to avoid causing any dangerous electric potential and currents to the telephone system.

5) It shall not be possible to cause acoustic shock to telephone users under any normal condition or when the acoustic coupler develops any single fault.

6) The mechanical arrangements of the transducer shall not cause mechanical damage to the telephone instrument.

7) In addition to the contents of this Recommendation, the regulations of the national Administration must also be complied with.

2 that acoustically coupled equipment be compatible with "hard-wired counterparts" at the remote location to the extent that:

1) The characteristics of the equivalent V Series (V.21, V.23, etc.) modem line signals are complied with (otherwise communication will be impossible).

2) An equivalent V.24 interface is provided to the DTE, with the following exceptions:
   - circuit 108 is power ON indicator only, and cannot be used to control the connection of the modem to the line;
   - circuit 125 is inoperative; only manual answering can be accomplished.

3) Acoustically coupled modem equipment designed to operate with remote modems:
   - which have automatic answering capability, and
   - which are specifically dedicated and are adapted (by means of optionally extended answer tone duration) to working with acoustically coupled calling stations

   shall operate in the mode prescribed in Recommendation V.25, § 6 where placement of the telephone instrument handset on the acoustic coupler by the operator is tantamount to depressing a data button, as specified in § 6.

   These modems shall also comply with the response time requirements of circuits 106 and 109 as specified in the appropriate modem Recommendation.

Recommendation V.16

MEDICAL ANALOGUE DATA TRANSMISSION MODEMS

(Geneva, 1976)

The CCITT,

considering that

(a) computer-aided automatic ECG (electro-cardiogram) interpretation is being made available by special diagnostic centres to general practitioners and hospitals at remote places and suitable transmission equipment is necessary for this reason;

(b) such a service can be implemented to advantage in a special data collection system using simple remote stations and a high-quality central unit;

(c) for such applications particularly suitable and compatible transmission facilities are necessary which must not interfere with other telephone services;

(d) analogue as well as digitalized transmission of the analogue data (e.g. ECG records) are in principle possible;

(e) in most cases, however, on-line transmission with analogue transmission methods can be implemented more easily and economically;

(f) in practice, analogue transmission generally promises a sufficient degree of quality;

(g) in cases of emergency and monitoring of implanted pacemakers, very simple, acoustically coupled equipment may be of great assistance to the persons concerned;

unanimously declares the following view

1 Analogue transmission of medical analogue data, e.g. ECGs, should be permitted in the public telephone network. Reliable, sufficiently interference-free transmission cannot be taken for granted on every connection or route. Therefore, it is necessary to test the connections under consideration before such a service is definitely introduced.

2 This service requires two basically different transmission devices (modems):

1) transmission equipment for simultaneous transmission of three ECG signals on a telephone channel from a remote station to the central station, preferably for direct galvanic coupling to the telephone channel;

2) transmission equipment, preferably for emergency use and for monitoring of implanted pacemakers, to simultaneously transmit only one ECG signal from a remote station to a central station with acoustic or galvanic coupling to a telephone channel.

The ECG station usually consists of an ECG recorder, including separating amplifier, data input/output device and the modem specified in this Recommendation (see Figure 1/V.16).

The central station usually comprises the central modem specified herein and the interpretation system for ECGs (e.g. a computer programmed for ECG interpretation).

This Recommendation covers the modems, the desired transmission characteristics of the ECG transmission channel as well as the necessary interchange circuits and the method of transmitting the digital data associated with the ECG (e.g. patients' identification codes, control signals in both transmission directions and the interpretation record).

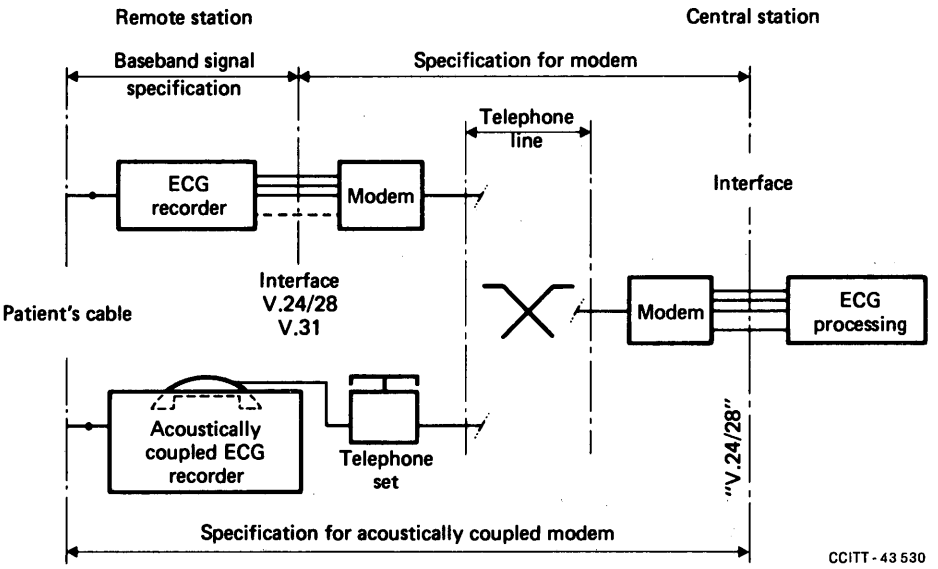


FIGURE 1/V.16

Example of analogue transmission of medical analogue data

3 Modems for simultaneous analogue transmission of three ECG records

3.1 *Basic characteristics of the analogue channels*

The equipment specified below is mainly intended for operation with direct galvanic coupling to telephone lines.

3.1.1 *Baseband signal*

Baseband signal requirements at the modem input:

– number of simultaneously transmitted ECG records	3
– frequency response of the separating amplifier	flat
– signal-to-noise ratio with 10 Hz square wave signals ± 1 V	⩾ 50 dB (unweighted)
– full scale limit (see Note 1)	± 2.5 V
– linearity deviation of an ECG channel related to full scale and the optimum straight line	1%
– permissible group delay distortion of the input signal at the modulator input (including channel filter in the baseband)	from 3 to 60 Hz $\Delta\tau \leqslant 2$ ms (outside this range, see Figure 2/V.16)
– spectrum: if a.c. coupling is applied, a time constant of $\tau = 3.2$ s, corresponding to a lower cut-off frequency of 0.5 Hz, should be used.	
– baseband pre-emphasis (see Note 2) (between separating amplifier and modem)	rise of 6 dB/octave; cut-off frequency: 15 Hz

Note 1 – Existing instruments (ECG recorders, etc.) are designed for ± 2.5 V full scale. If, however, the International Electrotechnical Commission specifies ± 1 V or ± 1.25 V as the full scale limit, this value should be adopted. The slope of the modulator characteristic (see § 3.1.2 below) must then be adjusted accordingly.

Note 2 – This value will require further study if, at a later date, amplitude compandors are used to improve the signal-to-noise ratio.

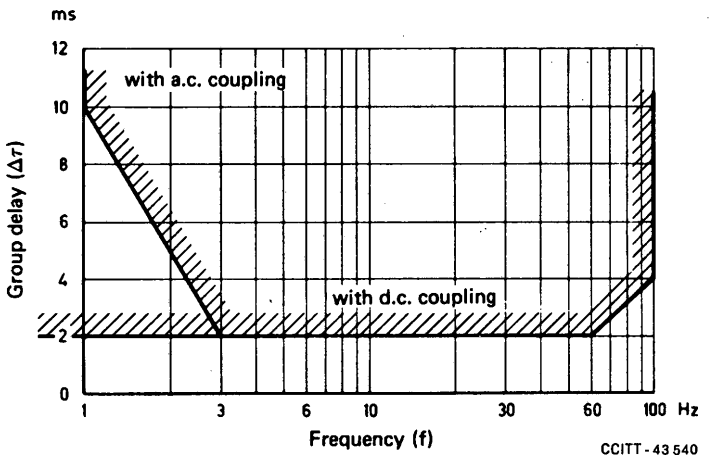


FIGURE 2/V.16

Permissible group-delay distortion in the baseband

3.1.2 *Requirements for the transmission equipment (modems)*

The modem should be capable of transmitting baseband signals with a bandwidth of up to approximately 100 Hz. The transmission equipment (modems) should not deteriorate the performance of the baseband signal as specified under § 3.1.1 above by more than 10%. The exact value of the admissible deterioration needs further study.

Since the centre channel of the transmission equipment will in future be used for digital transmission of ECG-associated digital data and other biological data, it must be capable of transmitting d.c. components. The same should apply to the other channels.

– *line signals* for transmitting the ECG:	signals as specified under § 3.1.1 above
– modulation method:	frequency modulation
– subcarrier frequencies f_n and associated maximum transmission levels p_n:	
f_1 = 950 Hz ± 6 Hz f_2 = 1400 Hz ± 15 Hz (see Note 1) f_3 = 2100 Hz ± 15 Hz	p_1 = 7 dB p_2 = 5 dB p_3 = 3 dB lower than the resulting level p_0 as specified in Recommendation V.2
– resulting maximum level:	p_0 as specified in Recommendation V.2
– simultaneous transmission of all three subcarriers is mandatory, if subcarriers f_1 and/or f_3 are used.	
– maximum frequency deviation per channel in the case of linear operation:	Δf = ± 100 Hz
– slope of the modulator characteristic (subcarrier deviation sensitivity):	40 Hz/V (see Note 2)
– a positive signal should cause a rise in the subcarrier frequency	
– FM channel bandwidth (3 dB points):	⩽ 350 Hz
– resulting level accepted by receiver (upper threshold-level):	– 6 dBm to –43 dBm
– lower threshold level:	–46 dBm

Note 1 – This frequency selection makes allowance for the following boundary conditions:

a) best possible decoupling between the three ECG channels. Nonlinear distortion may cause a small degree of cross-talk;

b) CCITT standardized subcarrier frequencies (2100 Hz and 1400 Hz) should be used as far as possible;

c) no interference to existing CCITT signalling systems by simulation of switching signals.

Some of the existing ECG transmission systems use subcarrier frequencies f_1 = 1075 Hz, f_2 = 1935 Hz, f_3 = 2365 Hz. Due to the relatively slow modulation by ECGs, the modulated subcarrier frequencies f_2 and f_3 may simulate signals of CCITT Signalling Systems No. 2 and No. 4. This would cause interference to the ordinary telephone service. Where this kind of interference is not to be expected, use of the subcarrier frequencies concerned should be allowed over a transition period covering two CCITT study periods. Thereafter, the aforementioned frequencies (950 Hz, 1400 Hz and 2100 Hz) only should be used in the interest of mutual compatibility of the ECG transmission systems from different suppliers.

Note 2 – This value should be changed to 100 Hz/V, or 80 Hz/V if the full-scale voltage of ± 1 V or ± 1.25 V (see § 3.1.1 above) is applied.

3.2 *Forward digital data transmission from the remote station to the central station*

The analogue centre channel with a subcarrier frequency f_2 = 1400 Hz should be used for transmission of ECG-associated digital data. Channel characteristics are:

– centre frequency:	f_2 = 1400 Hz (see Note)
symbol 1, (mark):	$f_z = f_2 - 80$ Hz
symbol 0, (space):	$f_a = f_2 + 80$ Hz
– coding:	International Alphabet No. 5 as indicated in Recommendations V.3 and V.4, with start/stop transmission
– nominal modulation rate:	100 bauds
– power level:	$p_2 \leqslant -11$ dBm

Note – In addition to the aforementioned signalling system, the following systems for forward digital data transmission are also in use:

a) tri-level code, derived from frequencies $f_{1,2,3}$ and $f_{1,2,3}$ ± approximately 100 Hz;

b) serial code with f_1 = 1075 Hz ± 40 Hz and frequency shift keying (FSK);

c) signalling with push-button telephone frequencies as specified in Recommendation Q.23 [1].

These variants should be allowed to remain in use for a transition period of two study periods. Afterwards, only the above recommended version should be used in order to obtain mutual technical compatibility of the instruments. This should also apply to future developments.

3.3 *Digital transmission in the backward direction from the central station to the remote station*

In order to send back interpretation results, control signals, etc., a digital backward channel with the following parameters should be provided:

– modulation by frequency shift keying with the following frequencies:	
symbol 1 (mark):	f_z = 390 Hz (see Note)
symbol 0 (space):	f_a = 570 Hz
– nominal modulation rate:	200 bauds
– coding:	International Alphabet No. 5 as indicated in Recommendations V.3 and V.4, with start/stop transmission
– transmission level:	as specified in Recommendation V.2
– idle condition:	symbol 1 (mark), 390 Hz
– level accepted by receiver:	– 6 dBm to –40 dBm
– lower threshold level:	–46 dBm.

Note – f_z = 390 Hz is in accordance with Recommendation V.23. For single tone signalling, f = 389 Hz (EIA standard for tone signalling) should be allowed for a transition period of two study periods. Afterwards, the above CCITT standard should be applied.

3.4 *Calibration signal*

At the beginning of the ECG recording a standardized calibration signal can be transmitted from the ECG recorder. By transmitting the combination ENQ (0/5) of International Alphabet No. 5 to the remote station (ECG recorder) the central station should call up and repeat this calibration signal whenever desired.

3.5 *Quality control*

In order to monitor the transmission quality and eliminate those parts of the transmitted ECG which contain interference pulses, suitable monitoring measures should be provided in the central modem. If a part of the transmitted ECG is disturbed, the central unit should send the signal DEL to the remote station.

A 40-dB signal-to-noise ratio in the baseband ECG channel is provisionally recommended as threshold level. The exact value needs further study.

3.6 *Interchange circuits*

The following interchange circuits should be optional. If interchange circuits are required, the following circuits should be provided:

3.6.1 *Interchange circuits between recording system and remote station modem*

If interchange circuits are necessary between the recorder and the modem, their functions should be in accordance with Recommendation V.24, and their electrical values in accordance with Recommendation V.28 or V.31, except circuits carrying analogue signals.

3.6.2 *Interchange circuits between the central modem and the interpretation system*

If these interchange circuits are necessary, they should also be in accordance with Recommendations V.24 and V.28.

The choice of the required interchange circuits needs further study.

3.7 *Procedures*

The required procedures also need further study with respect to mutual compatibility, echo suppressor disabling, answering tones, etc.

Note – A frequency scheme of subcarrier frequencies and associated digital channels is given in Figure 3/V.16.

4 Modem for simultaneous analogue transmission of one ECG record

4.1 *General*

This specification enables single channel equipment for direct galvanic coupling or acoustic coupling to be designed which is compatible with the centre channel of the three-channel transmission equipment described in § 3 above.

4.2 Baseband signal when transmitting from the remote station to the central unit as specified in § 3.1.1 above but with the following amendments to be made to the parameters of the line signals:

- frequency: f_2 = 1400 Hz;
- power level: $p_2 \leqslant -6$ dBm.

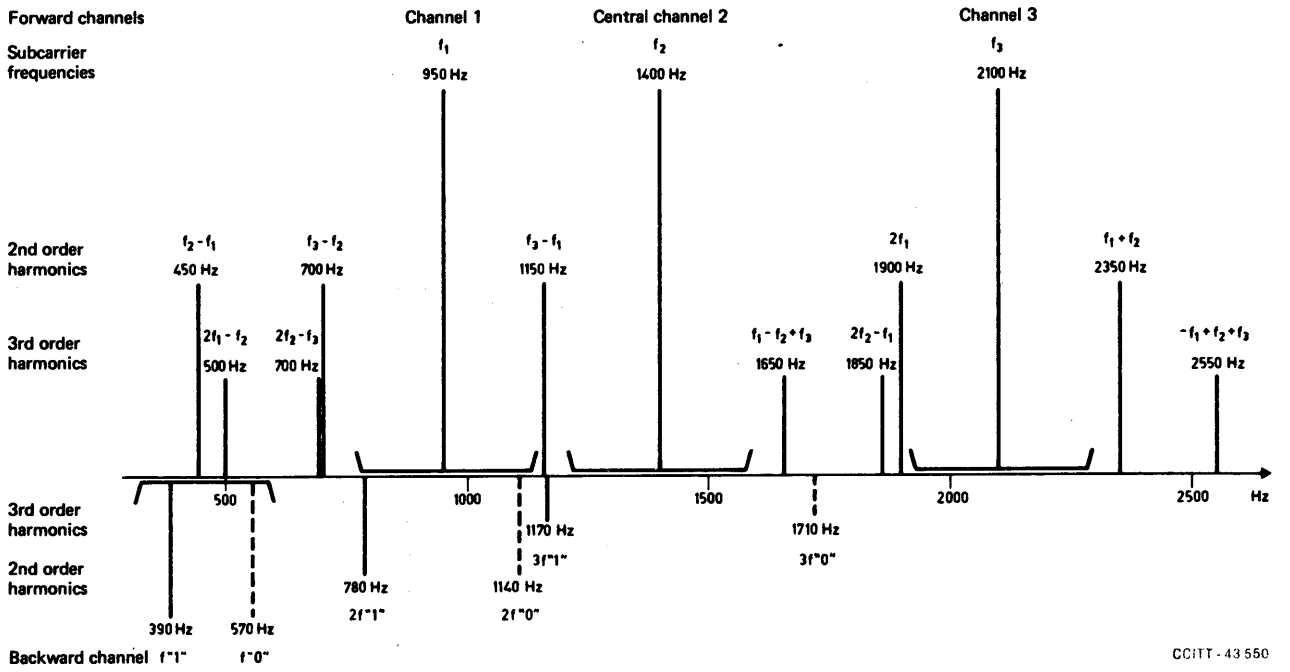


FIGURE 3/V.16

Frequency scheme of subcarrier frequencies and associated digital channels

In the case of acoustic coupling the above power level should not be exceeded at the output of the telephone set. The full scale limit may be extended to ± 5 mV. Linear operation is required up to ± 2.5 mV in this case. The slope of the modulator characteristic should be 40 Hz/mV for linear operation. These parameters are related to the patient's cable.

4.3 *Digital transmission in the forward direction*

Due to the limited number of possible applications, the use of the digital forward transmission channel should be optional. If provided, it should be in accordance with the digital transmission method described under § 3.2 above.

4.4 *Digital transmission in the backward direction*

The use of the digital backward channel should be optional. If provided, it should be in accordance with § 3.3 above. If no digital backward channel is provided, the answering tone (389 Hz) should be sent.

4.5 *Single channel central modem*

If required, a single channel central modem for direct galvanic coupling to the telephone line can also be designed with the parameters of the centre channel. The maximum deviation may be extended to 200 Hz. Here, all means for transmission of ECG-associated digital data are optional. If provided, they should be in accordance with the digital transmission method described under §§ 3.2 and 3.3 above.

Reference

[1] CCITT Recommendation *Technical features of push-button telephone sets*, Vol. VI, Rec. Q.23.

Recommendation V.19

MODEMS FOR PARALLEL DATA TRANSMISSION USING TELEPHONE SIGNALLING FREQUENCIES

(Geneva, 1976; amended at Malaga-Torremolinos, 1984)

Systems for parallel data transmission can be used economically when the transmitting sets (outstations) use the signalling frequencies of push-button telephone sets to transmit data to a central receiving set (instation) via the switched telephone network.

1 Scope

In many networks, the introduction of keyboard telephone sets allows simple, one-way data transmission at speeds up to about 10 characters per second to be made from a large number of push-button telephone sets serving as outstations to a common instation, via the general switched telephone network. Transmissions in the instation-to-outstation direction are generally confined to simple acoustic signals and voice replies.

The CCITT therefore

unanimously recommends

that the modems to be used for stations operating in the general switched telephone network should meet the specifications shown below.

2 General characteristics

2.1 *Data channel*

The transmission system uses two sets of frequencies in accordance with Recommendation Q.23 [1]. Each character is transmitted in the form of two simultaneously transmitted frequencies. These two frequencies belong to two separate sub-assemblies. Each of these two assemblies consists of four frequencies ["2 (1/4)" code]. This coding can thus be used to transmit 16 different character combinations and perhaps more (see Note).

The actual transmission consists in sending a frequency pair for a time greater than 30 ms, followed by a silence period of not less than 25 ms.

Note – In order to stretch the set of characters, several frequency pairs may be transmitted before the silence period. It should be noted that in this case character coding and decoding will not be effected by the DCE but by the DTE.

2.2 *Backward channel*

The following possibilities might be considered:

a) a telephone channel not simultaneous with data transmission in the forward direction;

b) a backward channel for audible signalling;

c) a backward channel for electrical signalling.

Possibilities b) and c) are provided on a basis of non-simultaneity or, optionally, simultaneity with the data transmission channels in the forward direction.

A loudspeaker will be built into the outstation modem. Optionally, a continuous signalling output may be provided. If the national regulations permit, an output for response to the channel may also be provided as an option.

3 Frequency assignments

3.1 *Data transmission channel*

The 2 groups of 4 frequencies specified in Recommendation Q.23 [1] are defined as follows:

– low group frequencies: 697, 770, 852, 941 Hz;

– high group frequencies: 1209, 1336, 1477, 1633 Hz.

The frequency pairs are assigned to the different digits as shown in Table 1/V.19.

TABLE 1/V.19

	B_1 = 1209 Hz	B_2 = 1336 Hz	B_3 = 1477 Hz	B_4 = 1633 Hz
A_1 = 697 Hz	1	2	3	A
A_2 = 770 Hz	4	5	6	B
A_3 = 852 Hz	7	8	9	C
A_4 = 941 Hz	*	0	#	D

3.2 *Backward channel*

For audible signals and electrical signalling, the backward channel frequency will be 420 Hz. This frequency may be amplitude-modulated at a rate of up to 5 bauds.

Use may also be made of an FM backward channel similar to that of the Recommendation V.23 type modem, or of the No. 2 transmission channel of a Recommendation V.21 type modem (if the frequency 1633 Hz is not used). These two types of backward channel may be used at the same time as the data frequencies in the forward direction; the use of these backward channels is optional.

4 Tolerances

4.1 *Data frequency tolerances*

The data frequency tolerances are defined in Recommendation Q.23 [1]; the difference between each frequency and its nominal frequency must not exceed ± 1.8% of the nominal frequency. Apart from this tolerance of ± 1.8% on transmission, the instation receiver should be able to accept a difference of ± 6 Hz due to the carrier systems.

4.2 *Frequency tolerance on backward channel*

The tolerance of 420 Hz on the backward channel should be ± 4 Hz; the receiver of the outstation should also be able to accept a difference of ± 6 Hz due to the carrier systems.

5 Line power levels

On the basis of Recommendation V.2, the following maximum power levels are recommended for each frequency transmitted, measured at the relative zero point:

– 13 dBm0 for the data transmission channel without the simultaneous backward channel;

– 16 dBm0 for the data transmission channel with the simultaneous backward channel;

– 10 dBm0 for the non-simultaneous backward channel;

– 16 dBm0 for the simultaneous backward channel.

6 Power levels on reception

In view of the provision of Recommendation V.2 and the statistical values of the maximum transmission loss between subscribers, it is recommended that the instation receiver should be able to detect frequency pairs received at – 45 dBm.

Note – Studies should be continued with a view to permitting levels on reception below – 45 dBm.

7 Character reception

A character will be detected and delivered to the DTE interface if, and only if, the two frequencies corresponding to the character are detected and are stable for at least 10 ms.

The silent period will be detected and delivered to the DTE interface if no frequency belonging to the code appears for at least 10 ms.

Note – During silent periods, the microphone of the telephone set is connected to the telephone line, so that interfering signals (ambient noise, speech) may be received. The receiver must be fitted with devices capable of distinguishing between these interfering signals and data signals (speech protection). It would be advisable to study further the method of assessing receiver response to the simulation of data signals by interfering signals. A reproducible test signal should be defined, so that comparable measurements can be made.

8 Detection of line signal received on the data channel

Circuit 109 must be in the ON position when a character is received; the circuit may be switched from ON to OFF:

1) on detection of the silent period;

2) after a time-out of 60 ± 10 ms following detection of the silent period.

9 Timing for characters received

By its very principle, the system is asynchronous; however, it may be useful to provide the DTE, on an optional basis, with a signal which indicates the sampling times of the data wires. In this case, it is advisable to use circuit 131, which will switch from OFF to ON when the character reaches the interface, and then back to OFF after a time T. This time will be chosen in such a way that the data are stable at the DTE interface.

The value T = 15 ms may be recommended by way of example.

This clock may optionally be disabled on reception of a silent period.

10 Interface of instation modem

The functional characteristics of the interchange circuits concerned are as defined in Recommendation V.24 (see Note 1).

10.1 *List of interchange circuits concerned*

102 Signal ground or common return

104 Received data [8 circuits. These circuits are designated A_1, A_2 ... B_4 according to their correspondence with the relevant frequency in Table 1/V.19 (see Note 2 below)]

105 Request to send (see Note 3 below)

107 Data set ready

108/1 Connect data set to line (see Note 4 below)

108/2 Data terminal ready (see Note 4 below)

109 Data channel received line signal detector

125 Calling indicator

130 Transmit backward tone

191 Transmitted voice answer (see Note 3 below)

The following interchange circuits are optional:

110 Data signal quality detector

131 Received character timing

Note 1 – Manufacturers who marketed a modem of this type prior to the publication of this Recommendation may regard the interface defined in this paragraph as optional.

Note 2 – To make the interface compatible with the relevant specifications of Recommendation V.20, the combination A_4, B_4 may be transmitted on circuit 104 instead of a pause ("1" on all circuits), provided circuit 107 is in the ON position and circuit 105 is in the OFF position. This simulated idle combination is optional.

Note 3 – These circuits are required if the "telephone channel" facility is provided in the modem. The electrical characteristics of interchange circuit 191 are still under study.

Note 4 – Circuit 108 must be available either as circuit 108/1 – *Connect data set to line*, or as circuit 108/2 – *Data terminal ready.*

10.2 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

11 Interface of outstation modems

In view of the purpose of these modems, which are or will be more or less integrated in economic terminals, the specification of the interface is liable to result in a much higher equipment cost. Hence no interface is recommended.

Reference

[1] CCITT Recommendation *Technical features of push-button telephone sets*, Rec. Q.23.

PARALLEL DATA TRANSMISSION MODEMS STANDARDIZED FOR UNIVERSAL USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

(former Recommendation V.30, Mar del Plata, 1968;
amended at Geneva, 1972 and 1980, and at Malaga-Torremolinos, 1984)

There is a need for one-way data transmission systems where a large number of low-cost sending stations (outstations) transmit to a central receiving station (instation) over the switched telephone network.

The following systems are desired:

a) transmitting 16-character combinations;

b) transmitting 64-character combinations;

c) transmitting 256-character combinations.

In most cases a character signalling rate of 20 characters per second will be sufficient; 40 characters per second may be required for some applications of the 16-character combination system.

The transmission from the instation to the outstations is limited either to simple acknowledgement signals (data collection systems) or to analogue signals (voice-answering systems).

The use of normal push-button telephone sets in the outstation for some of these applications may be of advantage for the user. However, it is recognized that for the time being on some telephone systems there exist certain limitations in the frequency band 600 to 900 Hz. This is due to the characteristics of the telecommunication path, such as signalling frequencies and metering pulses. Therefore, for a universal system the frequency band of the data channel is 900 to 2000 Hz, which excludes the use of the normal push-button telephone set.

A so-called parallel data-transmission system using two or three times one out of four frequencies can fulfil the above requirements.

For these reasons, the CCITT

unanimously declares the following

1 Parallel data-transmission systems can be used economically when a large number of low-cost sending stations (outstations) wish to transmit to a central receiving station (instation) over the switched telephone network (or on leased telephone circuits).

Apart from the possibility of the use, on a restricted scale, of a system that is compatible with multifrequency push-button telephone signalling devices, the following system is recommended as a universally applicable system for the switched telephone circuits.

2 Facilities

2.1 *Data channel*

The basic system has a maximum of 16-character combinations and a modulation rate of up to 40 bauds. This permits a character signalling rate of up to 20 characters per second when an inter-character rest condition is used, or up to 40 characters per second with the use of a binary timing channel. This basic system consists of two groups of four frequencies, one frequency from each group being transmitted simultaneously (two times one out of four).

The basic system includes provision for expansion up to 64-character combinations by the addition of a third four-frequency group (three times one out of four). No use is foreseen for the system with 64-character combinations at character signalling rates above 20 characters per second, within this class of inexpensive parallel transmission equipment.

An expansion of the basic system to cater for 256 characters (up to 20 characters per second) is achieved by using only two groups for the conveyance of data, each character being transmitted in two sequential parts. The two half characters are positively identified by the two different conditions of a binary channel. The timing channel mentioned above is recommended to be used for this purpose.

Where an inter-character rest condition is required the full number of frequency combinations in the modem will not be available to the user as character combinations:

a) with the 16-frequency combination system, only 15 characters will be available unless a timing channel is used from frequency group B;

b) with the 64-frequency combination system only 63 characters are available.

These recommended systems have an inherent transmission error-detecting capability.

2.2 *Backward channel*

Provision is made for the following facilities:

a) a speech channel non-simultaneous with forward data;

b) a backward channel for audible signalling;

c) a backward channel for electrical signalling purposes.

Facilities b) and c) are provided, either non-simultaneous or optionally simultaneous with the forward data channels.

A loudspeaker will be provided in the outstation modem. On an optional basis a d.c. signalling output will be provided. If national regulations permit, a voice-answering output will also be provided on an optional basis.

3 Frequency allocations

3.1 *Data channels*

Frequency allocations and designations as shown in Table 1/V.20 are recommended.

TABLE 1/V.20

Group \ Channel No.	1	2	3	4
A	920 Hz	1000 Hz	1080 Hz	1160 Hz
B	1320 Hz	1400 Hz	1480 Hz	1560 Hz
C	1720 Hz	1800 Hz	1880 Hz	1960 Hz

For the basic 16-character system only groups A and C are used.

If an inter-character rest condition is used, during the time no input data circuits are operated, rest frequencies are sent to line. The highest frequency in each group is recommended to be the rest frequency.

3.2 *Timing channel*

If a timing channel is provided in the 16-character system this should consist of a selected pair of group B frequencies. The recommended frequencies are F_{B2} = 1400 Hz and F_{B3} = 1480 Hz.

In the case where this timing channel will be used to identify the two halves of the character in the 256-character system, the higher frequency is transmitted simultaneously with the first half of the character.

No timing channel is provided in the 64-character combination system.

3.3 *Backward channel*

For the backward channel, two non-exclusive options exist.

3.3.1 *Amplitude modulated 5 bit/s backward channel*

The frequency of the amplitude modulated backward channel for audible and electrical signalling shall be 420 Hz. This tone may be amplitude modulated at rates of up to 5 bit/s.

3.3.2 *Frequency modulated 75 bit/s backward channel*

The modulation rate and characteristic frequencies for this backward channel are as follows:

	[F_Z] [(symbol 1,] [mark)]	[F_A] [(symbol 0,] [space)]
Modulation rate up to 75 bauds	420 Hz	480 Hz

In the absence of any signal on the backward channel interface, the condition *Z* signal is to be transmitted.

The frequency modulated backward channel can be used simultaneously with the forward data frequencies.

3.4 *Tolerances*

The tolerances on both data and backward frequencies should be ± 4 Hz.

The receiver should cater for ± 6 Hz difference due to carrier systems in addition to the transmitter tolerance of ± 4 Hz.

4 Power levels

Based on Recommendation V.2 the following maximum power levels measured at the zero relative level point are recommended for each transmitted frequency:

4.1 *Data and timing channels*

4.1.1 16-character system without timing channel and with a non-simultaneous backward channel: −13 dBm0.

4.1.2 All other cases: −16 dBm0.

4.2 *Backward channel*

4.2.1 Non-simultaneous: −10 dBm0.

4.2.2 Simultaneous: −16 dBm0.

In systems where either the simultaneous or the non-simultaneous backward channel is used, all power levels should be −16 dBm0.

The maximum difference between any data tone at the transmitter terminal should be 1 dB.

5 Threshold levels of the data channel received signal detector

When the level of the received signal in group C exceeds −49 dBm, circuit 109 shall be ON. When the level of this received signal is less than −54 dBm, circuit 109 shall be OFF. The detector circuit which causes circuit 109 to turn ON or OFF shall exhibit hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for the ON to OFF transition.

Group C was chosen for this purpose because it is the most critical from a received level point of view.

6 Threshold levels on the backward channels

The expected minimum level is for the amplitude modulated backward channel is −45 dBm for the 420 Hz tone. This information is provided to assist equipment manufacturers.

Level of the received line signal of the frequency modulated backward channel:

greater than −43 dBm circuit 122 ON

less than −48 dBm circuit 122 OFF.

The condition of circuit 122 for levels between −43 dBm and −48 dBm is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

7 Instation modem interface

The functional characteristics of interchange circuits comply with Recommendation V.24.

7.1 *List of interchange circuits:*

102 Signal ground or common return

104 Received data [12 or 8 circuits depending on whether Group B is provided or not. These received data circuits are designated A1, A2 ... C4, each corresponding to its relevant frequency (see Table 1/V.20)]

105 Request to send (see Note 2)

107 Data set ready

108/1 Connect data set to line (see Note 1)

108/2 Data terminal ready (see Note 1)

109 Data channel received line signal detector

118 Transmitted backward channel data (see Note 2)

120 Transmit backward channel line signal (see Note 2)

121 Backward channel ready (see Note 2)

125 Calling indicator

130 Transmit backward tone (see Note 3)

191 Transmitted voice answer (see Note 4)

The following optional interchange circuits may be provided:

110 Data signal quality detector

124 Select frequency groups

131 Received character timing

Note 1 – This circuit shall be capable of use as circuit 108/1 – *Connect data set to line* or circuit 108/2 – *Data terminal ready*, depending upon its use.

Note 2 – These circuits are required if the 75 bit/s frequency modulated backward channel is provided in the modem. See also Note 4.

Note 3 – This circuit is required if the 5 bit/s amplitude modulated backward channel is provided in the modem.

Note 4 – These circuits are required if the speech channel facility is provided in the modem. The electrical characteristics of interchange circuits 191 and 192 are left for further study. The pin allocation on the interface connector is the same for circuits 191A and 121 and 191B and 118, respectively. If both the speech channel and the 75 bit/s backward channel are provided in the modem, means have to be provided to switch between those circuits.

7.2 The electrical characteristics of the interchange circuits comply with Recommendation V.28.

Data circuits: when the frequency corresponding to the circuit is ON, the appropriate interchange circuit will be negative. When the frequency in this channel is OFF, the interchange circuit will be positive.

For timing purposes in the 256-character system, a single interchange circuit is selected from Group B so that positive polarity indicates the first half of the character period and a negative polarity indicates the second half of the character.

8 Outstation modem interface

The functional characteristics of interchange circuits comply with Recommendation V.24.

8.1 *List of essential interchange circuits:*

102 Signal ground or common return (see Note 4)

103 Transmitted data (nine or six circuits depending on whether Group B is provided or not). These circuits are designated A1, A2 ... C3, each corresponding to its relevant frequency (see Table 1/V.20)

105 Request to send

129 Request to receive

8.2 The following optional interchange circuits may be provided:

107 Data set ready

108/1 Connect data set to line

108/2 Data terminal ready

119 Received backward channel data (see Note 1)

122 Backward channel received line signal detector (see Note 2)

125 Calling indicator

192 Received voice answer (see Note 3)

When the optional timing channel is used then the appropriate data circuits are operated.

Note 1 – The electrical characteristics for this circuit are for further study. See also Note 4.

Note 2 – This circuit carries the data of the 5 bit/s amplitude modulated backward channel, if provided.

Note 3 – See § 7.1, Note 4 above.

Note 4 – The transmitted data circuits (103) will all use the same common return (102). The control circuits may operate each on their own return circuit. The pin allocation on the interface connector is the same for circuits 192 and 119. If both the speech channel and the 75 bit/s backward channel are provided in the modem, means have to be provided to switch between those circuits.

8.3 *Electrical characteristics*

The data and control interchange circuits at the outstation will be operated by the opening or closing of contacts carrying only direct current. The electrical characteristics of interchange circuits comply with Recommendation V.31, except circuit 119. The electrical characteristics for this interchange circuit are for further study.

9 Correspondence for each group (Table 2/V.20)

TABLE 2/V.20

At outstation closing of circuit	Number of the channel on line	At instation negative polarity on circuit
1	1	1
2	2	2
3	3	3
None	4	4

Not more than one circuit per group may be closed at a time.

10 Character set

This Recommendation includes the allocation of transmission frequencies to the interchange circuits.

The allocation of interchange circuits to the code combinations to be transmitted, i.e. definition of a character set, must conform to the conditions defined in this Recommendation and must take into account the application requirements and the type of input media (paper tape, punched cards, keyboards, etc.).

For this reason the recommendation for a character set is primarily for ISO in collaboration with CCITT.

Note – Examples of alphabets and coding methods are given in references [1], [2], [3] and [4].

References

[1] *Coding methods for parallel transmission*, White Book, Vol. VIII, Supplement 20, ITU, Geneva, 1969.

[2] *Proposals of coding for parallel transmission*, White Book, Vol. VIII, Supplement 21, ITU, Geneva, 1969.

[3] *Parallel transmission on switched telephone circuits*, Blue Book, Vol. VIII, Supplement 56, ITU, Geneva, 1964.

[4] *Low-speed parallel data sets*, Blue Book, Vol. VIII, Supplement 57, ITU, Geneva, 1964.

Recommendation V.21

300 BITS PER SECOND DUPLEX MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK[1)]

(Geneva, 1964; amended at Mar del Plata, 1968, and at Geneva, 1972, 1976 and 1980, and at Malaga-Torremolinos, 1984)

Note – The modem, designed for use on connections set up by switching in the general telephone network, can obviously be used on leased lines.

A system of data transmission at a low data signalling rate, such that data could be transmitted over a telephone circuit operated alternatively for telephone calls and data transmissions, using simple input/output equipment and easy operating procedures, would be economical.

The data signalling rate must be such as to allow the use of current types of data sources and sinks, especially electromechanical devices.

The system for data transmission will be duplex, either for simultaneous two-way data transmission or for the transmission of signals sent in the backward direction for error-control purposes. The transmission must be such that use can be made of normal telephone circuits, and this applies both to the bandwidth available and to the restrictions imposed by signalling in the telephone networks.

The two correspondents are brought into contact by a telephone call, and the circuit is put into the data-transmission position:

a) manually by agreement between the operators, or

b) automatically.

[1)] See Note under § 2 of this Recommendation.

For these reasons, the CCITT

unanimously declares the following view

1 Data transmission may take place at low data signalling rates on telephone calls set up on switched telephone circuits (or on leased telephone circuits).

2 The communication circuit for data transmission is a duplex circuit whereby data transmission in both directions simultaneously is possible at 300 bit/s or less.

The modulation is a binary modulation obtained by frequency shift, resulting in a modulation rate being equal to the data signalling rate.

Note – Attention is drawn to the fact that there may be in operation some old-type V.21 modems for which the maximum data signalling rate is 200 bit/s.

3 For channel No. 1, the nominal mean frequency is 1080 Hz.

For channel No. 2, it is 1750 Hz.

The frequency deviation is ± 100 Hz. In each channel, the higher characteristic frequency (F_A) corresponds to a binary 0.

The characteristic frequencies[2)] as measured at the modulator output must not differ by more than ± 6 Hz from the nominal figures.

A maximum drift frequency of ± 6 Hz is assumed for the line. Hence the demodulation equipment must tolerate drifts of ± 12 Hz between the frequencies received and their nominal values.

4 Data may be transmitted by synchronous or asynchronous procedures. With synchronous operation, the modem will not have to provide the signals which would be necessary to maintain synchronism when transmission is not proceeding.

5 When echo control device disabling is required, it is recommended that the procedures specified in Recommendation V.25 be followed.

6 The maximum power output of the modem into the line shall not exceed 1 mW.

The power level of the modem should be adjusted to make allowance for loss between this equipment and the point of entry to an international circuit, so that the corresponding nominal level of the signal at the international circuit input shall not exceed −13 dBm0 (see Recommendation V.2, § 2).

7 a) When both channels are used for simultaneous both-way data transmission, channel No. 1 is used for transmission of the caller's data (i.e. the person making the telephone call) towards the called station, while channel No. 2 is used for transmission in the other direction.

b) When one channel is used for data transmission and the other is used for transmission of check signals, service signals, etc., only, it is channel No. 1 which is used for transmission from the calling to the called station regardless of the direction in which the data are transmitted.

c) The procedure for the assignment of the channels described under a) and b) above applies in the case of the general service of data transmission, making it possible to transmit data or check signal, service signal, etc., bilaterally between any two subscribers. In special cases which do not come under this rule, the procedure of assignment of the channels is determined by the prior agreement between the correspondents, bearing in mind the requirement proper to each service.

[2)] The nominal characteristic frequencies;
channel No. 1 (F_A = 1180 Hz and F_Z = 980 Hz);
channel No. 2 (F_A = 1850 Hz and F_Z = 1650 Hz).

8 Interchange circuits

8.1 *List of interchange circuits essential for the modems when used on the general switched telephone network or non-switched leased telephone circuits* (see Table 1/V.21)

The configurations of interchange circuits are those essential for the particular switched network or leased circuit requirement indicated. Where one or more of such requirements are provided in a modem, then all of the appropriate interchange circuit facilities should be provided.

TABLE 1/V.21

Interchange circuit		General switched telephone network including terminals equipped for manual calling, manual answering, automatic calling, automatic answering (Note 1)	Non-switched leased telephone circuits (Note 1)	
Number	Designation		Point-to-point	Multipoint
102	Signal ground or common return	X	X	X
103	Transmitted data	X	X	X
104	Received data	X	X	X
105	Request to send	–	X (Note 2)	X
106	Ready for sending	X	X	X
107	Data set ready	X	X	X
108/1	Connect data set to line	X (Note 3)	X	X
108/2	Data terminal ready	X (Note 3)	X (Note 4)	–
109	Data channel received line signal detector	X	X	X
125	Calling indicator	X	–	–
126	Select transmit frequency	–	–	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommandation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 9).

Note 2 – Circuit 105 is not required when alternate voice/data service is used on non-switched leased point-to-point circuits.

Note 3 – The circuit shall be capable of operation as circuit 108/1 – *connect dat set to line* or circuit 108/2 – *data terminal ready* depending ont its use.

Note 4 – In the leased point-to-point case, where alternate voice/data service is to be provided, circuit 108/2 may be used optionally.

8.2 *Response times of circuits 106 and 109*

8.2.1 *Definitions*

8.2.1.1 Circuit 109 response times are the times that elapse between the connection or removal of a tone to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuit 109.

The test tone should have a frequency corresponding to the characteristic frequency of binary 1 and be derived from a source with an impedance equal to the nominal input impedance of the modem under test.

The level of the test tone should fall into the level range between 1 dB above the actual threshold of the received line signal detector and the maximum admissible level of the received signal. At all levels within this range the measured response times shall be within the specified limits.

8.2.1.2 Circuit 106 response times are the times from the connection of an ON or OFF condition on:

- circuit 105 (where it is provided) to the appearance of the corresponding OFF or ON condition on circuit 106;
- circuit 109 (where circuit 105 is not provided) to the appearance of the corresponding ON or OFF condition on circuit 106.

8.2.2 *Response times*

TABLE 2/V.21

Circuit 106		
OFF to ON	20-50 ms (see Note 1)	400-1000 ms (see Note 2)
ON to OFF		⩽ 2 ms
Circuit 109		
OFF to ON	⩽ 20 ms (see Note 1)	300-700 ms (see Note 2)
ON to OFF		20-80 ms

Note 1 – These times are used on leased point-to-point networks without alternate voice data facilities and on leased multipoint facilities.

Note 2 – These times are used in the general switched network service and on leased point-to-point circuits with alternate voice data.

8.3 *Threshold of data channel received line signal detector*

Level of received line signal at received line signal terminals of modem for all types of connection, i.e. general switched telephone network or non-switched leased telephone circuit:

greater than −43 dBm circuit 109 ON

less than −48 dBm circuit 109 OFF

The condition of circuit 109 for levels between −43 dBm and −48 dBm is not specified except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than for the ON to OFF transition.

Where transmission conditions are known on switched or leased circuits, Administrations should be permitted at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

8.4 *Fault condition of interchange circuits*

See Recommendation V.28, § 7 for association of the receiver failure detection types).

8.4.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

8.4.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

8.4.3 All other circuits not referred to above may use failure detection type 0 or 1.

9 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

10 The following information is provided to assist equipment manufacturers:

a) The nominal range of attenuations in subscriber-to-subscriber connections is from 5 to 30 dB at the reference frequency (800 or 1000 Hz), assuming up to 35 dB attenuation at the frequency 1750 Hz.

b) The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

Reference

[1] CCITT Recommendation *Echo suppressors*, Vol. III, Rec. G.164.

Recommendation V.22

1200 BITS PER SECOND DUPLEX MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK AND ON POINT-TO-POINT 2-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1980; amended at Malaga-Torremolinos, 1984; and at Melbourne, 1988)

1 Introduction

1.1 This modem is intended for use on connections on General Switched Telephone Networks (GSTNs), and on point-to-point circuits when suitably conditioned.

The principal characteristics of this modem are as follows:

a) duplex operation on 2-wire GSTN and point-to-point leased circuits,

b) channel separation by frequency division,

c) differential phase shift modulation for each channel with synchronous line transmission at 600 bauds (nominal),

d) inclusion of a scrambler,

e) inclusion of test facilities.

1.2 Recognizing the wide range of application, this Recommendation provides for three alternative configurations. The choice of alternative is a matter for the Administration concerned. The facilities given by the alternatives are:

Alternative A

1200 bit/s synchronous
600 bit/s synchronous (optional)

Alternative B

1200 bit/s synchronous
600 bit/s synchronous (optional) } as in Alternative A

1200 bit/s start-stop
600 bit/s start-stop (optional)

Alternative C

1200 bit/s synchronous
600 bit/s synchronous (optional)
1200 bit/s start-stop
600 bit/s start-stop (optional) } as in Alternative B

An asynchronous mode having capability of handling 1200 bit/s start-stop and anisochronous data at up to 300 bit/s.

The selection of the asynchronous mode is made during the handshaking sequence (see § 6). This gives compatibility between Alternative B and Alternative C.

Note – The possibility of transmitting low speed anisochronous data in Alternatives A and B is left for further study.

2 Line signals

2.1 *Carrier and guard tone frequencies*

The carrier frequencies shall be 1200 ± 0.5 Hz for the low channel and 2400 ± 1 Hz for the high channel. A guard tone of 1800 Hz ± 20 Hz, to be transmitted only when the modem is transmitting in the high channel, may be disabled as a national option. An alternative guard tone of 550 ± 20 Hz may be incorporated as a national option. The question of international calls between countries requiring different guard tones is left for further study.

2.2 *Data and guard tone line signal levels*

The 1800-Hz guard tone shall be at a level of 6 ± 1 dB below the level of the data power in the high channel. The level of the optional 550 Hz tone is for further study. The total power transmitted to line shall be in accordance with Recommendation V.2 and shall be the same for transmission in either channel. Because of the 1800-Hz guard tone, the power level of data signals in the high channel will be approximately 1 dB lower than data signals in the low channel.

2.3 *Fixed compromise equalizer*

Fixed compromise equalization shall be incorporated in the modem. Such equalization shall be equally shared between transmitter and receiver. The characteristics of the equalizer shall be the responsibility of each Administration to recommend nationally. The possibility of producing compromise characteristics for international implementation is for further study.

2.4 *Spectrum* and *group-delay characteristic*

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal shall have a frequency spectrum equivalent to the square root of a raised cosine shaping with a 75% roll-off and within the limits of Figure 1/V.22. Similarly, the group delay of the transmitter output shall be within ± 150 microseconds over the frequency range 900 Hz-1500 Hz (low channel) and 2100 Hz-2700 Hz (high channel). These figures are provisional.

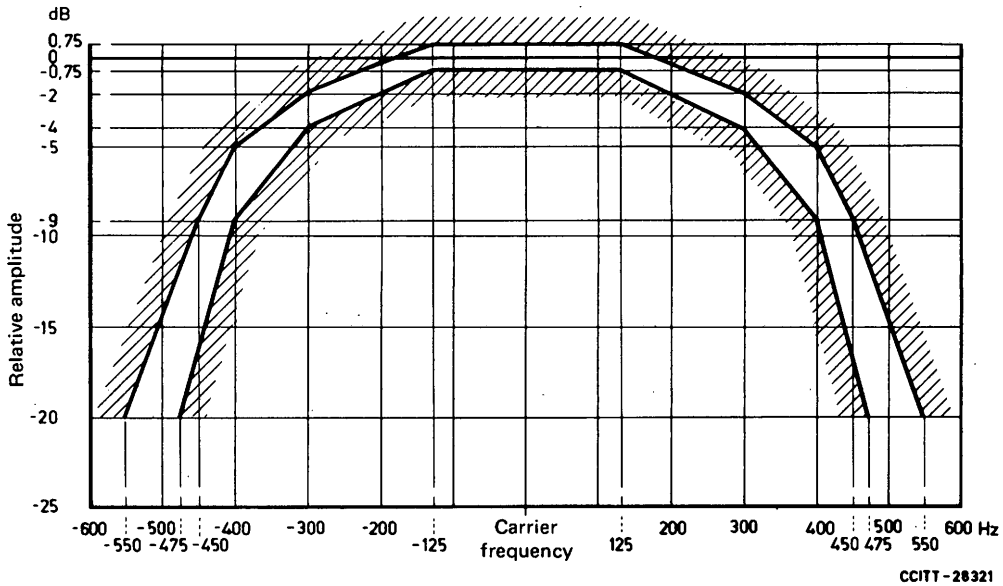


FIGURE 1/V.22

Amplitude limits for transmitted line signal (unequalized)

2.5 *Modulation*

2.5.1 *Data signalling rates*

Alternatives A and B: The data signalling rate transmitted to line shall be 1200 bit/s or 600 bit/s ± 0.01% with a modulation rate of 600 baud ± 0.01%.

Alternative C: In Modes i), ii), iii) and iv) (§ 4) the data signalling rates are as in Alternatives A and B. In Mode v), the data signalling rate transmitted to line shall be 1205 ± 1 bit/s with a modulation rate of 602.5 ± 0.5 baud. Optionally in Mode v), the line rate shall be 1223 ± 2 bit/s with a modulation rate of 611.5 ± 1 baud.

2.5.2 *Encoding of data bits*

2.5.2.1 *1200 bits per second*

The data stream to be transmitted shall be divided into groups of 2 consecutive bits (dibits). Each dibit shall be encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.22). At the receiver, the dibits shall be decoded and the bits reassembled in correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.22

Dibit values (1200 bit/s)	Bit values (600 bit/s)	Phase change (Modes i, ii, iii, iv)	Phase change (Mode v)
00	0	+ 90°	+270°
01	–	0°	+180°
11	1	+270°	+ 90°
10	–	+180°	0°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5.2.2 *600 bits per second*

Each bit shall be encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.22).

2.6 *Received signal frequency tolerance*

Noting that the frequency tolerance of the transmitter carriers is ± 1 Hz or less, and assuming a maximum shift of ± 6 Hz in the connection, the receiver shall be able to accept errors of at least ± 7 Hz in the received frequencies.

3 Interchange circuits

3.1 *Table of interchange circuits* (Note 1 of Table 2/V.22)

Essential and optional interchange circuits are listed in Table 2/V.22.

TABLE 2/V.22

Interchange circuits (Note 1)

Interchange circuit		Notes
No.	Description	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	Note 2
106	Ready for sending	
107	Data set ready	
108/1	Connect data set to line	Note 3
108/2	Data terminal ready	Note 3
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	Note 4
113	Transmitter signal element timing (DTE source)	Note 5
114	Transmitter signal element timing (DCE source)	Note 6
115	Receiver signal element timing (DCE source)	Note 6
125	Calling indicator	Note 7
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.5).

Note 2 – Some automatic calling equipments are designed to emit a calling tone to line by turning ON circuit 105 to the calling modem. The general switched telephone network (GSTN) constant carrier handshake is such that no calling tone will be emitted by the V.22 modem when used with these equipments.

Note 3 – This circuit shall be capable of operation as circuit 108/1 or 108/2 depending on its use.

Note 4 – This circuit is optional if only the 1200 bit/s speed [modes i) and ii) as defined in §§ 4.1, 4.2 and 4.3] is provided in the modem. If the 600 bit/s speed [modes iii) and iv)] is also provided, this circuit is essential.

Note 5 – When the modem is not operating in a synchronous mode any signals on this circuit shall be disregarded. Many DTEs operating in an asynchronous mode do not have a generator connected to this circuit.

Note 6 – When the modem is not operating in a synchronous mode, this circuit shall be clamped to the OFF condition. Many DTEs operating in an asynchronous mode do not terminate this circuit.

Note 7 – This circuit is for use with the general switched telephone network only.

3.2 *Circuits 106 and 109 response times* (see Table 3/V.22)

Circuit 106 response times are from the application of an ON or OFF condition on circuit 105. See also § 6 for operating sequences.

TABLE 3/V.22

	Constant carrier	Controlled carrier
Circuit 106		
OFF to ON	⩽ 2 ms	210 to 275 ms
ON to OFF	⩽ 2 ms	⩽ 2 ms
Circuit 109		
OFF to ON	105 to 205 ms	105 to 205 ms
ON to OFF	10 to 24 ms	10 to 24 ms

3.3 *Circuit 109 thresholds*

High channel threshold:

greater than −43 dBm — circuit 109 ON
less than −48 dBm — circuit 109 OFF

Low channel threshold:

greater than −43 dBm — circuit 109 ON
less than −48 dBm — circuit 109 OFF

The condition of circuit 109 between the ON and OFF levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than for the ON to OFF transition.

Circuit 109 thresholds are specified at the input to the modem excluding the effects of the compromise equalizer.

Circuit 109 shall not respond to the 1800-Hz or 550-Hz guard tones, or the 2100-Hz (nominal) answer tone during the handshake sequence.

Administrations are permitted to change these thresholds where transmission conditions are known.

3.4 *Circuit 111 and data rate control*

Data rate selection may be by switch (or similar means) or by circuit 111 or a combination of both.

The ON condition on circuit 111, where provided, shall select 1200 bit/s operation and the OFF condition shall select 600 bit/s operation.

3.5 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.6 *Fault condition of interchange circuits*

(See Recommendations V.28, § 7 for association of the receiver failure detection types.)

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection type 0 or 1.

4 Modes of operation over the DTE/DCE interface

4.1 *Alternative A*

The modem can be configured for the following modes of operation:

Mode i) 1200 bit/s ± 0.01% synchronous

Mode iii) 600 bit/s ± 0.01% synchronous (optional).

In these modes of operation, the modem shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or circuit 114. The data shall then be scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.2.

In addition to standard V.24 transmitter timing arrangements, the modem shall provide capabilities to derive transmit signal element timing from receiver signal element timing.

4.2 *Alternative B*

The modem can be configured for the following modes of operation:

Mode i) 1200 bit/s ± 0.01% synchronous

Mode ii) 1200 bit/s start-stop 8, 9, 10 or 11 bits per character

Mode iii) 600 bit/s ± 0.01% synchronous } optional

Mode iv) 600 bit/s start-stop 8, 9, 10 or 11 bits per character } optional

The synchronous modes are as given in Alternative A.

In the start-stop modes, the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of 1200 or 600 bits per second. The start-stop data to be transmitted shall be converted, in conformity with Recommendation V.14, to a synchronous data stream suitable for transmission in accordance with § 4.1

Demodulated data shall be decoded in accordance with § 2.5.2, then descrambled in accordance with § 5 and then passed to the converter in conformity with Recommendation V.14 for regaining the data stream of start-stop characters.

The intracharacter signalling rate provided to the DTE over circuit 104 shall be in the ranges given in Table 4/V.22 when operating in the basic or in the extended signalling rate ranges, respectively.

TABLE 4/V.22

Intracharacter signalling rate range

Data rate	Signalling rate range	
	Basic	Extended
600 bit/s	600 to 606 bit/s	600 to 614 bit/s
1200 bit/s	1200 to 1212 bit/s	1200 to 1227 bit/s

4.3 *Alternative C*

The modem can be configured for the following modes of operation.

Mode i) 1200 bit/s ± 0.01% synchronous

Mode ii) 1200 bit/s start-stop 8, 9, 10 or 11 bits per character

Mode iii) 600 bit/s ± 0.01% synchronous } optional

Mode iv) 600 bit/s start-stop 8, 9, 10 or 11 bits per character } optional

Mode v) An asynchronous mode having capability of handling 1200 bit/s start-stop and anisochronous data at up to 300 bit/s.

Modes i) to iv) are as given in Alternative B.

4.3.1 *Basic modes*

In Alternative C, the modem shall incorporate Modes i), ii), iii) and iv) given in Alternative B, plus Mode v), in which the modem transmitter sends data at a rate always greater than the input data rate, and thus disables the receiver buffer. The GSTN handshaking sequence allows automatic selection of Modes ii) or v). Modes i), iii) and iv) must be selected at installation. On leased circuits there is no automatic mode selection. The line encoding for specific dibit values is described in Table 1/V.22.

4.3.2 *Transmitter*

In Mode v), the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of a 0 to 300 bit/s or 1200 bit/s automatically. The transmitter buffer that converts incoming data to a synchronous data stream at 1205 bit/s or 1223 bit/s shall:

a) start its asynchronous bit counter on either data transition,

b) always transmit the last bit received over circuit 103 after the bit counter has elapsed,

c) sample incoming data during the bit count at 1205 Hz or 1223 Hz depending upon line rate.

This will assure that incoming data at 0 to 300 bit/s shall pass through the buffer with a maximum introduced distortion of 25% at 300 bit/s (and 12.5% at 150 bit/s), and that break signals pass through the buffer unchanged.

The length and structure of incoming characters shall be the same as given in Alternative B. Within Mode v) at 1200 bit/s asynchronous, two adjacent character formats, e.g. 9- and 10-bit character, can be handled automatically. As in Alternative B, the modem shall derive its line signal clock from internal clock circuits, or alternatively, from receiver signal element timing, as an installation option.

4.3.3 *Basic signalling rate range*

In Mode v), the intracharacter signalling rate provided by the DTE on circuit 103 must be:

1205 bit/s line rate	0 to 301 bit/s and 1170 to 1204 bit/s
1223 bit/s line rate	0 to 305 bit/s and 1190 to 1221 bit/s

Selection of line rate is made in the transmitter by installer option and automatically detected in the receiver.

5 Scrambler and descrambler

5.1 *Scrambler*

A self synchronizing scrambler having the generating polynomial $1 \oplus x^{-14} \oplus x^{-17}$ shall be included in the modem transmitter. The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. The scrambler output data sequence

$$D_s = D_i \oplus D_s \cdot x^{-14} \oplus D_s \cdot x^{-17}$$

where

D_S is the data sequence at the output of the scrambler

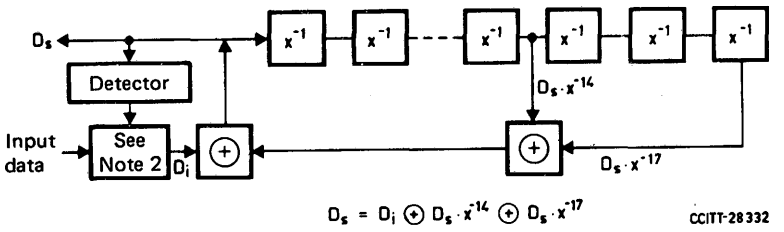
D_i is the data sequence applied to the scrambler

$\oplus$ denotes modulo 2 addition

$\cdot$ denotes binary multiplication

Figure 2/V.22 shows a suitable implementation.

To prevent occasional inadvertent instigation of remote loop 2 caused by scrambler lockup, circuitry shall be included to detect a sequence of 64 consecutive ones at the scrambler output (D_s) and, if detected, invert the next input to the scrambler, D_i. This circuitry will not operate during handshaking or during the instigation of remote loop 2.



Note 1 – Marks (binary 1) and spaces (binary 0) at the V.24 interface correspond to ones and zeros, respectively, in this logic diagram.

Note 2 – Circuitry shall be included to detect a sequence of 64 consecutive binary ones at the scrambler output (D_S) and, if detected, invert the next input to the scrambler (D_i).

FIGURE 2/V.22

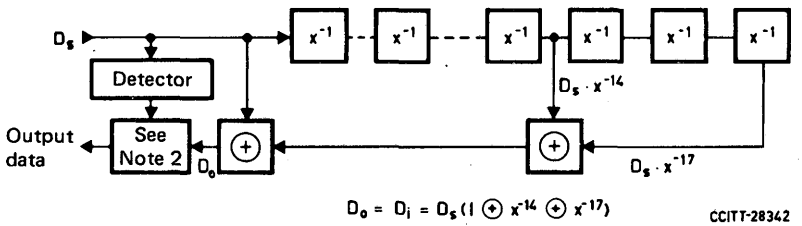
Scrambler

5.2 *Descrambler*

A self synchronizing descrambler having the polynomial $1 \oplus x^{-14} \oplus x^{-17}$ shall be provided in the modem receiver. The message data sequence produced after demodulation shall be effectively multiplied by the generating polynomial $1 \oplus x^{-14} \oplus x^{-17}$ to form the descrambled message. The coefficients of the recovered message sequence taken in descending order form the output data sequence D_o, which is given by

$$D_o = D_s(1 \oplus x^{-14} \oplus x^{-17})$$

Figure 3/V.22 shows a suitable implementation.



Note 1 – Marks (binary 1) and spaces (binary 0) at the V.24 interface correspond to ones and zeros, respectively, in this logic diagram.

Note 2 – Circuitry may be included to detect a sequence of 64 consecutive ones at the input to the descrambler (D_S) and, if detected, invert the next output from the descrambler, (D_O). This detector should not begin operating until the handshaking sequence is complete. If this circuitry is included, detection of the initiation signal described in § 7.1.1 (unscrambled binary ones) should be performed at the point D_O.

FIGURE 3/V.22

Descrambler

6 Operating sequences

6.1 *Channel and operating mode selection*

On the general switched telephone network, the modem at the calling data station shall transmit in the low channel and receive in the high channel (call mode). The modem at the answering data station shall receive in the low channel and transmit in the high channel (answer mode).

Where calls are established on the GSTN by operators, bilateral agreement between users on channel allocation will be necessary. On point-to- point leased circuits, channel allocation will be by bilateral agreement between Administrations or users. In these cases the method of selection of call or answer mode is a national matter.

On point-to-point leased circuits, selection of Modes i) to v) will be by bilateral agreement between Administrations or users. The method of selection is a national matter.

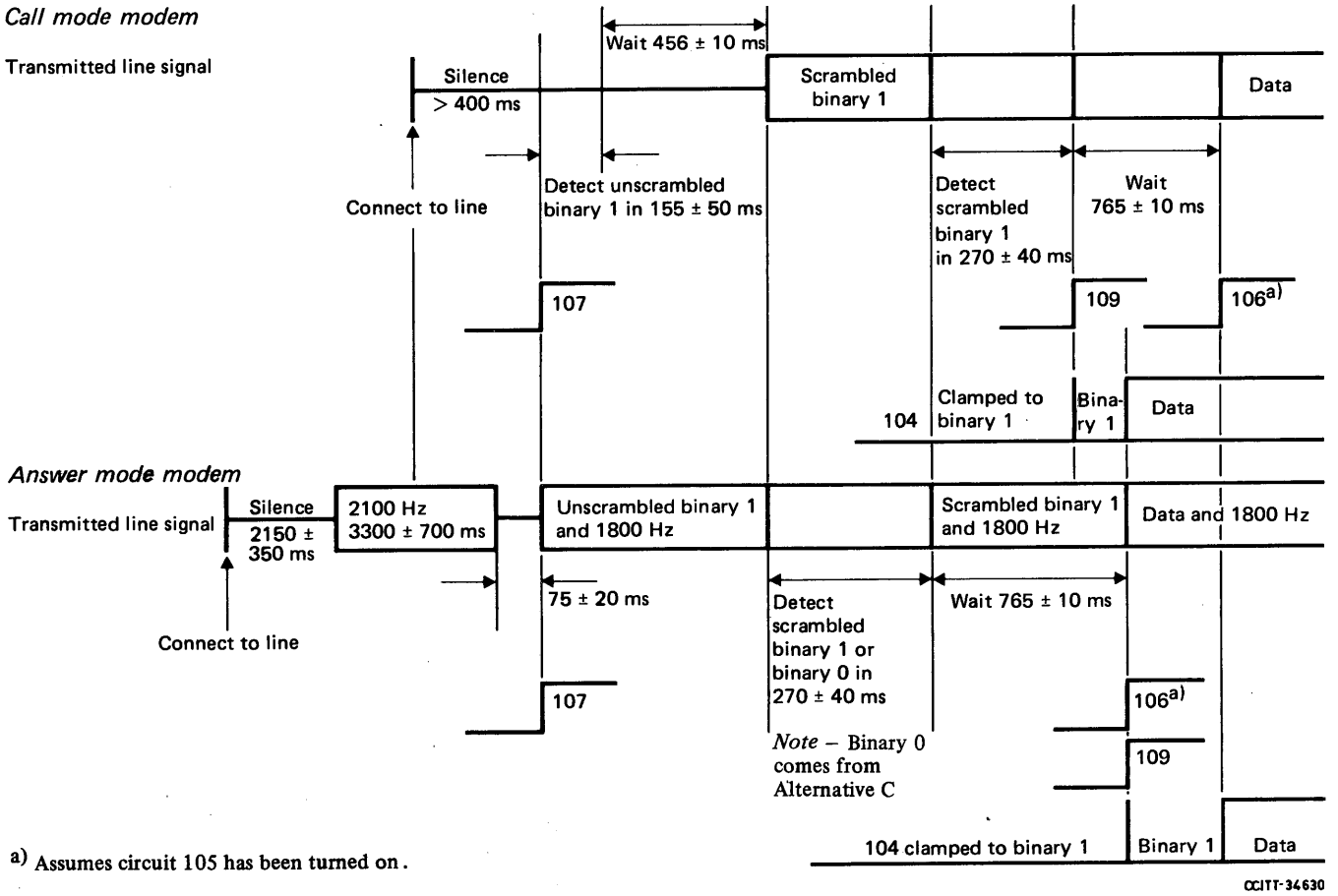
6.2 *V.25 automatic answering sequence*

The V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted on point-to-point leased circuits or on national connections on the GSTN, where permitted by the Administration.

6.3 *Operating sequences for Alternatives A and B*

6.3.1 *GSTN - constant carrier*

The means of achieving initial synchronism between the call mode modem and the answer mode modem on international GSTN connections is shown in Figure 4/V.22. The alternative handshake without V.25 automatic answering is shown in Figure 5/V.22.



a) Assumes circuit 105 has been turned on.

FIGURE 4/V.22

Handshake sequence for Alternatives A and B (with V.25 auto-answering)

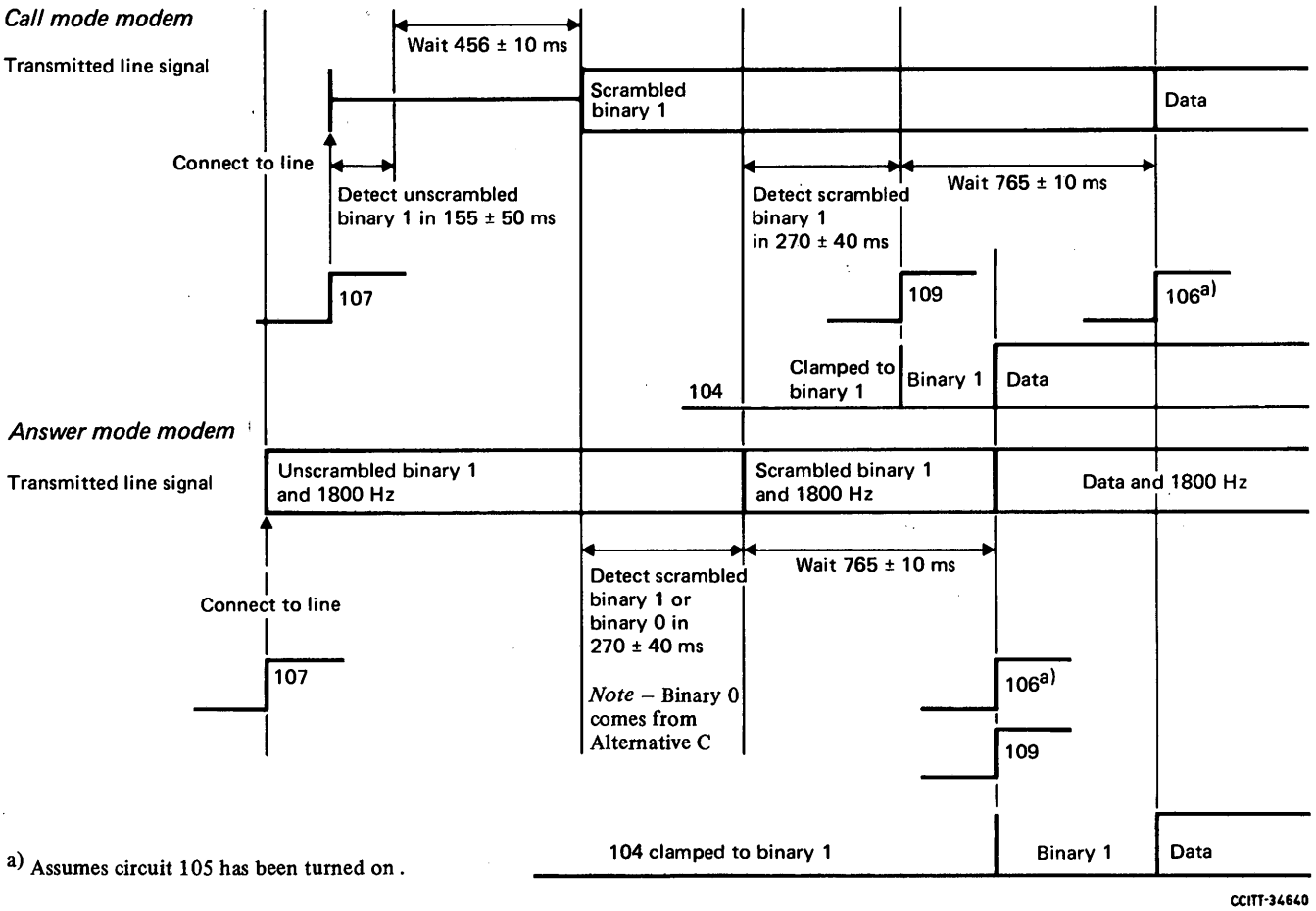


FIGURE 5/V.22

Handshake sequence for Alternatives A and B (without V.25 auto-answer sequence)

6.3.1.1 *Call mode modem*

Once the call mode modem has connected to line, it shall be conditioned to receive signals in the high channel and shall apply an ON condition to circuit 107 in accordance with Recommendation V.25. The modem shall remain silent until unscrambled binary 1 is detected for 155 ± 50 ms, and after waiting for 456 ± 10 ms shall transmit scrambled binary 1 in the low channel. Upon detecting scrambled binary 1 in the high channel in 270 ± 40 ms, the modem shall turn circuit 109 ON, then wait a further 765 ± 10 ms. Circuit 106 shall then respond to the condition of circuit 105 according to Table 3/V.22 constant carrier mode. When circuit 106 is OFF, circuit 103 shall be clamped to the binary 1 condition.

Note – Manufacturers may wish to note that in certain countries, for national purposes, modems are in service which emit an answering tone of 2225 Hz instead of unscrambled binary 1.

6.3.1.2 *Answer mode modem*

Once the answer mode modem has connected to line and immediately following the V.25 answer sequence, the modem shall be conditioned to receive signals in the low channel. It shall then apply an ON condition to circuit 107 and transmit unscrambled binary 1. Upon detecting scrambled binary 1 or 0 in the low channel in 270 ± 40 ms, the modem shall transmit scrambled binary 1 in the high channel, and after waiting for 765 ± 10 ms, apply an ON condition to circuit 109. Circuit 106 shall then respond to the condition of circuit 105 according to Table 3/V.22, constant carrier mode. When circuit 106 is OFF, circuit 103 shall be clamped to the binary 1 condition.

Where both modems are manually connected to line this sequence will apply irrespective of whether the call or answer mode modem is connected to line first.

After completion of the handshake sequence, any inadvertent loss and reappearance of the received line signal should not cause another handshake sequence to be generated. Circuit 109 should respond with the response times given in Table 3/V.22.

6.3.2 *GSTN and point-to-point leased circuits – controlled carrier*

Once an ON condition has been applied to circuit 105 by the DTE, the modem shall transmit a synchronizing signal corresponding to binary 1 applied to circuit 103. The ON condition shall be applied to circuit 106, 210 to 275 ms after starting to transmit the synchronizing signal. The receiving modem shall establish timing and descrambler synchronization and then turn circuit 109 ON in 105 to 205 ms.

Each direction of transmission shall be independently controlled.

Note – Controlled carrier operation on GSTN is optional. For circuits with echo suppressors, controlled carrier working is not recommended.

6.4 *Operating sequence for Alternative C*

Refer to Figure 6/V.22.

6.4.1 *GSTN – constant carrier*

6.4.1.1 *Call mode modem*

If configured for Modes i), iii), or iv), the handshake sequence proceeds as for Alternative B. If configured for Mode v), the handshaking sequence shall automatically select Mode ii) or v). This sequence shall be as follows:

Once the call mode modem has connected to line, it shall be conditioned to receive signals in the high channel and shall apply an ON condition to circuit 107 in accordance with Recommendation V.25. The modem shall remain silent until unscrambled binary 1 [Mode ii)] is detected for 155 ± 50 ms and after waiting for 456 ± 10 ms shall transmit scrambled binary 0 [Mode ii)] in the low channel. Upon detecting scrambled binary 1 [Mode ii)] in the high channel within 270 ± 40 ms, the modem shall turn circuit 109 ON, enter Mode ii), then wait a further 765 ± 10 ms. Upon detecting scrambled binary 1 [Mode v)] in the high channel in 270 ± 40 ms, the modem shall turn ON circuit 109, enter Mode v), then wait a further 765 ± 10 ms. Circuit 106 shall then respond to the condition of circuit 105 according to Table 3/V.22 constant carrier mode. When circuit 106 is OFF, circuit 103 shall be clamped to the binary 1 condition.

See also the note in § 6.3.1.1.

6.4.1.2 *Answer mode modem, Mode v)*

Once the answer mode modem has connected to line and immediately following the V.25 answer sequence, the modem shall be conditioned to receive signals in the low channel. It shall then apply an ON condition to circuit 107 and transmit unscrambled binary 1 [Mode ii)].

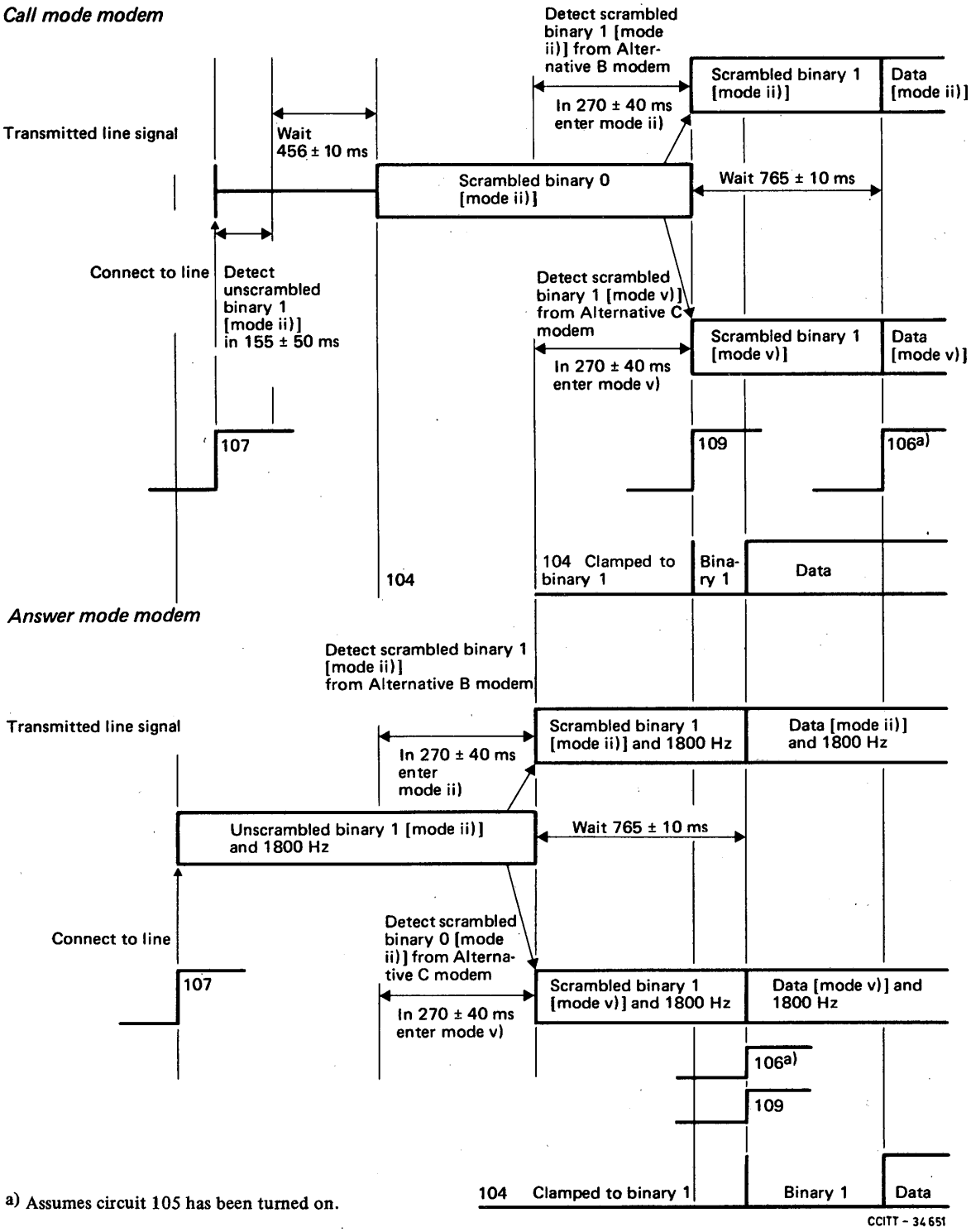
If scrambled binary 0 [Mode ii)] is detected in the low channel for 270 ± 40 ms, the modem shall enter Mode v), transmit scrambled binary 1 [Mode v)] in the high channel and after waiting for 765 ± 10 ms apply an ON condition to circuit 109.

If scrambled binary 1 [Mode ii)] is detected in the low channel for 270 ± 40 ms, the modem shall enter Mode ii), transmit scrambled binary 1 [Mode ii)] in the high channel and after waiting for 765 ± 10 ms apply an ON condition to circuit 109.

Circuit 106 shall respond to the condition of circuit 105 according to Table 3/V.22 constant carrier mode. When circuit 106 is OFF circuit 103 shall be clamped to the binary 1 condition.

6.4.2 *GSTN and point-to-point leased circuits*

Controlled carrier operation as in § 6.3.2.



a) Assumes circuit 105 has been turned on.

FIGURE 6/V.22

Handshake sequence for Alternative C (without V.25 auto-answer sequence)

7 Testing facilities

7.1 *Test loops*

Test loops 2 (local and remote) and 3 as defined in Recommendation V.54 shall be provided. Interface operation shall be as defined in Recommendation V.54. Instigation and termination sequences are not compatible with Recommendation V.54.

7.1.1 *Instigation of remote loop 2*

Signals controlling the application of remote loop 2 may only be transmitted after the synchronizing handshake has been completed.

As in Recommendation V.54, the modems are referred to as modem A and modem B.

When modem A is instructed to instigate a remote loop 2, the modem shall transmit an initiation signal of unscrambled binary 1.

Modem B shall detect 154-231 ms of the initiation signal, and then transmit to modem A scrambled alternate binary ones and zeros (reversals) at 1200 bit/s (or 600 bit/s).

Modem A shall detect 231-308 ms of scrambled reversals, cease transmission of the initiation signal, and then transmit scrambled binary 1 at 1200 bit/s (or 600 bit/s).

Modem B shall detect the loss of initiation signal and activate loop 2 within modem B.

Modem A, upon receiving 231-308 ms of scrambled binary 1 shall indicate to the DTE that it may begin sending test messages.

7.1.2 *Termination of remote loop 2*

When modem A is instructed to terminate a remote loop 2, the line signal shall be suppressed for a period of 77 ± 10 ms, after which transmission shall be restored.

Modem B detects the loss of line signal in 17 ± 7 ms and detects the reappearance of the signal within 155 ± 50 ms, after which it returns to normal operation.

7.2 *Self tests*

7.2.1 *Self test end-to-end*

Upon activation of the self-test switch an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate shall be applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals shall be connected to the output of the descrambler. The presence of errors shall be indicated by a visual indicator. All generating interchange circuits except 114 (if used), 115 and 142 shall be clamped to the binary 1 or OFF condition. If circuit 113 is used, the DCE shall disregard this interchange circuit and use its internal clock.

7.2.2 *Self test with loop 3*

Loop 3 shall be applied to the modem as defined in Recommendation V.54. The self-test switch shall be activated and DCE operation shall be as in § 7.2.1.

7.2.3 *Self test with remote loop 2*

The modem shall be conditioned to instigate a loop 2 at the remote modem as specified in § 7.1. The self-test switch shall be activated and DCE operation shall be as in § 7.2.1.

It shall be possible to perform the above tests (§§ 7.2.1, 7.2.2 and 7.2.3) with or without the DTE connected to the modem. These tests employ an internally generated data pattern that is controlled by a switch on the DCE.

7.2.4 During any self-test mode, interchange circuits 103, 105 and 108 will be ignored. Note that self tests do not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver.

Note – Inclusion of remote loop signalling according to Recommendation V.54 is for further study.

2400 BITS PER SECOND DUPLEX MODEM USING THE FREQUENCY DIVISION TECHNIQUE STANDARDIZED FOR USE ON THE GENERAL SWITCHED TELEPHONE NETWORK AND ON POINT-TO-POINT 2-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Malaga-Torremolinos, 1984; and at Melbourne, 1988)

The CCITT,

considering

(a) that there is a demand for data transmission at 2400 bit/s in the duplex mode over the General Switched Telephone Network (GSTN) and on point-to-point 2-wire leased telephone-type circuits;

(b) that there is a demand to have the fall-back mode compatibility with modems in accordance with Recommendation V.22;

(c) that in this case the frequency division technique shall be used,

(unanimously) declares

that the characteristics of the modems for this service shall provisionally be as follows:

1 Introduction

These modems are intended for use on connections on the GSTN and on point-to-point 2-wire leased telephone-type circuits (see Note). The principal characteristics of these modems are as follows:

a) duplex mode of operation on the GSTN and point-to-point leased circuits,

b) channel separation by frequency division,

c) quadrature amplitude modulation for each channel with synchronous line transmission at 600 baud (nominal),

d) inclusion of a scrambler,

e) inclusion of an adaptive equalizer and a compromise equalizer,

f) inclusion of test facilities,

g) data signalling rates of:

2400 bit/s synchronous,

2400 bit/s start-stop,

1200 bit/s synchronous,

1200 bit/s start-stop,

h) it is compatible with a V.22 modem operating in Modes i) or ii) at the 1200 bit/s signalling rate and includes automatic bit rate recognition.

Note – In certain countries the use of such modems over the GSTN may not be allowed.

2 Line signals

2.1 *Carrier and guard tone frequencies*

The carrier frequencies shall be 1200 ± 0.5 Hz for the low channel and 2400 ± 1 Hz for the high channel. A guard tone of 1800 ± 20 Hz, to be transmitted only when the modem is transmitting in the high channel, may be disabled as a national option. An alternative guard tone of 550 ± 20 Hz, to be transmitted only when the modem is transmitting in the high channel, may be incorporated as a national option.

2.2 *Data and guard tone line signal levels*

The 1800 Hz or 550 Hz guard tones shall be levels 6 ± 1 dB or 3 ± 1 dB, respectively, below the level of the data signal power in the high channel. Because of the 1800 Hz guard tone, the power level of data signals in the high channel will be approximately 1 dB lower than that of data signals in the low channel.

2.3 *Fixed compromise equalizer*

Fixed compromise equalization shall be incorporated in the modem transmitter.

2.4 *Spectrum and group delay characteristics*

The transmitted line signals, excluding the characteristics of the fixed compromise equalizer, shall have a frequency amplitude spectrum equivalent to the square root of a raised cosine shaping with 75% roll-off and within the limits shown in Figure 1/V.22 *bis*. Similarly, the group delay of the transmitter output shall be within the range of ± 150 microseconds over the frequency ranges 900-1500 Hz (low channel) and 2100-2700 Hz (high channel). These figures are provisional.

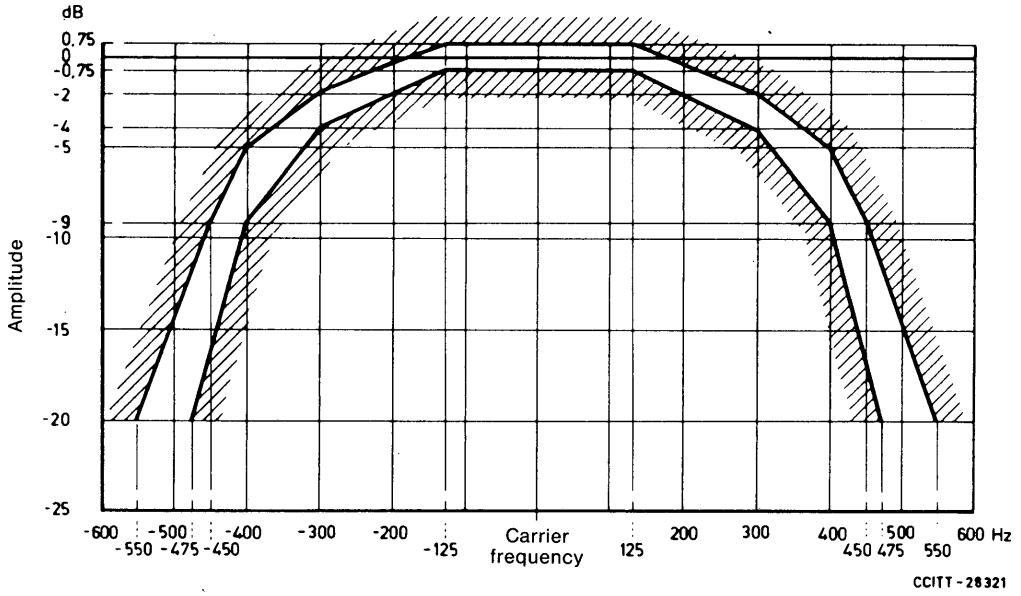


FIGURE 1/V.22 *bis*

Amplitude limits for transmitted line signal (unequalized)

2.5 *Modulation*

2.5.1 *Data signalling rates*

The data rate transmitted to line shall be 2400 bit/s or 1200 bit/s ± 0.01% with a modulation rate of 600 baud ± 0.01%.

2.5.2 *Encoding of data bits*

2.5.2.1 *2400 bits per second*

The data stream to be transmitted shall be divided into groups of 4 consecutive bits (quadbits). The first two bits of a quadbit shall be encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. (See Figure 2/V.22 *bis* and Table 1/V.22 *bis*.)

The last two bits of each quadbit define one of 4 signalling elements associated with the new quadrant (see Figure 2/V.22 *bis*). The left hand bits in Table 1/V.22 *bis* and Figure 2/V.22 *bis* are the first of each pair in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.22 *bis*

Line encoding

First two bits in quadbit (2400 bit/s) or dibit values (1200 bit/s)	Phase quadrant change	
00	1 → 2 2 → 3 3 → 4 4 → 1	90°
01	1 → 1 2 → 2 3 → 3 4 → 4	0°
11	1 → 4 2 → 1 3 → 2 4 → 3	270°
10	1 → 3 2 → 4 3 → 1 4 → 2	180°

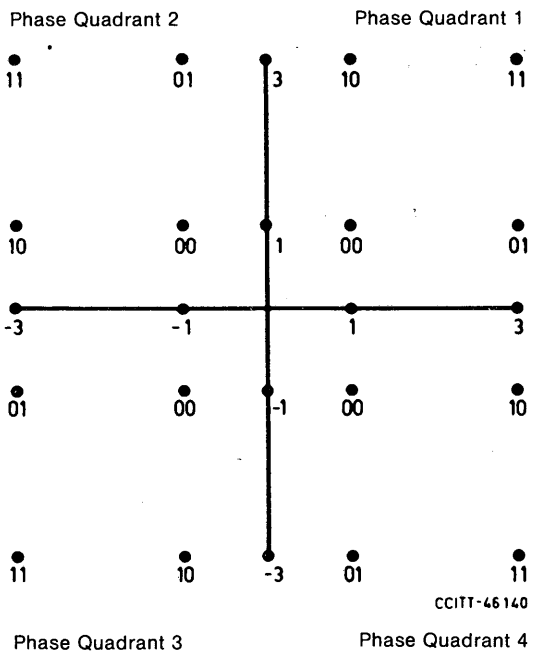


FIGURE 2/V.22 *bis*

Signal constellation

2.5.2.2 *1200 bits per second*

The data stream to be transmitted shall be divided into groups of 2 consecutive bits (dibits). The dibits shall be encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element (see Table 1/V.22 *bis*). The signalling elements corresponding to 01 in the signal constellation (Figure 2/V.22 *bis*) shall be transmitted irrespective of the quadrant concerned. This ensure compatibility with Recommendation V.22.

2.6 *Received signal frequency tolerance*

The receiver shall be able to operate with received frequency offsets of up to ± 7 Hz.

3 Interchange circuits

3.1 *Essential and optional interchange circuits*

These are listed in Table 2/V.22 *bis.*

3.2 *Circuits 106 and 109 response times*

After the handshaking sequences, circuit 106 will follow OFF to ON or ON to OFF transitions of circuit 105 within 3.5 ms. The OFF to ON transition of circuit 109 is part of the handshake sequence specified in § 6. Circuit 109 shall turn OFF 40 to 65 ms after the level of the received signal appearing at the line terminal of the modem falls below the relevant threshold defined in § 3.3. In the fall-back mode, the response time may be reduced to a value in the 10 to 24 ms range specified in Recommendation V.22. Following a dropout, after the initial handshake, circuit 109 shall turn ON 40 to 205 ms after the level of the received signal appearing at the line terminal of the modem exceeds the relevant threshold defined in § 3.3.

3.3 *Circuit 109 threshold*

High channel threshold:

- greater than −43 dBm — circuit 109 ON
- less than −48 dBm — circuit 109 OFF

Low channel threshold:

- greater than −43 dBm — circuit 109 ON
- less than −48 dBm — circuit 109 OFF

The condition of circuit 109 between the ON and OFF levels is not specified except that the signal detector shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for the ON to OFF transition.

Circuit 109 thresholds are specified at the input to the modem when receiving scrambled binary 1.

Administrations are permitted to change these thresholds where transmission conditions are known.

Circuit 109 shall not respond to the 1800 Hz or the 550 Hz guard tones, or the 2100 Hz (nominal) answer tone during the handshake sequence.

3.4 *Circuit 111 and data rate control*

Data rate selection may be by switch (or similar means) or by circuit 111 or a combination of both.

The ON condition on circuit 111, where provided, shall select 2400 bit/s operation and the OFF condition shall select 1200 bit/s operation.

TABLE 2/V.22 *bis*

Interchange circuit (Note 1)

Interchange circuit		Notes
No.	Description	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	Note 2
106	Ready for sending	
107	Data set ready	
108/1	Connect data set to line	Note 3
108/2	Data terminal ready	Note 3
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	Note 4
112	Data signalling rate selector (DCE source)	
113	Transmitter signal element timing (DTE source)	Note 5
114	Transmitter signal element timing (DCE source)	Note 6
115	Receiver signal element timing (DCE source)	Note 6
125	Calling indicator	Note 7
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 – All essential interchange circuits and any others which are provided must comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided must be properly terminated in the data terminal equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.5).

Note 2 – Some automatic calling equipments are designed to emit a calling tone to line by turning ON circuit 105 to the calling modem. The general switched telephone network (GSTN) constant carrier handshake is such that no calling tone will be emitted by the V.22 *bis* modem when used with these equipments.

Note 3 – This circuit shall be capable of operation as circuit 108/1 or 108/2 depending on its use.

Note 4 – This circuit is optional.

Note 5 – When the modem is not operating in a synchronous mode at the interface, any signals on this circuit shall be disregarded. Many DTEs operating in an asynchronous mode do not have a generator connected to this circuit.

Note 6 – When the modem is not operating in a synchronous mode at the interface, this circuit shall be clamped to the OFF condition. Many DTEs operating in an asynchronous mode do not terminate this circuit.

Note 7 – This circuit is for use with the general switched telephone network only.

3.5 *Electrical characteristics of interchange circuits*

3.5.1 Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.6 *Fault condition of interchange circuits*

See Recommendation V.28, § 7 for association of the receiver failure detection types.)

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Modes of operation

The modem can be configured for the following modes of operation:

Mode 1 2400 bit/s ± 0.01% synchronous

Mode 2 2400 bit/s start-stop 8, 9, 10 or 11 bits per character

Mode 3 1200 bit/s ± 0.01% synchronous

Mode 4 1200 bit/s start-stop 8, 9, 10 or 11 bits per character.

4.1 *Transmitter*

4.1.1 In the synchronous modes of operation, the modem shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or circuit 114. The data shall then be scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.

4.1.2 In the start-stop modes, the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of 2400 or 1200 bits per second. The start-stop data to be transmitted shall be converted in conformity with Recommendation V.14 to a synchronous data stream suitable for transmission in accordance with § 4.1.1

4.2 *Receiver*

Demodulated data shall be decoded in accordance with § 2.5.2, then descrambled in accordance with § 5.2 and then passed to the converter in conformity with Recommendation V.14 for regaining the data stream of start-stop characters.

The intracharacter signalling rate provided to the DTE over circuit 104 shall be in the ranges given in Table 3/V.22 *bis* when operating in the basic or in the extended signalling rate ranges, respectively.

TABLE 3/V.22 *bis*

Intracharacter signalling rate range

Data rate	Signalling rate range	
	Basic	Extended
2400 bit/s	2400 to 2424 bit/s	2400 to 2455 bit/s
1200 bit/s	1200 to 1212 bit/s	1200 to 1227 bit/s

5 Scrambler and descrambler

5.1 *Scrambler*

A self synchronizing scrambler having the generating polynomial $1 \oplus x^{-14} \oplus x^{-17}$ shall be included in the modem transmitter. The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. The scrambler output data sequence shall thus be:

$$D_s = D_i \oplus D_s \cdot x^{-14} \oplus D_s \cdot x^{-17}$$

where

D_s is the data sequence at the output of the scrambler

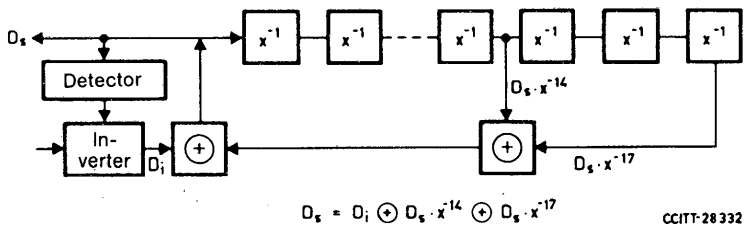
D_i is the data sequence applied to the scrambler

$\oplus$ denotes module 2 addition

$\cdot$ denotes binary multiplication.

Figure 3/V.22 *bis* shows a suitable implementation.

To prevent occasional inadvertent instigation of remote loop 2 caused by scrambler lockup, circuitry shall be included to detect a sequence of 64 consecutive ones at the scrambler output (D_s) and, if detected, invert the next input to the scrambler (D_i) and reset the counter of 64 consecutive ones. This circuitry shall operate whenever the scrambler is operational. No scrambler initialization is required during the handshake or retrain sequence.



Note – Marks (binary 1) and spaces (binary 0) at the V. 24 interface correspond to ones and zeros, respectively, in this logic diagram.

FIGURE 3/V.22 *bis*
Scrambler

5.2 *Descrambler*

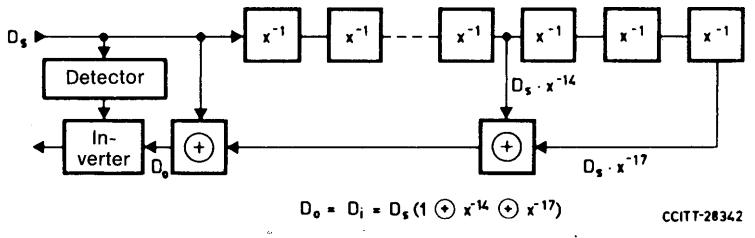
A self synchronizing descrambler having the polynomial $1 \oplus x^{-14} \oplus x^{-17}$ shall be provided in the modem receiver. The message data sequence produced after demodulation shall be effectively multiplied by the generating polynomial $1 \oplus x^{-14} \oplus x^{-17}$ to form the descrambled message. The coefficients of the recovered message sequence taken in descending order form the output data sequence D_o, which is given by

$$D_o = D_s(1 \oplus x^{-14} \oplus x^{-17})$$

where the notation is as defined in § 5.1.

Circuitry may be included to detect a sequence of 64 consecutive ones at the input to the descrambler (D_s) and, if detected, invert the next output from the descrambler (D_o). This detector shall operate whenever the descrambler is operational.

Figure 4/V.22 *bis* shows a suitable implementation.



Note – Marks (binary 1) and spaces (binary 0) at the V. 24 interface correspond to ones and zeros, respectively, in this logic diagram.

FIGURE 4/V.22 *bis*
Descrambler

6 Operating sequences

6.1 *Channel allocation and signalling rate selection*

6.1.1 *GSTN*

On the general switched telephone network, the modem at the calling data station shall transmit in the low channel and receive in the high channel (call mode). The modem at the answering data station shall receive in the low channel and transmit in the high channel (answer mode).

In some situations however, such as when calls are established on the GSTN by operators, bilateral agreement on channel allocations will be necessary.

Signalling rate selection at the call mode modem shall be either manual or by means of a logical condition applied on circuit 111 (if this circuit is provided). The handshake sequence, as defined in § 6.3.1, allows each modem to automatically condition itself to operate at the correct signalling rate.

6.1.2 *Point-to-point leased circuits*

Channel allocation and signalling rate selection on point-to-point leased circuits will, in general, be by bilateral agreement between users.

6.2 *V.25 automatic answering sequence*

The V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted in national connections on point-to-point leased circuits or on the GSTN, where permitted by the Administrations.

6.3 *Handshake sequence*

6.3.1 *GSTN*

The means of achieving synchronism between the calling modem and the answering modem on international GSTN connections is shown in Figures 5/V.22 *bis*, 6/V.22 *bis* and 7/V.22 *bis*. Both calling and answering modems shall be manually conditioned to operate either in the synchronous modes (Modes 1 and 3), or in the start-stop modes (Modes 2 and 4). If both calling and answering modems are V.22 *bis* modems, the handshake will normally condition both modems to operate at 2400 bit/s. If however one or both of the modems has been set to operate at 1200 bit/s, either manually or via circuit 111, then the handshake will condition both modems to operate at 1200 bit/s. If either the calling or answering modem is a V.22 modem operating in V.22 Modes i) or ii) the handshake will condition both the V.22 *bis* and V.22 modem to operate at 1200 bit/s. The signalling rate is communicated to the DTE by a logical condition on circuit 112. The handshake sequence is independent of which modem, calling or answering, is connected to line first.

6.3.1.1 *Interworking at 2400 bit/s*

6.3.1.1.1 *Calling modem*

a) On connection to line the calling modem shall be conditioned to receive signals in the high channel at 1200 bit/s and transmit signals in the low channel at 1200 bit/s in accordance with § 2.5.2.2. It shall apply an ON condition to circuit 107 in accordance with Recommendation V.25. The modem shall initially remain silent.

b) After 155 ± 10 ms of unscrambled binary 1 has been detected, the modem shall remain silent for a further 456 ± 10 ms then transmit an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s for 100 ± 3 ms. Following this signal the modem shall transmit scrambled binary 1 at 1200 bit/s.

c) If the modem detects scrambled binary 1 in the high channel at 1200 bit/s for 270 ± 40 ms, the handshake shall continue in accordance with §§ 6.3.1.2.1 c) and d). However, if unscrambled repetitive double dibit 00 and 11 at 1200 bit/s is detected in the high channel, then at the end of receipt of this signal the modem shall apply an ON condition to circuit 112.

d) 600 ± 10 ms after circuit 112 has been turned ON the modem shall begin transmitting scrambled binary 1 at 2400 bit/s, and 450 ± 10 ms after circuit 112 has been turned ON the receiver may begin making 16-way decisions.

e) Following transmission of scrambled binary 1 at 2400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the modem shall be ready to transmit data at 2400 bit/s.

f) When 32 consecutive bits of scrambled binary 1 at 2400 bit/s have been detected in the high channel the modem shall be ready to receive data at 2400 bit/s and shall apply an ON condition to circuit 109.

6.3.1.1.2 *Answering modem*

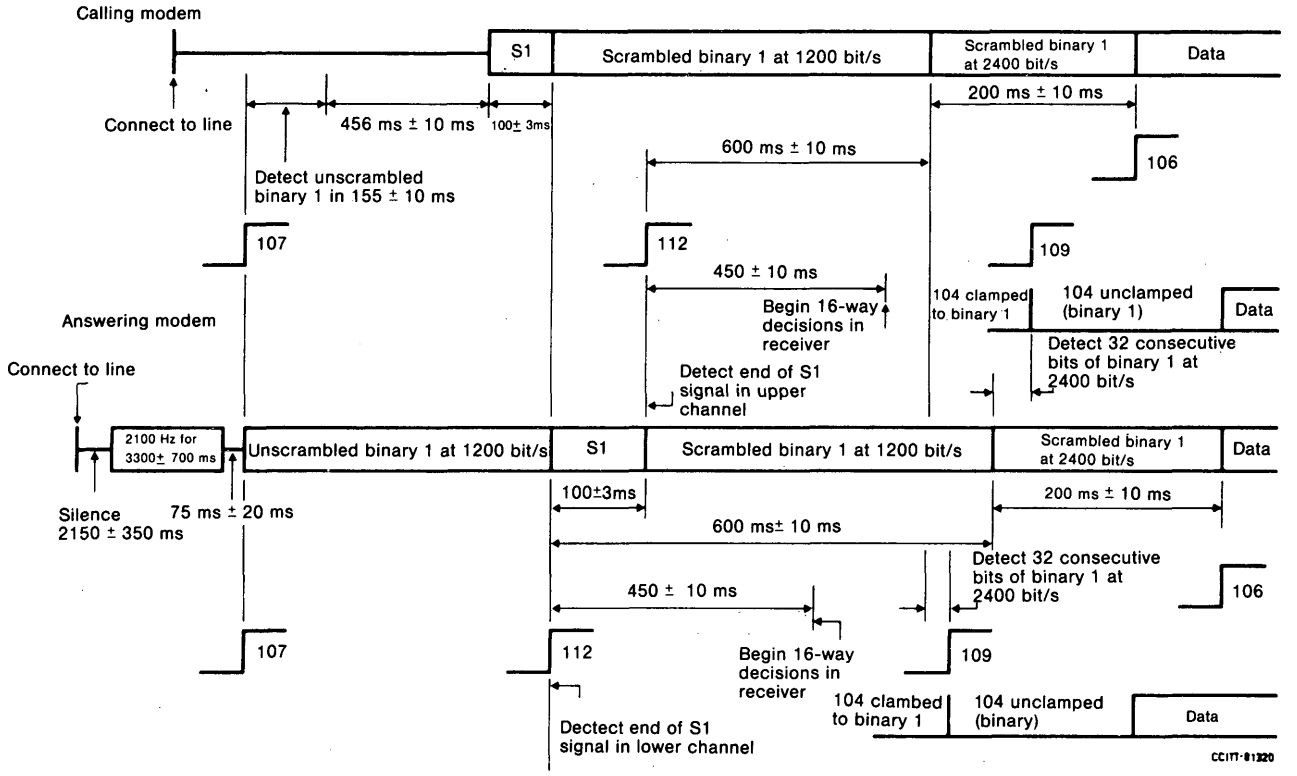
a) On connection to line the answering modem shall be conditioned to transmit signals in the high channel at 1200 bit/s in accordance with § 2.5.2.2 and receive signals in the low channel at 1200 bit/s. Following transmission of the answer sequence in accordance with Recommendation V.25, the modem shall apply an ON condition to circuit 107 and then transmit unscrambled binary 1 at 1200 bit/s.

b) If the modem detects scrambled binary 1 or 0 in the low channel at 1200 bit/s for 270 ± 40 ms, the handshake shall continue in accordance with §§ 6.3.1.2.2 b) and c). However, if unscrambled repetitive double dibit 00 and 11 at 1200 bit/s is detected in the low channel, at the end of receipt of this signal the modem shall apply an ON condition to circuit 112 and then transmit an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s for 100 ± 3 ms. Following these signals the modem shall transmit scrambled binary 1 at 1200 bit/s.

c) 600 ± 10 ms after circuit 112 has been turned ON the modem shall begin transmitting scrambled binary 1 at 2400 bit/s, and 450 ± 10 ms after circuit 112 has been turned ON the receiver may begin making 16-way decisions.

d) Following transmission of scrambled binary 1 at 2400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the modem shall be ready to transmit data at 2400 bit/s.

e) When 32 consecutive bits of scrambled binary 1 at 2400 bit/s have been detected in the low channel the modem shall be ready to receive data at 2400 bit/s and shall apply an ON condition to circuit 109.



V.22 bis signal:
S1 = Unscrambled double dibit 00 and 11 at 1200 bit/s for 100 ± 3 ms.

FIGURE 5/V.22 *bis*

Handshake sequence at 2400 bit/s (with V.25 automatic ansvering)

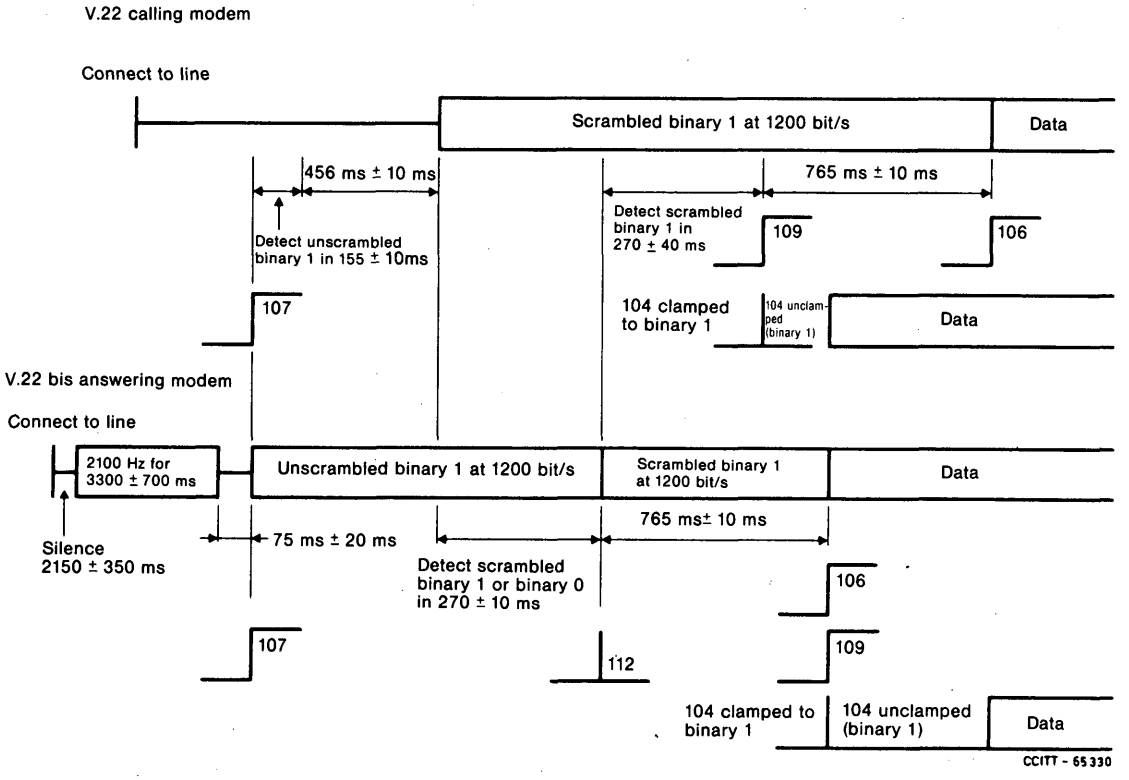


FIGURE 6/V.22 *bis*

Handshake sequence at 1200 bit/s with V.22 calling modem (with V.25 automatic answering)

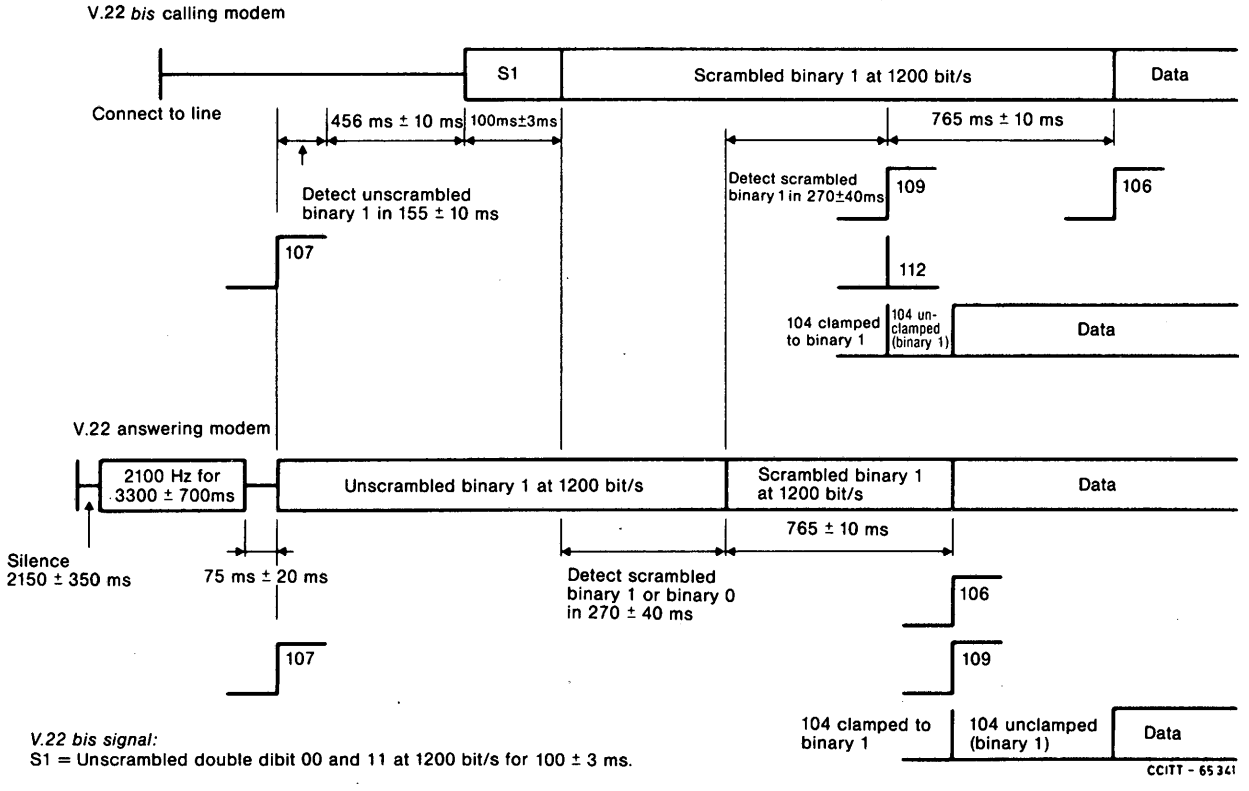


FIGURE 7/V.22 *bis*

Handshake sequence at 1200 bit/s with V.22 answering modem (with V.25 automatic answering)

6.3.1.2 *Interworking at 1200 bit/s*

The following handshake is identical to the Recommendation V.22 alternative A and B handshake.

6.3.1.2.1 *Calling modem*

a) On connection to line the calling modem shall be conditioned to receive signals in the high channel at 1200 bit/s and transmit signals in the low channel at 1200 bit/s in accordance with § 2.5.2.2. It shall apply an ON condition to circuit 107 in accordance with Recommendation V.25. The modem shall initially remain silent.

b) After 155 ± 10 ms of unscrambled binary 1 has been detected, the modem shall remain silent for a further 456 ± 10 ms then transmit scrambled binary 1 at 1200 bit/s (a preceding V.22 *bis* signal, as shown in Figure 7/V.22 *bis*, would not affect the operation of a V.22 answer modem).

c) On detection of scrambled binary 1 in the high channel at 1200 bit/s for 270 ± 40 ms the modem shall be ready to receive data at 1200 bit/s and shall apply an ON condition to circuit 109 and an OFF condition to circuit 112.

d) 765 ± 10 ms after circuit 109 has been turned ON, circuit 106 shall be conditioned to respond to circuit 105 and the modem shall be ready to transmit data at 1200 bit/s.

6.3.1.2.2 *Answering modem*

a) On connection to line the answering modem shall be conditioned to transmit signals in the high channel at 1200 bit/s in accordance with § 2.5.2.2 and receive signals in the low channel at 1200 bit/s.

Following transmission of the answer sequence in accordance with V.25 the modem shall apply an ON condition to circuit 107 and then transmit unscrambled binary 1 at 1200 bit/s.

b) On detection of scrambled binary 1 or 0 in the low channel at 1200 bit/s for 270 ± 40 ms the modem shall apply an OFF condition to circuit 112 and shall then transmit scrambled binary 1 at 1200 bit/s.

c) After scrambled binary 1 has been transmitted at 1200 bit/s for 765 ± 10 ms the modem shall be ready to transmit and receive data at 1200 bit/s, shall condition circuit 106 to respond to circuit 105 and shall apply an ON condition to circuit 109.

Note - Manufacturers may wish to note that in certain countries, for national purposes, modems are in service which emit an answering tone of 2225 Hz instead of unscrambled binary 1.

6.3.2 *Point-to-point leased circuits*

6.3.2.1 *Interworking at 2400 bit/s*

Operation on leased circuits shall be continuous carrier in both directions. On initial power on and after line signal interruptions, operation shall be according to § 6.5.

6.4 *Retrain sequence (2400 bit/s operation)*

A retrain may be initiated during data transmission between two V.22 *bis* modems if either modem incorporates a means of detecting loss of equalization.

Transmission of a retrain sequence shall be initiated either by detection of loss of equalization or by detection of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem.

The following sequence of events shall take place during the retrain:

a) Following detection of loss of equalization or the end of detection of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem, the OFF condition shall be applied to circuit 106 and circuit 104 may be clamped to binary 1. The modem shall transmit an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s for 100 ± 3 ms. Following this signal the modem shall transmit scrambled binary 1 at 1200 bit/s.

b) 600 ± 10 ms after the end of detection of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem, the modem shall begin transmitting scrambled binary 1 at 2400 bit/s and 450 ± 10 ms after the end of this detection the receiver may begin making 16-way decisions.

c) Following transmission of scrambled binary 1 at 2400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the modem shall be ready to transmit data at 2400 bit/s.

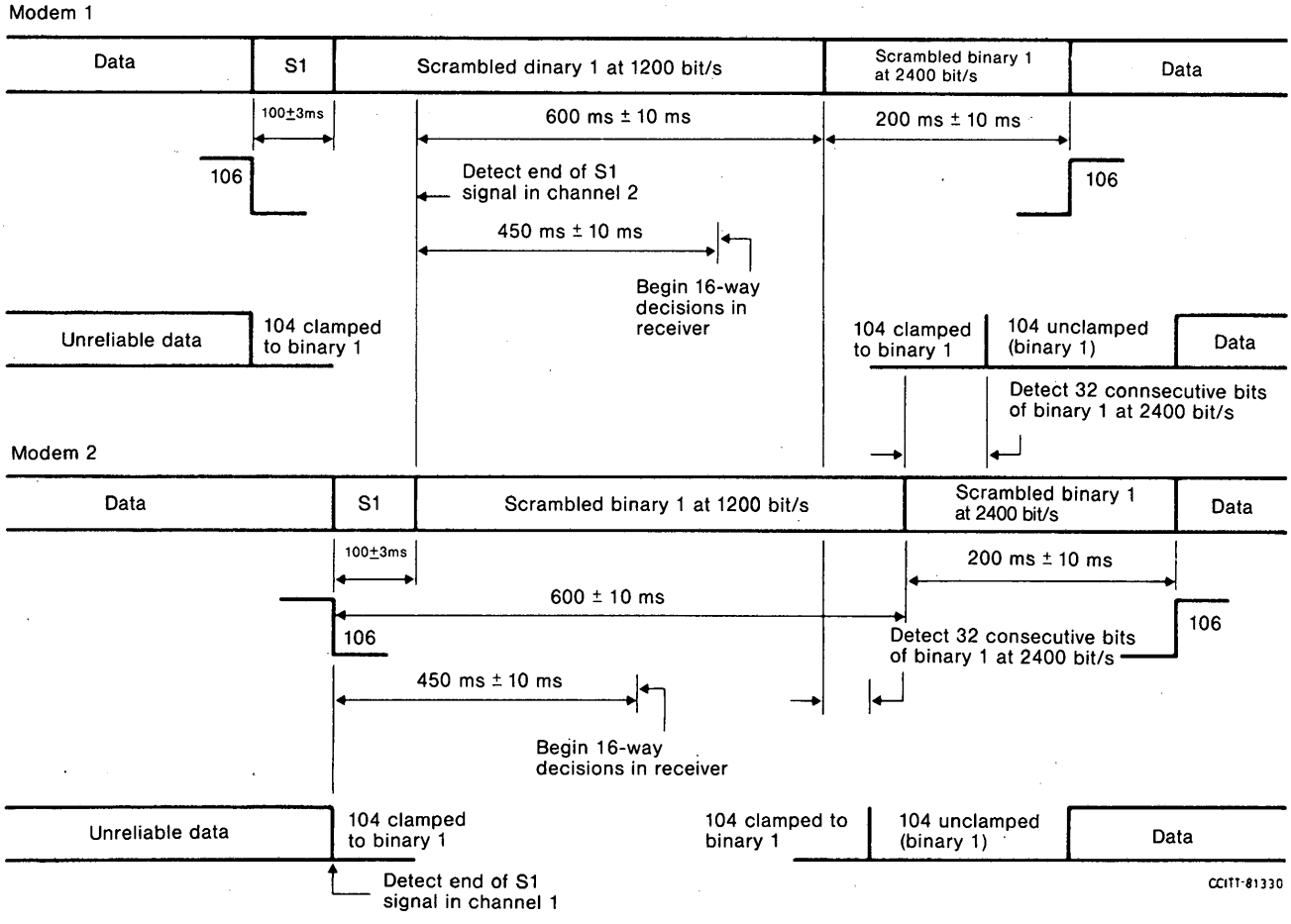
d) When 32 consecutive bits of scrambled binary 1 at 2400 bit/s have been detected from the remote modem, the modem shall be ready to receive data at 2400 bit/s and shall remove the clamp from circuit 104.

A retrain between two modems is shown in Figure 8/V.22 *bis*. Clocks presented on circuits 114 and 115 shall remain at 2400 bit/s during the entire retrain sequence.

If a modem has transmitted a retrain signal and has not received unscrambled repetitive double dibit 00 and 11 at 1200 bit/s immediately prior, or during, or within a time interval equal to the maximum expected two-way propagation delay, the modem shall return to the beginning of the retrain signal as defined above and repeat the procedure until unscrambled repetitive double dibit 00 and 11 is received from the remote modem. A time interval of 1.2 seconds is recommended for the maximum expected two-way propagation delay.

If the modem fails to synchronize on the received retrain sequence, the modem shall transmit another retrain signal.

During this retraining, circuits 109 and 107 shall remain ON.



V.22 bis signal:
S1 = Unscrambled double dibit 00 and 11 at 1200 bit/s for 100 ± 3 ms.

FIGURE 8/V.22 *bis*
A retrain at 2400 bit/s

6.5 *Operation after loss of line signal*

When the modem detects loss of received line signal (as specified in §§ 3.2 and 3.3) it shall turn OFF circuit 109 and shall clamp circuit 104 to binary 1. If received line signal is then detected (as specified in §§ 3.2 and 3.3) the modem shall turn ON circuit 109 but shall leave circuit 104 clamped to binary 1. If during the next 100 ms the modem detects a retrain sequence it shall proceed according to § 6.4 above. If the modem has not detected a retrain sequence by the end of the same 100 ms it shall remove the clamp from circuit 104. If at any time after turning ON circuit 109 following a drop out the modem detects loss of equalization, it shall proceed according to § 6.4 above.

6.6 *Optional rate signalling*

A modem may optionally instigate a rate change in response to a change in circuit 111 or manually, by a switch (or other means). The request may be made to change the operating rate from 1200 bit/s to 2400 bit/s or from 2400 bit/s to 1200 bit/s without disconnection from the GSTN (Note 1).

6.6.1 *Instigation of a rate change*

a) Upon initiation of a rate change, manually or by a change in the condition of circuit 111, the modem shall apply an OFF condition to circuit 106, clamp circuit 104 to binary ones and shall transmit unscrambled repetitive double dibit 00 and 11 at 1200 bit/s for 100 ± 3 ms. During this procedure, circuits 109 and 107 shall remain on.

b) Following this, the modem shall transmit scrambled R1 as defined in Table 3/V.22 *bis* at a rate of 1200 bit/s.

c) 450 ± 10 ms after detection of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem, the receiver shall examine the descrambled repetitive dibits R2 from the distant modem to determine the operating rate for subsequent transmission as defined in Table 3/V.22 *bis*; at this time, the receiver may begin making decisions at the rate indicated by R2 which may differ from R1.

d) 600 ± 10 ms after detection of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem, the transmission shall begin transmission of scrambled binary ones at a rate indicated by the dibit R2 from the distant modem. Following transmission of 200 ± 10 ms of scrambled binary ones, the modem shall condition circuit 106 to respond to circuit 105 and the modem shall be ready to transmit data.

e) When 32 consecutive bits of scrambled binary one at the rate indicated by dibit R2 from the distant modem have been detected, the modem shall set circuit 112 to indicate the operating rate and unclamp circuit 104.

f) If a modem has transmitted a rate change sequence and has not received unscrambled repetitive double dibit 00 and 11 at 1200 bit/s immediately prior, or during, or within a time interval equal to the maximum expected two-way propagation delay, the modem may return to the beginning of the rate change sequence as defined above and repeat the procedure until unscrambled repetitive double dibit 00 and 11 is received from the remote modem. A time interval of 1.2 seconds is recommended for the maximum expected two-way propagation delay.

6.6.2 *Response to a rate change*

a) When the modem detects unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem, the modem shall turn circuit 106 OFF and clamp circuit 104 to binary one. During this procedure, circuit 109 and 107 shall remain on.

b) When the end of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem is detected, the modem shall condition its receiver for operation at 1200 bit/s and examine the descrambled repetitive dibit R1 (Note 2).

c) After having detected 32 consecutive rate dibits R1, at 1200 bit/s, the modem shall transmit unscrambled repetitive double dibit 00 and 11 at 1200 bit/s for 100 ± 3 ms followed by transmission of scrambled repetitive dibit R2 defining the operating rate (Note 3).

d) 450 ± 10 ms after the detection of 32 consecutive rate dibits R1 at 1200 bit/s from the distant modem, the modem may condition its receiver to begin operation at the data rate indicated by R2.

e) 600 ± 10 ms after the detection of 32 consecutive rate dibits R1 at 1200 bit/s, the modem shall begin transmission of scrambled binary ones at the data rate indicated by R2. After 200 ± 10 ms of scrambled binary ones, the modem shall condition circuit 106 to respond to circuit 105 and the modem shall be ready to transmit data.

f) When 32 consecutive bits of scrambled binary one, at the rate indicated by the dibit R2 have been detected from the distant modem, the modem shall set circuit 112 to indicate the operating rate and unclamp circuit 104.

Note 1 – This mode of operation, where implemented, should be provided on both GSTN circuits and leased circuits.

Note 2 – In the event where the initiating modem is requesting a retrain, the responding modem may delay transmission of the S1 sequence (which should be transmitted immediately following the detection of the end of receipt of the S1 sequence per § 6.4) by more than 32 dibit duration after receipt of the end of the S1 sequence from the initiating modem.

Note 3 – It is the intent that for a rate change to occur, dibit R2 be set equal to dibit R1. Modems not supporting this option may return a dibit R2 that differs from R1.

TABLE 4/V.22 *bis*

Operating rate	Dibit R1 and R2
2400	11
1200	01 or 10

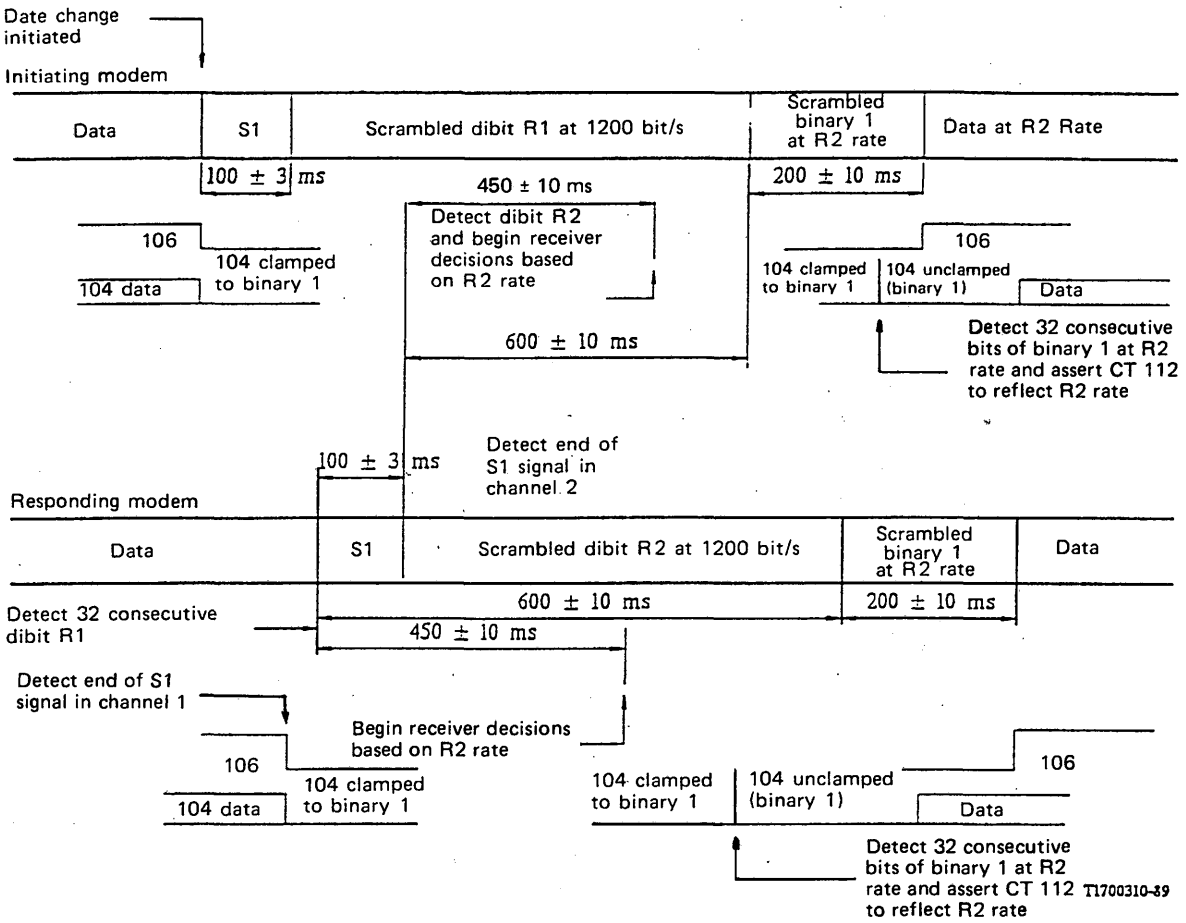


FIGURE 9/V.22 bis

Optional rate change sequence

7 Testing facilities

7.1 *Test loops*

Test loops 2 (local and remote) and 3 as defined in Recommendation V.54 shall be provided. Interface operation shall be as defined in Recommendation V.54. Instigation and termination sequences are not compatible with Recommendation V.54.

7.1.1 *Instigation of remote loop 2*

Signals controlling the application of remote loop 2 may only be transmitted after the synchronizing handshake has been completed.

As in Recommendation V.54, the modems are referred to as Modem A and Modem B.

When Modem A is instructed to instigate a remote loop 2, the modem shall transmit an initiation signal of unscrambled binary 1 at 2400 bit/s (or 1200 bit/s).

Modem B shall detect 154-231 ms of the initiation signal, and then transmit to Modem A scrambled alternating binary ones and zeros (reversals) at 2400 bit/s (or 1200 bit/s).

Modem A shall detect 231-308 ms of scrambled reversals, cease transmission of the initiation signal, and then transmit scrambled binary 1 at 2400 bit/s (or 1200 bit/s).

Modem B shall detect the loss of initiation signal and achieve loop 2 within Modem B.

Modem A, upon receiving 231-308 ms of scrambled binary 1 shall indicate to the DTE that it may begin sending test messages.

7.1.2 *Termination of remote loop 2*

When Modem A is instructed to terminate a remote loop 2 the line signal shall be suppressed for a period of 77 $\pm$ 10 ms, after which transmission shall be restored.

Modem B detects the loss of line signal in 40 to 65 ms and detects the re-appearance of the signal within 155 $\pm$ 50 ms, after which the modem B returns to normal operation.

7.2 *Self tests*

7.2.1 *Self test end-to-end*

Upon activation of the self test switch, an internally generated data pattern of alternative binary ones and zeros (reversals) at the selected bit rate shall be applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals, shall be connected to the output of the descrambler. The presence of errors shall be indicated by a visual indicator. All generating interchange circuits except 114 (if used), 115, 125 and 142 shall be clamped to the binary 1 or OFF condition. If circuit 113 is used, the DCE shall disregard this interchange circuit and use its internal clock.

7.2.2 *Self test with loop 3*

Loop 3 shall be applied to the modem as defined in Recommendation V.54. The self-test switch shall be activated and DCE operation shall be as in § 7.2.1.

7.2.3 *Self test with remote loop 2*

The modem shall be conditioned to instigate a loop 2 at the remote modem as specified in § 7.1. The self-test switch shall be activated and DCE operation shall be as in § 7.2.1.

It shall be possible to perform the above tests (in §§ 7.2.1, 7.2.2 and 7.2.3) with or without the DTE connected to the modem. These tests employ an internally generated data pattern that is controlled by a switch on the DCE.

7.2.4 During any self-test mode, interchange circuits 103, 105 and 108 will be ignored. Note that self tests do not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver.

Note – Inclusion of remote loop signalling according to Recommendation V.54 is for further study.

600/1200-BAUD MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

(Geneva, 1964; amended at Mar del Plata, 1968, Geneva, 1972, 1976 and 1980, Malaga-Torremolinos, 1984 and at Melbourne, 1988)

Note – The modem, designed for use on connections set up by switching in the general telephone network, can obviously be used on leased lines.

1 The principal characteristics recommended for a modem to transmit data at medium speed in the general switched telephone network are as follows:

- use of modulation rates up to 600/1200 bauds on the communication channel (see Recommendation V.5);
- frequency modulation with synchronous or asynchronous mode of operation;
- inclusion of a backward channel at modulation rates up to 75 bauds for error control, use of this channel being optional.

2 Modulation rates and characteristic frequencies for the forward data-transmission channel

	F_0	F_Z (symbol 1, mark)	F_A symbol 0, space)
Mode 1: up to 600 bauds	1500 Hz	1300 Hz	1700 Hz
Mode 2: up to 1200 bauds	1700 Hz	1300 Hz	2100 Hz

It is understood that the modem would be used in mode 1 when the presence of long loaded cables and/or the presence on some connections of signalling receivers operating close to 2000 Hz would prevent satisfactory transmission in mode 2. The modem could be used in mode 2 on suitable connections.

3 Tolerances on the characteristic frequencies for the forward channel

It should be possible with all rates of modulation to permit a tolerance, at the transmitter, of ± 10 Hz on both the F_A and F_Z frequencies. This tolerance should be considered as a limit.

Acceptance of these tolerances would give a tolerance of ± 10 Hz for the mean-frequency $F_0 = (F_A + F_Z)/2$.

The tolerance on the frequency difference $F_A - F_Z$ with regard to the nominal value would be ± 20 Hz.

A maximum frequency drift of ± 6 Hz has been assumed in the connection between the modems which might consist of several carrier circuits connected in tandem. This would make the tolerances on the mark and space frequencies at the receiving modem ± 16 Hz.

4 Modulation rate and characteristic frequencies for the backward channel

The modulation rate and characteristic frequencies for the backward channel are as follows:

	F_Z (symbol 1, mark)	F_A (symbol 0, space)
Modulation rate up to 75 bauds	390 Hz	450 Hz

In the absence of any signal on the backward channel interface, the condition Z signal is to be transmitted.

5 Tolerances on the characteristic frequencies of the backward channel

As the backward channel is a VF telegraph-type channel, the frequency tolerances should be as recommended in Recommendation R.35 [1] for frequency-shift voice-frequency telegraphy.

The ± 6-Hz frequency drift in the connection between the modems postulated in § 3 above would produce additional distortion in the backward channel. This should be taken into account in the design.

6 Division of power between the forward and backward channels

Considering the following table which shows the levels of power for total power remaining equal to 1 mW:

Forward channel level (dBm)	*Backward channel level* (dBm)
0	$-\infty$
−1	−7
−2	−4
−3	−3

equal division of power between the forward and backward channels could be recommended provisionally.

7 The following information is provided to assist equipment manufacturers:

a) The nominal range of attenuations in subscriber-to-subscriber connections is from 5 to 30 dB at the reference frequency (800 or 1000 Hz), assuming up to 35-dB attenuation at the recommended mean frequency (F_0) of the forward channel.

b) A convenient range of sensitivity at the mean frequency F_0 for data receivers has been found to be −40 to 0 dBm for the forward channel at the subscribers' terminals.

c) The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

8 Interchange circuits

The configurations of interchange circuits are those essential for the particular switched network or leased circuit requirement as indicated in Tables 1/V.23 and 2/V.23. Where one or more of such requirements are provided in a modem, then all the appropriate interchange circuits should be provided.

8.1 *List of interchange circuits essential for the modems when used on the general switched telephone network, including terminals equipped for manual calling or answering or automatic calling or answering* (see Table 1/V.23).

8.2 *List of interchange circuits essential for the modems when used on non-switched leased telephone circuits* (see Table 2/V.23)

8.3 *Response times of circuits 106 and 109, 121 and 122*

8.3.1 *Definitions*

8.3.1.1 Circuits 109 and 122 response times are the times that elapse between the connection or removal of a tone to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuits 109 and 122.

The test tone should have a frequency corresponding to the characteristic frequency of binary 1 and be derived from a source with an impedance equal to the nominal input impedance of the modem.

The level of the test tone should fall within the level range between 3 dB above the actual threshold of the received line signal detector and the maximum admissible level of the received signal. At all levels within this range the measured response times shall be within the specified limits.

TABLE 1/V.23

Interchange circuit		Forward (data) channel one-way system (Note 1)				Forward (data) channel either way system (Note 1)	
No.	Designation	Without backward channel		With backward channel		Without backward channel	With backward channel
		Transmit end	Receive end	Transmit end	Receive end		
102	Signal ground or common return	X	X	X	X	X	X
103	Transmitted data	X	–	X	–	X	X
104	Received data	–	X	–	X	X	X
105	Request to send	–	–	–	–	X	X
106	Ready for sending	X	–	X	–	X	X
107	Data set ready	X	X	X	X	X	X
108/1 or 108/2 (Note 2)	Connect data set to line Data terminal ready	X	X	X	X	X	X
109	Data channel received line signal detector	–	X	–	X	X	X
111	Data signalling rate selector (DTE)	X	X	X	X	X	X
114 (Note 3)	Transmitter signal element timing (DCE)	X	–	X	–	X	X
115 (Note 3)	Receiver signal element timing (DCE)	–	X	–	X	X	X
118	Transmitted backward channel data	–	–	–	X	–	X
119	Received backward channel data	–	–	X	–	–	X
120	Transmit backward channel line signal	–	–	–	–	–	X
121 (Note 4)	Backward channel ready	–	–	–	X	–	X
122 (Note 4)	Backward channel received line signal detector	–	–	X	–	–	X
125	Calling indicator	X	X	X	X	X	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 9).

Note 2 – This circuit shall be capable of operation as circuit 108/1 – *Connect data set to line* or circuit 108/2 – *Data terminal ready* depending on its use.

Note 3 – These circuits are required when the optional clock is implemented in the modem.

Note 4 – These circuits are not required if the modem is operating in an asymmetrical duplex mode.

TABLE 2/V.23

Interchange circuit		Forward (data) channel one-way system (Note 1)				Forward data channel either way or both ways simultaneously system (Note 1)	
No.	Designation	Without backward channel		With backward channel		Without backward channel	With backward channel
		Transmit end	Receive end	Transmit end	Receive end		
102	Signal ground or common return	X	X	X	X	X	X
103	Transmitted data	X	–	X	–	X	X
104	Received data	–	X	–	X	X	X
105	Request to send	X	–	X	–	X	X
106	Ready for sending	X	–	X	–	X	X
107	Data set ready	X	X	X	X	X	X
108/1	Connect data set to line	X	X	X	X	X	X
109	Data channel received line signal detector	–	X	–	X	X	X
111	Data signalling rate selector (DTE)	X	X	X	X	X	X
114 (Note 2)	Transmitter signal element timing (DCE)	X	–	X	–	X	X
115 (Note 2)	Receiver signal element timing (DCE)	–	X	–	X	X	X
118	Transmitted backward channel data	–	–	–	X	–	X
119	Received backward channel data	–	–	X	–	–	X
120	Transmit backward channel line signal	–	–	–	X	–	X
121	Backward channel ready	–	–	–	X	–	X
122	Backward channel received line signal datector	–	–	X	–	–	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 9).

Note 2 – These circuits are required when the optional clock is implemented in the modem.

8.3.1.2 Circuit 106 response times are from the connection of an ON or OFF condition on:

- circuit 105 (where it is provided) to the appearance of the corresponding ON or OFF condition on circuit 106;
- circuit 122 (where circuit 105 is not provided) to the appearance of the corresponding ON or OFF condition on circuit 106 in a configuration having a single data channel together with a single backward channel only.
- circuit 107 (where circuits 105 and 122 are not provided) to the appearance of the corresponding ON or OFF condition on circuit 106;

8.3.1.3 Circuit 121 response times are from the connection of an ON or OFF condition on:

- circuit 120 (where it is provided) to the appearance of the corresponding ON or OFF condition on circuit 121;
- circuit 109 (where circuit 120 is not provided) to the appearance of the corresponding ON or OFF condition on circuit 121.

8.3.2 *Response times*

TABLE 3/V.23

Circuit 106		
OFF to ON	750 ms to 1400 ms (see Note 1)	a) 20 ms to 40 ms (see Note 2) b) 200 ms to 275 ms (see Note 2)
ON to OFF	⩽ 2 ms	
Circuit 109		
OFF to ON	300 ms to 700 ms (see Note 1)	10 ms to 20 ms (see Note 1)
ON to OFF	5 ms to 15 ms	
Circuit 121		
OFF to ON	80 ms to 160 ms	
ON to OFF	⩽ 2 ms	
Circuit 122		
OFF to ON	< 80 ms	
ON to OFF	15 ms to 80 ms	

Note 1 – For automatic calling and answering, the longer response times of circuits 106 and 109 are to be used during call establishment only.

Note 2 – The choice of response times depends upon the system application:
a) no protection given against line echoes;
b) protection given against line echoes.

Note 3 – The above parameters are provisional and are the subject of further study.

8.4 *Threshold of data channel and backward channel received line signal detectors*

Level of received line signal at receive line terminals of modem for all types of connections, i.e. general switched telephone network or non-switched leased telephone circuits:

greater than	−43 dBm	circuits 109/122 ON
less than	−48 dBm	circuits 109/122 OFF

The condition of circuits 109 and 122 for levels between −43 dBm and −48 dBm is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

Where transmission conditions are known on switched or leased circuits, Administrations should be permitted at the time of modem installation to change these response levels of the received line signal detectors to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

8.5 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

i) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 milliseconds following the ON to OFF transition on circuit 105. The use of this additional delay is optional, based on system considerations;

ii) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

8.6 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types).

8.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

8.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

8.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

9 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

10 Equipment for the disablement of echo suppressors

When echo control device disabling is required, it is recommended that the procedures specified in Recommendation V.25 be followed.

11 Inclusion of a clock in the modem

A clock is not an essential item in the standardized modem. However, the modem may conveniently include a clock when used primarily for synchronous transmission.

If such a clock is included in the modem, a synchronizing pattern consisting of alternate binary 0 and binary 1 at clock rate should be transmitted for the whole interval between the OFF to ON transitions of interchange circuits 105 and 106. Users should note that part of this synchronizing pattern may appear at the distant receiver on circuit 104 after the OFF to ON transition of circuit 109. The data terminal equipment should make provision to differentiate between these false signals and true data.

Reference

[1] CCITT Recommendation *Standardization of FMVFT systems for a modulation rate of 50 bauds*, Vol. VII, Rec. R.35.

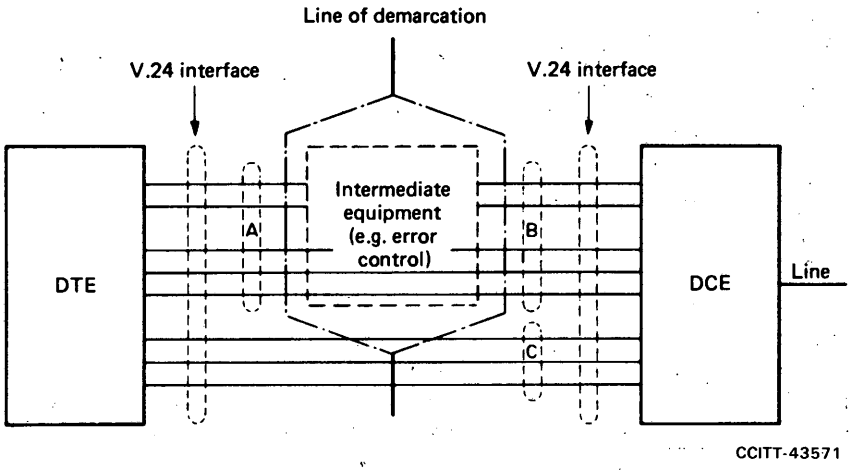
Recommendation V.24

LIST OF DEFINITIONS FOR INTERCHANGE CIRCUITS BETWEEN DATA TERMINAL EQUIPMENT (DTE) AND DATA CIRCUIT-TERMINATING EQUIPMENT (DCE)

(Geneva, 1964, amended at Mar del Plata, 1968, Geneva, 1972, 1976 and 1980, Malaga-Torremolinos, 1984 and at Melbourne, 1988)

1 Scope

1.1 This Recommendation applies to the interconnecting circuits being called interchange circuits at the interface between DTE and DCE for the transfer of binary data, control and timing signals and analogue signals as appropriate. This Recommendation also applies to both sides of separate intermediate equipment, which may be inserted between these two classes of equipment (see Figure 1/V.24).



Without intermediate equipment the selections A and B are identical.
Selection C may be a selection specifically for automatic calling.

FIGURE 1/V.24

Illustration of general layout of equipment

Electrical characteristics for interchange circuits are detailed in appropriate Recommendations for electrical characteristics, or in certain special cases, in Recommendations for DCE.

In any type of practical equipment a selection will be made from the range of interchange circuits defined in this Recommendation, as appropriate.

The actual interchange circuits to be used in a particular DCE are those indicated in the appropriate Recommendation.

The required interchange circuits specified in the DCE Recommendations which make reference to this Recommendation apply only to the DCE side of the interface. Only those circuits necessary to assure satisfactory operation of the application the DTE is intending to support need be controlled or monitored by the DTE. (See note to § 3.4 for proper handling of unimplemented circuits).

The usage and operational requirements of the interchange circuits and the interaction between them are recommended in § 4. For proper operation of the DCE it is important that the guidelines in § 4 are observed.

1.2 The DCE may include signal converters, timing generators, pulse regenerators, and control circuitry, together with equipment to provide other functions such as error control, automatic calling and automatic answering. Some of this equipment may be separate intermediate equipment or it may be located in the DTE.

1.3 The range of interchange circuits defined in this Recommendation is applicable, for example:

a) to synchronous and asynchronous data communications;

b) to data transmission on leased line service, either 2-wire or 4-wire, either point-to-point or multipoint operation;

c) to data transmission on switched network service, either 2-wire or 4-wire;

d) where short interconnecting cables are used between DTE and DCE. An explanation of short cables is given in § 2 below.

1.4 A DTE interface conforming to this Recommendation may also be used for attachment to a Public Data Network (PDN). For these cases, additional information on interchange circuit implementation and operational requirements may be recorded in Series X Recommendations.

2 Line of demarcation

The interface between DTE and DCE is located at a connector, which is the interchange point between these two classes of equipment. Separate connectors may be provided for the interchange circuits associated with the signal-conversion or similar equipment and those associated with the parallel automatic calling equipment. For mechanical characteristics of the interface refer to ISO 2110 or ISO 4902 as appropriate.

The connector(s) will not necessarily be physically attached to the DCE and may be mounted in a fixed position near the DTE.

An interconnecting cable or cables will normally be provided with the DTE. The use of short cables is recommended. Their length should be limited solely by the load capacitance and other electrical characteristics specified in the relevant Recommendation on electrical characteristics.

3 Definitions of interchange circuits

3.1 *100 series – General application*

A list of these interchange circuits is presented in tabular form in Table 1/V.24.

Circuit 102 – Signal ground or common return

This conductor establishes the signal common return for unbalanced interchange circuits with electrical characteristics according to Recommendation V.28 and the d.c. reference potential for interchange circuits according to Recommendations V.10, V.11 and V.35.

Within the DCE, this circuit shall be brought to one point, and it shall be possible to connect this point to protective ground or earth by means of a metallic strap within the equipment. This metallic strap can be connected or removed at installation, as may be required to meet applicable safety regulations or to minimize the introduction of noise into electronic circuitry. Caution should be exercised to prevent the establishment of ground loops carrying high currents.

TABLE 1/V.24

100-series interchange circuits by category

Interchange circuit number	Interchange circuit name	Ground	Data		Control		Timing	
			From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	2	3	4	5	6	7	8	9
102	Signal ground or common return	X						
102a	DTE common return	X						
102b	DCE common return	X						
102c	Common return	X						
103	Transmitted data			X				
104	Received data		X					
105	Request to send					X		
106	Ready for sending				X			
107	Data set ready				X			
108/1	Connect data set to line					X		
108/2	Data terminal ready					X		
109	Data channel received line signal detector				X			
110	Data signal quality detector				X			
111	Data signal rate selector (DTE)					X		
112	Data signal rate selector (DCE)				X			
113	Transmitter signal element timing (DTE)							X
114	Transmitter signal element timing (DCE)						X	
115	Receiver signal element timing (DCE)						X	
116/1	Back-up switching in direct mode					X		
116/2	Back-up switching in authorized mode					X		
117	Standby indicator				X			
118	Transmitted backward channel data			X				
119	Received backward channel data		X					
120	Transmit backward channel line signal					X		
121	Backward channel ready				X			
122	Backward channel received line signal detector				X			
123	Backward channel signal quality detector				X			
124	Select frequency groups					X		
125	Calling indicator				X			
126	Select transmit frequency					X		
127	Select receive frequency					X		
128	Receiver signal element timing (DTE)							X
129	Request to receive					X		
130	Transmit backward tone					X		
131	Received character timing						X	
132	Return to non-data mode					X		
133	Ready for receiving					X		
134	Received data present				X			
136	New signal					X		
140	Loopback/Maintenance test					X		
141	Local loopback					X		
142	Test indicator				X			
191	Transmitted voice answer					X		
192	Received voice answer				X			

Circuit 102a – DTE common return

This conductor is connected to the DTE circuit common return and is used as the reference potential for the unbalanced Recommendation V.10-type interchange circuit receivers within the DCE.

Circuit 102b – DCE common return

This conductor is connected to the DCE circuit common return and is used as the reference potential for the unbalanced Recommendation V.10-type interchange circuit receivers within the DTE.

Note – Where a mixture of Recommendations V.10 and V.11 circuits is used in the same interface, separate provision must be made for the Recommendation V.10 common return circuits 102a and 102b, and for a d.c. reference potential conductor circuit 102, or protective ground connection, as required.

Circuit 102c – Common return

This conductor establishes the signal common return for single-current interchange circuits controlled by contact closure with electrical characteristics according to Recommendation V.31, in cases where a common return is used.

Within the equipment containing the signal source of the interchange circuit, this conductor must be isolated from signal ground and protective ground, irrespective of whether it is located within the DCE or within the DTE.

Circuit 103 – Transmitted data

Direction: To DCE

The data signals originated by the DTE:

1) to be transmitted via a data channel to one or more remote data stations,
2) to be passed to the DCE for maintenance test purposes under control of the DTE, or
3) for the programming or control of serial automatic calling DCEs,

are transferred on this circuit to the DCE.

Circuit 104 – Received data

Direction: From DCE

The data signals generated by the DCE:

1) in response to data channel line signals received from a remote data station,
2) in response to the DTE maintenance test signals, or
3) in response to (or as an echo of) programming or control signals from the DTE where a serial automatic calling facility is implemented in the DCE,

are transferred on this circuit to the DTE.

Note – The reception conditions for maintenance test signals are specified with circuit 107.

Circuit 105 – Request to send

Direction: To DCE

Signals on this circuit control the data channel transmit function of the DCE.

The ON condition causes the DCE to assume the data channel transmit mode.

The OFF condition causes the DCE to assume the data channel non-transmit mode, when all data transferred on circuit 103 have been transmitted.

Circuit 106 – Ready for sending

Direction: From DCE

Signals on this circuit indicate whether the DCE is prepared to accept data signals for transmission on the data channel or for maintenance test purposes under control of the DTE.

The ON condition indicates that the DCE is prepared to accept data signals from the DTE.

The OFF condition indicates that the DCE is not prepared to accept data signals from the DTE.

Circuit 107 – Data set ready

Direction: From DCE

Signals on this circuit indicate whether the DCE is ready to operate.

The ON condition, where circuit 142 is OFF or is not implemented, indicates that the signal converter or similar equipment is connected to the line and that the DCE is ready to exchange further control signals with the DTE to initiate transfer of data.

The ON condition, in conjunction with the ON condition of circuit 142, indicates that the DCE is prepared to exchange data signals with the DTE for maintenance test purposes.

The OFF condition, in conjunction with the ON condition on circuit 106, indicates that the DCE is ready to exchange data signals associated with the programming or control of serial automatic calling DCEs.

The OFF condition, in conjunction with the OFF condition on circuit 106, indicates:

1) that the DCE is not ready to operate in the data transfer phase,
2) that the DCE has detected a fault condition (which may be network or DCE dependent) which has lasted longer than some fixed period of time, such period of time being network dependent, or
3) in switched network operation, that the DCE has detected a disconnect indication from the remote station or from the network.

The OFF condition, in conjunction with the ON condition on circuit 142, indicates that the DCE is involved in tests from the network or remote station.

Circuit 108/1 – Connect data set to line

Direction: To DCE

Signals on this circuit control switching of the signal-converter or similar equipment to or from the line.

The ON condition on this circuit, except as noted below, causes the DCE to connect the signal-converter or similar equipment to the line and to maintain this connection.

The ON condition on this circuit may also be used to initiate a direct call facility for automatic calling DCEs.

The OFF condition on this circuit, except as noted below, causes the DCE to remove the signal-converter or similar equipment from the line, when the transmission to the line of all data previously transferred on circuit 103 and/or circuit 118 has been completed.

The OFF condition on this circuit may also be used to direct the DCE to abort or to clear a direct call facility operation (see Recommendation V.25 *bis*).

Circuit 108/2 – Data terminal ready

Direction: To DCE

Signals on this circuit control switching of the signal-converter or similar equipment to or from the line.

The ON condition, indicating that the DTE is ready to operate, prepares the DCE to connect the signal-conversion or similar equipment to the line and maintains this connection after it has been established by supplementary means.

The DTE is permitted to present the ON condition on circuit 108/2 whenever it is ready to transmit or receive data.

The OFF condition causes the DCE to remove the signal-converter or similar equipment from the line, when the transmission to line of all data previously transferred on circuit 103 and/or circuit 118 has been completed.

The OFF condition of this circuit may also be used to direct the DCE to abort or to clear a serial automatic calling operation (see Recommendation V.25 *bis*).

Circuit 109 – Data channel received line signal detector

Direction: From DCE

Signals on this circuit indicate whether the received data channel line signal is within appropriate limits, as specified in the relevant Recommendation for DCE.

Circuit 109 may also be in the ON condition during the exchange of data signals between the DCE and the DTE, associated with the programming or control of serial automatic calling DCEs.

The OFF condition indicates that the received signal is not within appropriate limits.

Circuit 110 – Data signal quality detector

Direction: From DCE

Signals on this circuit indicate whether there is a reasonable probability of an error in the data received on the data channel. The signal quality indicated conforms to the relevant DCE Recommendation.

The ON condition indicates that there is no reason to believe that an error has occurred.

The OFF condition indicates that there is a reasonable probability of an error.

Circuit 111 – Data signalling rate selector (DTE source)

Direction: To DCE

Signals on this circuit are used to select one of the two data signalling rates of a dual rate synchronous DCE, or to select one of the two ranges of data signalling rates of a dual range asynchronous DCE.

The ON condition selects the higher rate or range of rates.

The OFF condition selects the lower rate or range of rates.

Circuit 112 – Data signalling rate selector (DCE source)

Direction: From DCE

Signals on this circuit are used to select one of the two data signalling rates or ranges of rates in the DTE to coincide with the data signalling rate or range of rates in use in a dual rate synchronous or dual range asynchronous DCE.

The ON condition selects the higher rate or range of rates.

The OFF condition selects the lower rate or range of rates.

Circuit 113 – Transmitter signal element timing (DTE source)

Direction: To DCE

Signals on this circuit provide the DCE with signal element timing information.

The condition on this circuit shall be ON and OFF for nominally equal periods of time and the transition from ON to OFF condition shall nominally indicate the centre of each signal element on circuit 103.

Circuit 114 – Transmitter signal element timing (DCE source)

Direction: From DCE

Signals on this circuit provide the DTE with signal element timing information.

The condition on this circuit shall be ON and OFF for nominally equal periods of time. The DTE shall present a data signal on circuit 103 in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of circuit 114.

Circuit 115 – Receiver signal element timing (DCE source)

Direction: From DCE

Signals on this circuit provide the DTE with signal element timing information.

The condition of this circuit shall be ON and OFF for nominally equal periods of time, and a transition from ON to OFF condition shall nominally indicate the centre of each signal element on circuit 104.

Circuit 116/1 – Back-up swtiching in direct mode

Direction: To the DCE

Signals on this circuit control switching of the DCE between normal and standby facilities.

The ON condition causes the DCE to connect to the standby facility.

The OFF condition causes the DCE to disconnect from the standby facility, when the transmission to line of all data previously transferred on circuit 103 has been completed, and the DCE then reconnects to the normal facility.

Circuit 116/2 – Back-up switching in authorized mode

Direction: To the DCE

Signals on this circuit control switching of the DCE between normal and standby facilities.

The ON condition indicates that the DTE is ready to switch from the normal to the standby facility and prepares the DCE to switch to the standby facility when necessary.

The OFF condition causes the DCE to disconnect from the standby facility, when the transmission to line of all data previously transferred on circuit 103 has been completed, and the DCE then reconnects to the normal facility.

Circuit 117 – Standby indicator

Direction: From DCE

Signals on this circuit indicate whether the DCE is conditioned to operate in its standby mode with the predetermined facilities replaced by their reserves.

The ON condition indicates that the DCE is conditioned to operate in its standby mode.

The OFF condition indicates that the DCE is conditioned to operate in its normal mode.

Circuit 118 – Transmitted backward channel data

Direction: To DCE

This circuit is equivalent to circuit 103, except that it is used to transmit data via the backward channel.

Circuit 119 – Received backward channel data

Direction: From DCE

This circuit is equivalent to circuit 104, except that it is used for data received on the backward channel.

Circuit 120 – Transmit backward channel line signal

Direction: To DCE

This circuit is equivalent to circuit 105, except that it is used to control the backward channel transmit function of the DCE.

The ON condition causes the DCE to assume the backward channel transmit mode.

The OFF condition causes the DCE to assume the backward channel non-transmit mode, when all data transferred on circuit 118 have been transmitted to line.

Circuit 121 – Backward channel ready

Direction: From DCE

This circuit is equivalent to circuit 106, except that it is used to indicate whether the DCE is conditioned to transmit data on the backward channel.

The ON condition indicates that the DCE is conditioned to transmit data on the backward channel.

The OFF condition indicates that the DCE is not conditioned to transmit data on the backward channel.

Circuit 122 – Backward channel received line signal detector

Direction: From DCE

This circuit is equivalent to circuit 109, except that it is used to indicate whether the received backward channel line signal is within appropriate limits, as specified in the relevant Recommendation for DCE.

Circuit 123 – Backward channel signal quality detector

Direction: From DCE

This circuit is equivalent to circuit 110, except that it is used to indicate the signal quality of the received backward channel line signal.

Circuit 124 – Select frequency groups

Direction: To DCE

Signals on this circuit are used to select the desired frequency groups available in the DCE.

The ON condition causes the DCE to use all frequency groups to represent data signals.

The OFF condition causes the DCE to use a specified reduced number of frequency groups to represent data signals.

Circuit 125 – Calling indicator

Direction: From DCE

Signals on this circuit indicate whether a calling signal is being received by the DCE.

The ON condition indicates that a calling signal is being received.

The OFF condition indicates that no calling signal is being received, and this condition may also appear during interruptions of a pulse-modulated calling signal.

Circuit 126 – Select transmit frequency

Direction: To DCE

Signals on this circuit are used to select the required transmit frequency of the DCE.

The ON condition selects the higher transmit frequency.

The OFF condition selects the lower transmit frequency.

Circuit 127 – Select receive frequency

Direction: To DCE

Signals on this circuit are used to select the required receive frequency of the DCE.

The ON condition selects the lower receive frequency.

The OFF condition selects the higher receive frequency.

Circuit 128 – Receiver signal element timing (DTE source)

Direction: To DCE

Signals on this circuit provide the DCE with signal element timing information.

The condition on this circuit shall be ON and OFF for nominally equal periods of time. The DCE shall present a data signal on circuit 104 in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of the signal on circuit 128.

Circuit 129 – Request to receive

Direction: To DCE

Signals on this circuit are used to control the receive function of the DCE.

The ON condition causes the DCE to assume the receive mode.

The OFF condition causes the DCE to assume the non-receive mode.

Circuit 130 – Transmit backward tone

Direction: To DCE

Signals on this circuit control the transmission of a backward channel tone.

The ON condition causes the DCE to transmit a backward channel tone.

The OFF condition causes the DCE to stop the transmission of a backward channel tone.

Circuit 131 – Received character timing

Direction: From DCE

Signals on this circuit provide the DTE with character timing information, as specified in the relevant Recommendation for DCE.

Circuit 132 – Return to non-data mode

Direction: To DCE

Signals on this circuit are used to restore the non-data mode provided with the DCE, without releasing the line connection to the remote station.

The ON condition causes the DCE to restore the non-data mode. When the non-data mode has been established, this circuit must be turned OFF.

Circuit 133 – Ready for receiving

Direction: To DCE

Signals on this circuit control the transfer of data on circuit 104, indicating whether the DTE is capable of accepting a given amount of data (e.g. a block of data), specified in the appropriate Recommendation for an intermediate function, for example, error control.

The ON condition must be maintained whenever the DTE is capable of accepting data, and causes the intermediate equipment or DCE to transfer the received data to the DTE.

The OFF condition indicates that the DTE is not able to accept data, and causes the intermediate equipment or DCE to retain the data.

Circuit 134 – Received data present

Direction: From DCE

Signals on this circuit are used to separate information messages from supervisory messages, transferred on circuit 104, as specified in the appropriate Recommendation for intermediate equipment, e.g. error control equipment.

The ON condition indicates the data which represent information messages.

The OFF condition shall be maintained at all other times.

Circuit 136 – New signal

Direction: To DCE

Signals on this circuit are used to control the response times of the DCE receiver.

The ON condition of circuit 136 instructs the DCE receiver to prepare itself to detect rapidly the disappearance of the line signal (e.g., by disabling the response time circuitry associated with circuit 109). After the received line signal falls below the threshold of the received line signal detector, the DCE will:

1) turn OFF circuit 109, and
2) prepare itself to detect rapidly the appearance of a new line signal (e.g., by resetting the receiver timing recovery circuitry).

Once turned ON, circuit 136 may be turned OFF after one unit interval and must be turned OFF after circuit 109 is turned OFF. Circuit 136 shall be OFF at all other times.

Circuit 140 – Loopback/Maintenance test

Direction: To DCE

Signals on this circuit are used to initiate and release loopback or other maintenance test conditions in DCEs.

The ON condition causes initiation of the maintenance test condition.

The OFF condition causes release of the maintenance test condition.

Circuit 141 – Local loopback

Direction: To DCE

Signals on this circuit are used to control the loop 3 test condition in the local DCE.

The ON condition of circuit 141 causes the establishment of the loop 3 test condition in the local DCE.

The OFF condition of circuit 141 causes the release of the loop 3 test condition in the local DCE.

Circuit 142 – Test indicator

Direction: From DCE

Signals on this circuit indicate whether a maintenance condition exists.

The ON condition indicates that a maintenance condition exists in the DCE, precluding reception or transmission of data signals from or to a remote DTE.

The OFF condition indicates that the DCE is not in a maintenance test condition.

Circuit 191 – Transmitted voice answer

Direction: To DCE

Signals generated by a voice answer unit in the DTE are transferred on this circuit to the DCE.

The electrical characteristics of this analogue interchange circuit are part of the appropriate DCE Recommendation.

Circuit 192 – Received voice answer

Direction: From DCE

Received voice signals, generated by a voice answering unit at the remote DTE, are transferred on this circuit to the DTE.

The electrical characteristics of this analogue interchange circuit are part of the appropriate DCE Recommendation.

3.2 *200-series – Specifically for parallel automatic calling*

A list of these interchange circuits is presented in tabular form in Table 2/V.24.

For parallel automatic calling procedures, refer to Recommendation V.25 for the general switched telephone network and Recommendation S.16 [1] for the telex network.

TABLE 2/V.24

200-series interchange circuits specifically for automatic calling

Interchange circuit number	Interchange circuit name	From DCE	To DCE
201	Signal ground or common return	X	X
202	Call request		X
203	Data line occupied	X	
204	Distant station connected	X	
205	Abandon call	X	
206	Digit signal (2^0)		X
207	Digit signal (2^1)		X
208	Digit signal (2^2)		X
209	Digit signal (2^3)		X
210	Present next digit	X	
211	Digit present		X
213	Power indication	X	

Circuit 201 – Signal ground or common return

This conductor establishes the signal common reference potential for all 200-series interchange circuits. Within the parallel automatic calling equipment this circuit shall be brought to one point, and it shall be possible to connect this point to protective ground or earth by means of a metallic strap within the equipment. This metallic strap can be connected or removed at installation as may be required to meet applicable regulations or to minimize the introduction of noise into electronic circuitry. Caution should be exercised to prevent the establishment of ground loops carrying high currents.

Circuit 202 – Call request

Direction: To DCE

Signals on this circuit are used to condition the parallel automatic calling equipment to originate a call and to switch the automatic calling equipment to or from the line.

The ON condition causes the DCE to condition the parallel automatic calling equipment to originate a call and to connect this equipment to the line.

The OFF condition causes the automatic calling equipment to be removed from the line and indicates that the DTE has released the automatic calling equipment.

Circuit 203 – Data line occupied

Direction: From DCE

Signals on this circuit indicate whether or not the associated line is in use (e.g. for automatic calling, data transmission or voice communication, test procedures).

The ON condition indicates that the line is in use.

The OFF condition indicates that the line is not in use, and that the DTE may originate a call.

Circuit 204 – Distant station connected

Direction: From DCE

Signals on this circuit indicate whether a connection has been established to a remote data station (or telex station).

The ON condition indicates the receipt of a signal from a remote DCE signalling that a connection to that equipment has been established.

The OFF condition shall be maintained at all other times.

Circuit 205 – Abandon call

Direction: From DCE

Signals on this circuit indicate whether a preset time has elapsed between successive events in the calling procedure.

The ON condition indicates that the call should be abandoned.

The OFF condition indicates that call origination can proceed.

Digit signal circuits:

Circuit 206 – Digit signal (2^0)

Circuit 207 – Digit signal (2^1)

Circuit 208 – Digit signal (2^2)

Circuit 209 – Digit signal (2^3)

Direction: To DCE

On these circuits the DTE presents the code combinations shown in Table 3/V.24, being the digits of the data station (or telex station) to be called and the delimiting control characters.

TABLE 3/V.24

Information	Binary states			
	209	208	207	206
Digit 1	0	0	0	1
Digit 2	0	0	1	0
Digit 3	0	0	1	1
Digit 4	0	1	0	0
Digit 5	0	1	0	1
Digit 6	0	1	1	0
Digit 7	0	1	1	1
Digit 8	1	0	0	0
Digit 9	1	0	0	1
Digit 0	0	0	0	0
Control character EON	1	1	0	0
Control character SEP	1	1	0	1

The control character EON (end of number) causes the DCE to take appropriate action to await an answer from the called data station.

The control character SEP (separation) indicates the need for a pause between successive digits or in front of the digit series, and causes the parallel automatic calling equipment to insert the appropriate time interval.

The code combinations listed above are intended to apply only to equipment using Recommendations V.25 and S.16 [1].

Circuit 210 – Present next digit

Direction: From DCE

Signals on this circuit indicate whether the parallel automatic calling equipment is ready to accept the next code combination.

The ON condition indicates that the automatic calling equipment is ready to accept the next code combination.

The OFF condition indicates that the automatic calling equipment is not ready to accept signals on the digit signal circuits.

Circuit 211 – Digit present

Direction: To DCE

Signals on this circuit control the reading of the code combination presented on the digit signal circuits.

The ON condition causes the automatic calling equipment to read the code combination presented on the digit signal circuits.

The OFF condition on this circuit prevents the automatic calling equipment from reading a code combination on the digit signal circuits.

Circuit 213 – Power indication

Direction: From DCE

Signals on this circuit indicate whether power is available within the parallel automatic calling equipment.

The ON condition indicates that power is available within the automatic calling equipment.

The OFF condition indicates that power is not available within the automatic calling equipment.

3.3 *Circuit failures (electrical)*

The following interchange circuits, where implemented, shall be used to detect either a power-off condition in the equipment connected through the interface or the disconnection of the interconnecting cable:

Circuit 105 – Request to send
Circuit 107 – Data set ready
Circuit 108/1 – Connect data set to line
Circuit 108/2 – Data terminal ready
Circuit 120 – Transmit backward channel line signal
Circuit 202 – Call request
Circuit 213 – Power indication

The criteria used to determine a failure condition shall be specified in the appropriate Recommendation for electrical characteristics.

The receiver for these circuits shall interpret the power-off condition or the disconnection of the interconnecting cable as an OFF condition on these circuits.

3.4 *Optional circuits*

In some modem Recommendations optional facilities are defined which require control from the DTE via optional (non-essential) circuits. Additional optional facilities may exist in DCEs also requiring control via interchange circuits defined in this Recommendation.

The DCE should provide means to disable an option, when necessary, in case the DTE is not equipped with circuitry to control this option.

In case the DCE does not provide an option, proper operation of the DTE should not rely on any specific response from the DCE when the DTE activates the control circuit related to that option.

Note – DTEs may be in existence which do not comply with the above requirements. Therefore, for an interim period, DCEs not providing a certain option may provide means to respond to the DTE invocation of that option in the proper way. Especially, this may be the case for simplex or duplex DCEs not providing a carrier switch option (continuous carrier operation) but still responding with circuit 106 to circuit 105.

For an interim period of time, receiver circuits may be provided in a DTE or a DCE for which no generator is provided in the complementary equipment. Therefore, in cases where a receiver is not connected to a generator, it is suggested that means be provided in the equipment where the receiver is located to inhibit or disregard any possible false triggering of this receiver.

4 Operational requirements

In the following, operational requirements are given for the usage of interchange circuits. It also explains in further detail the required correlation between interchange circuits, where implemented.

4.1 *Data circuits*

It is evident that proper data transmission may be impaired when the required condition is not present on an implemented control interchange circuit. Therefore, the DTE shall not transfer, on circuit 103, data which is for transmission to line or for maintenance purposes unless an ON condition is present on all of the following four circuits, where implemented: circuit 105, circuit 106, circuit 107 and circuit 108/1 or 108/2.

The DTE may transfer, on circuit 103, data which is for the programming or control of serial automatic calling DCEs when an ON condition is present on circuits 106 and 108/2, and an OFF condition is present on circuit 107. In this situation, the condition of circuit 105 need not be considered, and may be ON for DTE convenience.

All data transferred on circuit 103 during the time an ON condition is present on all of the above four circuits, where implemented, shall be transmitted by the DCE.

Refer also to §§ 4.4 and 4.5 below for further explanation.

The DTE shall not transfer data on circuit 118 unless an ON condition is present on all of the following four circuits, where implemented: circuit 120, circuit 121, circuit 107 and circuit 108/1 or 108/2.

All data transferred on circuit 118 during the time an ON condition is present on all of the above four circuits, where implemented, shall be transmitted by the DCE.

4.2 *Idle periods*

During intervals when circuit 105 and circuit 106 are in the ON condition and no data are available for transmission, the DTE may transmit binary 1 condition, reversals or other sequences to maintain timing synchronizing, e.g. SYN coded characters, idle characters according to the data link control procedure used, etc.

Specific requirements, where applicable, are stated in the appropriate DCE Recommendations.

4.3 *Clamping*

4.3.1 In all applications the DCE shall hold, where implemented:

a) circuit 104 in the binary 1 condition when circuit 109 is in the OFF condition, and

b) circuit 119 in the binary 1 condition when circuit 122 is in the OFF condition.

4.3.2 In addition a DCE constrained to half-duplex operation on a 2-wire line shall also hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition, and for a short time interval (to be specified in Recommendations for DCE) following the ON to OFF transition on circuit 105; and

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition, when circuit 120 is in the ON condition, and for a short time interval (to be specified in Recommendations for DCE) following the ON to OFF transition on circuit 120.

4.4 *Operation of circuits 107, 108/1 and 108/2*

4.4.1 *In switched and leased line operations*

Signals on circuit 107 are to be considered as responses to signals which initiate connection to line, e.g. circuit 108/1. However, the conditioning of a data channel, such as equalization and clamp removal, cannot be expected to have been completed when circuit 107 is turned ON.

A wiring option shall be provided within the DCE to select either circuit 108/1 or circuit 108/2 operation.

Under certain test conditions, both the DTE and the DCE may exercise some of the interchange circuits. Thus, when circuits 107, 108/1 or 108/2 are both OFF, the DTE is to ignore the conditions on all other interchange circuits from the DCE, except those on circuit 125 and the timing circuits, and the DCE is to ignore the conditions on all other interchange circuits from the DTE.

During the maintenance phases specified in Recommendation V.54, when the DTE is not involved in the test, circuit 142 is in the ON condition and circuit 107 is in the OFF condition. Circuit 107 shall not respond to circuits 108/1 or 108/2. When the DTE is involved in the test, circuit 142 is in the ON condition and circuit 107 shall respond to circuit 108/1 or 108/2.

4.4.2 *In leased line operations*

Where circuit 108 is not implemented in the DTE, the condition on this circuit is assumed to be permanently ON.

Where circuit 108 is implemented in the DTE, it shall be implemented as circuit 108/1.

4.4.3 *In switched line operations*

When the DCE is conditioned for automatic answering of calls, answering of incoming calls occurs only in response to a combination of the calling signal and an ON condition of circuit 108/1 or 108/2.

The OFF condition of circuit 108/1 or 108/2 shall not disable the operation of circuit 125.

When circuit 108/2 is in the ON condition and circuit 107 is in the OFF condition, the DTE may communicate with serial automatic calling DCEs on circuits 103 and 104. This state is recognized by an ON condition on circuit 106.

When circuit 108/1 or 108/2 is turned OFF, it shall not be turned ON again until circuit 107 is turned OFF.

In the case where the DCE turns circuit 107 OFF first, the DTE shall consider the call aborted and shall proceed as described below:

1) In the case of circuit 108/1, the DTE shall turn this circuit OFF with minimal delay and shall hold the circuit in the OFF condition for a minimum of 500 ms. After that period of time, the DTE may turn circuit 108/1 back ON either to initiate a new direct call or to respond to an incoming call signalled by circuit 125 coming ON.

   The DCE shall not answer an incoming call or initiate a new call until circuit 108/1 has first been turned OFF and then back ON again.

2) In the case of circuit 108/2, the DTE shall turn this circuit OFF with minimal delay and shall hold the circuit in the OFF condition for a minimum of 500 ms. After that period of time, the DTE may turn circuit 108/2 back ON either to initiate a new serial automatic calling procedure or to signal the DCE that it is prepared to accept an incoming call.

The DCE shall answer an incoming call or initiate a new call until circuit 108/2 has been turned OFF and then back ON again or after a minimum delay (provisional value 2 s).

4.5 *Interrelationship of circuits 103, 105 and 106*

The DTE signals its intent to transmit data by turning ON circuit 105. It is then the responsibility of the DCE to enter the transmit mode, i.e. be prepared to transmit data, and also to alert the remote DCE and condition it to receive data. The means by which a DCE enters the transmit mode and alerts and conditions the remote DCE are described in the appropriate DCE Recommendation.

When the transmitting DCE turns circuit 106 ON with circuit 107 in the ON condition, the DTE is permitted to transfer data across the interface on circuit 103. By turning ON circuit 106 with circuit 107 ON, it is implied that all data transferred across the interface prior to the time that any one of the four circuits (105, 106, 107 and 108/1 or 108/2) is again turned OFF, will be transferred to the line; however, the ON condition of circuit 106 is not necessarily a guarantee that the remote DCE is in the receive mode. (Depending on the complexity and sophistication of the transmitting signal converter, there may be a delay ranging from less than a millisecond up to several seconds between the time a bit is transferred across the interface until the time a signal element representing this bit is transmitted on the line.)

When the transmitting DCE turns circuit 106 ON, with circuit 107 in the OFF condition, the DTE is permitted to transfer programming or control signals to a serial automatic calling DCE across the interface on circuit 103.

During data transfer, the DTE shall not turn circuit 105 OFF before the end of the last bit (data bit or stop element) is transferred across the interface on circuit 103. Similarly, in certain duplex switched network applications where circuit 105 is not implemented (see the specific DCE Recommendations), this requirement applies equally when circuit 108/1 or 108/2 is turned OFF to terminate a switched network call.

Where circuit 105 is provided, the ON and OFF conditions on circuit 106 during the data transfer phase (i.e. circuit 107 ON) shall be responses to the ON and OFF conditions on circuit 105. Circuit 106 may, however, be turned OFF during the data transfer and test phases independent of the condition of circuit 105 to signal the DTE to interrupt the transfer of data on circuit 103, transmitted data, for a finite period of time (e.g., for DCE flow control purposes or DCE/DCE resynchronization). It should be noted that data presented on circuit 103 after circuit 106 turns OFF may be disregarded by the DCE. It should also be noted that circuit 106 may be turned back ON again at any time, provided that circuit 105 is ON at that time. For the appropriate response times of circuit 106, and for the operation of circuit 106 when circuit 105 is not provided, refer to the relevant Recommendation for the DCE.

For serial automatic calling DCEs, the ON and OFF conditions on circuit 106 outside the data transfer phase (i.e. circuit 107 OFF) shall be dependent on the interface state during the automatic call set-up and associated procedures. The transitions on circuit 106 for this application shall be as detailed in Recommendation V.25 *bis*.

When circuit 105 and circuit 106 are both OFF, the DTE shall maintain a binary 1 condition on circuit 103. When circuit 105 is turned OFF it shall not be turned ON again until circuit 106 is turned OFF by the DCE.

Note – These conditions also apply to the relationship between circuits 120, 121 and 118.

4.6 *Timing circuits*

It is desirable that the transfer of timing information across the interface shall not be restricted to periods when actual transmission of data is in progress; however, during intervals when timing information is not transferred across the interface, the circuit involved should be held in the OFF condition. The following conditions apply:

4.6.1 *Circuit 113 – Transmitter signal element timing* (DTE source)

Where circuit 113 is used, the DTE shall transfer timing information across the interface on this circuit at all times that the timing source in the DTE is capable of generating this information, e.g. when the DTE is in a power-on condition.

4.6.2 *Circuit 114 – Transmitter signal element timing* (DCE source)

Where circuit 114 is used, the DCE shall transfer timing information across the interface on this circuit at all times that the timing source in the DCE is capable of generating this information, e.g. when the DCE is in a power-on condition. It is recognized that a DCE which derives power from the central office battery over the local telephone loop is in a power-off condition when disconnected from the loop, i.e. on-hook.

4.6.3 *Circuit 115 – Receiver signal element timing* (DCE source)

Where circuit 115 is used, the DCE shall transfer timing information across the interface on this circuit at all times that the timing source is capable of generating this information.

It is recognized that a DCE which derives power from the serving central office via the local telephone loop, is in a power-off condition with timing sources stopped, when the DCE is disconnected from the line. It is also recognized that some timing sources will not continue to run indefinitely without a driving (external synchronization) signal.

Accuracy and stability of this signal as defined in the DCE Recommendations are required only when circuit 109 is ON. Drift during the OFF condition of circuit 109 is acceptable; however, resynchronization of the signal on circuit 115 must be accomplished as rapidly as possible following the turning ON of circuit 109 for the next transmission as indicated in the relevant DCE Recommendation.

4.7 *Circuit 125 – Calling indicator*

The operation of circuit 125 shall not be impaired or disabled by any condition on any other interchange circuit.

4.8 *Usage of circuits 126 and 127*

Originally, these circuits were defined for operational control of a 2-wire, frequency-divided duplex DCE, such as the Recommendation V.21-type modem. Transmitter and receiver control were separated, so that local testing of both data channels might be performed as national Administrations required.

The modem according to Recommendation V.21 does not require separate operational control by the DTE of circuits 126 and 127 since it selects the transmit and receive frequencies according to the condition of circuit 125 in switched network operation.

However, the use of circuits 126 and 127 may become necessary in certain types of non-centralized multipoint operation.

4.9 *Circuit 140 – Loopback/Maintenance Test*

4.9.1 *Usage of circuit 140*

Circuit 140 can be used in conjunction with coded commands on circuit 103 in accordance with the provisions of Recommendation V.54.

In systems not including the use of circuit 103, i.e., no coded commands, circuit 140 controls only the remote loopback (loop 2).

In systems that involve the use of circuit 103, additional maintenance applications of circuit 140 are possible. These additional applications remain for further study.

4.9.2 *Interrelationship of circuits 105, 106 and 140*

For automatic control of loop 2 test, circuit 106 is under the control of circuit 140 and circuit 105 is disregarded by the DCE.

4.10 *Interrelationship of circuits 202 to 211*

Circuit 202

Circuit 202 must be turned OFF between calls or call attempts and shall not be turned ON before circuit 203 is turned OFF.

Circuit 204

The ON condition of this circuit must be maintained until the DTE has released the automatic calling equipment, i.e. until circuit 202 is turned OFF.

Circuit 205

The OFF condition shall be maintained on this circuit after circuit 204 comes ON.

The initial time interval starts when circuit 202 comes ON. Subsequent time intervals start each time circuit 210 is turned OFF.

Circuits 206, 207, 208 and 209

The conditions on these four circuits shall not change whilst circuit 211 is ON.

Circuit 210

When circuit 210 is turned OFF, it shall not be turned ON again before circuit 211 is turned OFF.

Circuit 211

Circuit 211 shall neither be turned ON when circuit 210 is in the OFF condition, nor until after the DTE has presented the required code combination on the digit signal circuits.

Circuit 211 shall not be turned OFF before circuit 210 is turned OFF.

Reference

[1] CCITT Recommendation *Connection to the telex network of an automatic terminal using a V.24 DCE/DTE interface*, Vol. VII, Rec. S.16.

Recommendation V.25

AUTOMATIC ANSWERING EQUIPMENT AND/OR PARALLEL AUTOMATIC CALLING EQUIPMENT ON THE GENERAL SWITCHED TELEPHONE NETWORK INCLUDING PROCEDURES FOR DISABLING OF ECHO CONTROL DEVICES FOR BOTH MANUALLY AND AUTOMATICALLY ESTABLISHED CALLS

(Mar del Plata, 1968; amended at Geneva, 1972 and 1976, Malaga-Torremolinos, 1984)

1 Scope

1.1 This Recommendation is concerned with the setting-up of a data connection when automatic answering equipment and/or parallel automatic calling equipment is used over international circuits. The automatic calling procedures defined in this Recommendation make use of the 200-series interchange circuits and are known as "parallel" automatic calling. Automatic calling procedures, which make use of only the 100-series interchange circuits, are known as "serial" automatic calling and are defined in Recommendation V.25 *bis*.

Automatic calling and answering equipment used within any single Administration's area or between two Administrations by bilateral agreement is not necessarily constrained by these proposals. In particular, the use of 2100 Hz answering tone, as described in this Recommendation, could be substituted by another tone when the equipment is used over circuits not equipped with echo control devices. Similarly, the calling tone could be omitted by bilateral agreements but attention is drawn to §§ 7 and 8 below.

In addition, the provisions for echo canceller disabling and for a "calling station response" prior to the termination of answer tone are optional and only applicable to data circuit-terminating equipment (DCE) for which the series V Recommendation specifically calls for such provision(s).

1.2 This Recommendation describes the sequence of events involved in establishing a connection between a parallel automatic calling data station [1] and an automatic answering data station for Series V Recommendations modems specified for general switched network operations. The system configuration proposed is shown in Figure 1/V.25.

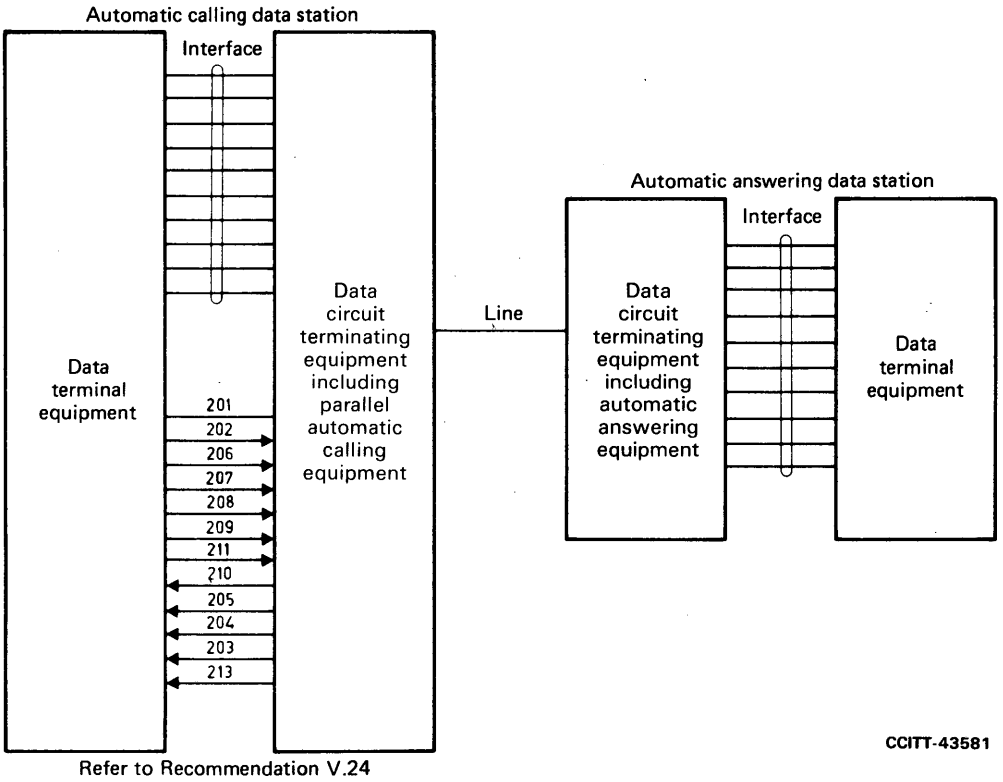


FIGURE 1/V.25

System configuration

Consideration is given only to:

a) the events which affect the interfaces between the data terminal equipment and the data circuit-terminating equipment, and

b) the events on the line during establishment of a data call.

Interactions within the data circuit-terminating equipment are not considered, since such consideration is unnecessary for purposes of international standardization.

[1] In this Recommendation, the term "data station" is synonymous with the term "terminal installation for data transmission" [1].

1.3 The proposed procedures are intended to be suitable for the four types of calls, namely:

a) parallel automatic calling data station to automatic answering data station;

b) manual data station to automatic answering data station;

c) parallel automatic calling data station to manual data station;

d) disabling of echo suppressors in the case of manual data stations.

1.4 The data terminal equipment is responsible for:

a) during call establishment:

i) ensuring that the data circuit-terminating equipment is available for operation,

ii) providing the telephone number,

iii) deciding to abandon the call if it is unsuccessfully completed;

b) after call is established:

i) establishing identities,

ii) exchanging such traffic as is appropriate,

iii) initiating disconnect at calling and answering data station.

2 Abbreviations and definitions

The following abbreviations are used in this Recommendation:

CT 104 = Circuit 104 – Received data
CT 105 = Circuit 105 – Request to send
CT 106 = Circuit 106 – Ready for sending
CT 107 = Circuit 107 – Data set ready
CT 108/1 = Circuit 108/1 – Connect data set to line
CT 108/2 = Circuit 108/2 – Data terminal ready
CT 109 = Circuit 109 – Data channel received line signal detector
CT 119 = Circuit 119 – Received backward channel data
CT 120 = Circuit 120 – Transmit backward channel line signal
CT 121 = Circuit 121 – Backward channel ready
CT 122 = Circuit 122 – Backward channel received line signal detector
CT 125 = Circuit 125 – Calling indicator
CT 201 = Circuit 201 – Signal ground or common return
CT 202 = Circuit 202 – Call request
CT 203 = Circuit 203 – Data line occupied
CT 204 = Circuit 204 – Distant station connected
CT 205 = Circuit 205 – Abandon call
CT 206 = Circuit 206 – Digit signal (2^0)
CT 207 = Circuit 207 – Digit signal (2^1)
CT 208 = Circuit 208 – Digit signal (2^2)
CT 209 = Circuit 209 – Digit signal (2^3)
CT 210 = Circuit 210 – Present next digit
CT 211 = Circuit 211 – Digit present
CT 213 = Circuit 213 – Power indication
DCE = Data circuit-terminating equipment
DTE = Data terminal equipment
EON = End-of-number control character
SEP = Separation control character

The following definitions apply to this Recommendation:

calling tone

The tone transmitted from the calling end. This may be 1300 Hz or any tone corresponding to binary 1 of the DCE in use.[2), 3)]

answering tone

The tone transmitted from the called end.[3)]

starting signal

Binary 1, synchronizing signal or equalizer training signal, as appropriate.[3)]

calling station response

A tone or signal transmitted from the calling DCE in response to its detection, as defined in this Recommendation, of answering tone.[2), 4), 3)]

parallel automatic calling

A procedure by which a DTE, by use of the 200-series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in parallel form on interchange circuits 206 through 209.

serial automatic calling

A procedure by which a DTE, by use of the 100-series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in serial form on interchange circuit 103 (see Recommendation V.25 *bis*).

3 Interface procedures at call-originating data station

Event

3.1 DTE checks if CT 213 ON, and the following circuits OFF: CT 202, CT 210, CT 205, CT 204, CT 203.

3.2 DTE puts CT 202 ON.

3.3 DTE puts CT 108/2 ON (CT 108/2 can be placed in the ON condition at any time up to and including event 3.16).

3.4 For half-duplex modems, DTE puts CT 105 ON if the calling end wishes to transmit first. CT 105 can be placed ON at any time up to and including event 3.20.

3.5 Line goes "off hook".

3.6 DCE puts CT 203 ON.

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2) The calling tone and calling station response should not contain power in the band 2100 ± 250 Hz.

3) The power levels of the signals specified in this Recommendation shall conform to the levels specified in Recommendation V.2.

4) The specification of the calling station response and the timing of its transmission are the subject of the individual Series V Recommendation for the DCE involved. The specifications in this Recommendation cover only limitations on its transmission during call establishment.

3.7 Telephone system puts dial tone on line[5].

3.8 DCE puts CT 210 ON.

3.9 DTE presents the first or appropriate digit on CT 206, CT 207, CT 208 and CT 209.

3.10 DTE puts CT 211 ON after digit signals have been presented.

3.11 DCE dials first digit; then takes CT 210 OFF.

3.12 DTE takes CT 211 OFF.

3.13 Events 3.8 to 3.12 are repeated (but this process may be interrupted by SEP) until the last digit signal is presented and transferred. Event 3.8 is then repeated but event 3.14 follows.

3.14 DTE presents EON on CT 206, CT 207, CT 208 and CT 209; it then puts CT 211 ON.

3.15 DCE takes CT 210 OFF.

3.16 DTE takes CT 211 OFF and puts CT 108/2 ON, if not previously ON.

3.17 The interrupted calling tone, as shown in Figures 2/V.25, 3/V.25 and 4/V.25 is transmitted to line from the calling DCE.

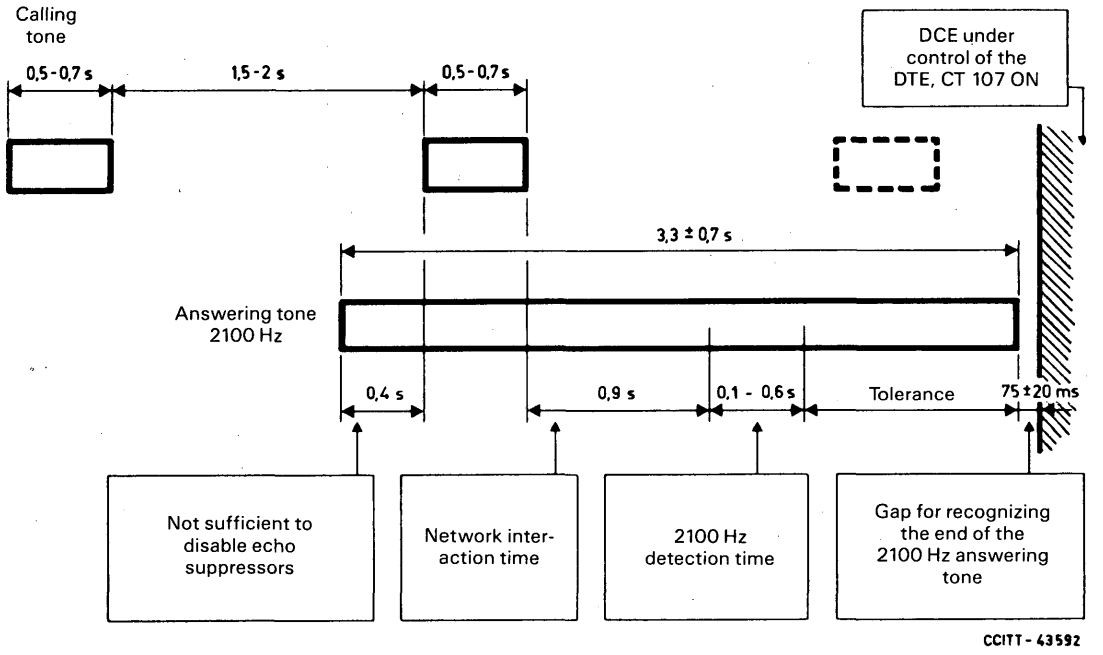
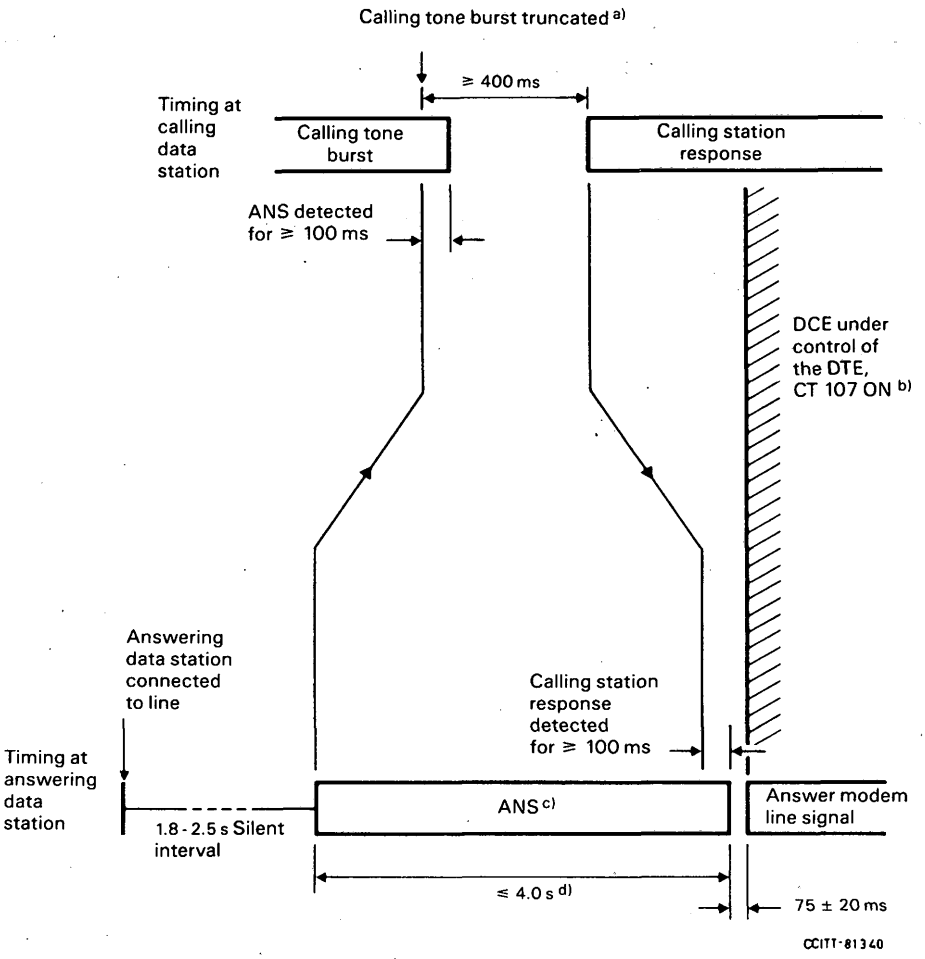


FIGURE 2/V. 25

Timing of line signals

[5] Some countries apply the second dial tone to the line after the initial digit is transferred.



a) If ANS is detected during a calling tone burst, the burst may be truncated. If it is not truncated, the calling station response must be delayed until at least 400 ms after the end of the burst.

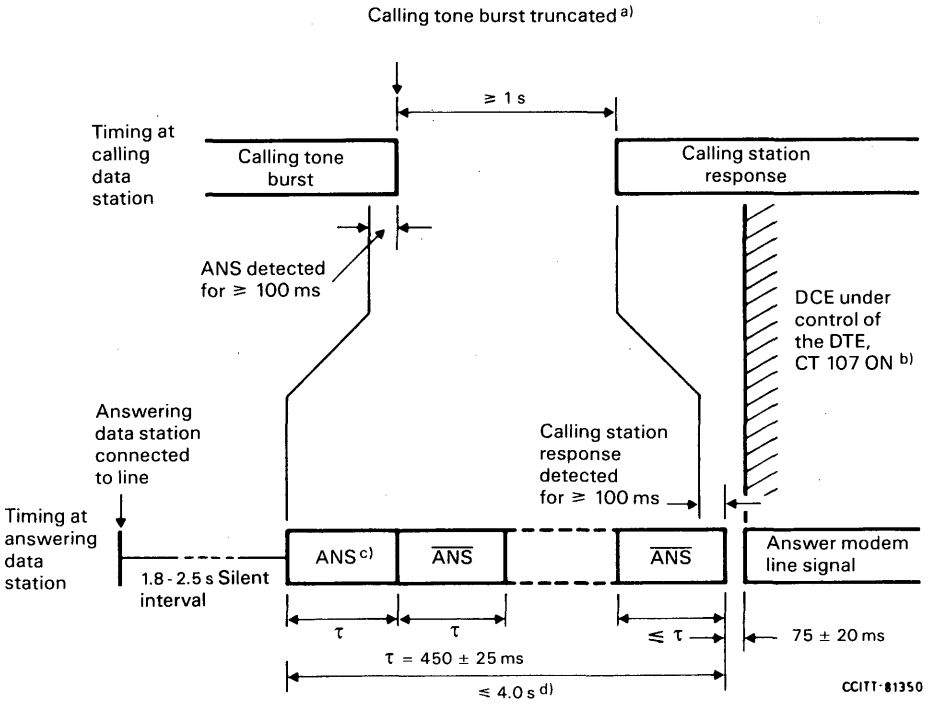
b) See § 3.20 for exception.

c) ANS denotes the answer tone.

d) If a calling station response is not received, the answer tone shall continue for 3.3 ± 0.7 seconds.

FIGURE 3/V.25

Timing of line signals – Optional calling station response



a) If ANS is detected during a calling tone burst, the burst may be truncated. If it is not truncated, the calling station response must be delayed until at least 1 second after the end of the burst.

b) See § 3.20 for exception.

c) ANS denotes the answer tone. $\overline{\text{ANS}}$ denotes the answer tone with its phase reversed.

d) The answer tone duration must be at least 2.6 seconds if a calling station response is not received.

FIGURE 4/V.25

Timing of line signals, optional provision for echo canceller disabling and for calling station response

3.18 a) If the call is answered by a data station, then 2100-Hz tone is received by the calling DCE. Echo suppressors are disabled during coincidence of a silent period in the interrupted calling tone (event 3.17) with 2100 Hz answering tone. The 2100-Hz answering tone must not activate CT 104 and CT 109.

b) If the call is not answered, or is answered by a non-data station, then no 2100 Hz is received at the calling data station. If no answering tone is received after an elapsed time, CT 205 comes ON. This time is measured from event 3.15 and selectable in the range of 10-40 seconds. The DTE must respond by turning CT 202 OFF.

3.19 When a 2100-Hz answer tone has been recognized by the DCE for a period of 100 to 600 ms, the interrupted calling tone is discontinued by the DCE as shown in Figures 2/V.25, 3/V.25 and 4/V.25. The DCE transfers control of the connection to the telephone line from CT 202 to CT 108/2.

The DCE may, as shown in Figures 3/V.25 and 4/V.25, transmit the calling station response following the detection of a continuation of the 2100-Hz answer tone for a period of at least 400 ms after the transmission of the calling tone is terminated. As indicated in Figure 4/V.25, the required duration (≥ 1 s) of the continuous 2100-Hz period, which must follow the termination of the calling tone, is longer if the answer tone includes phase reversals to disable echo cancellers.

3.20 The DCE examines the line to determine the end of the 2100-Hz answering tone. The DCE detects an absence of the 2100-Hz tone for 75 ± 20 ms, and then puts CT 107 ON:[6]

i) If CT 105 is ON, the starting signal is put on the line. After its delay as specified in the appropriate Series V Recommendation, CT 106 comes ON and the DTE can then transmit data.

ii) If CT 105 is OFF, the incoming starting signal is recognized and after its delay as specified in the appropriate Series V Recommendation, the DCE puts CT 109 ON to allow the examination of CT 104 by the DTE.

iii) For the duplex modem case, where CT 105 is not used, the starting signal is put on the line after CT 107 is put ON. The DCE then puts ON CT 109 and CT 106 after a delay as specified in the appropriate Series V Recommendation.

Note – There may be an interim period during which certain existing V.21 modems may not be able to provide the silent period between the end of the answering tone and the application of the starting signal. In this case, the use of a selective answering tone detector (see § 11 below) will be essential.

3.21 The DCE turns ON CT 204. The DTE then may turn OFF CT 202 without disconnecting the call.

Note 1 – After event 3.19, both CT 202 and CT 108/2 must be turned OFF to disconnect. The ON of CT 205 is an indication to DTE disconnect.

Note 2 – Where CT 105 or CT 120 is not implemented, the timing of CT 106 or CT 121 shall be related to CT 107 and CT 109 respectively.

4 Interface procedure at answering data station

Event

4.1 Ringing received on line. DCE puts CT 125 ON.

4.2 a) If CT 108/2 is ON, DCE goes "off hook".

b) If CT 108/1 or CT 108/2 is OFF, the DCE waits for CT 108/1 or CT 108/2 to come ON, and then goes "off hook". If CT 108/1 or CT 108/2 does not turn ON, then the call is not answered.

4.3 The DCE goes "off hook", maintains silence on the line for a period between 1.8 and 2.5 s, then transmits 2100-Hz[7] answer tone for a period, as shown in Figures 2/V.25 and 3/V.25. Where it is intended to disable network echo cancellers [3] as well as echo suppressors [2], reversals (180°)[8] in the phase of the 2100-Hz tone shall be introduced, as indicated in Figure 4/V.25, at intervals of 425 to 475 ms. The 2100-Hz answer tone, with continued reversals in its phase, shall continue for 3.3 ± 0.7 s unless a calling station response is received, in which case the 2100-Hz tone may be discontinued after detection of the response for 100 ms.

For the very special application in which an automatically answering modem is permanently dedicated to receive calls only from acoustically coupled originating stations, the modem may, optionally, extend the duration of the answer tone to ten seconds to compensate for operator reaction time in placing the telephone handset on the acoustic coupler. All other timeouts remain the same and the protocol is as defined in § 6. Use of the extended answer tone is restricted expressly to this unique application.

4.4 At the end of the 2100-Hz transmission, the DCE shall not transmit (i.e. provide a silent period) for 75 ± 20 ms. The DCE puts CT 107 ON after this silent period.[6]

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[6] For some DCEs requiring extended training sequences, the associated Series V Recommendation may specify that CT 107 be put ON at some later time, during the handshake sequence, which is more consistent with the specification in Recommendation V.24 of CT 107.

[7] The 2100-Hz tolerance will be ± 15 Hz in accordance with Recommendation G.164 [2].

[8] The reversal in phase shall be accomplished such that the phase is within 180 ± 10 degrees in 1 ms and that the amplitude of the 2100-Hz tone is not more than 3 dB below its steady state value for more than 400 μs.

5 Proposed line procedures

The line procedures outlined consider the half-duplex case of the Series V Recommendations modems. For reasons of simplicity, the same timing of line signals will be used for duplex modems (including modems with backward channel).

Systems which operate in the half-duplex mode and which employ automatic calling equipment shall determine by prearrangement which of the two data stations – calling or answering – shall first transmit to the other upon the establishment of the data connection. As indicated in § 3 above, the DTE at the data station which is to transmit first must put CT 105 ON, at the appropriate point in the call establishment sequence. For correct operation, it is necessary that the longer response times of CT 106 and CT 109 as specified in the appropriate Series V Recommendation are used during call establishment.

Figures 2/V.25, 3/V.25 and 4/V.25 show the timing of line signals when automatic calling and automatic answering are employed. The sequence of operation is as follows:

After the DCE has dialled the digits of the directory number for the automatic answering data station, followed by the EON character, the DCE sends the calling tone to the answering data station. The calling tone consists of a series of interrupted bursts of binary 1 signal or 1300 Hz, ON for a duration of not less than 0.5 s and not more than 0.7 s and OFF for a duration of not less than 1.5 s and not more than 2.0 s.

1.8 to 2.5 s after the answering data station is connected to the line (i.e., CT 125 and CT 108 are ON), it sends a continuous 2100-Hz answering tone for a duration of not more than 4.0 s. If it is intended to disable network echo cancellers as well as echo suppressors, the answering station reverses the phase of the tone at intervals of 425 to 475 ms (see Figure 4/V.25).

The answering tone propagates towards the calling data station and, during the course of one or two interruptions between bursts of calling tone, causes any echo suppressors on the circuit to disable. If the phase reversals are included in the signal, any echo cancellers in the circuit would also be disabled. The answering tone is recognized by the calling data station for a period of between 100 ms and 600 ms after its arrival. The calling station discontinues the calling tone and may transmit a calling station response. The answering station, after detecting the calling station response, may discontinue transmission of the tone. The answering station shall provide a silent interval of 75 + 20 ms in its transmitted output following the discontinuance of the 2100-Hz tone.

The calling data station recognizes the end of the answering 2100-Hz tone for a period of 75 ± 20 ms. At the end of this interval, the DCE may put CT 107 ON. Similarly, the answering data station delays for a period of 75 ± 20 ms after discontinuing the answer tone before it may put CT 107 ON.[9)]

To keep the echo suppressor disabled, it is necessary to ensure that following the 75 ± 20 ms silent period after the transmission of the 2100-Hz answering tone from the answering data station, which serves to disable the echo suppressor or echo canceller during the silent period in the calling tone, energy is maintained as specified in Recommendation G.164 [2].

During the automatic calling and answering procedures, the echo suppressors will be disabled and the echo cancellers will be disabled if the required sequence is transmitted. If signal gaps, at the echo suppressor or canceller, exceed 100 ms at any time, e.g. during modem turn-around, they may become re-enabled. This requires that, to maintain the disabled state of echo control devices on circuits with satellite links, the answering data station resume transmission after the 75 ± 20 ms silent period unless a calling station response is received prior to the silent interval and appropriately continued.

6 Manual data station calling automatic answering data station

The procedure for establishment of a call from a manual data station to an automatic answering data station is similar to that from an automatic calling data station, except that no tone is transmitted from the calling data station until the answering data station has answered. The manual operator dials the required number, hears 2100 Hz returned from the automatic answering data station and then presses his data button to connect the data circuit-terminating equipment to the line during the period that 2100 Hz is being received. CT 107 comes ON at the time specified in event 3.20. Where the calling station is acoustically coupled to the line, placement of the telephone handset on the acoustic coupler is logically equivalent to pressing a "data" button on a permanently installed DCE.

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9) For some DCEs requiring extended training sequences, the associated Series V Recommendation may specify that CT 107 be put ON at some later time, during the handshake sequence, which is more consistent with the specification in Recommendation V.24 of CT 107.

Satisfactory disabling of echo suppressors by the answering tone, however, will require that no speech signals from the microphone at the calling data station enter the telecommunications circuit for a period of at least 1 s during the receipt of answering tone. This may be accomplished by a handset switch or other appropriate means.

7 Automatic calling data station calling manual data station

An operator answering a call from an automatic calling equipment hears an interrupted calling tone of 0.5 to 0.7 s ON and 1.5 to 2.0 s OFF. The data button must be depressed to connect the DCE to line. A period of up to 4.0 s of 2100-Hz tone is transmitted to the calling data station to disable echo suppressors and/or echo cancellers and to notify the calling data station that the connection is being established. This sequence is followed by data transmission, as required.

8 Disabling of echo suppressors in the case of manual data stations

The procedures as described in §§ 6 and 7 above with regard to the manually operated data stations, can obviously be used for disabling echo suppressors when manual switching from voice conversation to data is required, which is the preferred principle of operation. Considering the type of DCE designed to be used in conjunction with manual connection set-up, it will be necessary to equip the DCE with a 2100-Hz answering tone generator. To avoid modifying existing equipment at the data station which receives the answering tone, the following procedure may replace the operation principle of § 6 above. The manual operator operates his data key after the end of the 2100-Hz answering tone. The data station which is to transmit the answering tone is to be agreed between the operators while still in the voice mode.

Care must be exercised in cases of half-duplex modems where transmission of data is started from the data station which transmits the answering tone, to avoid mutilation of the initial data.

Note – Where disabling of echo suppressors is not required in the half-duplex modem case, the 2100-Hz answering tone need not be transmitted. However, the delay between CT 105 to CT 106 ON conditions should be longer than 100 ms in consideration of the echo suppressor suppression hangover time.

9 Protection of ordinary telephone users

As both automatic calling and automatic answering data stations transmit tones to line during call establishment, a normal telephone user who becomes inadvertently connected to one will receive tone signals for a period of sufficient duration to indicate clearly to him that he is incorrectly connected.

10 Manual selection of automatic answering, data mode and voice mode

It is recognized that, at the data station, means should be provided to allow the operator to select between automatic and manual answering of calls. If a call is manually answered, voice mode shall be established. Subsequent switching to the data mode shall be performed by the procedure as specified in § 7 above.

Selection of manual or automatic answering of subsequent calls shall be possible after entering the data mode. As an option, automatic answering may be arranged for all subsequent incoming calls. In this case, manual answering may still be achieved by keeping CT 108/2 OFF to cause an audible signal to occur at the telephone instrument.

The DCE shall be disconnected from the line whenever CT 108/1 or CT 108/2 is turned OFF, irrespective of the means employed in establishing the connection.

Procedures for switching to the voice mode between data transmission within the same call shall ensure that CT 107 is turned OFF while in the voice mode.

11 2100-Hz tone recognition

To protect the 2100-Hz tone detector against faulty operation resulting from interference generated by the interrupted calling tone, the detector may be inhibited during the ON periods of the calling tone.

Additionally, in cases where automatic calling equipment is used to set up the call, the 2100-Hz detector must not respond to spurious tones which may arise from speech or service signals during call establishment. It is suggested that the answering tone detection be prevented when the 2100-Hz signal is accompanied by any other signal of comparable level within the ranges 350 Hz to 1800 Hz and 2500 Hz to 3400 Hz.

Note – The relative inhibiting signal levels recommended for the echo suppressor disabling tone detector of Recommendation G.164 [2] are a useful guide for 2100-Hz tone detector inhibiting levels.

References

[1] CCITT Definition: *Terminal installation for data transmission*, Vol. X (Terms and Definitions).

[2] CCITT Recommendation *Echo suppressors*, Vol. III, Rec. G.164.

[3] CCITT Recommendation *Echo cancellers*, Vol. III, Rec. G.165.

Recommendation V.25 bis

AUTOMATIC CALLING AND/OR ANSWERING EQUIPMENT ON THE GENERAL SWITCHED TELEPHONE NETWORK (GSTN) USING THE 100-SERIES INTERCHANGE CIRCUITS

(Malaga-Torremolinos, 1984; modified at Melbourne, 1988)

1 Scope

1.1 This Recommendation is concerned with the setting up of a data connection on the general switched telephone network where the automatic calling equipment used interfaces to the data terminal equipment via the 100-series interchange circuits.

This procedure is known as serial automatic calling. Procedures for parallel automatic calling are defined in Recommendation V.25.

1.2 The Recommendation describes the sequence of events involved in establishing a connection between a serial automatic calling data station [1] and an automatic answering data station for Series V Recommendation modems specified for general switched telephone operation. The system configuration is shown in Figure 1/V.25 *bis*.

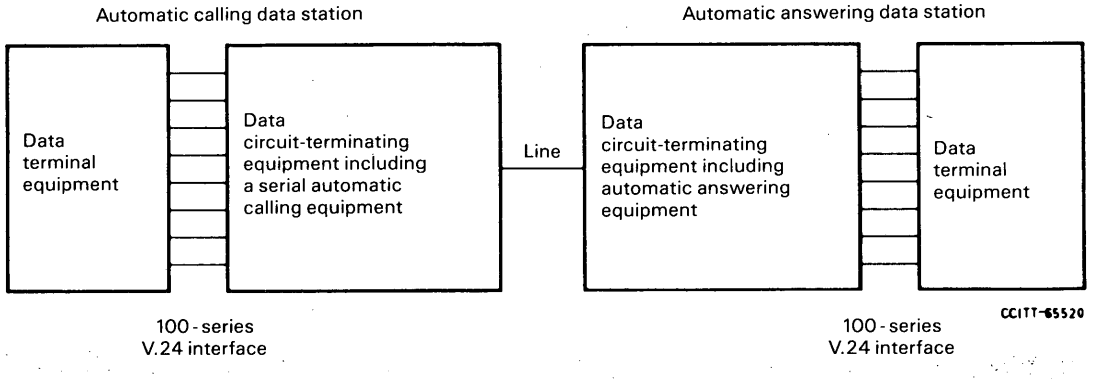


FIGURE 1/V.25 *bis*

[1] In this Recommendation, the term "data station" is synonymous with the term "terminal installation for data transmission".

1.3 The procedures are intended to be suitable for the following three types of call:

a) serial automatic calling data station to automatic answering data station;

b) manual calling data station to automatic answering data station;

c) serial automatic calling data station to manual answering data station.

It is intended that data terminal equipment designed to control automatic calling equipment in accordance with this Recommendation will also be suitable for use with manually controlled data circuit-terminating equipment, and also that data circuit-terminating equipment incorporating serial automatic calling equipment may be manually controlled where necessary.

1.4 The procedures described should allow automatic calling equipment conforming to this Recommendation to interwork with automatic answering equipment conforming to Recommendation V.25. Similarly, the procedures herein described for automatic answering allow interworking with automatic calling equipment conforming to Recommendation V.25.

1.5 The data terminal equipment is responsible:

a) during call establishment:

i) for ensuring that the data circuit-terminating equipment is available for operation,

ii) for providing the telephone number or selecting a telephone number pre-programmed into the data circuit-terminating equipment,

iii) for deciding to abandon the call if it is unsuccessfully completed;

b) after call establishment:

i) for controlling data transfer,

ii) for initiating disconnect at calling or answering data stations.

1.6 This Recommendation deals with call establishment and clearing. Any specific use of Recommendation V.24 interchange circuits herein described only applies during these phases. The management of interchange circuits and the line during the data transmission phase is not part of this Recommendation.

Details of interface procedures following the OFF to ON transition of circuit 107 on entry of the data transmission phase can be found in the relevant modem Recommendations.

1.7 Annex A gives guidance on the maintenance facilities which may be associated with an automatic calling data circuit-terminating equipment. Methods for testing the automatic calling functions of the data circuit-terminating equipment are included.

1.8 References to automatic calling in the remainder of this Recommendation may be taken as serial automatic calling unless otherwise stated.

2 Abbreviations and definitions

The following abbreviations are used in this Recommendation:

DCE = Data circuit-terminating equipment

DTE = Data terminal equipment.

The following definitions apply to this Recommendation:

command

An instruction issued by the DTE to the DCE as part of the automatic calling procedure.

indication

An instruction or response issued by the DCE to the DTE as part of the automatic calling procedure.

Note – In this Recommendation the terms "indication" and "response" are not to be taken in the sense defined in Recommendation X.210.

parameter

A variable which may accompany Commands or Indications.

parallel automatic calling

A procedure by which a DTE, by use of the 200-series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in parallel form on interchange circuits 206 to 209.

serial automatic calling

A procedure by which a DTE, by use of the 100-series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in serial form on circuit 103.

3 General

3.1 The automatic calling and/or answering data stations can be operated, according to this Recommendation, in two modes:

- The "addressed call and/or answer authorized by the DTE (circuit 108/2)" mode gives at a calling data station extensive facilities by means of instructions exchanged between the DTE and the DCE on circuits 103 and 104. It gives an answering data station the capacity to accept "a priori" an incoming call.
- The "direct call and/or answer controlled by the DTE (circuit 108/1)" mode gives at a calling data station the capacity of calling a number (or a sequence of numbers) pre-recorded in the DCE, by means of the 108/1 control circuit. It gives to an answering data station the capacity of accepting incoming calls on a "per call" basis.

3.2 Though automatic answering data stations as well as automatic calling and answering data stations may implement both modes of operation, they are configured at installation to operate in either one or the other of the two modes.

4 Addressed call and/or answer authorized by the DTE (circuit 108/2)

4.1 *Interface procedure*

4.1.1 *Interchange circuits involved*

The interchange circuits used in this automatic calling/answering procedure are listed in Table 1/V.25 *bis*. Their use during the automatic calling/answering procedures is described below.

TABLE 1/V.25 *bis*

Interchange circuit		Direction	
Number	Name	from DCE	to DCE
103	Transmitted data		X
104	Received data	X	
106	Ready for sending	X	
107	Data set ready	X	
108/2	Data terminal ready		X
125	Calling indicator	X	

4.1.1.1 *Circuit 103 – Transmitted data*

The instructions issued by the DTE during the automatic calling procedure, known as *commands*, are transmitted to the DCE on this circuit.

4.1.1.2 *Circuit 104 – Received data*

Responses from the DCE to DTE Commands, known as *indications*, are transmitted to the DTE on this circuit. Optionally, circuit 104 may convey the echo of the commands transmitted on circuit 103 (for further study).

4.1.1.3 *Circuit 106 – Ready for sending*

The DCE shall turn circuit 106 ON in response to the DTEs circuit 108/2 being ON.

The DCE shall turn circuit 106 OFF:

i) on connection to line when answering tone is detected;

ii) when the DCE aborts the call set-up under the control of DTE by turning 108/2 in the OFF condition.

4.1.1.4 *Circuit 107 – Data set ready*

The DCE shall turn circuit 107 ON:

i) at the end of the automatic call set-up procedure, to indicate to the DTE that the connection is established and the DCE connected to line;

ii) on completion of manual call set-up procedure.

The DCE shall turn circuit 107 OFF:

i) to indicate to the DTE that the connection has been cleared down during the data transfer phase (to be permitted where national regulations require it);

ii) in response to a clear request by the DTE turning OFF circuit 108/2.

4.1.1.5 *Circuit 108/2 – Data terminal ready*

The DTE turns circuit 108/2 ON:

i) to enable the DCE to set up a connection either manually or automatically;

ii) to indicate to the DCE that it is ready to accept an incoming call.

The DTE shall turn circuit 108/2 OFF:

i) to instruct the DCE to clear down the connection during data transfer;

ii) to instruct the DCE to abort the call set-up procedure;

iii) to indicate to the DCE that it is not ready to accept an incoming call.

4.1.1.6 *Circuit 125 – Calling indicator*

The DCE should provide circuit 125 to indicate to the DTE an incoming call. This incoming call will override a call request prior to seizure of the line. The usage of circuit 125 in the DTE is optional.

4.1.1.7 *Other interchange circuits*

The state of other interchange circuits is not part of the procedure. However, to ensure maximum compatibility with existing equipment, the other interchange circuits provided should retain their normal function during the automatic calling procedure.

Particularly to ensure correct operation of the DTE, the condition of circuit 109 should follow the condition of circuit 106.

The DTE may choose to hold circuit 105 ON during the automatic calling procedure, but the DCE is not required to recognize this condition.

4.1.2 *Control information format*

Call set-up is achieved by the use of interchange circuits 106, 107 and 108 together with messages exchanged between the DTE and the DCE on circuits 103 and 104. These messages consist of commands or indications from the DTE or DCE respectively, and may be accompanied by *parameters* where necessary. The commands/indications required for the automatic calling procedure are outlined in Table 2/V.25 *bis* and Table 3/V.25 *bis* together with their parameters.

The use of commands/indications other than one of the call request commands (CR–) and the invalid indication (INV) is optional in the DTE and DCE respectively.

The commands/indications and their parameters are described below.

4.1.2.1 *Call request commands*

These commands from the DTE instruct the DCE to initiate a call set-up procedure. The commands shall include a suffix to indicate the type of call request concerned (see Table 3/V.25 *bis*) and shall be accompanied by one or more of the following parameters:

i) the number to be dialled. (In applications where additional dial tones are required, separators, "wait tone", etc., may be included in this number);

ii) the identification number of the data station;

iii) the DCE memory address which contains the number to be dialled, this having been previously programmed;

Note – Manufacturers should note that the response time to a Call Request Command is determined by the time required to execute line procedures (see § 6.1).

4.1.2.2 *Program commands*

These commands from the DTE instruct the DCE to enter a programming state. The commands shall be accompanied by one or more of the following parameters:

i) the DCE memory address into which the number to be dialled is to be stored;

ii) the number which is to be stored;

iii) the identification number of the data station.

Where a DCE does not contain the programming capability, this DCE shall reply to a program command by an *invalid* indication.

Where a DTE is not capable of programming the DCE, it may still initiate call attempts using the *call request* command in the normal way.

4.1.2.3 *List request commands*

These commands from the DTE instruct the DCE to list the numbers that have been programmed in its memory with or without their status. The commands shall include a suffix to indicate the type of list concerned. The command may be accompanied by parameters to select items to be listed. These parameters are for further study.

4.1.2.4 *Disregard incoming call command*

This command from the DTE instructs the DCE not to answer the current incoming call which is, or has been, signalled from the DCE to the DTE.

4.1.2.5 *Connect incoming call command*

This command from the DTE instructs the DCE to connect an incoming call that has been disregarded due to a previous disregard incoming call command.

4.1.2.6 *Call failure indication*

This indication may be issued by the DCE in response to a *call request* command from the DTE and may be accompanied by a parameter stating the reason for the failure of the call.

The following parameters indicate the possible conditions that may result in a call failure on the GSTN:

i) engaged tone;

ii) number not stored;

iii) local DCE busy, (e.g. DCE involved in an operation invoked from the front panel);

iv) ring tone, (the remote end was ringing but the call is aborted on time-out)

v) abort call, (the call is aborted on time-out)

vi) answer tone not detected, (the other end was recognized as going off hook but the V.25 answer tone was not detected);

vii) forbidden call, (call attempts to this number are blocked by the DCE due to national regulations) (Note);

viii) other parameters dependent on national network variations.

Note – Procedure for clearance of forbidden call numbers is not covered in this Recommendation.

The provision of the *call failure* indication is optional in the DCE. For this reason, the DTE should also be capable of recognizing call failure by means of a time out.

4.1.2.7 *Delayed call indication*

This indication from the DCE may be implemented depending on national regulations, and informs the DTE that, for example, owing to repeated unsuccessful call attempts, call attempts to this number are blocked by the DCE for a time given by the accompanying parameter.

4.1.2.8 *Incoming call indication*

This indication may be provided by the DCE to inform the DTE that a ring tone has been detected on the telephone line.

Note – In the event of collision between an incoming call and a call request, the incoming call will have priority.

4.1.2.9 *Valid indication*

This indication may be provided by the DCE to acknowledge call request, program, disregard incoming call and correct incoming call commands, and to inform the DTE that the command has been accepted.

4.1.2.10 *Invalid indication*

This indication shall be provided by the DCE when it receives an invalid command, or receives a command which it is incapable of executing either because it does not implement the function or because the function is invoked at a wrong time in the V.25 *bis* process. This indication may be accompanied by a parameter stating the reason for the invalid situation.

The following parameters indicate the possible conditions that may result in an invalid situation:

i) command unknown error,

ii) message syntax error,

iii) parameter syntax error,

iv) parameter value error.

4.1.2.11 *List indications*

A series of such indications may be provided by the DCE to list specific items stored in its memory according to the *list request* command previously made by the DTE. These indications will be accompanied by one or more of the following parameters:

i) the DCE memory address into which the number is stored;

ii) the number stored;

iii) the status of this number (for further study);

iv) the identification number of the data station.

Note – When the list request command invokes edition of an empty list, a list indication with no parameter may be issued.

4.1.2.12 *Call connecting indication*

This indication may be provided by the DCE to inform the DTE that the connection procedures are about to be completed.

TABLE 2/V.25 *bis*

Set of commands and indications (Note 1)

Command/indication	DTE to DCE (command)	DCE to DTE (indication)	Parameters
Call request	X		– Number to be dialled
			– Memory address of the number to be dialled
			– Identification number
Program	X		– Number to be dialled
			– Memory address for the number to be dialled
			– Identification number
List request	X		– (Note 2)
Disregard incoming call	X		– None
Connect incoming call	X		– None
Call failure		X	– Engaged tone
			– Number not stored
			– Local DCE busy
			– Ring tone (time out)
			– Abort call (time out)
			– V.25 answer tone not detected
			– Forbidden call (nationally dependent parameters)
Delayed call		X	– Time to permissible call request (minutes)
Incoming call		X	– None
Valid		X	– None
Invalid		X	– Optionally, error code
List		X	– Memory address
			– Number to be dialled
			– Status (Note 2)
			– Identification number
Call connecting		X	– (Note 2)

Note 1 – DTE manufacturers should note that a set of indications may not be implemented in a DCE, and allowance for this, by use of suitable time-outs, should be made.

Note 2 – This item is for further study.

TABLE 3/V.25 *bis*

Encoding of commands and indications

Command/indication	IA5 characters	Parameter format				
Call request with:						
number provided:	CRN	CRN	Number to be dialled XXXXX..... XXXX			
number provided with the identification number:	CRI	CRI	Number to be dialled XXXXX..XXXX	;	Identification number YY....YY	
memory address provided:	CRS	CRS	Memory address XXXXX...XX			
Program:						
normal:	PRN	PRN	Memory address XXXXX..XX	;	Number to be dialled XXXXX...XXXX	
identification:	PRI	PRI	identification number XXXXX..... XX			
List request of:						
stored number:	RLN	RLN	For further study ZZZ..... Z			
forbidden numbers:	RLF	RLF	For further study ZZZ..... Z			
delayed call numbers:	RLD	RLD	For further study ZZZ..... Z			
identification number:	RLI	RLI				
Disregard incoming call:	DIC	DIC				
Connect incoming call:	CIC	CIC				
Call failure indication:	CFI	CFI	Failure type XX			
Delayed call:	DLC	DLC	Time duration (in minutes) XXX...XX			
Incoming call:	INC	INC				
Valid:	VAL	VAL				
Invalid:	INV	INV	Optionally, error type XX			
List of:						
			Memory address		Number to be dialled	Status (for further study)
stored numbers:	LSN	LSN	XXXX..XX	;	YYYY..YYY	; ZZZZ (Note)
forbidden numbers:	LSF	LSF	XXXX..XX	;	YYYY..YYY	; ZZZZ (Note)
delayed call numbers:	LSD	LSD	XXXX..XX	;	YYYY..YYY	; ZZZZ (Note)
identification number:	LSI	LSI	Identification number XXXX.... XX (Note)			
Call connecting:	CNX	CNX	ZZZ.... Z (for further study)			

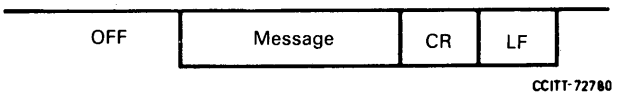
Note – When the list request command invokes edition of an empty list, a list indication with no parameter may be issued.

4.1.3 *Format for commands and indications*

Commands and indications may be encoded in the formats specified below, according to application.

4.1.3.1 *Asynchronous operation*

The format for asynchronous operation shall be as shown in Figure 2/V.25 *bis*.



Note - In commands from the DTE the *new line* function may sometimes be encoded in a way other than CR + LF (see Recommendation T.50, § 4.1.2.2) and allowance for this should be provided.

FIGURE 2/V.25 *bis*

In this mode of operation, the character format shall be one start element followed by 8-bit data units and one-unit stop element. The 8-bit data units are formed by a 7-bit IA5 character in accordance with Recommendation T.50 together with an even parity unit in accordance with Recommendation V.4.

Where the DCE operating rate is variable, the transmision rate for commands and parameters should be the maximum data rate permitted by the modem Recommendation, i.e.: 300, 600, 1200 and 2400 bit/s.

Note – These bit rates are the minimum which should be provided. The addition of other bit rates is for further study.

Depending on the application, characters may or may not be echoed by the DCE (for further study).

4.1.3.2 *Synchronous character oriented operation*

The format for synchronous character oriented operation shall be in accordance with ISO 1745, and shall be as shown in Figure 3/V.25 *bis*.

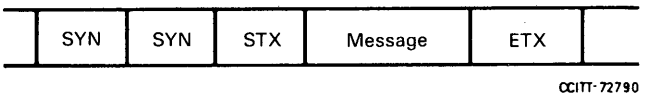


FIGURE 3/V.25 *bis*

Generally the command/indication is terminated by ETX. However, when a succession of indications is transmitted (e.g. succession of LSN indications), ETB should be used instead of ETX with all but the last indication of the succession, to indicate that other indications are coming.

In this mode of operation, consecutive 8-bit data units are used. The 8-bit data units are formed by a 7-bit IA5 character in accordance with Recommendation T.50 with an odd parity bit in accordance with Recommendation V.4.

The bit rate used for the data transfer shall apply.

4.1.3.3 *Synchronous bit oriented operation*

HDLC (High Level Data Link Control) format shall be used for synchronous bit oriented operation, and shall be as shown in Figure 4/V.25 *bis*.

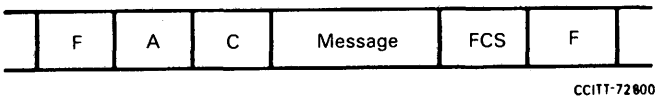


FIGURE 4/V.25 *bis*

The message is the information field of a UI frame transmitted with the global address. Generally the P/F bit is set to 1. Consequently, the A and C fields are generally as follows:

A = 11111111 C = 11001000
LSB MSB

However, when a succession of indications is transmitted (e.g. succession of LSN indications), the P/F bit should be set to 0, i.e. the control field is changed to:

C = 11000000
LSB MSB

with all but the last indication of the succession, to indicate that other indications are coming.

The introduction of other addresses is for further study.

Within the message, consecutive 8-bit data units are used and submitted to the HDLC framing (zero insertion). The 8-bit data units are formed by a 7-bit IA5 character in accordance with Recommendation T.50 together with an eighth bit set indifferently either to "one" or "zero", or the odd parity. No parity checking will be done on reception.

The transmission mode and the bit rate used for the data transfer shall apply.

4.1.4 *Message format and encoding*

The message format shall comprise:

i) a three-character command/indication (see Table 3/V.25 *bis*);

ii) one or more parameters separated by ";" characters (see Tables 4/V.25 *bis* and 5/V.25 *bis*); these parameters may include " " and "." as presentation characters (see Table 6/V.25 *bis*).

A detailed description of the command/indication syntax is contained in Table 6/V.25 *bis*. A general presentation of this syntax is offered in Appendix I.

4.1.5 *Command/indication exchange protocol*

The exchange of commands and indications between the DTE and the DCE can be regarded as asynchronous and balanced.

4.1.5.1 The following basic rules apply:

- Every command is to be followed by, at least, one indication or by circuit 107 going ON in the case of successful call.
- Several indications may be issued by the DCE one after the other, either of the same nature or of a different nature.
- The issue by the DTE of new commands other than DIC prior to the reception of the indication to the previous command may abort the execution of this previous command and should therefore be avoided.

TABLE 4/V.25 *bis*

Parameter enconding
(Number to be dialled)

Alphabet for number to be dialled	IA5 coding
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
Wait tone	:
Pause (Note 1)	<
Separator 3 (Note 2)	=
Separator 4 (Note 2)	>
Dialling to be continued in pulse mode (Note 4)	P
Dialling to be continued in DTMF mode (Note 4)	T
Flash (Notes 3 and 4)	&

Note 1 – Usage and duration of this parameter are a national matter.

Note 2 – For national use.

Note 3 – The flash duration is a national matter.

Note 4 – Optionally accepted parameter.

TABLE 5/V.25 *bis*

Parameter encoding
(Failure and error types)

Parameter	IA5 coding
Engaged tone	ET
Number not stored	NS
Local DCE busy	CB
Ring tone	RT
Abort call	AB
Answer tone not detected	NT
Forbidden call	FC
Command unknown/Unexpected error	CU
Message syntax error	MS
Parameter syntax error	PS
Parameter value error	PV

TABLE 6/V.25 *bis*

Detailed description of the V.25 bis command/indication syntax

description language:

a | b denotes the set (a, b)

a b denotes the set (ab)

a* denotes the set (e, a, aa, aaa, . . .)

(e = empty)

description:

```
message          = command | indication
command          = CR_command | PR_command | RL_command | DIC_command | CIC_command |
indication       = LS_indication | CFI_indication | DLC_indication | INC_indication | VAL_indication |
                   INV_indication | CNX_indication |
CR_command       = CRN_command | CRI_command | CRS_command
PR_command       = PRN_command | PRI_command
RL_command       = RLN_command | RLF_command | RLD_command | RLI_command
LS_indication    = LSN_indication | LSF_indication | LSD_indication | LSI_indication
CRN_command      = 'CRN' number
CRI_command      = 'CRI' number delimiter identification
CRS_command      = 'CRS' address
PRN_command      = 'PRN' address delimiter number
PRI_command      = 'PRI' identification
RLN_command      = 'RLN' | ('RLN' RL_parameter)
RLF_command      = 'RLF' | ('RLF' RL_parameter)
RLD_command      = 'RLD' | ('RLD' RL_parameter)
RLI_command      = 'RLI'
DIC_command      = 'DIC'
CIC_command      = 'CIC'
LSN_indication   = ('LSN' address delimiter number) | ('LSN' address delimiter number delimiter status) | 'LSN'
LSF_indication   = ('LSF' address delimiter number) | ('LSF' address delimiter number delimiter status) | 'LSF'
LSD_indication   = ('LSD' address delimiter number) | ('LSD' address delimiter number delimiter status) | 'LSD'
LSI_indication   = 'LSI' identification | 'LSI'
CFI_indication   = 'CFI' failure_type
DLC_indication   = 'DLC' time_duration
INC_indication   = 'INC'
VAL_indication   = 'VAL'
INV_indication   = 'INV' | ('INV' error_type)
CNX_indication   = 'CNX' | ('CNX' CNX_parameter)
number           = presentation* (digit | special) (digit | special | presentation)*
identification   = presentation* digit (digit | presentation)*
address          = presentation* digit (digit | presentation)*
failure_type     = presentation* ('ET' | 'NS' | 'CB' | 'RT' | 'AB' | 'NT' | 'FC')
RL_parameter     = to be defined *****
time_duration    = presentation* digit (digit | presentation)*
error_type       = presentation* ('MS' | 'CU' | 'PS' | 'PV')
status           = to be defined *****
CNX_parameter    = to be defined *****
digit            = '0' | '1' | '2' | '3' | '4' | '5' | '6' | '7' | '8' | '9'
special          = '&' | ':' | '>' | '<' | '=' | 'P' | 'T'
presentation     = ' ' | '.'
delimiter        = ';'
```

4.1.5.2 *Erroneous command/indication*

- Whenever a command/indication is detected with a level II framing error (incorrect framing, parity or FCS, see § 4.1.3), this command/indication is disregarded.
- Whenever a DCE detects an error in the message of a command or receive a command which cannot be executed, it acknowledges negatively this command by issuing an *invalid* indication (INV). The letters within opcodes for commands and indications shall be upper case letters. Optionally, DCEs are allowed to accept the presence of corresponding lower case letters in place of specified upper case letters within the three letter opcode of a command.

4.1.5.3 *Command/indication succession*

Table 7/V.25 *bis* lists for all the commands defined:

- the state of the interface in which the command may be issued,
- the state to which the interface moves after the issue of the command,
- the indications pertinent to that command,
- the state to which the interface moves after the issue of the indication,
- the consequence of this indication for the action initiated by the command.

Note – The state diagram of the interface is shown in Figure 5/V.25 *bis*. In addition an SDL description of the message exchange, as per the Z.100 serie Recommendations, is offered in Annex B.

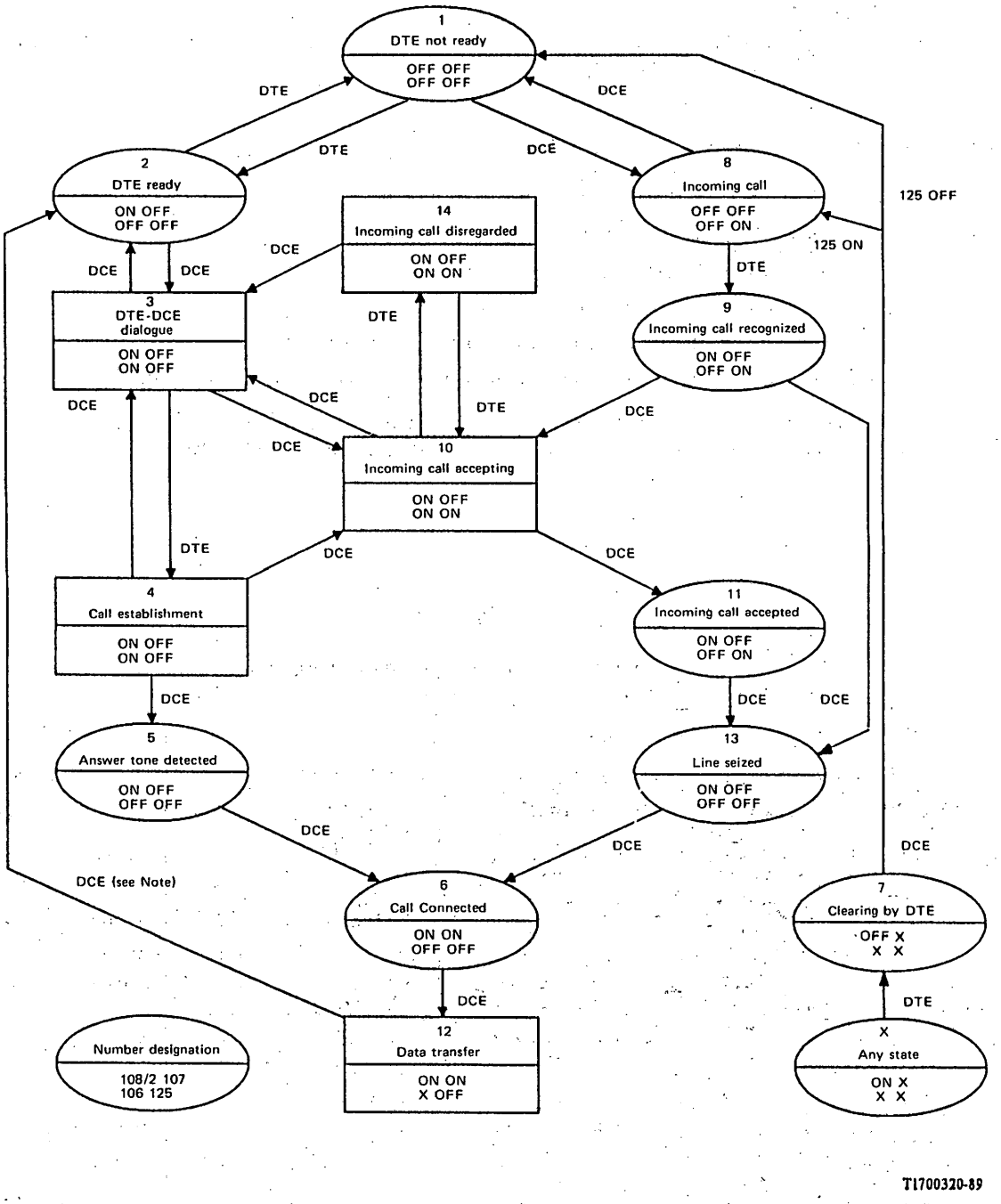
TABLE 7/V.25 *bis*

Commands, indications and their consequences

DTE command	From state	To state	DCE response	To state	Consequence
Call Request (CR_)	3	NC	VAL/CFI VAL/CNX VAL/INC VAL_ VAL/DLC	4/3 4/5 4/10 4/10 4/3	Failed Accepted Aborted Aborted Failed
Program (PR_) [a]	3/10/14	NC	VAL CNX(10)	NC 11	Accepted Aborted
List Request (RL_) [a]	3/10/14	NC	LS_ CNX(10)	NC 11	Accepted Aborted
Disregard Incoming Call (DIC)	10	NC	VAL	14	Incoming call not accepted
Connect Incoming Call (CIC)	14	NC	VAL/CNX VAL	11 3	Incoming call accepted Incoming call not accepted
Any command	X	NC	INV	NC	Failed

NC No change

[a] Reception of INC – circuit 125 turning ON or OFF and/or the issue of DIC – does not interfere with Program and List commands and their responses.



Note – Procedures after disconnection by the DCE are described in Recommendation V.24, § 4.4.3.

FIGURE 5/V.25 *bis*

Addressed call 108/2 response mode

4.2 *Interface procedures at the calling data station*

The DTE/DCE interface procedure for automatic calling and answering is shown in the state diagram in Figure 5/V.25 *bis*.

The call set-up procedure is as follows:

- When the DTE is not ready to answer an incoming call or to enter the dialogue with the DCE, the interface is in state 1, *DTE not ready*.
- Prior to entering the dialogue with the DCE, the DTE shall signal 108/2 = ON and the interface is then in state 2, *DTE ready*.
- The DCE signals to the DTE that it is ready to enter the dialogue with the DTE by signalling 106 = ON, state 3, *DTE-DCE dialogue*. In this state, the DTE can issue commands and the DCE may issue indications.
- To initiate a call set-up, the DTE shall issue a *call request* command which should be acknowledged by the DCE either with an invalid or a valid indication. In the latter case the interface moves to state 4, call establishment. If the *call request* command contains a PSTN (public switched telephone network) number, the DCE shall proceed with the call set-up procedure. If it contains a DCE memory address, the DCE shall use its stored number.
- The DCE remains in state 4 during the dialling process.
- If the call is established and the answering tone is detected (see § 6.1), a call connecting indication should be issued by the DCE, the interface moves to state 5, *answer tone detected*, and circuit 106 is turned OFF.
- If the call fails, the DCE may issue a *call failure* or a delayed call indication while in state 4 and return to state 3. During transmission of a calling station identification and the subsequent disconnection from the line following a call failure, the DCE may turn circuit 106 OFF and return to state 2, when it is not capable of handling new commands from the DTE.
- On completion of the line procedures (see § 6.1), circuit 107 is turned ON and the interface moves to state 6, *call connected*. From this state the DTE may enter the *data transfer* phase, state 12, in the normal manner.
- While the DCE is in state 3 or state 4, prior to going *off hook*, an incoming call shall be signalled to the DTE using circuit 125 and/or using the *incoming call* indication. The interface then moves to state 10, *incoming call accepting*. If in this state the DTE wishes not to answer the incoming call, it may issue a *disregard incoming call* command. In this case the interface will move to state 14 and allow exchange of indications and commands other than *call request*. The collision of a call request with an incoming call before the latter has been detected is for further study.
- The DTE may clear a call or call attempt at any time by turning circuit 108/2 OFF, state 7, *clearing by DTE*. The interface will then move to state 1 or 8 for circuit 125 OFF or ON respectively.

4.3 *Interface procedures at the answering data station*

The DTE/DCE interface procedure for automatic calling and answering is shown in the state diagram in Figure 5/V.25 *bis*. The procedure is as follows:

- When the DTE is not ready to answer an incoming call or to enter the dialogue with the DCE, the interface is in state 1, *DTE not ready*.
- Prior to entering the dialogue with the DCE, the DTE shall signal 108/2 = ON and the interface is then in state 2, *DTE ready*.
- The DCE signals to the DTE that it is ready to enter the dialogue with the DTE by signalling 106 = ON, state 3, *DTE-DCE dialogue*. In this state the DTE can issue commands and the DCE may issue indications.
- An incoming call is indicated to the DTE using circuit 125 and/or with an *incoming call* indication, and by this means the interface will move from state 3 or 4 to state 10, *incoming call accepting*. (In the case of state 4, the incoming call may only be detected prior to the DCE going *off hook*.)
- If an incoming call occurs when the DTE is in state 1, *DTE not ready*, the DCE moves to state 8, *incoming call*. The DTE may then turn circuit 108/2 ON, in response to this call or in order to enter the dialogue with the DCE. The interface thus moves to state 9, *incoming call recognized*. The DCE will respond by turning circuit 106 ON and thus also in this case the interface moves to state 10.

- While in state 10, the DTE may reject the incoming call by turning circuit 108/2 OFF or issue a *disregard incoming call* command which should be acknowledged by the DCE either with an invalid or valid indication. In the latter case, the interface will move to state 14 and allow exchange of indications and commands other than *call request.* If no *disregard incoming call* command has been issued within a period determined by national regulations, or when this command is reset by a subsequent *connect incoming call* command which should be acknowledged by the DCE either with an invalid or a valid indication, the DCE shall accept the incoming call, may issue a Call Connecting indication and move to state 11, *incoming call accepted* turning circuit 106 OFF, and from there to state 13, *line seized,* by turning circuit 125 OFF.
- Simple DCEs, having no programming capabilities, have in the past, been provided which do not respond to the DIC and CIC commands.
- In this case the DCE will connect the incoming call immediately or after a predetermined period dependent on national regulations, thus moving directly from state 9, *incoming call recognized* to state 13, *line seized.*
- On completion of the line procedures (see § 6.1), circuit 107 is turned ON and the interface moves to state 6, *call connected.* From this state the DTE may enter the *data transfer* phase, state 12 in the normal manner.

5 Direct call and/or answer controlled by the DTE (circuit 108/1)

The *direct call* operating mode provides the DTE with the facility of setting up a call on the PSTN to a predefined data station, without a message exchange between the DTE and the DCE. The PSTN number to be called (or sequence of PSTN numbers) is recorded in the DCE. This Recommendation does not cover the method for recording the number in the DCE.

5.1 *Interchange circuits involved*

The interchange circuits used in this automatic calling/answering procedure are listed in Table 8/V.25 *bis.*

TABLE 8/V.25 *bis*

Interchange circuit		Direction	
Number	Name	from DCE	to DCE
107	Data set ready	X	
108/1	Connect data set to line		X
125	Calling indicator	X	

5.1.1 *Circuit 107 – Data set ready*

The DCE shall turn circuit 107 ON:

i) at the end of the automatic call set-up procedure, to indicate to the DTE that the connection is established and the DCE connected to line;

ii) on completion of manual call set-up procedure.

The DCE shall turn circuit 107 OFF:

i) to indicate to the DTE that the connection has been cleared down during the data transfer phase (to be permitted where national regulations require it);

ii) in response to a clear request by the DTE turning OFF circuit 108/1 while in the data transfer state.

5.1.2 *Circuit 108/1 – Connect data set to line*

The DTE shall turn circuit 108/1 ON:

i) to instruct the DCE to seize the line, dial the pre-recorded number and execute the connection procedure on the PSTN as the caller party;

ii) to instruct the DCE to seize the line and execute the connection procedure on the PSTN as the called party if circuit 125 is in the ON condition.

The DTE shall turn circuit 108/1 OFF:

i) to instruct the DCE to clear down the connection during data transfer;

ii) to instruct the DCE to abort the call set-up procedure;

iii) to indicate to the DCE that it is not ready to accept an incoming call.

5.1.3 *Circuit 125 – Calling indicator*

The DCE shall provide circuit 125.

5.2 *Interface procedure at the calling data station*

The state diagram shown in Figure 6/V.25 *bis* displays the allowed transitions between the different interface states. The call set-up appears on the left side of Figure 6/V.25 *bis* and proceeds as follows:

- The DTE, whenever it wishes to initiate a call, checks that circuit 125 is in the OFF condition, then turns ON circuit 108/1. A timer (T1) is started on the transition from state 1, *idle* to state 2.
- The DCE turns ON circuit 107 when it has recognized the successful establishment of the call, thus moving to state 3, *data transfer.*
- If the first call attempt is unsuccessful, the DCE may make further attempts according to its programming and national regulations. During this period, the interface remains in state 2.
- When in state 1, the DCE will turn circuit 125 ON whenever an incoming call occurs, and the interface moves to state 5, *incoming call.* State 6, *incoming call accepted,* is reached when the DTE turns ON circuit 108/1 to accept the call, which in turn leads to state 7, *answering station connecting.* The DCE may abort the incoming call by turning OFF circuit 108/1 when in state 7, and return to state 1.
- When in state 2, the DCE will turn circuit 125 ON whenever an incoming call has been detected prior to the DCE seizing the line. The interface then moves to state 6 as incoming calls have priority over call set-up attempts. The DCE should remain in state 6 for at least 100 ms (this value is for further study) before entering state 7, to allow the DTE to recognize the ON condition on circuit 125.
- While in state 2, the DTE can abort the call attempt by turning OFF circuit 108/1. This may be done if timer T1 expires with circuit 107 remaining in the OFF condition.

Note – Timeout T1 could range from 1 to 5 minutes depending on the programming of the DCE and national regulations.

5.3 *Interface procedure at the answering data station*

This mode provides the DTE with the facility of accepting an incoming call on a "per call" basis.

This operating mode is shown on the right hand side of the state diagram shown in Figure 6/V.25 *bis* and proceeds as follows:

- The DCE turns ON circuit 125 whenever it detects a ringing signal on the line and moves from state 1, *idle,* to state 5, *incoming call.*
- If the DTE does not want to accept the call, it may hold circuit 108/1 in the OFF condition. After the end of the ringing signal, the interface returns to state 1.
- If the DTE wishes to accept the call, it turns circuit 108/1 ON, and moves from state 5, *incoming call,* to state 6, *incoming call accepted,* and then to state 7, *answering station connecting.*
- In state 7, *answering station connecting,* the DCE accepts the call as detailed in § 6. While in this state the DTE may abort the connection by turning OFF circuit 108/1.
- On completion of the connection procedure, the DCE turns ON circuit 107, moving then from state 7, *answering station connecting,* to state 3, *data transfer.*

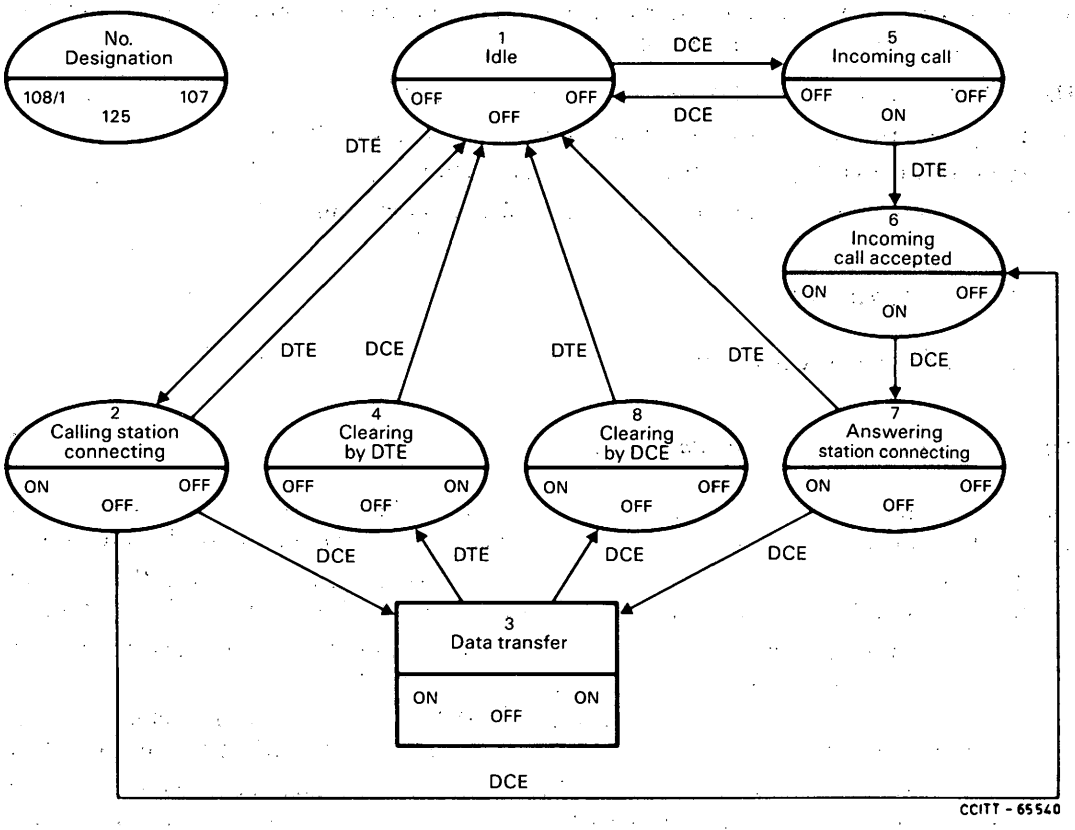


FIGURE 6/V.25 *bis*

Simplified procedure for direct call 108/1 answer mode

6 Line procedures

6.1 *Line procedure at the calling DCE*

- Whenever the DCE has received the *call request* (see Figure 5/V.25 *bis* and Figure 6/V.25 *bis*), the DCE seizes the line by going *off hook*.
- Dialling may proceed when dial tone has been detected, or, where national regulations permit this, after a fixed time delay. The value of this delay will be dependent on the national network.
- On completion of dialling, or, where possible, on recognizing the other end going off hook, a calling tone as specified in Recommendation V.25 is transmitted.
- During interruptions of the calling tone, the DCE monitors the line in order to detect call progress tones from the network and/or the answering tone, as specified in Recommendation V.25 provided by the remote DCE. If no answering tone is detected within a time-out, the DCE may go on hook and may issue an appropriate *call failure* indication. It may slso issue *call failure* indication on recognition of specific signalling tones from the network.
- When the answering tone has been recognized by the DCE as detailed in Recommendation V.25, the DCE should issue a call connecting indication and then turn circuit 106 to the OFF condition.
- All other actions including the turning ON of circuit 107 and the completion of the connection procedure, are as detailed in Recommendation V.25.

The policy for handling unsuccessful calls may be dependent on the national networks. In this respect, a first level action by the call originating data station, which could involve blocking, by either the DCE or the DTE, of call attempts is not part of this Recommendation.

A second level action, which could permit the Administrations to trace erroneous calls when a subscriber complains, should be, where required by the Administration, implemented in the following way:

6.1.1 *Calling station identification* (where required by the Administration)

To enable the Administrations to have means to trace the originator of erroneous calls, an identification message has to be transmitted on the line by the call originating data station.

6.1.1.1 *Criteria for transmission of identification information*

The calling station identification information should be transmitted after the transmission of the calling tone when:

- the answering tone is not received within a time interval T2 from the end of the last digit dialled, or
- the answering tone is not received within a time interval T3 from detection of the remote end by DCE going *off hook*.

The choice of time outs T2 and T3 and their durations is dependent on national regulations.

Whenever the DCE enters the transmission of the identification information on the line, it will defer the execution of any *clearing request* made by the DTE which puts circuit 108 in the OFF condition until the transmission of this identification information is completed.

The complete identification information should be transmitted successively 3 times or more.

6.1.1.2 *Modulation method*

The identification signal should be asynchronously frequency modulated with the frequencies 1300 Hz (mark) and 2100 Hz (space) in such a way that it is possible to receive this signal with a modem according to Recommendation V.23.

The modulation rate should be 1200 bauds. In cases where this rate cannot be realized, a modulation rate of 300 bauds should be used.

6.1.1.3 *Format of identification information*

The identification information should be encoded according to International Alphabet No. 5 with one start bit, one stop bit and an even parity bit according to Recommendations T.50 and V.4. The first digits of the identification number should contain the country code of the subscriber's telephone number.

6.1.1.4 *Implementation*

In addition to the contents of this Recommendation, the regulations of the national Administrations must also be complied with. The additional requirements may be:

- the use of the CRI command with or without the identification number;
- generation and storage of the identification number;
- complete structure and content of the identification number (except the first two digits);
- recording and detection of the identification information.

6.2 *Line procedure at the answering DCE*

- When ringing is received on the line, the DCE turns ON circuit 125 and where implemented, issues an *incoming call* indication if circuits 108/2 and 106 are in the ON condition.
- If circuit 108/1 or circuit 108/2 is OFF, the DCE waits for circuit 108 to be turned ON.
- If circuit 108/2 is ON, and the *disregard incoming call* command is not received within a period of time determined by national regulations, the DCE may issue, where implemented, a call connecting indication and then goes off hook.
- When circuit 108/1 is ON, the DCE goes *off hook* after a period of time determined by national regulations.

– If circuit 108 is not turned ON, then the call is not answered.
– Whenever the DCE goes *off hook*, it turns OFF circuit 106 if not already OFF.
– After going *off hook*, the DCE completes the connection procedure and turns circuit 107 ON, as detailed in Recommendation V.25.

7 Manual calling and answering

The operational procedures for manual calling to an automatic answering data station, and automatic calling to a manual answering data station, are the same as detailed in Recommendation V.25, §§ 6 and 7, with the exception that circuit 106 has to be turned OFF before turning ON circuit 107, in the mode *addressed call and/or answer authorized by the DTE.*

Where the answering data station is expected to have a manual answering mode, this may be indicated to the calling DCE. The method for doing this is for further study.

ANNEX A

(to Recommendation V.25 *bis*)

Test facilities

Guidance on maintenance facilities

This annex contains information on test facilities thought to be desirable in relation to implementations of Recommendation V.25 *bis* automatic calling procedures.

The adoption of such procedures and especially the provision of centralized maintenance facilities by Administrations may not be assumed.

In order to enable a fault to be located in either the DTE or the DCE, the DTE should not be involved in the test. The test may be initiated, e.g. by pressing a button on the DCE, whereas indication of the test result may be presented, e.g. by means of a visual indicator.

The actual test consists of two stages: a DCE self-test and a test in cooperation with a maintenance centre. In which order these two stages are activated is not specified in this Recommendation. The test of the modem part of the DCE will not be part of this Recommendation, but should be performed separately according to Recommendation V.54.

A.1 *DCE self-test stage*

In this stage, the DCE will test as many functions and hardware as reasonably possible.

The test should comprise a loop at the DTE-DCE interface similar to Recommendation V.54 loop 2 including all circuits normally exercised during the call set-up and clear phase. Further parts of the test depend on the DCE implementation, e.g. in case of a microprocessor-based design a functional test of the CPU, RAM and ROM would be appropriate.

A.2 *DCE test with maintenance centre*

In this stage, the procedure is as follows:

A.2.1 The user sets up manually a call with the maintenance centre (MC).

A.2.2 On answering the call, the MC will send an answering tone of appropriate length to ensure detection by the DCE.

A.2.3 As soon as the answering tone is detected, the DCE should be connected with the line.

A.2.4 After detecting the end of the answering tone, the DCE starts sending the dialling digits 1, 2, 3, 4, 5, 6, 7, 8, 9, 0 in accordance with the regulations of the Administration involved.

Note – They shall have the same spacing as during the automatic call set-up.

A.2.5 In case not all numbers are detected faultlessly, the MC will send a 2100 Hz tone for 0.4 ± 0.1 s indicating a negative test result and disconnect from the line.

A.2.6 On detecting the 2100 Hz tone, the DCE will end the test procedure and indicate a negative test result.

A.2.7 If all numbers are received correctly, the MC will send a 1300 Hz tone for 0.4 ± 0.1 s and start sending towards the DCE signalling tone to be defined by the Administration involved.

A.2.8 At the end of this sequence, a 2100 Hz tone will be sent for 0.4 ± 0.1 s and the MC will disconnect.

A.2.9 The DCE receiving the 2100 Hz tone will give a positive or negative indication depending on the test result and end the procedure.

Note – For pulse dialling, the open contact shall be coded by a 2100 Hz tone and the closed contact by no signal at all.

ANNEX B

(to Recommendation V.25 *bis*)

SDL Description of the addressed call – 108/2 Response Mode

This Annex provides an SDL description, as per the Z.100 serie Recommendations, of the message exchanges specified in the present Recommendation for the addressed call – 108/2 response mode. This part of the automatic calling procedure is specified in § 4 and Figure 5/V.25 *bis*, which have to be taken as the master in case of any ambiguity.

The process described hereafter in Figure B-2/V.25 *bis* the key of which is Figure B-1/V.25 *bis*, is invoked when the DCE enters state 3 "DTE-DCE dialogue", or state 10 "Incoming call accepting". It is terminated when the DCE enters state 5 "Answer tone detected", or state 11 "Incoming call accepted".

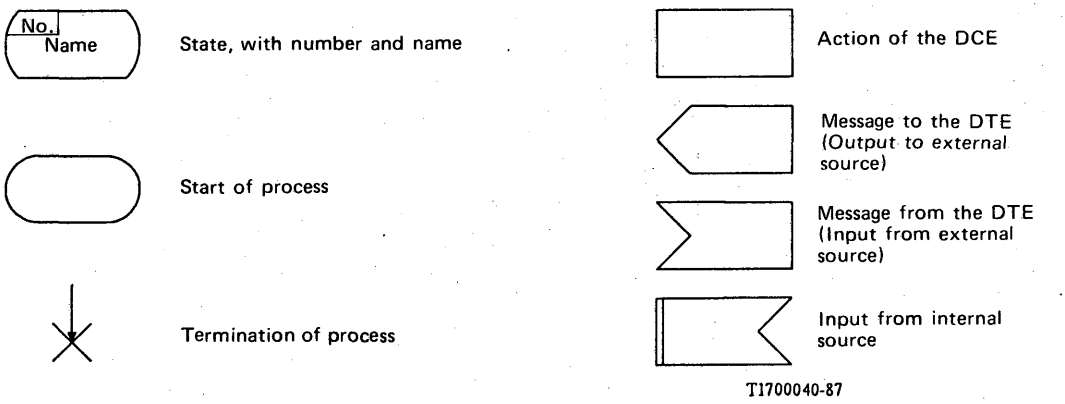
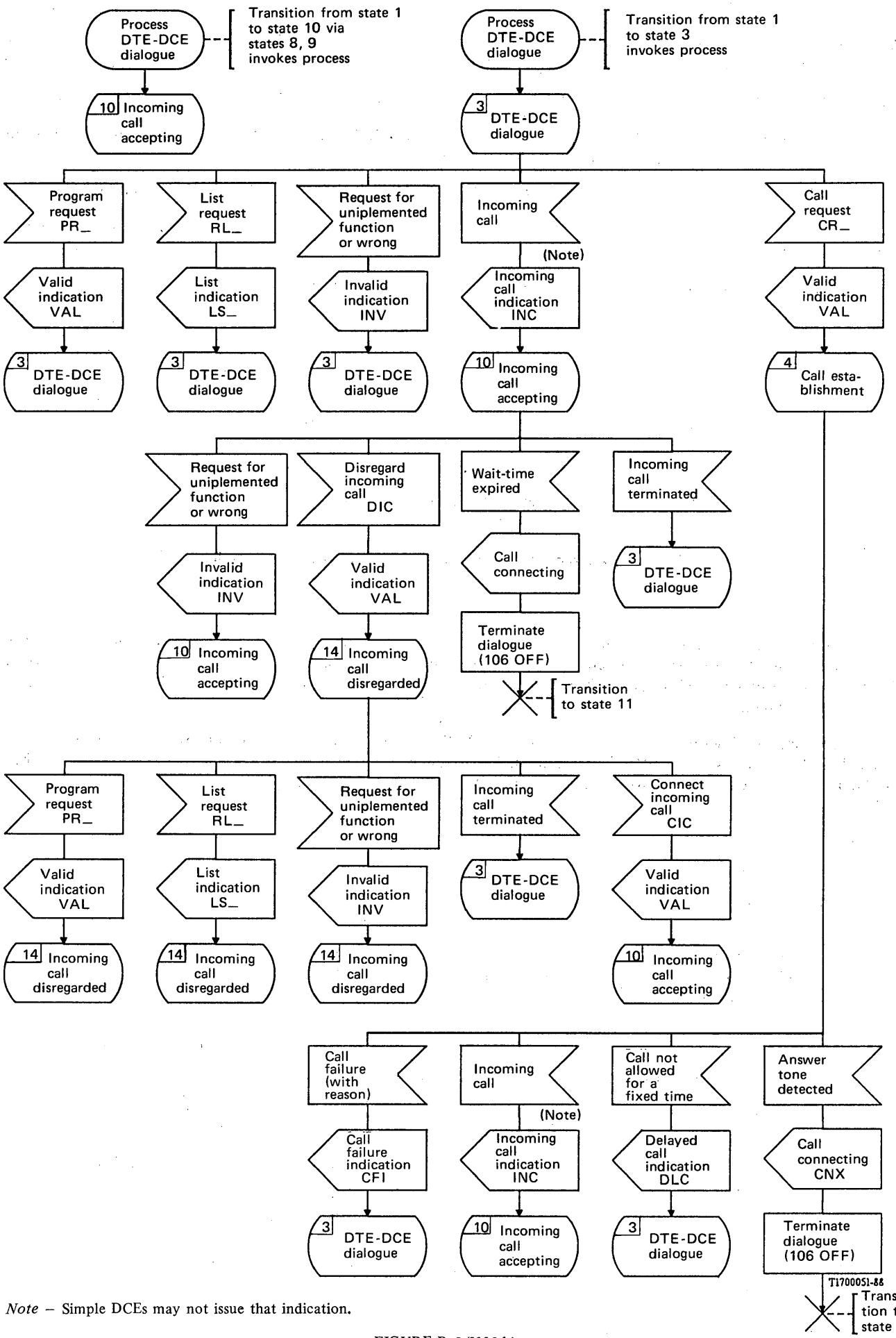


FIGURE B-2/V.25 *bis*

Key to SDL-diagram in Figure B-2/V.25 *bis*



Note – Simple DCEs may not issue that indication.

FIGURE B-2/V.25 *bis*

Detailed SDL-diagram, DCE-side

APPENDIX I

(to Recommendation V.25 *bis*)

General description of the V.25 bis command/indication syntax

The following table is a general presentation of the V.25 *bis* message syntax which is offered for guidance in the development of any application where harmonization with Recommendation V.25 *bis* is sought (Detailed description of the V.25 *bis* syntax is presented in Table 6/V.25 *bis*).

TABLE I-1/V.25 *bis*

General description of the V.25 bis message syntax

description language:

a | b denotes the set (a, b)

a b denotes the set (ab)

a* denotes the set (e, a, aa, aaa, . . .)
(e = empty)

description:

message	=	(opcode) | (opcode parameter_list)
opcode	=	letter letter letter
parameter list	=	parameter (delimiter parameter)*
parameter	=	(letter | digit | special | presentation) (letter | digit | special | presentation)*
letter	=	'A' | 'B' | 'C' | 'D' | 'E' | 'F' | 'G' | 'H' | 'I' | 'J' | 'K' | 'L' | 'M' | 'N' | 'O' | 'P' | 'Q' | 'R' | 'S' | 'T' | 'U' | 'V' | 'W' | 'X' | 'Y' | 'Z'
digit	=	'0' | '1' | '2' | '3' | '4' | '5' | '6' | '7' | '8' | '9'
special	=	'&' | ':' | '>' | '<' | '=' | 'P' | 'T'
presentation	=	' ' | '.'
delimiter	=	';'

Note – The syntax of the parameters depends on the message and should be specified in the message description.

Recommendation V.26

2400 BITS PER SECOND MODEM STANDARDIZED FOR USE ON 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Mar del Plata, 1968; amended at Geneva, 1972, 1976 and 1980, Malaga-Torremolinos, 1984)

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

1 The principal characteristics for this recommended modem for transmitting data at 2400 bits per second on 4-wire leased point-to-point and multipoint circuits conforming to Recommendation M.1020 [1] are as follows:

a) it is capable of operating in a full-duplex mode;

b) four-phase modulation with synchronous mode of operation;

c) inclusion of a backward (supervisory) channel at modulation rates up to 75 bauds in each direction of transmission, the use of these channels being optional.

2 Line signals

2.1 The carrier frequency is to be 1800 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Division of power between the forward and backward channels*

If simultaneous transmission of the forward and backward channels occurs in the same direction, a backward channel shall be 6 dB lower in power level than the data channel.

2.3 The data stream to be transmitted is divided into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element. At the receiver the dibits are decoded and the bits are reassembled in correct order. Two alternative arrangements of coding are listed in Table 1/V.26. The left-hand digit of the dibit is the one occurring first in the data stream.

TABLE 1/V.26

Dibit	Phase change (see Note)	
	Alternative A	Alternative B
00	0°	+45°
01	+90°	+135°
11	+180°	+225°
10	+270°	+315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

The meaning of phase change for alternatives A and B is illustrated by the line signal diagram in Figure 1/V.26.

2.4 *Synchronizing signal*

For the whole duration of the interval between the OFF to ON transitions of circuits 105 and 106, the line signal shall be that corresponding to the continuous transmission of dibit 11. This shall be known as the synchronizing signal.

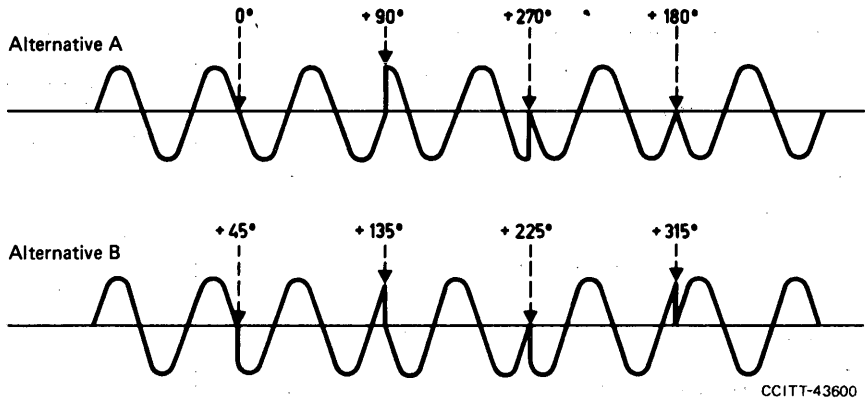


FIGURE 1/V.26

Note – Owing to several causes, the stability of timing recovery at the receiver is liable to be data-pattern sensitive. The presence of dibit 11 provides a stabilizing influence irrespective of the cause of lack of stability. Users are advised to include sufficient binary 1s in the data which will ensure that the dibit 11 will occur frequently. In certain cases, the use of a scrambling method may also facilitate timing recovery problems. However, prior agreement is required between users of a circuit.

3 Data signalling and modulation rates

The data signalling rate shall be 2400 bits per second ± 0.01%, i.e. the modulation rate is 1200 bauds ± 0.01%.

4 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance at the transmitter is ± 1 Hz and assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

5 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc., to be as recommended for backward channel in Recommendation V.23.

6 Interchange circuits

6.1 *List of interchange circuits concerned* (see Table 2/V.26)

6.2 *Threshold and response times of circuit 109*

A fall in level of the incoming line signal to −31 dBm or lower for more than 10 ± 5 ms will cause circuit 109 to be turned OFF. An increase in level to −26 dBm or higher will, within 10 ± 5 ms, turn this circuit ON. The condition of circuit 109 for levels between −26 dBm and −31 dBm is not specified except that the signal level detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition. These values shall be measured when the synchronizing signal as defined in § 2.4 above is being transmitted. It should be noted that the aforementioned times relate only to the defined function of circuit 109 and do not necessarily include the time for the modem to achieve bit synchronism.

Note – The signal levels specified above shall apply unless completion of Recommendation M.1020 [1] indicates otherwise.

TABLE 2/V.26

Interchange circuit		Forward (data) channel half-duplex or full-duplex (see Note)	
No.	Designation	Without backward channel	With backward channel
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105	Request to send	X	X
106	Ready for sending	X	X
107	Data set ready	X	X
108/1	Connect data set to line	X	X
109	Data channel received line signal detector	X	X
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
118	Transmitted backward channel data	–	X
119	Received backward channel data	–	X
120	Transmit backward channel line signal	–	X
121	Backward channel ready	–	X
122	Backward channel received line signal detector	–	X

Note – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 8).

6.3 *Response times of circuits 106, 121 and 122*

Circuit 106		
OFF to ON	65-100 ms (see Note 1) (Provisional)	25-45 ms (see Note 2) (Provisional)
ON to OFF	⩽ 2 ms	
Circuit 121		
OFF to ON	80 ms to 160 ms	
ON to OFF	⩽ 2 ms	
Circuit 122		
OFF to ON	< 80 ms	
ON to OFF	15 ms to 80 ms	

Note 1 – These times shall be used when infrequent operation of circuit 105 is required, e.g. as in many cases of point-to-point usage. Further study is required to verify the range quoted.

Note 2 – These times shall be used when frequent operation of circuit 105 is required, e.g. in many cases of multipoint usage. Further study is required with a view to reducing these times.

6.4 *Threshold of circuit 122*

– greater than −34 dBm: circuit 122 ON
– less than −39 dBm: circuit 122 OFF

The condition of circuit 122 for levels between −34 dBm and −39 dBm is not specified except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

6.5 *Fault condition of interchange ciruits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

6.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

6.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

6.5.3 All other circuits not referred to above may use failure detection types 0 or 1.

7 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114 and receiver signal element timing, circuit 115. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment instead of in the data circuit-terminating equipment and be transferred to the modem via circuit 113.

8 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110 [2].

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the Series V application which minimizes the number of interchange circuits.

9 The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

Reference

[1] CCITT Recommendation *Characteristics of special quality international leased circuits, with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

Recommendation V.26 *bis*

2400/1200 BITS PER SECOND MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

(Geneva, 1972; amended at Geneva, 1976 and 1980, Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that there is a demand for data transmission at 2400 bit/s over the general switched telephone network;

(b) that a majority of connections over the general switched telephone network within some countries are capable of carrying data at 2400 bit/s;

(c) that a much lower proportion of international connections in the general switched telephone service are capable of carrying data at 2400 bit/s;

unanimously declares the view

(1) that transmission at 2400 bit/s should be allowed on the general switched telephone network. Reliable transmission cannot be guaranteed on every connection or routing and tests should be made between the most probable terminal points before a service is provided.

The CCITT expects that developments during the next few years in modern technology will bring about modems of more advanced design enabling reliable transmission to be given on a much higher proportion of connections.

Note – The provisions of this Recommendation are to be regarded as provisional in order to provide service where it is urgently required and between locations where it is expected that a reasonably satisfactory service can be given. The study of improved methods of transmission at 2400 bits/s or above over the general switched telephone network will be urgently continued with the aim of recommending a method of transmission which will enable a more reliable service to be given over a high proportion of the connections encountered in normal service.

(2) that the characteristics of the modems for this service shall provisionally be the following:

1 Principal characteristics

a) Use of a data signalling rate of 2400 bit/s with carrier frequency, modulation and coding according to Recommendation V.26, Alternative B (see Note below) on the communication channel. Administrations and users should note that the performance of this modem on international connections may not always be suitable for this service without prior testing and conditioning if required.

b) Reduced rate capability at 1200 bit/s.

c) Inclusion of a backward channel at modulation rates up to 75 bauds, use of this channel being optional.

Note – Attention is drawn to the fact that there are some old-type modems currently in operation for which the coding method in accordance with Recommendation V.26, Alternative A, is used.

2 Line signals at 2400 and 1200 bit/s

2.1 The carrier frequency is to be 1800 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Phase distortion limits*

The transmitted line signal spectrum should have linear phase characteristics (to be obtained by means of filters or equalizers or digital means). The deviation of the phase distortion characteristic should not exceed the limits specified in Figure 1/V.26 *bis*.

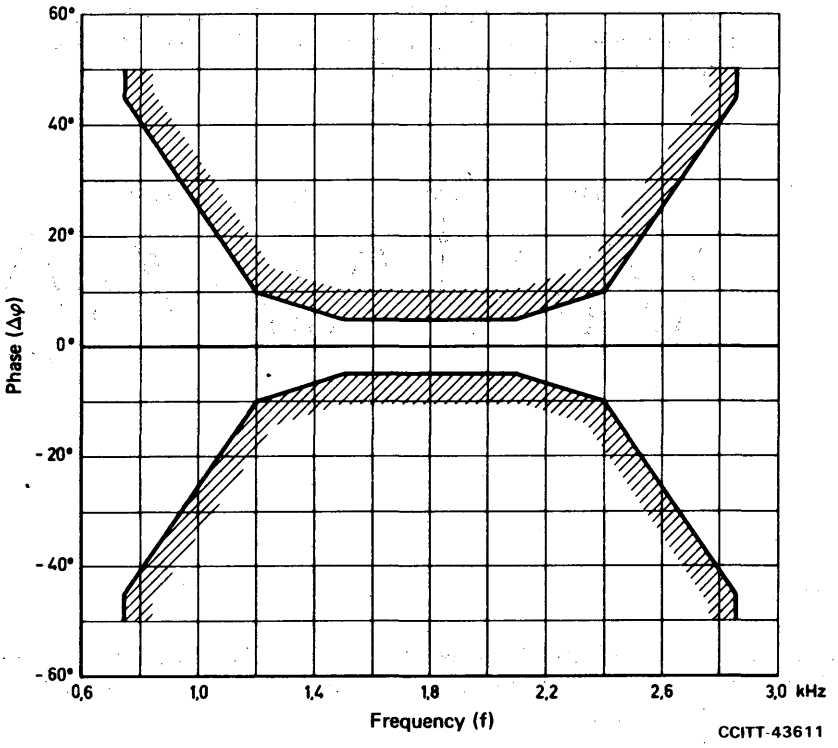


FIGURE 1/V.26 *bis*

Tolerance limit for phase distortion of the signal transmitted to the line

2.3 *Division of power between forward and backward channels*

Equal division of power between the forward and backward channels is recommended provisionally.

2.4 *Operation at 2400 bit/s*

2.4.1 The data stream to be transmitted is divided into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 1/V.26 *bis*). At the receiver the dibits are decoded and the bits are reassembled in correct order. The left-hand digit of the dibit is the one occurring first in the data stream.

The meaning of phase change is illustrated by the line signal diagram given in Figure 2/V.26 *bis*.

TABLE 1/V.26 *bis*

Dibit	Phase change (see Note)
00	+45°
01	+135°
11	+225°
10	+315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

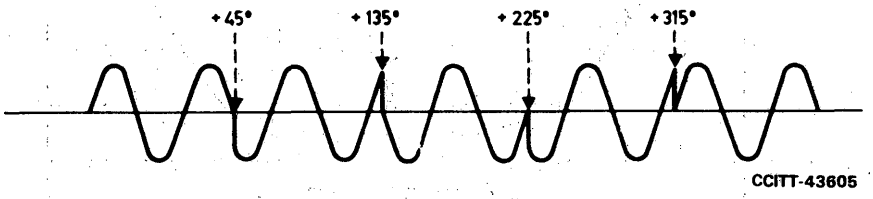


FIGURE 2/V.26 *bis*

2.4.2 *Synchronizing signal*

For the whole duration of the interval between the OFF to ON transitions of circuits 105 or 107 and 106, the line signal shall be that corresponding to the continuous transmission of dibit 11. This shall be known as the synchronizing signal (see § 5.2.2 below).

Note – Owing to several causes the stability of timing recovery at the receiver is liable to be data-pattern sensitive. The presence of dibit 11 provides a stabilizing influence irrespective of the cause of lack of stability. Users are advised to include sufficient binary 1s in the data which will ensure that the dibit 11 will occur frequently.

2.4.3 *Data signalling and modulation rates*

The data signalling rate shall be 2400 bit/s ± 0.01%, i.e. the modulation rate is 1200 bauds ± 0.01%.

2.5 *Operation at 1200 bit/s*

2.5.1 Coding and modulation used are 2-phase differential modulation with binary 0 for +90° and binary 1 for +270°.

2.5.2 The data signalling rate shall be 1200 bit/s ± 0.01%, the modulation rate remains at 1200 bauds ± 0.01%.

3 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance at the transmitter is ± 1 Hz and assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

4 Backward channel

4.1 *Modulation rate and characteristic frequencies for the backward channel*

The modulation rate and characteristic frequencies for the backward channel are as follows:

	F_z (symbol 1, mark)	F_A (symbol 0, space)
Modulation rate up to 75 bauds	390 Hz	450 Hz

In the absence of any signal on the backward channel interface, the condition Z signal is to be transmitted.

4.2 *Tolerances on the characteristic frequencies of the backward channel*

As the backward channel is a VF telegraph-type channel, the frequency tolerances should be as recommended in Recommendation R.35 [1] for frequency-shift voice-frequency telegraphy.

The ± 6 Hz frequency drift in the connection between the modems postulated in § 3 above would produce additional distortion in the backward channel. This should be taken into account in the design.

5 Interchange circuits

5.1 *List of essential interchange circuits*

The list of interchange circuits essential for the modems when used on the general switched telephone network, including terminals equipped for manual calling or answering or automatic calling or answering is given in Table 2/V.26 *bis*.

5.2 *Response times of circuits 106, 109, 121 and 122* (see Table 3/V.26 *bis*)

5.2.1 Circuit 109 response times are the times that elapse between the connection or removal of the test synchronizing signal to or from the modem receive line terminals and the appearance of the corresponding ON and OFF condition on circuit 109.

The level of the test synchronizing signal should fall within the level range between 3 dB above the actual OFF to ON threshold of the received line signal detector and the maximum admissible level of the received signal. At all levels within this range, the measured response times shall be within the specified limits.

5.2.2 Circuit 106 response times are from the connection to an ON or OFF condition on:

- circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106; or
- circuit 107 (where circuit 105 is not required to initiate the synchronizing signal) to the appearance of the corresponding ON or OFF condition on circuit 106.

TABLE 2/V.26 *bis*

Interchange circuit		Forward (data) channel one-way system (see Note 1)				Forward (data) channel either-way system (see Note 1)	
No.	Designation	Without backward channel		With backward channel		Without backward channel	With backward channel
		Transmit end	Receive end	Transmit end	Receive end		
102	Signal ground or common return	X	X	X	X	X	X
103	Transmitted data	X		X		X	X
104	Received data		X		X	X	X
105	Request to send	X		X		X	X
106	Ready for sending	X		X		X	X
107	Data set ready	X	X	X	X	X	X
108/1 or 108/2 (see Note 2)	Connect data set to line: Data terminal ready	X	X	X	X	X	X
109	Data channel received line signal detector		X		X	X	X
111	Data signalling rate selector (DTE source)	X	X	X	X	X	X
113	Transmitter signal element timing (DTE source)	X		X		X	X
114	Transmitter signal element timing (DCE source)	X		X		X	X
115	Receiver signal element timing (DCE source)		X		X	X	X
118	Transmitted backward channel data				X		X
119	Received backward channel data			X			X
120	Transmit backward channel line signal						X
121	Backward channel ready				X		X
122	Backward channel received line signal detector			X			X
125	Calling indicator	X	X	X	X	X	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 7).

Note 2 – This circuit shall be capable of operation as circuit 108/1 or circuit 108/2 depending on its use.

TABLE 3/V.26 *bis*

Response times

Circuit 106		
OFF to ON	750 ms to 1400 ms (see Note 1)	a) 65 ms to 100 ms (see Note 2) b) 200 ms to 275 ms (see Note 2)
ON to OFF	⩽ 2 ms	
Circuit 109		
OFF to ON	300 ms to 700 ms (see Note 1)	5 ms to 15 ms (see Note 1)
ON to OFF	5 ms to 15 ms	
Circuit 121		
OFF to ON	80 ms to 160 ms	
ON to OFF	⩽ 2 ms	
Circuit 122		
OFF to ON	< 80 ms	
ON to OFF	15 ms to 80 ms	

Note 1 – For automatic calling and answering, the longer response times of circuits 106 and 109 are to be used during call establishment only.

Note 2 – The choice of response times depends upon the system application: a) limited protection given against line echoes; b) protection given against line echoes.

Note 3 – The above parameters and procedures, particularly in the case of automatic calling and answering are provisional and are the subject of further study. Especially the shorter response times for circuit 109 may need revision to prevent remnants of the synchronizing signal from appearing on circuit 104.

5.3 *Threshold of data channel and backward channel received line signal detectors*

Level of received line signal at receive line terminals of modem for all types of connections, i.e. general switched telephone network or non-switched leased telephone circuits:

- greater than −43 dBm: circuits 109/122 ON
- less than −48 dBm: circuits 109/122 OFF

The condition of circuits 109 and 122 for levels between −43 dBm and −48 dBm is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

Where transmission conditions are known and allowed, it may be desirable at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

5.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

5.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

5.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114 and receiver signal element timing, circuit 115. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment instead of in the data circuit-terminating equipment and be transferred to the modem via circuit 113.

7 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

8 The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

9 When echo control device disabling is required, it is recommended that the procedures specified in Recommendation V.25 be followed.

10 Fixed compromise equalizer

A fixed compromise equalizer shall be incorporated into the receiver. The characteristics of this equalizer may be selected by Administrations but this should be the matter for further study.

Reference

[1] CCITT Recommendation *Standardization of FMVFT systems for a modulation rate of 50 bauds*, Vol. VII, Rec. R.35.

2400 BITS PER SECOND DUPLEX MODEM USING THE ECHO CANCELLATION TECHNIQUE STANDARDIZED FOR USE ON THE GENERAL SWITCHED TELEPHONE NETWORK AND ON POINT-TO-POINT 2-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

The CCITT,

considering

(a) that there is a demand for data transmission at 2400 bit/s in the duplex mode on the general switched telephone network (GSTN) and on point-to-point 2-wire leased telephone-type circuits;

(b) that there will be a demand to have compatibility with higher data signalling rate duplex modems in the fall-back mode;

(c) that in this case the echo cancellation technique (ECT) is foreseen,

unanimously declares

the view that the characteristics of the modems for this service shall provisionally be as follows:

1 Introduction

This modem is intended for use on connections on the GSTN and on point-to-point 2-wire leased telephone-type circuits (see Note 1). Its principal characterisics are as follows:

a) duplex mode of operation on the GSTN and point-to-point leased circuits,

b) half-duplex mode of operation (optional) on the GSTN and point-to-point leased circuits (Note 2),

c) channel separation by echo cancellation,

d) differential phase-shift modulation for each channel with synchronous line transmission at 1200 baud (nominal),

e) inclusion of a scrambler,

f) inclusion of a compromise or adaptive equalizer,

g) inclusion of test facilities,

h) operation with data terminal equipment (DTE) in the following modes:

2400 bit/s synchronous,

1200 bit/s synchronous (fall-back rate),

2400 bit/s start stop (optional),

1200 bit/s start stop (optional) (fall-back rate),

i) inclusion of an operating sequence intended to allow interworking with 2-wire duplex 4800 bit/s modem (which modem is for further study).

Note 1 – In certain countries the use of such a modem over the GSTN may not be allowed.

Note 2 – When the optional half-duplex mode of operation is used, provisions in § 7 shall supersede provisions given elsewhere in this Recommendation.

2 Line signals

2.1 *Carrier frequency*

The carrier frequency shall be 1800 ± 1 Hz. No separate pilot tones are provided.

2.2 *Data line signal level*

The power levels used will conform to Recommendation V.2.

2.3 *Equalizer*

If a fixed compromise equalizer is used, it shall be incorporated in the receiver. The characteristics of this equalizer may be selected by Administrations.

The possibility of producing compromise equalizer characteristics for international connections is for further study.

If an adaptive equalizer is used, it shall be able to converge on data signals at 2400 bit/s without a training sequence.

2.4 *Spectrum and group-delay characteristics*

A 100% raised cosine amplitude spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1200 Hz and 2400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1200 Hz and 2400 Hz.

The group-delay of the transmit filters shall be within ± 100 microseconds over the frequency range 1200-2400 Hz.

2.5 *Modulation*

2.5.1 *Data signalling rates*

The data signalling rate transmitted to line shall be 2400 bit/s or 1200 bit/s ± 0.01% with a modulation rate of 1200 baud ± 0.01%.

2.5.2 *Encoding of data bits*

2.5.2.1 *2400 bits per second*

At 2400 bit/s the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 1/V.26 *ter*). At the receiver, the dibits are decoded and reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.26 *ter*

Line encoding at 2400 bit/s

Dibit values	Phase change (see Note)
00	0°
01	90°
11	180°
10	270°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5.2.2 *1200 bits per second*

At 1200 bit/s each bit shall be encoded as a phase change relative to the phase of the preceding signal element (see Table 2/V.26 *ter*).

TABLE 2/V.26 *ter*

Line encoding at 1200 bit/s

Bit values	Phase change (see Note)
0	0°
1	180°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.6 *Received signal frequency tolerance*

The receiver shall be able to operate with frequency offsets in the signal received from the other modem of up to ± 7 Hz.

2.7 *Synchronizing signals*

Synchronizing signals are used in the operating sequence and in the half-duplex mode (see §§ 6.3 and 7). The synchronizing signals, for both data signalling rates, are divided into two segments as follows:

2.7.1 The composition of segment 1 is continuous 180° phase reversals for 32 symbol intervals.

2.7.2 Segment 2 is a pattern derived by scrambling binary ones with the scramblers defined in § 5. The length of the pattern is 64 bits (32 symbol intervals) for 2400 bit/s and 64 bit/s (64 symbol intervals) for 1200 bit/s. The patterns are defined in Table 3/V.26 *ter*. See also Appendix I.

TABLE 3/V.26 *ter*

Data signalling rate	Srambler (see § 5)	Segment 2 phase changes (in degrees)
2400 bit/s	GPC	0, 180, 180, 180, 180, 0, 0, 0, 0, 180, 180, 270, 90, 180, 0, 0, 90, 180, 0 ...
2400 bit/s	GPA	0, 180, 180, 180, 180, 0, 0, 0, 0, 180, 180, 270, 90, 180, 0, 180, 180, 270, 0 ...
1200 bit/s	GPC	0, 0, 180, 180, 180, 180, 180, 180, 180, 180, 0, 0, 0, 0, 0, 0, 0, 0, 180, 180, 180, 180, 180, 0, 0, 180, 180, 180, 0, 0, 0, 0, 0, 180, 180, 180 ...
1200 bit/s	GPA	0, 0, 180, 180, 180, 180, 180, 180, 180, 180, 0, 0, 0, 0, 0, 0, 0, 0, 180, 180, 180, 180, 180, 0, 0, 180, 180, 180, 0, 0, 180, 180, 180, 0, 180, 0 ...

3 Interchange circuits

3.1 *Essential and optional interchange circuits*

These are listed in Table 4/V.26 *ter.*

TABLE 4/V.26 *ter*

Interchange circuit (see Note 1)		Notes
No.	Designation	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	
106	Ready for sending	
107	Data set ready	
108/1 or	Connect data set to line	2
108/2	Data terminal ready	2
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	
112	Data signalling rate selector (DCE source)	3
113	Transmitter signal element timing (DTE source)	4
114	Transmitter signal element timing (DCE source)	5
115	Receiver signal element timing (DCE source)	5
125	Calling indicator	6
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.5).

Note 2 – This circuit shall be capable of operation as circuit 108/1 or circuit 108/2 depending on its use.

Note 3 – This circuit is optional.

Note 4 – When the modem is not operating in a synchronous mode at the interface, any signals on circuit 113 shall be disegarded. Many DTEs operating in an asynchronous mode do not have a generator connected to this circuit.

Note 5 – When the modem is not operating in a synchronous mode, this circuit shall be clamped to the OFF condition. Many DTEs operating in an asynchronous mode do not terminate this circuit.

Note 6 – This circuit is for use with the general switched telephone network only.

3.2 *Circuit 106 response times* (see Table 5/V.26 *ter*)

Circuit 106 response times are from the application of an ON or OFF condition on circuit 105. See also § 6.3 for conditions of circuit 106 during the operating sequence.

TABLE 5/V.26 *ter*

	Constant carrier
Circuit 106	
OFF to ON	⩽ 2 ms
ON to OFF	⩽ 2 ms

3.3 *Threshold and response times of circuit 109*

3.3.1 *Threshold*

The level of received line signal at the receive line terminals of the modem for all types of connections, i.e. the general switched telephone network or non-switched 2-wire leased telephone type circuits, is:

- greater than −43 dBm: circuit 109 ON
- less than −48 dBm: circuit 109 OFF

Where transmission conditions are known and allowed, it may be desirable at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

In addition, for use over special quality leased circuits (see Recommendation M.1020) the response levels of the received line signal detector shall be:

- greater than −26 dBm: circuit 109 ON
- less than −31 dBm: circuit 109 OFF

The condition of circuit 109 between the ON and OFF levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for the ON to OFF transition.

3.3.2 *Response time*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104.

The ON to OFF response time of circuit 109 is 5 ms to 15 ms. See also § 6.3 for the condition of circuit 109 during the operating sequence.

Following a drop-out after the initial handshake, circuit 109 shall be turned ON 40 to 50 ms after the level of the receiver signal appearing at the line terminal of the modem exceeds the relevant threshold defined in § 3.3.1.

3.4 *Timing arrangement*

Clocks shall be included in the modem to provide the DTE with transmitter element timing (circuit 114) and receiver signal element timing (circuit 115). The transmitter element timing may be originated in the DTE and be transferred to the modem via the appropriate interchange circuit, circuit 113.

3.5 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.6 *Fault condition of interchange circuits*

(See § 7 of Recommendation V.28 for association of the receiver failure detection types.)

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Modes of operation

The modem can be configured for the following modes of operation:

Mode i) 2400 bit/s ± 0.01% synchronous

Mode ii) 2400 bit/s start-stop 8, 9, 10 or 11 bits per character (optional)

Mode iii) 1200 bit/s ± 0.01% synchronous

Mode iv) 1200 bit/s start-stop 8, 9, 10 or 11 bits per character (optional).

4.1 *Transmitter*

4.1.1 In the synchronous modes of operation, the modem shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or circuit 114. The data shall then be scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.

When circuit 114 is used, the modem shall derive its line signal clock from the internal clock source or, alternatively, from the receive signal element timing.

4.1.2 In the start-stop modes, the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of 2400 or 1200 bit/s. The start-stop data to be transmitted shall be converted in conformity with Recommendation V.14 to a synchronous data stream suitable for transmission in accordance with § 4.1.1.

4.2 *Receiver*

4.2.1 In the synchronous modes of operation, the modem shall give synchronous data to the DTE on circuit 104 under control of circuit 115.

4.2.2 In the start-stop modes, demodulated synchronous data shall be passed to the converter in confirmity with Recommendation V.14 for regaining the data stream of start-stop characters.

The intracharacter signalling rate provided to the DTE over circuit 104 shall be in the ranges given in Table 6/V.26 *ter* when operating in the basic or in the extended signalling rate ranges, respectively.

TABLE 6/V.26 *ter*

Intracharacter signalling rate range

Data rate	Signalling rate range	
	Basic	Extended
2400 bit/s 1200 bit/s	2400 to 2424 bit/s 1200 to 1212 bit/s	2400 to 2455 bit/s 1200 to 1227 bit/s

5 Scrambler and descrambler

Each transmission direction uses a different scrambler. The way to allocate the scramblers/descramblers is described in § 6.1.1.

A self-synchronizing scrambler/descrambler shall be included in the modem. According to the direction of transmission (see § 6.1) the generating polynominal is: GPC = $1 + x^{-18} + x^{-23}$ or GPA = $1 + x^{-5} + x^{-23}$.

At the transmitter the scrambler shall effectively divide the message polynomial (of which the input data sequence represents the coefficients in descending order) by the scrambler generating polynomial to generate the transmitted sequence; at the receiver the received polynomial (of which the received data sequence represents the coefficient in descending order) shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix I.

6 Operating sequence

6.1 *Scrambler/descrambler allocation and signalling rate selection*

6.1.1 *General switched telephone network (GSTN)*

On the general switched telephone network the modem at the calling data station shall use the scrambler with the GPC generating polynomial and the descrambler with the GPA generating polynomial (call mode). The modem at the answering data station shall use the scrambler with the GPA generating polynomial and the descrambler with the GPC generating polynomial (answer mode).

In some situations, however, for example, when calls are established on the GSTN by operators, bilateral agreement on call mode/answer mode allocation will be necessary.

The calling and answering modems automatically condition themselves to operate at the correct data signalling rate by exchanging rate patterns at the bit rate of 1200 bit/s during the operating sequences, as defined in § 6.3.1.

6.1.2 *Point-to-point leased circuits*

Scrambler/descrambler allocation, data signalling rate selection and call mode and answer mode designation on point-to-point leased circuits will be by bilateral agreement between Administrations or users.

6.1.3 *Rate patterns*

The rate pattern is a scrambled sequence of a particular repeated octet transmitted 32 times.

Out of the possible 256 binary numbers, the 34 following hexadecimal numbers are selected:

01 – 03 – 05 – 07 – 09 – 0B – 0D – 0F – 11 – 13 – 15 – 17 – 19 – 1B – 1D – 1F – 25 – 27 – 2B – 2D – 2F – 33 – 35 – 37 – 3B – 3D – 3F – 55 – 57 – 5B – 5F – 6F – 77 – 7F

Each of the binary octets (numbers listed above) may be replaced by one of its rotations.

The transmission of an octet begins by the least significant bit.

Table 7/V.26 *ter* shows the relationship between an octet value and one or two bit rates (see Note 2 of the table) enabled in a modem.

TABLE 7/V.26 *ter*

Rate pattern octet coding

Octet (see Note 1)		Bit rate (bit/s)		
Hexadecimal	Binary	1200	2400	4800 (see Note 2)
	LSB			
01	0 0 0 0 0 0 0 1	X		
03	0 0 0 0 0 0 1 1		X	
05	0 0 0 0 0 1 0 1			X
07	0 0 0 0 0 1 1 1	X	X	
09	0 0 0 0 1 0 0 1		X	X

Note 1 – In the case of an interface according to Recommendation V.24, only two rates can be selected by circuits 111 and 112. A new kind of interface under study may enlarge the possibilities.

Note 2 – These octets assignments are provisional.

6.2 *V.25 automatic answering sequence*

The V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted on point-to-point leased circuits or on national connections on the GSTN, where permitted by the Administration.

6.3 *Operating protocol*

The means of achieving automatic bit rate selection, initial echo cancellation and synchronism between the call mode and the answer mode modems on international GSTN connections and leased lines are shown in Figure 1/V.26 *ter*.

The automatic bit rate selection, initial echo cancellation and synchronizing signals are based on a half-duplex procedure. After this procedure, both modems shall continue to operate adaptive echo cancellation during duplex data transmission.

The operating sequence is divided into three sub-sequences: A, B and C (see Note).

Sequence A is the answering sequence according to Recommendation V.25.

Sequence B is the data bit rate selection sequence operated at 1200 bit/s.

Sequence C is the echo cancelling sequence operated at the selected bit rate.

At the end of these three sequences, the modem is conditioned to transmit and receive data.

Note – Manufacturers should note that the impedance of the modems as seen by the telephone line should not be varied throughout the duration of the connection.

6.3.1 *Description*

6.3.1.1 *Sequence A (answering sequence)*

6.3.1.1.1 *Call mode modem*

a) On connection to line it shall condition the scrambler and the descrambler in accordance with § 6.1.1.

b) In accordance with Recommendation V.25, after the detection of the 2100 Hz tone and a silent period of 75 ± 20 ms, the modem shall apply an ON condition to circuit 107.

6.3.1.1.2 *Answer mode modem*

a) On connection to line it shall condition the scrambler and the descrambler in accordance with § 6.1.1.

b) In accordance with Recommendation V.25, the modem is silent during 2.15 ± 0.35 seconds, sends a 2100 ± 15 Hz tone for 3.3 ± 0.7 seconds, and then remains silent for 75 ± 20 ms.

c) In accordance with Recommendation V.25, after the silent period, it shall apply an ON condition to circuit 107.

6.3.1.2 *Sequence B (data bit rate selection sequence)*

The call and the answer mode modems are conditioned to transmit and receive at 1200 bit/s in a half-duplex mode.

6.3.1.2.1 *Call mode modem*

a) The modem waits until it detects at least 4 consecutive error free octets of the rate pattern (see Note 1).

The calling modem selects the maximum rate compatible with the answering modem or the maximum rate it can transmit.

b) Then, it remains silent during 250 ± 5 ms.

c) After that it transmits the synchronization sequence followed by 256 bits of a rate pattern corresponding to the selected bit rate in accordance with § 6.1.3.

d) Then, it applies the appropriate condition to circuit 112 (if used).

6.3.1.2.2 *Answer mode modem*

a) The modem transmits the receiver synchronization signals defined in § 2.7 followed by 256 bits of the rate pattern which indicates the set of rates available for the answering modem in accordance with § 6.2.

b) The modem remains silent until it detects at least 4 consecutive error-free octets of a rate pattern.

If a rate pattern is not detected within 2 seconds following the end of the rate pattern transmitted by the answering modem, it shall resume the operating sequence at the beginning of sequence B.

If the rate pattern indicates a rate not available, the modem shall disconnect from the line.

If the rate pattern indicates a rate available, the modem applies the appropriate condition to circuit 112 (if used).

c) Then, it remains silent again during 250 ± 5 ms.

d) In accordance with Recommendation G.164, the modem transmits a 2100 ± 15 Hz tone for 500 ± 50 ms to disable echo suppressors, then remains silent for 75 ± 20 ms.

6.3.1.3 *Sequence C (echo cancelling procedure)*

The call and the answer mode modems are conditioned to transmit, to receive and to cancel the echo at the selected data bit rate.

6.3.1.3.1 *Call mode modem*

a) The modem remains silent until 64 consecutive received scrambled binary 0s are detected. The modem shall then transmit the echo cancellation sequence (see Notes 2 and 3) until a sufficient degree of echo cancellation is available locally.

b) At the end of this sequence the modem shall be silent during 25 ± 3 ms and then transmit the receiver synchronization signals followed by scrambled binary 0s.

c) After detection of scrambled binary 0s, refinement of echo cancellation and detection of consecutive received scrambled binary 0s (Note 4) during a period of 64 bits, the calling modem shall apply the ON condition to circuit 109 and transmit scrambled binary 1s during a fixed period of 128 bits.

d) Then, the circuit 106 is enabled to respond to the condition of circuit 105 (see Notes 5 and 6).

6.3.1.3.2 *Answer mode modem*

a) The modem transmits the echo cancellation sequence (see Note 2) until a sufficient degree of echo cancellation is available locally (see Note 3).

b) After this sequence, the modem is silent during 25 ± 3 ms and then transmits the receiver synchronization signals followed by scrambled binary 0s.

c) After detection of a signal transmitted by the calling modem during a period of 50 ± 5 ms, the answering modem remains silent.

d) After detection of 64 consecutive received scrambled binary 0s, the modem transmits the receiver synchronization signals followed by scrambled binary 0s.

e) After refinement of echo cancellation and the detection of a further 64 consecutive scrambled binary 0s whilst operating in duplex mode, the modem transmits scrambled binary 1s.

f) After detection of 64 consecutive received scrambled binary 1s the modem applies an ON condition on circuit 109 and enables circui 106 to respond to the condition of circuit 105 (see Notes 5 and 6).

Note 1 – If 4 consecutive error-free octets of the rate pattern are not detected the modem remains silent.

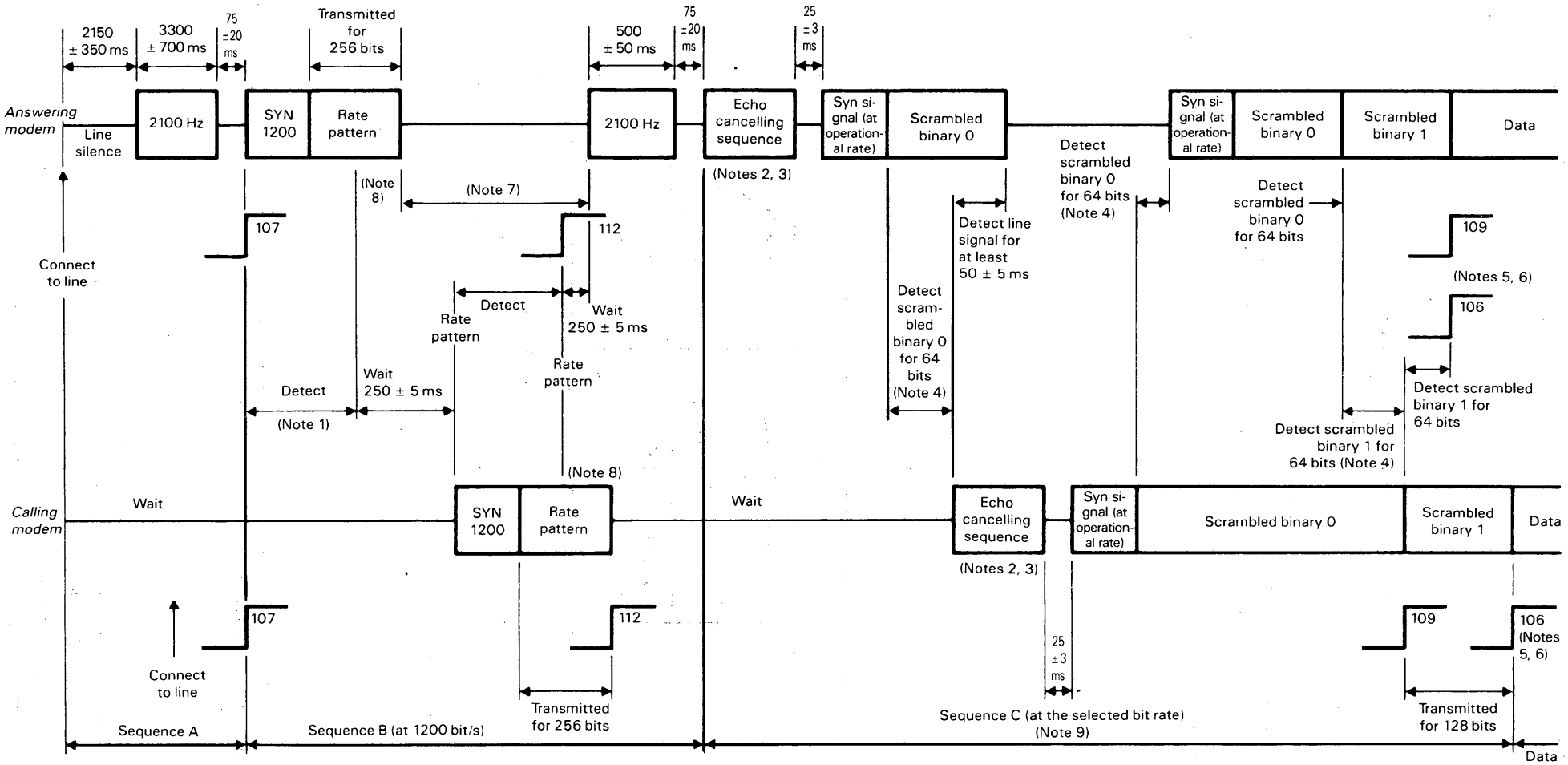
Note 2 – The echo cancellation sequence must not contain more than 32 consecutive unscrambled or scrambled binary 0s.

Note 3 – Manufacturers are cautioned that the time duration of the echo cancellation sequence has to be at least 650 ms when operating with network echo cancellers in accordance with Recommendation G.165.

Note 4 – The detection of scrambled binary 1s or 0s should start only after the receiver synchronization signals are completed.

Note 5 – When circuit 106 is in the OFF condition, circuit 103 shall be changed to the binary 1 condition.

Note 6 – Users may wish to note that if in the DTE a time-out exists between the ON conditions of circuit 107 and circuit 106, this time-out shall be greater than 15 seconds.



Notes 1 to 6 - See Notes 1 to 6 of § 6.3.

Note 7 - If 4 consecutive octets of rate pattern are not detected within 2 seconds, the modem resumes sequence B.

Note 8 - Rate pattern is defined in § 6.1.3.

Note 9 - Sequence C is defined for operation at 2400 bit/s and 1200 bit/s and is under study for the higher bit rate of 4800 bit/s.

FIGURE 1/V.26 *ter*

Operating sequences

7 Half-duplex mode of operation

This mode of operation is optional.

7.1 *Synchronizing signals*

The synchronizing signals for both data signalling rates are divided into segments.

7.1.1 *Segment 1*

The composition of segment 1 is continuous 180° phase reversals for 32 symbol intervals without protection against talker echo or for 256 symbol intervals with protection against talker echo.

7.1.2 *Segment 2*

As defined in § 2.7.2.

7.2 *Response times of circuits 106 and 109*

See Table 8/V.26 *ter*.

TABLE 8/V.26 *ter*

Response times				
Circuit 106	With protection against talker echo		Without protection against talker echo	
	2400 bit/s	1200 bit/s	2400 bit/s	1200 bit/s
OFF to ON	240 ± 10 ms	267 ± 10 ms	55 ± 2 ms	82 ± 2 ms
ON to OFF	⩽ 2 ms			
Circuit 109 OFF to ON	See § 7.2.1			
ON to OFF	5 to 15 ms			

7.2.1 *Circuit 109*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104. Circuit 109 is prevented from turning ON during reception of unmodulated carrier when the optional protection against talker echo is used.

7.2.2 *Circuit 106*

Circuit 106 response times are from the connection of an ON or OFF condition on:

- circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106; or
- circuit 107 (where circuit 105 is already ON) to the appearance of the corresponding ON or OFF condition on circuit 106 as defined in the operating sequence in § 7.4.

7.3 *Clamping of circuits 104 and 109*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations.

7.4 *Operating sequence*

The means of achieving automatic bit rate selection, and synchronism between the call mode and the answer mode modems on international GSTN connections and leased lines are shown in Figure 2/V.26 *ter.*

The operating sequence is divided in two sequences, A and B_1.

The sequence A is the answering sequence according to Recommendation V.25 defined in § 6.3.1.1 above.

The sequence B_1 is the data bit rate selection sequence operated at 1200 bit/s.

At the end of these two sequences, the modem may now transmit or receive data.

7.4.1 *Description of sequence B_1*

During the sequence B_1 circuits 106 and 109 are clamped to the OFF condition.

The call and the answer mode modems are conditioned to transmit and receive at 1200 bit/s in a half-duplex mode.

7.4.1.1 *Call mode modems*

a) The modem waits until it detects at least 4 consecutive error-free octets of the rate pattern (see Note 1, Figure 2/V.26 *ter*). The calling modem selects the maximum rate compatible with the answering modem or the maximum rate it can transmit.

b) Then, it remains silent during 250 ± 5 ms.

c) After that it transmits the synchronization sequence defined in § 7.1 followed by 256 bits of a rate pattern corresponding to the selected bit rate in accordance with § 6.1.3 (see Note 1, Figure 2/V.26 *ter*).

d) Then, it applies the appropriate condition to circuit 112 (if used).

e) The modem remains silent during 250 ± 5 ms, and then it enables circuit 106 to respond to circuit 105 and circuit 109 to operate as defined in § 7.2.1.

7.4.1.2 *Answer mode modem*

a) The modem transmits the receiver synchronization signals defined in § 7.1 followed by 256 bit of the rate pattern which indicates the set of rates available for the answering modem in accordance with § 6.1.3.

b) The modem remains silent until it detects at least 4 consecutive error-free octets of a rate pattern.

If a rate pattern is not detected within 2 seconds following the end of the rate pattern transmitted by the answering modem, it shall resume the operating sequence at the beginning of sequence B_1.

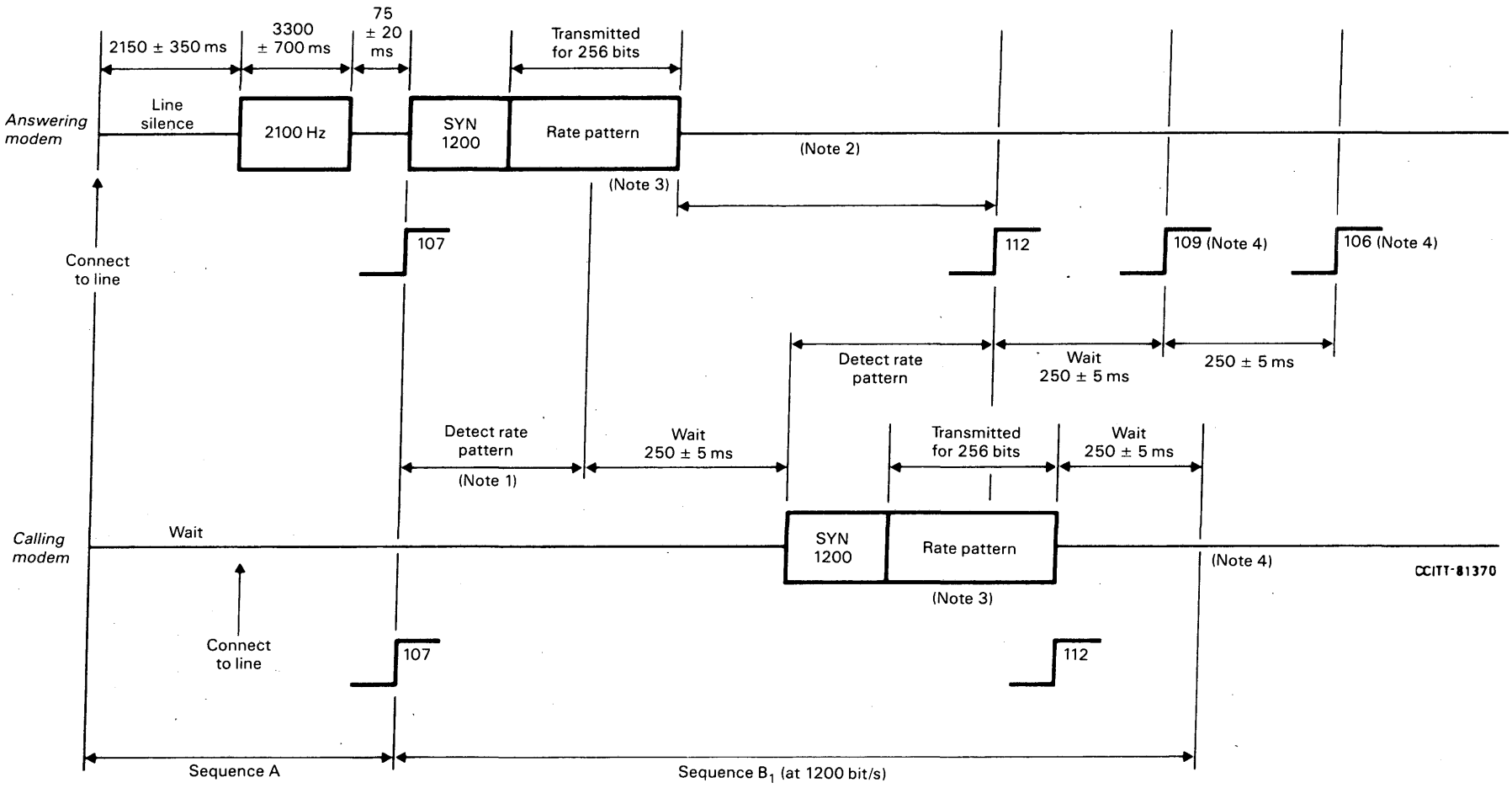
If the rate pattern indicates a rate not available, the modem shall disconnect from the line.

if the rate pattern indicates a rate available, the modem applies the appropriate condition to circuit 112 (if used).

c) Then, it remains silent again during 250 ± 5 ms.

d) After the silent period the modem enables circuit 109 to operate as defined in § 7.2.1.

e) The modem waits 250 ± 5 ms prior to enabling circuit 106 to respond to circuit 105.



Note 1 - If 4 consecutive error free octets of the rate pattern are not detected the modem remains silent.

Note 2 - If 4 consecutive error free octets of the rate pattern are not detected within 2 seconds the modem resumes sequence B_1.

Note 3 - Rate pattern is defined in § 6.1.2.

Note 4 - The condition of circuit 106 shall respond to circuit 105, and the circuit 109 shall operate as defined in § 7.2.1.

FIGURE 2/V.26 *ter*

Operating sequences in half-duplex mode

8 Testing facilities

Test loops 2 and 3 as defined in Recommendation V.54 shall be provided. Interface operation shall be as defined in Recommendation V.54.

8.1 *Remote loop 2*

Instigation and termination of remote loop 2 shall be in accordance with Recommendation V.54.

APPENDIX I

(to Recommendation V.26 *ter*)

Detailed scrambling and descrambling process

I.1 *Scrambling*

The message polynomial is divided by the generating polynomial GPC = $1 + x^{-18} + x^{-23}$ or GPA = $1 + x^{-5} + x^{-23}$ (see Figure I-1/V.26 *ter* and I-2/V.26 *ter* respectively), according to the transmission direction. The coefficients of the quotient of this division taken in descending order from the data sequence D_s to be transmitted. The expression of this sequence is:

$D_s = D_i \oplus D_s\, x^{-18} \oplus D_s\, x^{-23}$, when the generating polynomial GPC is used;

$D_s = D_i \oplus D_s\, x^{-5} \oplus D_s\, x^{-23}$, when GPA is used.

D_i is the data sequence applied to the scrambler.

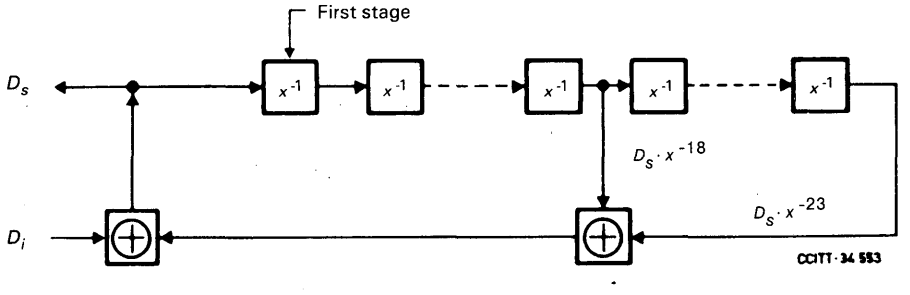


FIGURE I-1/V.26 *ter*

Scrambler with GPC generating polynomial

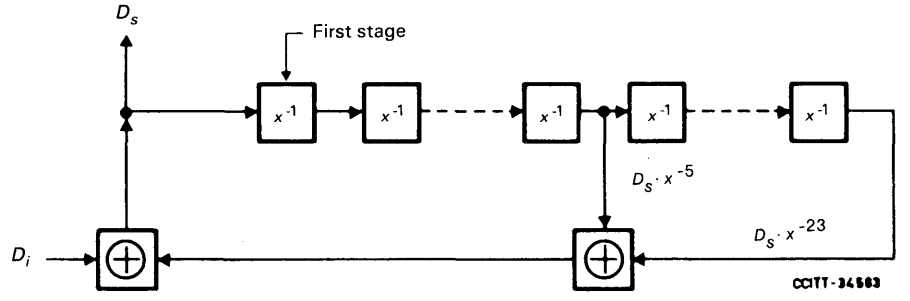


FIGURE I-2/V.26 *ter*

Scrambler with GPA generating polynomial

I.2 *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial GPC or GPA (see Figures I-3/V.26 *ter* and I-4/V.26 *ter* respectively) to form the recovered message polynomial. The coefficients of the recovered polynomial taken in descending order form the output data sequence D_o with the expression:

$$D_o = D_s (1 \oplus x^{-8} \oplus x^{-23})$$ for the GPC polynomial

or

$$D_o = D_s (1 \oplus x^{-5} \oplus x^{-23})$$ for the GPA polynomial.

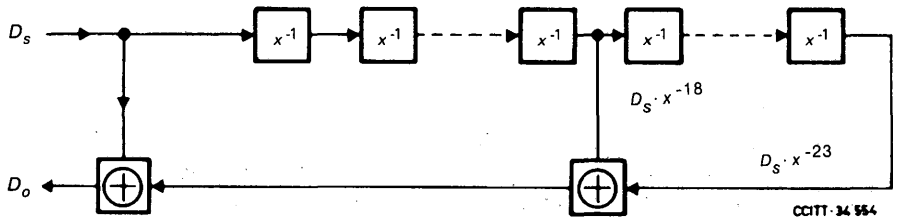


FIGURE I-3/V.26 *ter*

Descrambler with GPC polynomial

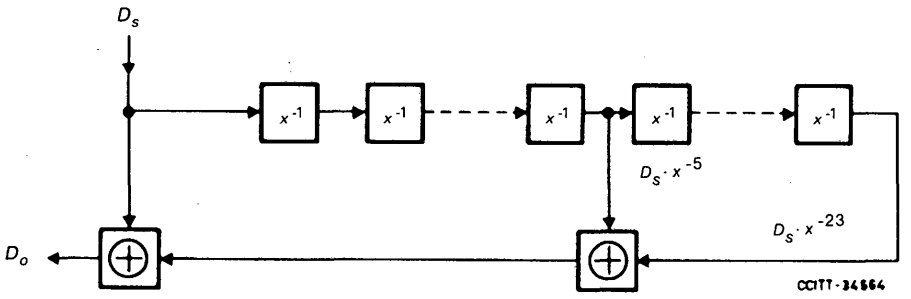


FIGURE I-4/V.26 *ter*

Descrambler with GPA polynomial

Note – The scrambler output patterns required to produce the synchronizing signal segment are as follows for both data rates:

GPC: 00 11 11 11 11 00 00 00 00 11 11 10 01 11 00 00 01 11 00
↑First bit

GPA: 00 11 11 11 11 00 00 00 00 11 11 10 01 11 00 11 11 10 00
↑First bit

Scrambler contents immediately preceding the output pattern above are as follows:

GPC: 10 01 11 11 11 11 11 11 00 00 01 1
↑

GPA: 01 10 00 00 11 10 00 00 11 10 00 0
First stage of scrambler ↑

4800 BITS PER SECOND MODEM WITH MANUAL EQUALIZER STANDARDIZED FOR USE ON LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1972; amended at Geneva, 1976 and 1980, Malaga-Torremolinos, 1984)

1 Introduction

This modem is intended to be used primarily on Recommendation M.1020 [1] circuits but this does not preclude the use of this modem over circuits of lower quality at the discretion of the Administration concerned.

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

The principal characteristics for this recommended modem for transmitting data at 4800 bits per second on leased circuits are as follows:

a) it is capable of operating in a full-duplex mode or half-duplex mode;

b) differential eight-phase modulation with synchronous mode of operation;

c) possibility of a backward (supervisory) channel at modulation rates up to 75 bauds in each direction of transmission, the use of these channels being optional;

d) inclusion of a manually adjustable equalizer.

2 Line signals

2.1 The carrier frequency is to be 1800 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Division of power between the forward and backward channels*

If simultaneous transmission of the forward and backward channels occurs in the same direction, a backward channel should be 6 dB lower in power level than the forward (data) channel.

2.3 The data stream to be transmitted is divided into groups of three consecutive bits (tribits). Each tribit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 1/V.27). At the receiver the tribits are decoded and the bits are reassembled in correct order. The left-hand digit of the tribit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

3 Data signalling and modulation rates

The data signalling rate shall be 4800 bits per second ± 0.01%, i.e. the modulation rate is 1600 bauds ± 0.01%.

4 Received signal frequency tolerance

The carrier frequency tolerance allowance at the transmitter is ± 1 Hz and assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

5 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc. to be as recommended for backward channel in Recommendation V.23. This does not preclude the use of a higher speed backward channel with operational capability of 75 bauds or higher, bearing the same characteristic frequencies as the V.23 backward channel.

6 Interchange circuits

6.1 *List of essential interchange circuits* (see Table 2/V.27)

TABLE 1/V.27

Tribit values			Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

TABLE 2/V.27

Interchange circuit		Forward (data) channel half-duplex of full-duplex (see Note 1)	
No.	Designation	Without backward channel	With backward channel
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105 (see Note 2)	Request to send	X	X
106	Ready for sending	X	X
107	Data set ready	X	X
108/1	Connect data set to line	X	X
109	Data channel received line signal detector	X	X
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
118	Transmitted backward channel data		X
119	Received backward channel data		X
120	Transmit backward channel line signal		X
121	Backward channel ready		X
122	Backward channel received line signal detector		X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics § 6.6).

Note 2 – No essential for 4-wire full-duplex continuous carrier operation.

6.2 *Threshold and response times of circuit 109*

A fall in level of the incoming line signal to −31 dBm or lower for more than 10 ± 5 ms will cause circuit 109 to be turned OFF. An increase in level to −26 ± 1 dBm or higher will turn this circuit ON after a delay of:

a) 13 ± 3 ms for fast operations,

b) 100 ms to 1200 ms for slow operation,

where the choice of the delay for slow operation depends upon the application. Delays within the range of b) may be provided for 4-wire full-duplex continuous carrier operation.

6.3 *Response time for circuit 106*

The time between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106 shall be optionally 20 ± 3 ms or 50 ± 20 ms.

6.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

6.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

6.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

6.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

6.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6.6 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114 and receiver signal element timing, circuit 115. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment and be transferred to the modem via circuit 113.

8 Synchronizing signal

During the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106, synchronizing signals for properly conditioning the receiving modem must be generated by the transmitting modem. These signals are defined as:

a) signals to establish basic demodulator requirements;

b) signals to establish scrambler synchronization.

The actual composition of the synchronization signals is continuous 180 degrees phase reversals on line for 9 ± 1 ms followed by continuous 1s at the input to the transmit scrambler for b). Condition b) shall be sustained until the OFF to ON transition of circuit 106.

9 Line signal characteristics

A 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter.

10 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial:

$$1 + x^{-6} + x^{-7}$$

with additional guards against repeating patterns of 1, 2, 3, 4, 6, 9 and 12 bits, shall be included in the modem. Appendix I shows a suitable logical arrangement.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial, to generate the transmitted sequence, and at the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix I.

11 Equalizer

A manually adjustable equalizer with the capability of compensating for the amplitude and group delay distortion within the limits of Recommendation M.1020 [1] shall be provided in the receiver. The transmitter shall be able to send an equalization pattern while the receiver shall incorporate a means of indicating correct adjustment of the equalizer controls. The equalizer pattern is generated by applying continuous 1s to the input of the transmitter scrambler defined above.

12 Alternative equalization and scrambler techniques

This Recommendation does not preclude the use of alternative equalization techniques, for example manually adjustable transmit equalizers for use in multipoint polled networks and for point-to-point networks with an unattended location.

These techniques, and their incorporation in the modem, and a new scrambler, should be the subject of further study.

Note – For modems with automatic adaptive equalizers, see Recommendation V.27 *bis*.

13 The following information is provided to assist equipment manufacturers:

- the data modem should have no adjustment for send level or receive sensitivity under the control of the operator;
- no fall-back rate has been included because the convenient rate would be 3200 bit/s, not a permitted rate;
- circuit 108/2 has not been included in the list of interchange circuits because it was considered that the modem would not be suitable for switched network use until an automatic equalizer had been recommended.

APPENDIX I

(to Recommendation V.27)

Detailed scrambling and descrambling processes

I.1 *Scrambling*

The message polynomial is divided by the generating polynomial $1 + x^{-6} + x^{-7}$. (See Figure I-1/V.27.) The coefficients of the quotient of this division are taken in descending order from the data sequence to be transmitted.

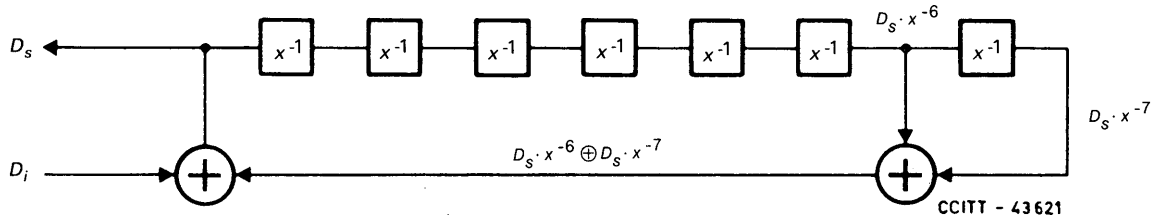
The transmitted bit sequence is continuously searched over a span of 45 bits for sequences of the form

$$p(x) = \sum_{i=0}^{32} a_i x^i$$

where

$a_i = 1$ or 0 and $a_i = a_{i+9}$ or a_{i+12}

If such a sequence occurs, the bit immediately following the sequence is inverted before transmission.



$D_s = D_i \oplus D_s x^{-6} \oplus D_s x^{-7}$

$D_i = D_s (1 \oplus x^{-6} \oplus x^{-7})$

FIGURE I-1/V.27

I.2 *Descrambling*

At the receiver the incoming bit sequence is continuously searched over a span of 45 bits for sequences of the form $p(x)$. If such a sequence occurs, the bit immediately following the sequence is inverted. The polynomial represented by the resultant sequence is then multiplied by the generating polynomial $1 + x^{-6} + x^{-7}$ to form the recovered message polynomial. The coefficients of the recovered polynomial, taken in descending order, form the output data sequence.

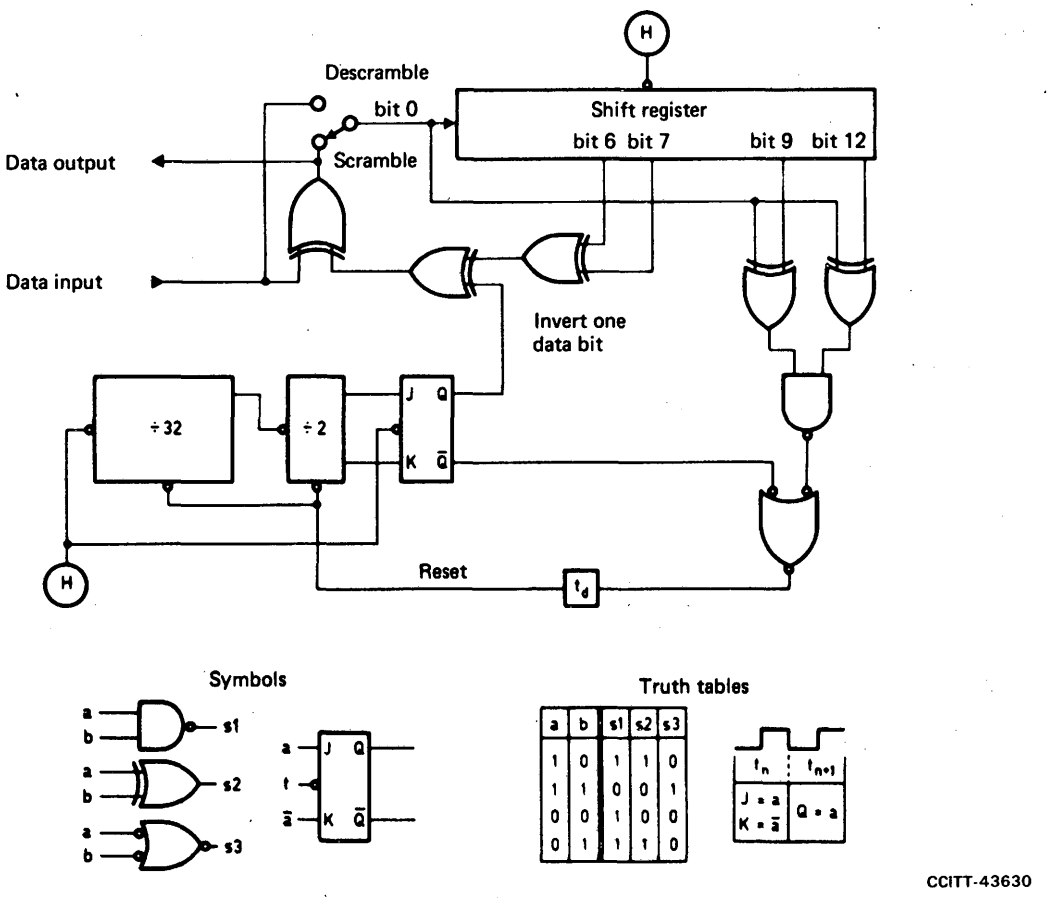
I.3 *Elements of scrambling process*

The factor $1 + x^{-6} + x^{-7}$ randomizes the transmitted data over a sequence length of 127 bits.

The equality $a_i = a_{i+9}$ in the guard polynomial $p(x)$ prevents repeated patterns of 1, 3 and 9 bits from occurring for more than 42 successive bits.

The equality $a_i = a_{i+12}$ in $p(x)$ prevents repeated patterns of 2, 4, 6 and 12 bits from occurring for more than 45 successive bits.

I.4 Figure I-2/V.27 is given as an indication only, since with another technique this logical arrangement might take another form.



Note 1 – Ⓗ represents the clock signal. The negative going transition is the active transition.

Note 2 – There is a delay time, due to physical circuits, between a negative going transition of Ⓗ and the end of the "0" state represented by *td* on the non-RESET wire; therefore the first coincidence between bit 0 and bit 9 or bit 12 is not taken into account by the counter.

Note 3 – The same voltage convention is used for data signals and logical circuits in the diagram.

FIGURE I-2/V.27

An example of scrambler and descrambler circuitry

Reference

[1] CCITT Recommendation *Characteristics of special quality international leased circuits, with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

4800/2400 BITS PER SECOND MODEM WITH AUTOMATIC EQUALIZER STANDARDIZED FOR USE ON LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

Introduction

This modem is intended to be used over any general leased circuits not necessarily conforming to Recommendation M.1020 [1]. A provision for a fast start-up sequence is made to allow the use of this modem for multipoint polling applications if the circuits used conform to Recommendation M.1020.

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems. This Recommendation does not eliminate the need for manually equalized modems according to Recommendation V.27 or application of other automatically equalized 4800 bits per second modems.

The provisions of this Recommendation are to be regarded as provisional in order to provide service where it is urgently required and between locations where it is expected that a reasonably satisfactory service can be given.

1 Principal characteristics

The principal characteristics for this recommended modem are very similar to the characteristics of a modem conforming to Recommendation V.27 with the exception of the equalizer used and these characteristics are as follows:

a) operates in a full-duplex or half-duplex mode over 4-wire leased circuits or in a half-duplex mode over 2-wire leased circuits;

b) at 4800 bits per second operation, modulation is 8-phase differentially encoded as described in Recommendation V.27;

c) reduced rate capability at 2400 bits per second with 4-phase differentially encoded modulation scheme as described in Recommendation V.26, Alternative A;

d) possibility of a backward (supervisory) channel at modulation rates up to 75 bauds in each direction of transmission, the provision and the use of these channels being optional;

e) inclusion of an automatic adaptive equalizer with a specific start-up sequence for Recommendation M.1020 [1] lines and an alternate start-up sequence for much lower grade lines.

2 Line signals at 4800 and 2400 bits per second operation

2.1 *Carrier frequency*

The carrier frequency is to be 1800 ± 1 Hz. No separate pilot tones are provided. The power levels used will conform to Recommendation V.2.

2.1.1 *Spectrum at 4800 bits per second*

A 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1000 Hz and 2600 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1000 Hz and 2600 Hz.

2.1.2 *Spectrum at 2400 bits per second*

A minimum of 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1200 Hz and 2400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1200 Hz and 2400 Hz.

2.2 *Division of power between the forward and backward channel*

If simultaneous transmission of the forward and backward channels occurs in the same direction, a backward channel should be 6 dB lower in power level than the forward (data) channel.

2.3 *Operation at 4800 bits per second*

2.3.1 *Data signalling and modulation rate*

The data signalling rate shall be 4800 bits per second ± 0.01%, i.e. the modulation rate is 1600 bauds ± 0.01%.

2.3.2 *Encoding data bits*

The data stream to be transmitted is divided into groups of three consecutive bits (tribits). Each tribit is encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.27 *bis*). At the receiver, the tribits are decoded and the bits are reassembled in correct order. The left-hand digit of the tribit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.27 *bis*

Tribit values			Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.4 *Operation at 2400 bits per second*

2.4.1 *Data signalling and modulation rate*

The data signalling rate shall be 2400 bits per second ± 0.01%, i.e. the modulation rate is 1200 bauds ± 0.01%.

2.4.2 *Encoding data bits*

At 2400 bits per second the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 2/V.27 *bis*). At the receiver, the dibits are decoded and reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 2/V.27 *bis*

Dibit values	Phase change (see Note)
00	0°
01	90°
11	180°
10	270°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5 *Operating sequences*

2.5.1 *Turn-ON sequence*

During the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106, synchronizing signals for proper conditioning of the receiving modem must be generated by the transmitting modem. These are signals to establish carrier detection, AGC if required, timing synchronization, equalizer convergence and descrambler synchronization.

Two sequences are defined, i.e.:

a) a short one for 4-wire circuits conforming to Recommendation M.1020 [1] operation,

b) a long one for 4-wire circuits which are much worse than Recommendation M.1020 [1] and for 2-wire circuits.

The sequences, for both data rates, are divided into three segments as in Table 3/V.27 *bis*.

TABLE 3/V.27 *bis*

	Segment 1	Segment 2	Segment 3	Total of Segments 1, 2 and 3	
Type of line signal	Continuous 180° phase reversals	0°-180° 2-phase equalizer conditioning pattern	Continuous scrambled ONEs	Total "**Turn**-ON" sequence time	
				4800 bit/s	2400 bit/s
Number of symbol intervals (SI) [a]	a) 14 SI b) 50 SI	a) 58 SI b) 1074 SI	8 SI	a) 50 ms b) 708 ms	a) 67 ms b) 943 ms

[a] SI = symbol intervals. The durations of Segments 1, 2 and 3 are expressed in number of symbol intervals, these numbers beign the same in fallback operation.

2.5.1.1 The composition of Segment 1 is continuous 180° phase reversals on line for 14 symbol intervals in the case of sequence a), for 50 symbol intervals in the case of sequence b).

2.5.1.2 Segment 2 is composed of an equalizer conditioning pattern which is derived from a pseudo-random sequence generated by the polynomial:

$$1 + x^{-6} + x^{-7}$$

2.5.1.2.1 For operation at 4800 bit/s the equalizer conditioning pattern is derived by using every third bit of the pseudo-random sequence defined in § 2.5.1.2. When the derived pattern contains a ZERO, 0° phase change is transmitted; when it contains a ONE, 180° phase change is transmitted. Segment 2 begins with 0°, 180°, 180°, 180°, 180°, 180°, 0°, ... according to the derived pattern and continues for 58 symbol intervals in the case of sequence a) and for 1074 symbol intervals in the case of sequence b). An example of the detailed sequence generation is described in Appendix I.

2.5.1.2.2 On leased circuits, considering that there exist modems which comply with § 2.5.1.2.1 at 4800 bit/s, but which differ in their "Turn-ON" sequences at 2400 bit/s, the following alternative equalizer conditioning patterns are defined:

i) In the first alternative, the equalizer conditioning pattern is identical to that defined in § 2.5.1.2.1.

ii) In the second alternative, the equalizer conditioning pattern is derived by using every second bit of the pseudo-random pattern defined in § 2.5.1.2. When the derived sequence contains a ZERO, 0° phase change is transmitted; when it contains a ONE, 180° phase change is transmitted. Segment 2 begins with 0°, 180°, 0°, 180°, 180°, 0°, 180°, ... according to the derived pattern and continues for 58 symbol intervals in the case of sequence a) and for 1074 symbol intervals in the case of sequence b).

2.5.1.3 Segment 3 commences transmission according to the encoding described in §§ 2.3 and 2.4 above with continuous data ONEs applied to the input of the data scrambler. Segment 3 is 8 symbol intervals. At the end of Segment 3, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

2.5.1.4 The phase change sequences for Segments 2 and 3 for 4800 bit/s and 2400 bit/s are shown in Table 4/V.27 *bis*.

TABLE 4/V.27 *bis* [a]

Data speed		Segment 2	Segment 3
4800 bit/s	Phase change	0° 180° 180° 180° 180° 180° 0° . . . . . 180° 180° 0° 0°	270° 225° 315° 90° 45° 45° 180° 180°
	PRS [b]	011 101 101 100 100 101 001 . . . . . 110 100 010 001	100 110 101 010 000 000 111 111
2400 bit/s alternative i)	Phase change	0° 180° 180° 180° 180° 180° 0° . . . . . 180° 180° 0° 0°	270° 90° 270° 270° 270° 270° 0° 0°
	PRS [b]	011 101 101 100 100 101 001 . . . . . 110 100 010 001	10 01 10 10 10 10 00 00
2400 bit/s alternative ii)	Phase change	0° 180° 0° 180° 180° 0° 180° . .180° 0° 180° 180° 180° 0°	0° 90° 90° 180° 270° 0° 180° 270°
	PRS [b]	01 11 01 10 11 00 10 . . .10 00 10 10 11 00	00 01 01 11 10 00 11 10
	Duration	⟵ 58 or 1074 symbol intervals ⟶ (Beginning and ending PRS and symbol sequences are the same for both durations)	⟵ 8 symbol intervals ⟶

[a] For a description of how the alternative sequences for Segments 2 and 3 may be generated, refer to the Note at the end of Appendix I.

[b] PRS is the pseudo-random sequence defined in § 2.5.1.2. The underlined bits determine the phase changes.

2.5.2 *Turn-OFF sequence*

The line signal emitted after the ON to OFF transition of circuit 105 is divided into two segments as shown in Table 5/V.27 *bis*.

TABLE 5/V.27 *bis*

	Segment A	Segment B	Total of Segments A and B
Type of line signal	Remaining data followed by continuous scrambled ONEs	No transmitted energy	Total "Turn-OFF" time
Duration	5 to 10 ms	20 ms	25 to 30 ms

If an OFF to ON transition of circuit 105 occurs during the Turn-OFF sequence, it will not be taken into account until the end of the Turn-OFF sequence.

In addition, in the case of half-duplex operation on two wires, if circuit 105 goes ON during the reception of the Segment A of the Turn-OFF sequence, optionally the transmission of the Turn-ON sequence shall be started within a time period of less than 20 ms after the end of reception of Segment A.

3 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance of the transmitter is ± 1 Hz and assuming a maximum drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

4 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc. to be as recommended for the backward channel in Recommendation V.23. This does not preclude the use of a higher speed backward channel with operational capability of 75 bauds or higher, bearing the same characteristic frequencies as the V.23 backward channel.

5 Interchange circuits

5.1 *List of essential interchange circuits* (Table 6/V.27 *bis*)

5.2 *Response times of circuits 106, 109, 121 and 122* (Table 7/V.27 *bis*)

5.2.1 *Circuit 109*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104.

5.2.2 *Circuit 106*

Circuit 106 response times are from the connection of an ON or OFF condition on circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106.

TABLE 6/V.27 *bis*

Interchange circuit		Forward (data) channel half-duplex or full-duplex (see Note)	
No.	Designation	Without backward channel	With backward channel
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105	Request to send	X	X
106	Ready for sending	X	X
107	Data set ready	X	X
108/1	Connect data set to line	X	X
109	Data channel received line signal detector	X	X
111	Data signal rate selector (DTE source)	X	X
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
118	Transmitted backward channel data		X
119	Received backward channel data		X
120	Transmit backward channel line signal		X
121	Backward channel ready		X
122	Backward channel received line signal detector		X

Note – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

TABLE 7/V.27 *bis*

Response times

Circuit 106	4800 bits per second	2400 bits per second
OFF to ON	a) 25 ms b) 708 ms	a) 67 ms b) 944 ms
ON to OFF	⩽ 2 ms	
Circuit 109 OFF to ON	See § 5.2.1	
ON to OFF	5 to 15 ms	
Circuit 121 OFF to ON	80 to 160 ms	
ON to OFF	⩽ 2 ms	
Circuit 122 OFF to ON	< 80 ms	
ON to OFF	15 to 80 ms	

Note – a) and b) refer to sequence a) and sequence b) as defined in § 2.5.1.

5.3 *Threshold of data channel and backward channel received line signal detectors*

Levels of received line signal at receiver line terminals:

– *For use over ordinary quality leased circuits* (ref. Recommendation M.1040 [2])

Threshold for circuits 109/122:

– greater than −43 dBm: OFF to ON
– less than −48 dBm: ON to OFF

– *For use over special quality leased circuits* (ref. Recommendation M.1020 [1])

Threshold for circuit 109:

– greater than −26 dBm: OFF to ON
– less than −31 dBm: ON to OFF

Threshold for circuit 122:

– greater than −34 dBm: OFF to ON
– less than −39 dBm: ON to OFF

The condition of circuits 109 and 122 for levels between the above levels is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

5.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

5.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

5.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangement

Clocks should be included in the modem to provide the data terminal equipment with transmitter element timing, circuit 114 and receiver signal element timing, circuit 115. The transmitter element timing may be originated in the data terminal equipment and be transferred to the modem via circuit 113.

8 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial:

$$1 + x^{-6} + x^{-7}$$

with additional guards against repeating patterns of 1, 2, 3, 4, 6, 8, 9 and 12 bits, shall be included in this modem. In Appendix I, Figure I-2/V.27 *bis* shows a suitable logical arrangement (see Note). The scrambler/descrambler is the same as that in Recommendation V.27 with the addition of circuitry to guard against repeating patterns of 8 bits.

Note – Figures I-1/V.27 *bis* and I-2/V.27 *bis* in Appendix I are given as an indication only, since with another technique these logical arrangements might take another form.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence, and at the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

9 Equalizer

An automatic adaptive equalizer shall be provided in the receiver. The receiver shall incorporate a means of detecting loss of equalization and be able to recover equalization from the normal data-modulated received line signal without initiating a new synchronizing signal from the distant transmitter.

10 Options

Since this modem is equipped with an automatic adaptive equalizer, and can operate on 2-wire lines, operation over the general switched network is possible. Thus, in the event of failure of the leased line, the general switched network may serve as a stand-by facility.

Options can be added to this modem in order to allow the use of the general switched network when the leased line fails. These options can also be added for use on 2-wire leased lines where echo protection is required.

Additional information for these options can be found in Recommendation V.27 *ter*.

11

The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

At 4800 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1100 Hz to 2500 Hz.

At 2400 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1300 Hz to 2300 Hz.

APPENDIX I

(to Recommendation V.27 *bis*)

A two phase equalizer training generator for 4800 bit/s

Rapid convergence for the equalizer with the least amount of circuitry is more readily accomplished by sending only an in-phase or out-of-phase carrier during training. This implies that the only tribits sent to the modulator will be 001 (0° phase) or 111 (180° phase). Refer to Figure I-1/V.27 *bis* for circuitry to generate the sequence and Figure I-3/V.27 *bis* for timing the sequence.

Let T1 be a timing signal equal to 1600 Hz (symbol clock), that is true (high) for one 4800-Hz period, and low for two 4800-Hz clock periods. T2 is the inversion of T1.

During T1 select the input to the scrambler, during T2 select the first stage of the scrambler. During the period when T2 is high, C forces the output high. This may be accomplished by circuitry shown in Figure I-2/V.27 *bis*.

If T1 is forced continually high and T2 is forced continually low, normal operation is restored.

In order to ensure consistent training, the same pattern should always be sent. To accomplish this, the data input to the scrambler should be in mark hold during the training, and the first seven stages of the scrambler should be loaded with 0011110 (right-hand-most first in time) on the first coincidence on T1 and the signal that will cause the mute should be removed from the transmitter output. [Generally this signal will be *Request To Send* (RTS)].

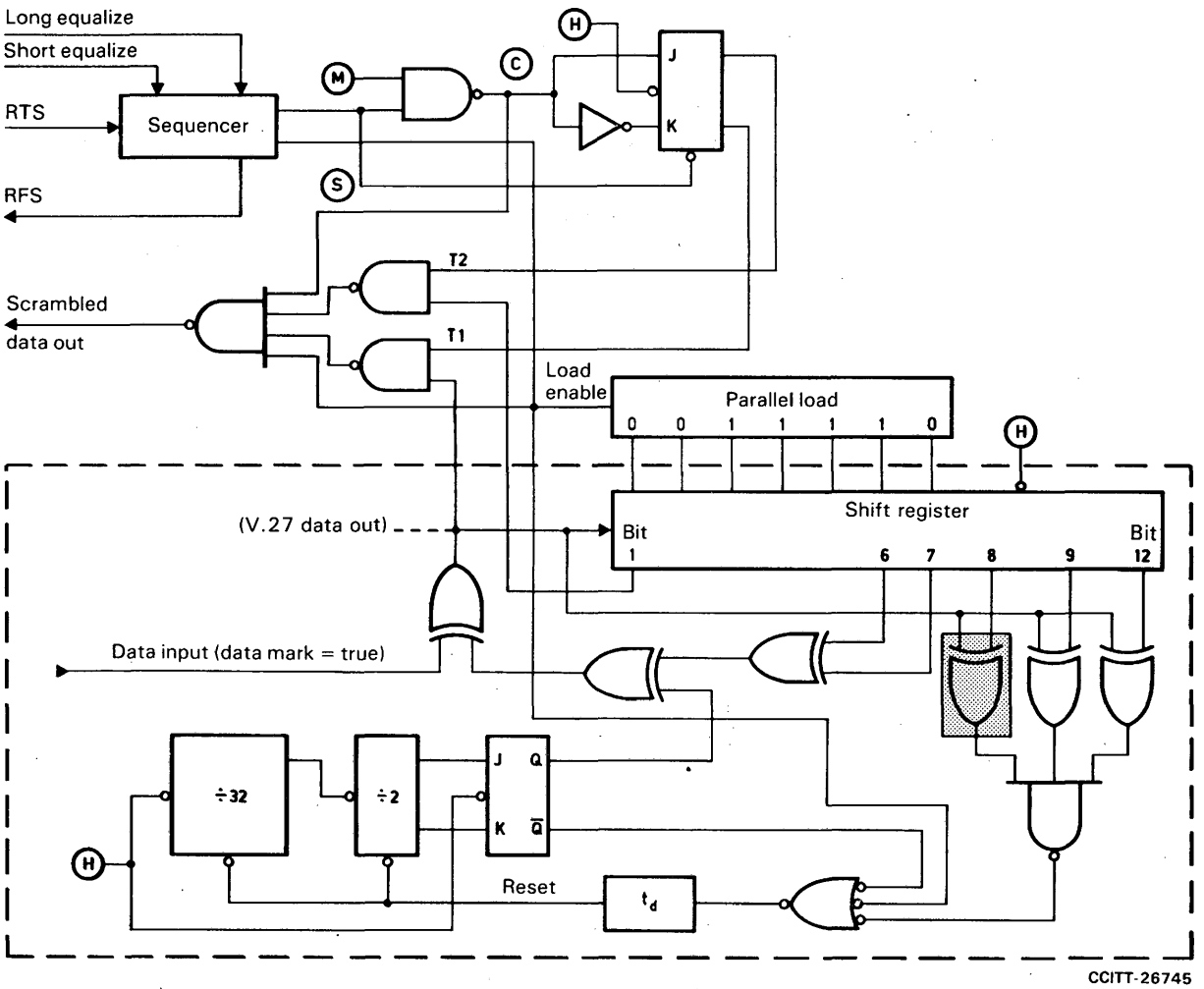
This particular starting point was chosen in order to ensure a pattern that has continuous 180° phase reversals at the beginning in order to ensure rapid clock acquisition, followed by a pattern that will ensure rapid equalizer convergence.

Within eight symbol intervals prior to the ON condition of *Ready For Sending* (RFS), the scrambler should be switched to normal operation, keeping the scrambler in mark hold until RFS, to synchronize the descrambler.

Note – At 2400 bits per second, a similar technique may be used with appropriate clocking changes, as shown in Table I-1/V.27 *bis*.

TABLE I-1/V.27 *bis*

		Segment 2	Segment 3
Clock Ⓗ	i)	3600 Hz	2400 Hz
	ii)	2400 Hz	2400 Hz
Clock Ⓜ	i)	1200 Hz	1200 Hz
	ii)	1200 Hz	1200 Hz



Note 1 – The dotted line encloses the V.27 scrambler.

Note 2 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 3 – Ⓗ is 3 times baud rate clock.

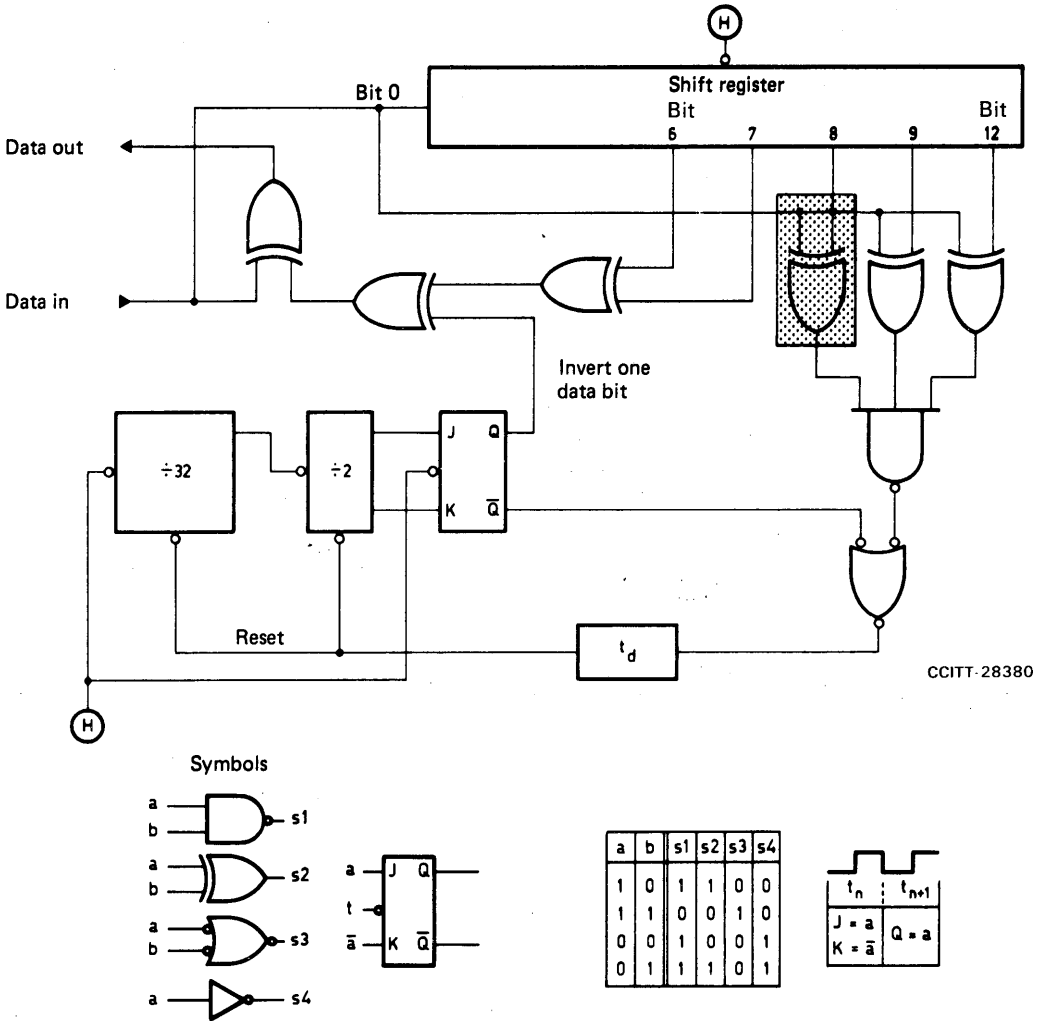
Note 4 – Ⓜ is baud rate clock (1600 Hz).

Note 5 – Diagrams shown with positive logic.

Note 6 – Signals Ⓒ and Ⓢ are identified only to correlate with Figure I-3/V.27 *bis*.

FIGURE I-1/V.27 *bis*

An example of sequence generator and scrambler circuitry for 4800 bit/s



Note 1 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 2 – (H) represents clock signal. The negative going transition is the active transition.

Note 3 – There is a delay time due to physical circuits between a negative going transition of (H) and the end of the "0" state represented by t_d on the non-reset wire; therefore the first coincidence between bit 0 and bit 8 or bit 9 or bit 12 is not taken into account by the counter.

FIGURE I-2/V.27 *bis*

An example of descrambler circuitry

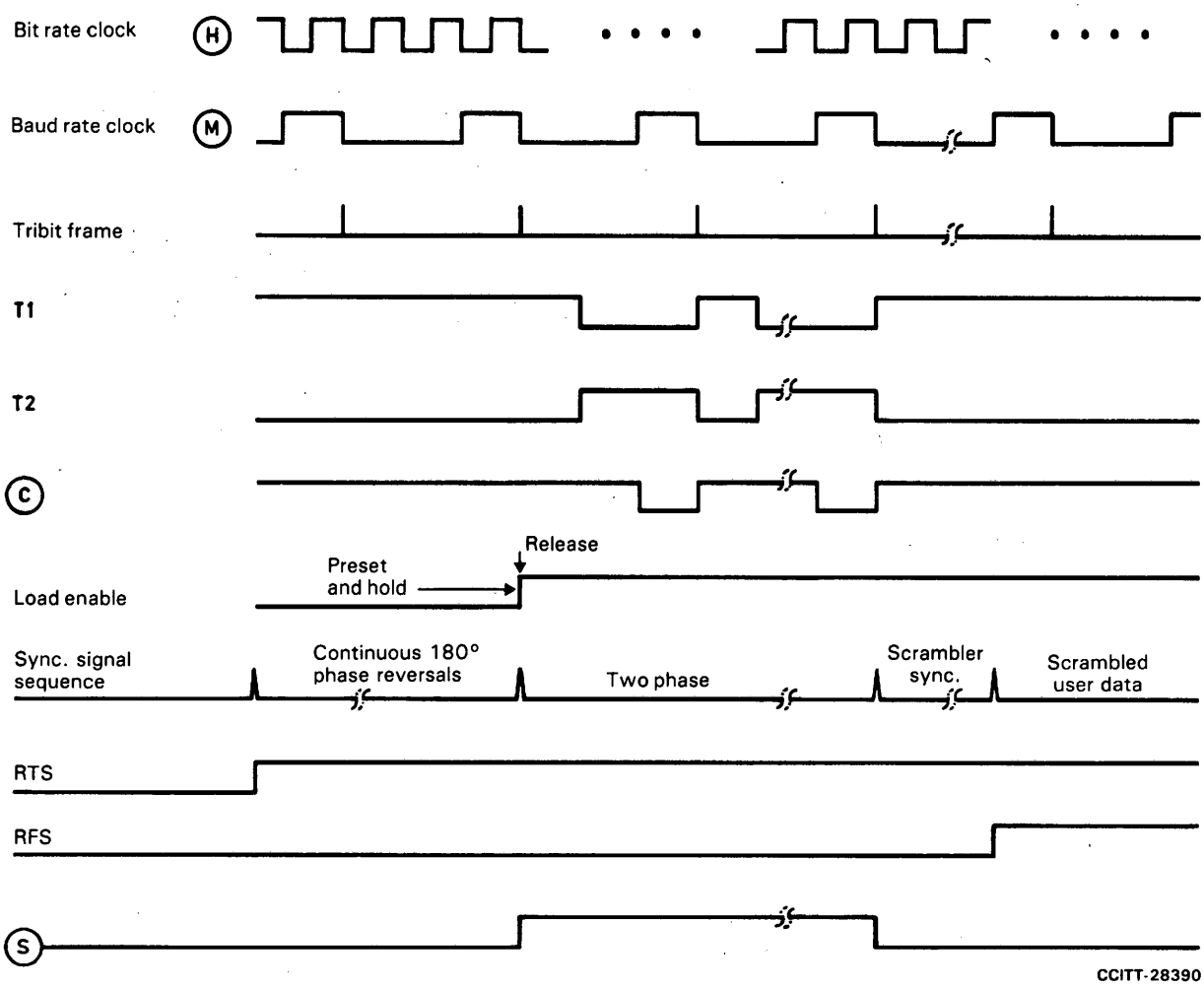


FIGURE I-3/V.27*bis*

Synchronizing signal sequence for 4800 bit/s (see Figure I-1/V.27*bis*)

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of ordinary quality international leased circuits*, Vol. IV, Rec. M.1040.

4800/2400 BITS PER SECOND MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that there is a demand for data transmission at 4800 bits per second over the general switched telephone network;

(b) that a majority of connections over the general switched telephone network within some countries are capable of carrying data at 4800 bits per second;

(c) that a lower proportion of international connections in the general switched telephone network are capable of carrying data at 4800 bits per second;

(d) that other international connections in the general switched telephone network may still support operations at 2400 bits per second using a built-in fallback capability;

unanimously declares the view

that transmission at 4800 bits per second should be allowed on the general switched telephone network. Reliable transmission cannot be guaranteed on every connection or routing and tests should be made between the most probable terminal points before a service is provided. The CCITT expects that developments during the next few years in modern technology will bring about modems of more advanced design enabling reliable transmission to be given on a much higher proportion of connections. The provisions of this Recommendation are to be regarded as provisional in order to provide service where it is urgently required and between locations where it is expected that a reasonably satisfactory service can be given;

that the characteristics of the modem for transmission at 4800 bits per second over the general switched telephone network shall provisionally be the following:

1 Principal characteristics

a) Use of data signalling rate of 4800 bits per second with 8-phase differentially encoded modulation as described in Recommendation V.27.

b) Reduced rate capability at 2400 bits per second with 4-phase differentially encoded modulation as described in Recommendation V.26, Alternative A.

c) Provision for a backward channel at modulation rates up to 75 bauds, use of this channel being optional.

d) Inclusion of an automatic adaptive equalizer.

2 Line signals at 4800 and 2400 bits per second operation

2.1 *Carrier frequency*

The carrier frequency is to be 1800 ± 1 Hz. No separate pilot tones are provided. The power levels used will conform to Recommendation V.2.

2.1.1 *Spectrum at 4800 bits per second*

The 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1000 Hz and 2600 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1000 Hz and 2600 Hz.

2.1.2 *Spectrum at 2400 bits per second*

A minimum of 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1200 Hz and 2400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1200 Hz and 2400 Hz.

2.2 *Division of power between the forward and backward channel*

Equal division between the forward and backward channels is recommended (if provided).

2.3 *Operation at 4800 bits per second*

2.3.1 *Data signalling and modulation rate*

The data signalling rate shall be 4800 bits per second ± 0.01%, i.e. the modulation rate is 1600 bauds ± 0.01%.

2.3.2 *Encoding data bits*

The data stream to be transmitted is divided into groups of three consecutive bits (tribits). Each tribit is encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.27 *ter*). At the receiver, the tribits are decoded and the bits are reassembled in correct order. The left-hand digit of the tribit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.27 *ter*

Tribit values			Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.4 *Operation at 2400 bits per second*

2.4.1 *Data signalling and modulation rate*

The data signalling rate shall be 2400 bits per second ± 0.01% i.e. the modulation rate is 1200 bauds ± 0.01%.

2.4.2 *Encoding data bits*

At 2400 bits per second the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 2/V.27 *ter*). At the receiver, the dibits are decoded and the bits are reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 2/V.27 *ter*

Dibit values	Phase change (see Note)
00	0°
01	90°
11	180°
10	270°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5 *Operating sequences*

2.5.1 *Turn-ON sequence*

During the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106, synchronizing signals for proper conditioning of the receiving modem must be generated by the transmitting modem. These are signals to establish carrier detect, AGC if required, timing synchronization, equalizer convergence and descrambler synchronization.

The synchronizing signals are defined in two separate sequences with the long sequence used once at the beginning of the established connection and the short sequence used for subsequent turn-around in which the equalizer training pattern is used to update and refine equalizer convergence.

Two sequences are defined, i.e.:

a) a short one for turn-around operation,

b) a longer one for initial establishment of connection.

The sequence b) is only used after the first OFF to ON transition of circuit 105 following the OFF to ON transition of circuit 107, or at the OFF to ON transition of circuit 107 if the circuit 105 is already ON. After every subsequent OFF to ON transition of circuit 105, the sequence a) is used.

The sequences, for both data rates, are divided into five segments as in Table 3/V.27 *ter*.

2.5.1.1 The composition of Segment 3 is continuous 180° phase reversals on line for 14 symbol intervals in the case of sequence a), for 50 symbol intervals in the case of sequence b).

2.5.1.2 Segment 4 is composed of an equalizer conditioning pattern which is derived from a pseudo-random sequence generated by the polynomial:

$$1 + x^{-6} + x^{-7}$$

For operation at both 4800 bit/s and 2400 bit/s, the equalizer conditioning pattern is derived by using every third bit of the pseudo-random sequence defined by the polynomial. When the derived pattern contains a ZERO, 0° phase change is transmitted; when it contains a ONE, 180° phase change is transmitted. Segment 4 begins with 0°, 180°, 180°, 180°, 180°, 180°, 0°, ... according to the derived pattern and continues for 58 symbol intervals in the case of sequence a) and for 1074 symbol intervals in the case of sequence b). An example of the detailed sequence generation is described in Appendix I.

2.5.1.3 Segment 5 commences transmission according to the encoding described in §§ 2.3 and 2.4 above with continuous data ONEs applied to the input of the data scrambler. Segment 5 is 8 symbol intervals. At the end of Segment 5, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

2.5.1.4 The phase change sequences for Segments 4 and 5 for 4800 bit/s and 2400 bit/s are shown in Table 4/V.27 *ter*.

TABLE 3/V.27 *ter*

	Segment 1	Segment 2	Segment 3	Segment 4	Segment 5	Total of Segments 1, 2, 3, 4 and 5	
Type of line signal	Unmodulated carrier	No transmitted energy	Continuous 180° phase reversals	0°-180° 2-phase equalizer conditioning pattern	Continuous scrambled ONEs	Nominal total "**Turn**-ON" sequence time	
						4800 bit/s	2400 bit/s
Protection against talker echo	185 ms to 200 ms	20 ms to 25 ms	a) 14 SI b) 50 SI	a) 58 SI b) 1074 SI	8 SI	a) 265 ms b) 923 ms	a) 281 ms b) 1158 ms
Without any protection	0 ms	0 ms	a) 14 SI b) 50 SI	a) 58 SI b) 1074 SI	8 SI	a) 50 ms b) 708 ms	a) 66 ms b) 943 ms

SI = symbol intervals. The durations of Segments 3, 4 and 5 are expressed in number of symbol intervals, these numbers being the same in the fallback operation.

TABLE 4/V.27 *ter* [a]

Data speed		Segment 4	Segment 5
4800 bit/s	Phase change	0° 180° 180° 180° 180° 180° 0° . . . . . 180° 180° 0° 0°	270° 225° 315° 90° 45° 45° 180° 180°
	PRS [b]	011 101 101 100 100 101 001 . . . . . 110 100 010 001	100 110 101 010 000 000 111 111
2400 bit/s	Phase change	0° 180° 180° 180° 180° 180° 0° . . . . . 180° 180° 0° 0°	270° 90° 270° 270° 270° 270° 0° 0°
	PRS [b]	011 101 101 100 100 101 001 . . . . . 110 100 010 001	10 01 10 10 10 10 00 00
	Duration	⟵ 58 or 1074 symbol intervals ⟶ (Beginning and ending PRS and symbol sequences are the same for both lengths)	⟵ 8 symbol intervals ⟶

[a] For a description of how the alternative sequences for Segment 4 and 5 may be generated, refer to the Note at the end of Appendix I.

[b] PRS is the pseudo-random sequence defined in § 2.5.1.2. The underlined bits determine the phase changes.

2.5.2 *Turn-OFF sequence*

The line signal emitted after the ON to OFF transition of circuit 105 is divided into two segments as in Table 5/V.27 *ter.*

TABLE 5/V.27 *ter*

	Segment A	Segment B	Total Turn-OFF time
Type of line signals	Remaining data followed by continuous scrambled ONEs	No transmitted energy	Total of Segments A and B
With or without protection against talker echo	5 ms to 10 ms	20 ms	25 ms to 30 ms

If an OFF to ON transition of circuit 105 occurs during the Turn-OFF sequence, it will not be taken into account until the end of the Turn-OFF sequence.

In addition, if circuit 105 goes ON during the reception of the Segment A of the Turn-OFF sequence, optionally the transmission of the Turn-ON sequence shall be started within a time period of less than 20 ms after the end of reception of Segment A.

3 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance of the transmitter is ± 1 Hz and assuming a maximum drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

4 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc. to be as recommended for backward channel in Recommendation V.23. This does not preclude the use of a higher speed backward channel with operational capability of 75 bauds or higher, bearing the same characteristic frequencies as the V.23 backward channel.

5 Interchange circuits

5.1 *List of interchange circuits*

Interchange circuits essential for the modem when used on the general switched telephone network, including terminals equipped for manual calling or automatic calling or answering are as in Table 6/V.27 *ter.*

5.2 *Response times of circuits 106, 109, 121 and 122* (see Tables 7/V.27 *ter* and 8/V.27 *ter*)

5.2.1 *Circuit 109*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104. Circuit 109 is prevented from turning ON during reception of unmodulated carrier when the optional protection against talker echo is used.

TABLE 6/V.27 *ter*

Interchange circuit		Forward (data) channel one-way system (see Note 1)				Forward (data) channel either-way system (see Note 1)	
No.	Designation	Without backward channel		With backward channel		Without backward channel	With backward channel
		Transmit end	Receive end	Transmit end	Receive end		
102	Signal ground or common return	X	X	X	X	X	X
103	Transmitted data	X		X		X	X
104	Received data		X		X	X	X
105	Request to send	X		X		X	X
106	Ready for sending	X		X		X	X
107	Data set ready	X	X	X	X	X	X
108/1 or 108/2 (see Note 2)	Connect data set to line / Data terminal ready	X	X	X	X	X	X
109	Data channel received line signal detector		X		X	X	X
111	Data signalling rate selector (DTE source)	X	X	X	X	X	X
113	Transmitter signal element timing (DTE source)	X		X		X	X
114	Transmitter signal element timing (DCE source)	X		X		X	X
115	Receiver signal element timing (DCE source)		X		X	X	X
118	Transmitted backward channel data				X		X
119	Received backward channel data			X			X
120	Transmit backward channel line signal						X
121	Bakward channel ready				X		X
122	Backward channel received line signal detector			X			X
125	Calling indicator	X	X	X	X	X	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 – This circuit shall be capable of operation as circuit 108/1 – *connect data set to line* or ciruit 108/2 – *data terminal ready* depending on its use.

TABLE 7/V.27 *ter*

Response times for operation at 4800 bits per second		
Circuit 106	With protection against talker echo	Without protection against talker echo
OFF to ON	a) 215 ± 10 ms + 50 ms b) 215 ± 10 ms + 708 ms	a) 50 ms b) 708 ms
ON to OFF	⩽ 2 ms	⩽ 2 ms
Circuit 109		
OFF to ON	See § 5.2.1	See § 5.2.1
ON to OFF	5 to 15 ms	5 to 15 ms
Circuit 121		
OFF to ON	80 to 160 ms	80 to 160 ms
ON to OFF	⩽ 2 ms	⩽ 2 ms
Circuit 122		
OFF to ON	< 80 ms	< 80 ms
ON to OFF	15 to 80 ms	15 to 80 ms

TABLE 8/V.27 *ter*

Response times for operation of 2400 bits per second		
Circuit 106	With protection against talker echo	Without protection against talker echo
OFF to ON	a) 215 ± 10 ms + 67 ms b) 215 ± 10 ms + 944 ms	a) 67 ms b) 944 ms
ON to OFF	⩽ 2 ms	⩽ 2 ms
Circuit 109		
OFF to ON	See § 5.2.1	See § 5.2.1
ON to OFF	5 to 15 ms	5 to 15 ms

Note 1 – a) and b) refer to sequence a) and sequence b) as defined to § 2.5.1.

Note 2 – The parameter and procedures, particularly in the case of automatic calling and answering, are provisional and are the subject of further study.

5.2.2 *Circuit 106*

Circuit 106 response times are from the connection of an ON or OFF condition on:

- circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106; or,
- circuit 107 (where circuit 105 is already ON) to the appearance of the corresponding ON or OFF condition on circuit 106.

5.3 *Threshold of data channel and backward channel received line signal detectors*

Level of received line signal at the receive line terminals of the modem for all types of connections, i.e. the general switched telephone network or non-switched 2-wire leased telephone circuits:

- greater than −43 dBm: circuits 109/122 ON
- less than −48 dBm: circuits 109/122 OFF

The condition of circuits 109 and 122 for levels between −43 dBm and −48 dBm is not specified except that the signal detectors shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

Where transmission conditions are known and allowed, it may be desirable at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

5.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

5.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

5.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangement

Clocks should be included in the modem to provide the data terminal equipment with transmitter element timing, circuit 114 and receiver signal element timing, circuit 115. The transmitter element timing may be originated in the data terminal equipment and be transferred to the modem via circuit 113.

8 Equalizer

An automatic adaptive equalizer shall be provided in the receiver.

9 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial:

$$1 + x^{-6} + x^{-7}$$

with additional guards against repeating patterns of 1, 2, 3, 4, 6, 8, 9 and 12 bits, shall be included in this modem. Figure I-2/V.27 *ter* shows a suitable logical arrangement (see Note). The scrambler/descrambler is the same as that in Recommendation V.27 with the addition of circuitry to guard against repeating patterns of 8 bits.

Note – Figures I-1/V.27 *ter* and I-2/V.27 *ter* are given as an indication only, since with another technique these logical arrangements might take another form.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence, and at the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

10 When echo control device disabling is required, it is recommended that procedures specified in Recommendation V.25 be followed.

11 The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

At 4800 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1100 Hz to 2500 Hz.

At 2400 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1300 Hz to 2300 Hz.

APPENDIX I

(to Recommendation V.27 *ter*)

A two-phase equalizer training generator for 4800 bit/s

Rapid convergence for the equalizer with the least amount of circuitry is more readily accomplished by sending only an in-phase or out-of-phase carrier during training. This implies that the only tribits sent to the modulator will be 001 (0° phase) or 111 (180° phase). Refer to Figure I-1/V.27 *ter* for circuitry to generate the sequence and Figure I-3/V.27 *ter* for timing the sequence.

Let T1 be a timing signal equal to 1600 Hz (symbol clock), that is true (high) for one 4800-Hz period, and low for two 4800-Hz clock periods. T2 is the inversion of T1.

During T1, select the input to the scrambler, during T2 select the first stage of the scrambler. During the period when T2 is high, C forces the output high. This may be accomplished by circuitry shown in Figure I-2/V.27 *ter*.

If T1 is forced continually high and T2 is forced continually low, normal operation is restored.

In order to ensure consistent training, the same pattern should always be sent. To accomplish this, the data input to the scrambler should be in mark hold during the training, and the first seven stages of the scrambler should be loaded with 0011110 (right-hand-most first in time) on the first coincidence on T1 and the signal that will cause the mute should be removed from the transmitter output. [Generally this signal will be *Request To Send* (RTS).]

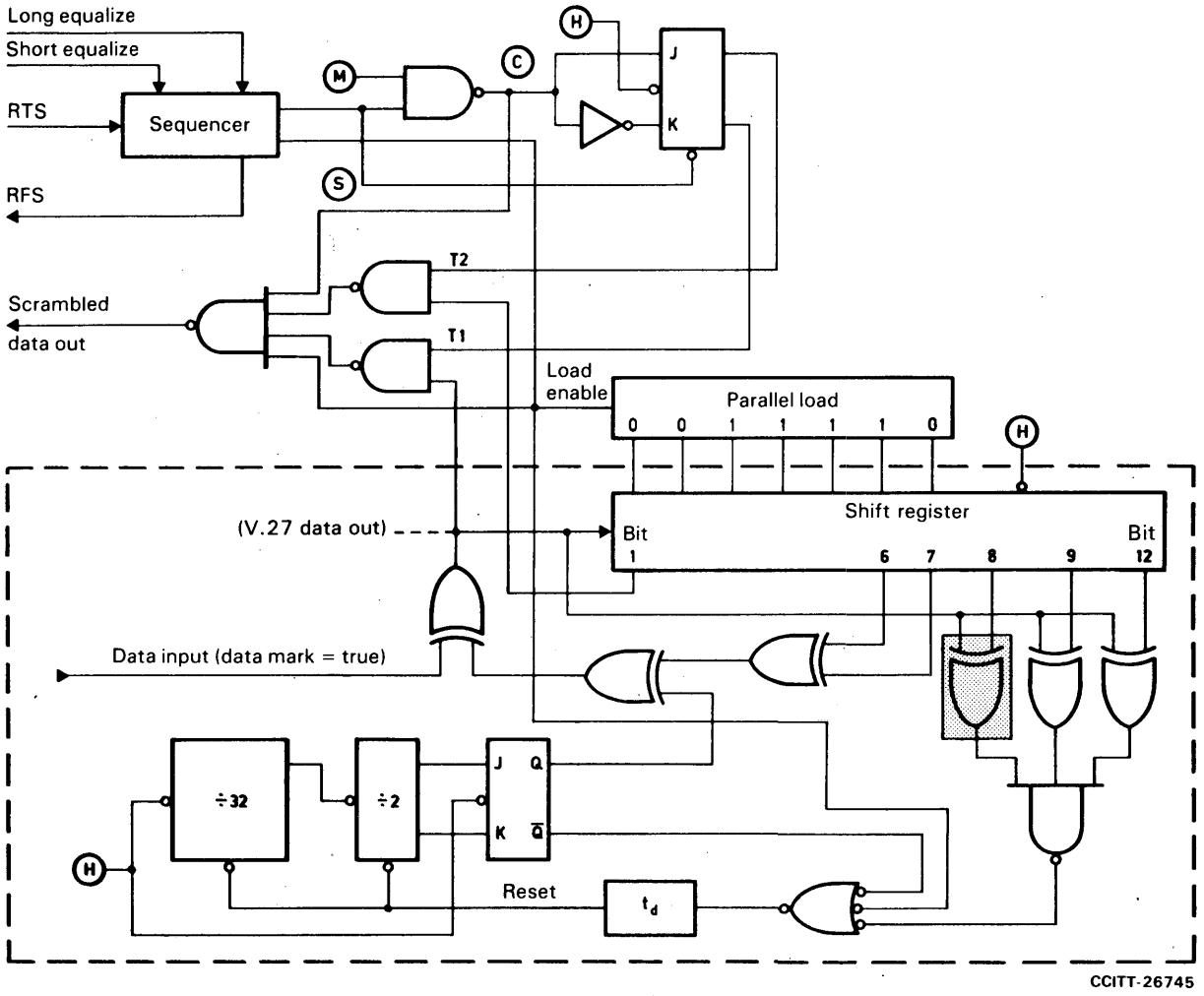
This particular starting point was chosen in order to ensure a pattern that has continuous 180° phase reversals at the beginning in order to ensure rapid clock acquisition, followed by a pattern that will ensure rapid equalizer convergence.

Within eight symbol intervals prior to the ON condition of *Ready For Sending* (RFS), the scrambler should be switched to normal operation, keeping the scrambler in mark hold until RFS to synchronize the descrambler.

Note – At 2400 bits per second, a similar technique may be used with appropriate clocking changes, as shown in Table I-1/V.27 *ter*.

TABLE I-1/V.27 *ter*

	Segment 4	Segment 5
Clock Ⓗ	3600 Hz	2400 Hz
Clock Ⓜ	1200 Hz	1200 Hz



Note 1 – The dotted line encloses the V.27 scrambler.

Note 2 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 3 – (H) is 3 times baud rate clock.

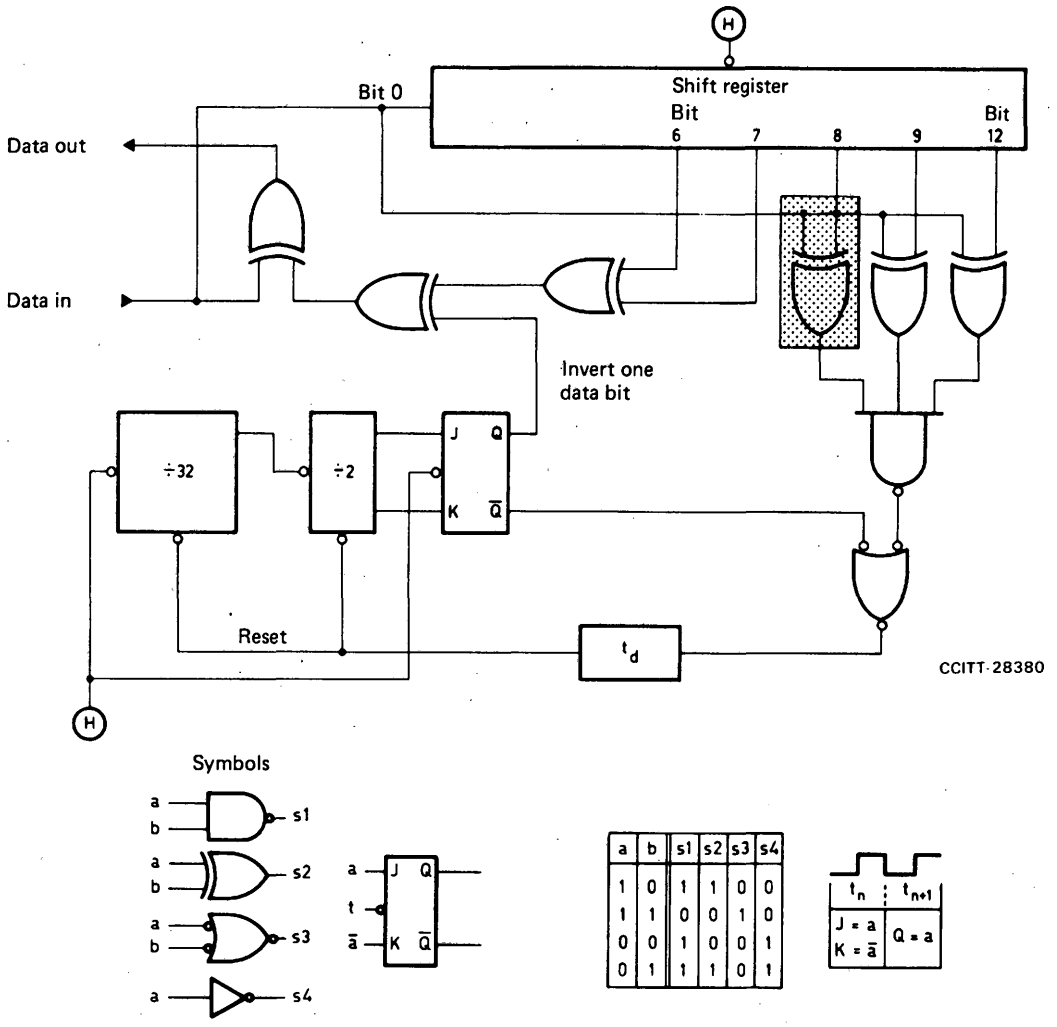
Note 4 – (M) is baud rate clock (1600 Hz).

Note 5 – Diagrams shown with positive logic.

Note 6 – Signals (C) and (S) are identified only to correlate with Figure I-3/V.27 *ter*.

FIGURE I-1/V.27 *ter*

An example of sequence generator and scrambler circuitry for 4800 bit/s



Note 1 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 2 – (H) represents clock signal. The negative going transition is the active transition.

Note 3 – There is a delay time due to physical circuits between a negative going transition of a (H) and the end of the "0" state represented by t_d on the non-reset wire; therefore the first coincidence between bit 0 and bit 8 or bit 9 or bit 12 is not taken into account by the counter.

FIGURE I-2/V.27 *ter*

An example of descrambler circuitry

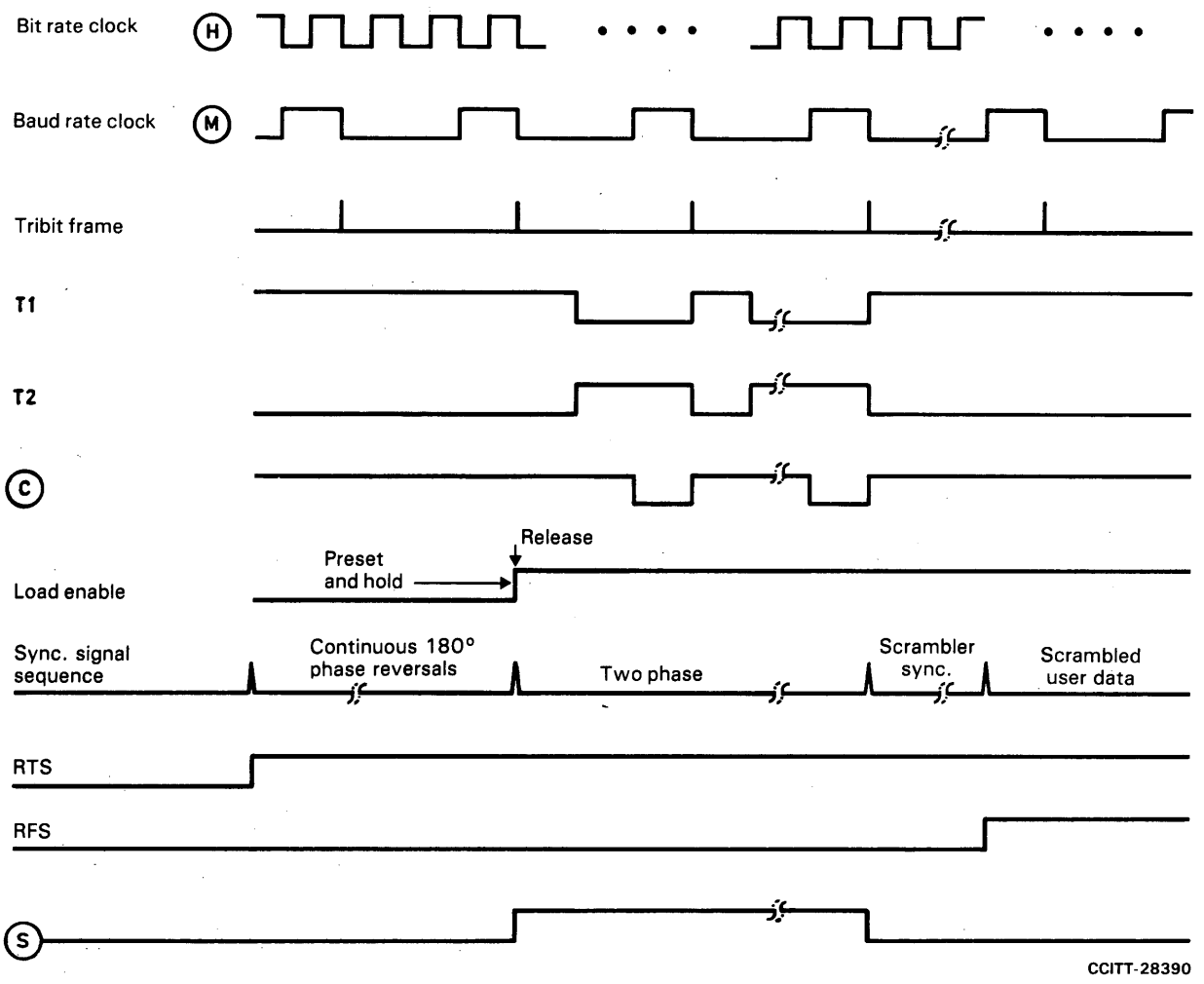


FIGURE I-3/V.27 *ter*

Synchronizing signal sequence for 4800 bit/s (see Figure I-1/V.27 *ter*)

Recommendation V.28

ELECTRICAL CHARACTERISTICS FOR UNBALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS

(Geneva, 1972; amended at Geneva, 1980, Malaga-Torremolinos, 1984, and at Melbourne, 1988)

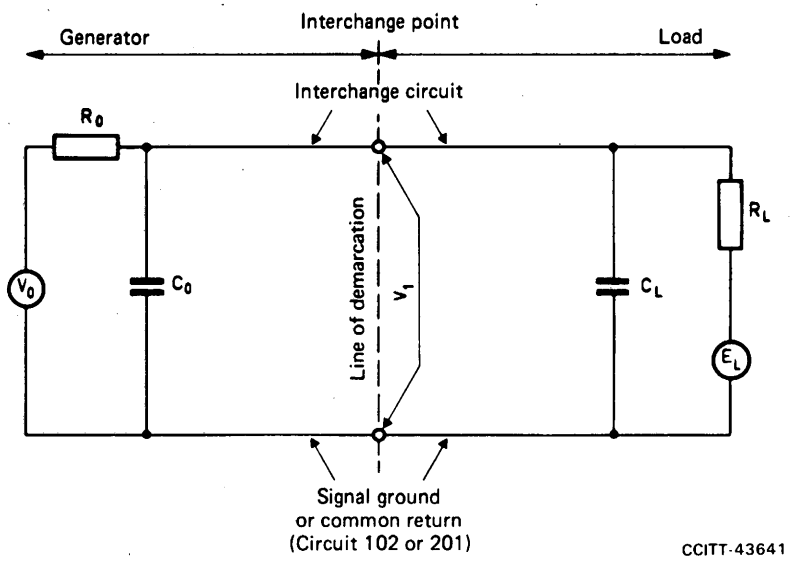
1 Scope

The electrical characteristics specified in this Recommendation apply generally to interchange circuits operating with data signalling rates below the limit of 20 000 bits per second.

2 Interchange equivalent circuit

Figure 1/V.28 shows the interchange equivalent circuit with the electrical parameters, which are defined below.

This equivalent circuit is independent of whether the generator is located in the data circuit-terminating equipment and the load in the data terminal equipment or vice versa.



V_0 is the open-circuit generator voltage.
R_0 is the total effective d.c. resistance associated with the generator, measured at the interchange point.
C_0 is the total effective capacitance associated with the generator, measured at the interchange point.
V_1 is the voltage at the interchange point with respect to signal ground or common return.
C_L is the total effective capacitance associated with the load, measured at the interchange point.
R_L is the total effective d.c. resistance associated with the load, measured at the interchange point.
E_L is the open-circuit load voltage (bias).

FIGURE 1/V.28

Interchange equivalent circuit

The impedance associated with the generator (load) includes any cable impedance on the generator (load) side of the interchange point.

The equipment at both sides of the interface may implement generators as well as receivers in any combination.

For data transmission applications, it is commonly accepted that the interface cabling is provided by the DTE. This introduces the line of demarcation between the DTE plus cable and the DCE. This line is also called the interchange point and is physically implemented in the form of a connector. The applications also require interchange circuits in both directions. This leads to an illustration as shown in Figure 2/V.28.

3 Load

The test conditions for measuring the load impedance are shown in Figure 3/V.28.

The impedance on the load side of an interchange circuit shall have a d.c. resistance (R_L) neither less than 3000 ohms nor more than 7000 ohms. With an applied voltage (E_m), 3 to 15 volts in magnitude, the measured input current (I) shall be within the following limits:

$$I_{\text{min., max.}} = \left| \frac{E_m \pm E_{L\,\text{max.}}}{R_{L\,\text{max., min.}}} \right|$$

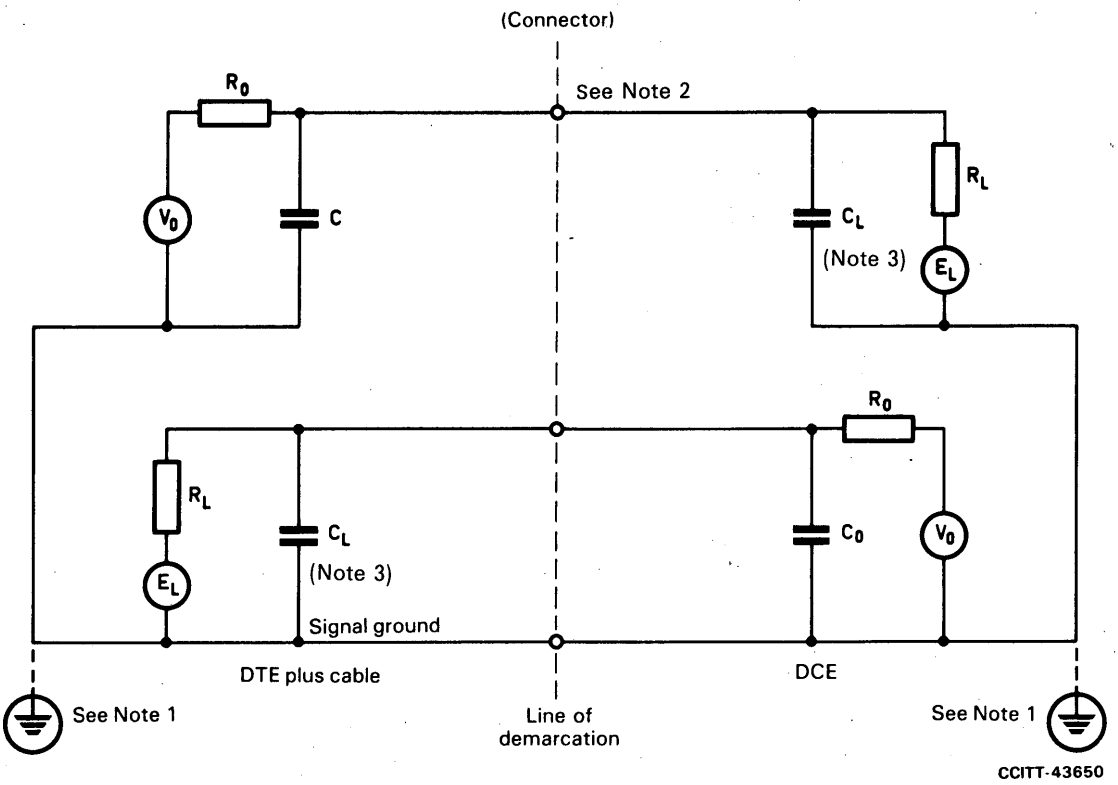
The open-circuit load voltage (E_L) shall not exceed 2 volts.

The effective shunt capacitance (C_L) of the load, measured at the interchange point, shall not exceed 2500 picofarads.

To avoid inducing voltage surges on interchange circuits the reactive component of the load impedance shall not be inductive.

Note – This is subject to further study.

The load on an interchange circuit shall not prejudice continuous operation with any input signals within the voltage limits specified in § 4. below.



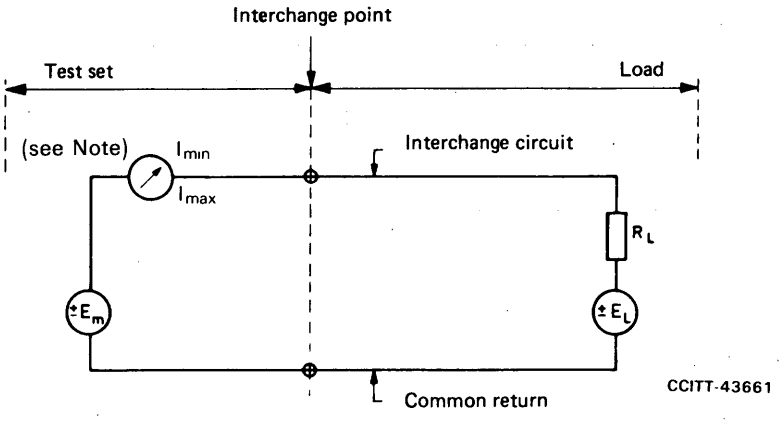
Note 1 – Signal ground may be further connected to external protective ground if national regulations require.

Note 2 – For data transmission over telephone-type facilities, ISO has specified a 25-pin connector and pin assignments in accordance with ISO 2110.

Note 3 – Many existing interchange circuit generators do not provide for meeting the maximum rise time requirement of Recommendation V.28, § 6 when driving a capacitance of greater than 2500 pF, the maximum permitted load capacitance (C_L), which includes the capacitance of the DTE supplied interface cable.

FIGURE 2/V.28

Practical representation of the interface



Note – The internal resistance of the ammeter shall be much less than the load resistance (R_L).

FIGURE 3/V.28

Equivalent test circuit

4 Generator

The generator on an interchange circuit shall withstand an open circuit and a short circuit between itself and any other interchange circuit (including generators and loads) without sustaining damage to itself or its associated equipment.

The open circuit generator voltage (V_0) on any interchange circuit shall not exceed 25 volts in magnitude. The impedance (R_0 and C_0) on the generator side of an interchange circuit is not specified; however, the combination of V_0 and R_0 shall be selected so that a short circuit between any two interchange circuits shall not result in any case in a current in excess of one-half ampere.

Additionally, when the load open-circuit voltage (E_L) is zero, the voltage (V_1) at the interchange point shall not be less than 5 volts and not more than 15 volts in magnitude (either positive or negative polarity), for any load resistance (R_L) in the range between 3000 ohms and 7000 ohms.

The effective shunt capacitance (C_0) at the generator side of an interchange circuit is not specified. However, in addition to any load resistance (R_L) the generator shall be capable of driving all of the capacitance at the generator side (C_0), plus a load capacitance (C_L) of 2500 picofarads.

Note 1 – For test purposes other than specified in this Recommendation (e.g. signal quality measurement), a transmitter test load of 3000 ohms may be used.

Note 2 – Relay or switch contacts may be used to generate signals on an interchange circuit, with appropriate measures to ensure that signals so generated comply with the applicable clauses of § 6 below.

5 Significant levels (V_1)

For data interchange circuits, the signal shall be considered in the binary 1 condition when the voltage (V_1) on the interchange circuit measured at the interchange point is more negative than minus 3 volts. The signal shall be considered in the binary 0 condition when the voltage (V_1) is more positive than plus 3 volts.

For control and timing interchange circuits, the circuit shall be considered ON when the voltage (V_1) on the interchange circuit is more positive than plus 3 volts, and shall be considered OFF when the voltage (V_1) is more negative than minus 3 volts (see Table 1/V.28).

Note – In certain countries, in the case of direct connection to d.c. telegraph-type circuits only, the voltage polarities in Table 1/V.28 may be reversed.

The region between plus 3 volts and minus 3 volts is defined as the transition region. For an exception to this, see § 7 below.

TABLE 1/V.28

Correlation table

$V_1 < -3$ volts	$V_1 > +3$ volts
1	0
OFF	ON

6 Signal characteristics

The following limitations to the characteristics of signals transmitted across the interchange point, exclusive of external interference, shall be met at the interchange point when the interchange circuit is loaded with any receiving circuit which meets the characteristics specified in § 3 above.

These limitations apply to all (data, control and timing) interchange signals unless otherwise specified.

1) All interchange signals entering into the transition region shall proceed through this region to the opposite signal state and shall not re-enter this region until the next significant change of signal condition, except as indicated in 6) below.

2) There shall be no reversal of the direction of voltage change while the signal is in the transition region, except as indicated in 6) below.

3) For control interchange circuits, the time required for the signal to pass through the transition region during a change in state shall not exceed one millisecond.

4) For data and timing interchange circuits, the time required for the signal to pass through the transition region during a change in state shall not exceed 1 millisecond or 3 per cent of the nominal element period on the interchange circuit, whichever is the less.

5) To reduce crosstalk between interchange circuits the maximum instantaneous rate of voltage change will be limited. A provisional limit will be 30 volts per microsecond.

6) When electromechanical devices are used on interchange circuits, points 1) and 2) above do not apply to data interchange circuits.

7 Detection of generator power-off or circuit failure

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator power-off condition;

2) receiver not interconnected with a generator;

3) open-circuited interconnecting cable;

4) short-circuited interconnecting cable.

The power-off impedance of the generator side of these circuits shall not be less than 300 ohms when measured with an applied voltage (either positive or negative polarity) not greater than 2 volts in magnitude referenced to signal ground or common return.

The interpretation of a fault condition by a receiver (or load) is application dependent. Each application may use a combination of the following classification:

Type 0: No interpretation. A receiver or load does not have detection capability.

Type 1: Data circuits assume a binary 1 state. Control and timing circuits assume an OFF condition.

The association of the circuit failure detection to particular interchange circuits in accordance with the above types is a matter of the functional and procedural characteristics specification of the interface.

The interchange circuits monitoring circuit fault conditions in the general telephone network interfaces are indicated in Recommendation V.24.

Recommendation V.29

9600 BITS PER SECOND MODEM STANDARDIZED FOR USE ON POINT-TO-POINT 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984, and at Melbourne, 1988)

1 Introduction

This modem is intended to be used primarily on special quality leased circuits, e.g. Recommendation M.1020 [1] or M.1025 [2] circuits but this does not preclude the use of this modem over circuits of lower quality at the discretion of the Administration concerned (see Notes 1 and 2).

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

The principal characteristics of this recommended modem for transmitting data at 9600 bits per second on leased circuits are as follows:

a) fallback rates of 7200 and 4800 bits per second;

b) capable of operating in a duplex or half-duplex mode with continuous or controlled carrier;

c) combined amplitude and phase modulation with synchronous mode of operation;

d) inclusion of an automatic adaptive equalizer;

e) optional inclusion of a multiplexer for combining data rates of 7200, 4800 and 2400 bits per second (see Note 3).

Note 1 – The principal use of this recommended modem is on 4-wire leased circuits. Other applications, such as stand-by operation on the switched network, should be points for further study.

The types of special quality circuits, e.g. M.1020 [1] or M.1025 [2] should be studied.

Note 2 – The values of some circuit characteristics, for example, noise and nonlinear distortion, are subject to further study.

Note 3 – When the multiplexer option is installed, provisions in § 12 may supersede provisions given in other sections.

Note 4 – Attention should be given to the selection of appropriate equalization techniques in the modem implementation, if acceptable performance on circuits conforming to Recommendation M.1025 is desired.

2 Line signals

2.1 The carrier frequency is to be 1700 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Signal space coding*

2.2.1 At 9600 bits per second, the scrambled data stream to be transmitted is divided into groups of four consecutive data bits (quadbits). The first bit (Q1) in time of each quadbit is used to determine the signal element amplitude to be transmitted. The second (Q2), third (Q3) and fourth (Q4) bits are encoded as a phase change relative to the phase of the immediately preceding element (see Table 1/V.29). The phase encoding is identical to Recommendation V.27.

The relative amplitude of the transmitted signal element is determined by the first bit (Q1) of the quadbit and the absolute phase of the signal element (see Table 2/V.29). The absolute phase is initially established by the synchronizing signal as explained in § 8 below.

Figure 1/V.29 shows the absolute phase diagram of transmitted signal elements at 9600 bits per second.

At the receiver the quadbits are decoded and the data bits are reassembled in correct order.

2.2.2 At the fallback rate of 7200 bits per second, the scrambled data stream to be transmitted is divided into groups of three consecutive data bits. The first data bit in time determines Q2 of the modulator quadbit. The second and third data bits determine Q3 and Q4 respectively of the modulator quadbit. Q1 of the modulator quadbit is a data ZERO for each signal element. Signal elements are determined in accordance with § 2.2.1 above. Figure 2/V.29 shows the absolute phase diagram of the transmitted signal elements at 7200 bits per second.

2.2.3 At the fallback rate of 4800 bits per second (see Table 3/V.29), the scrambled data stream to be transmitted is divided into groups of two consecutive data bits. The first data bit in time determines Q2 of the modulator quadbit and the second data bit determines Q3 of the modulator quadbit. Q1 of the modulator quadbit is a data ZERO for each signal element. Q4 is determined by inverting the modulo 2 sum of Q2 + Q3. The signal element is then determined in accordance with § 2.2.1 above. Figure 3/V.29 shows the absolute phase diagram of transmitted signal elements at 4800 bits per second.

The phase changes are identical with Recommendation V.26 (alternative A) and the amplitude is constant with a relative value of 3.

TABLE 1/V.29

Q2	Q3	Q4	Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

TABLE 2/V.29

Absolute phase	Q1	Relative signal element amplitude
0°, 90°, 180°, 270°	0	3
	1	5
45°, 135°, 225°, 315°	0	$\sqrt{2}$
	1	$3\sqrt{2}$

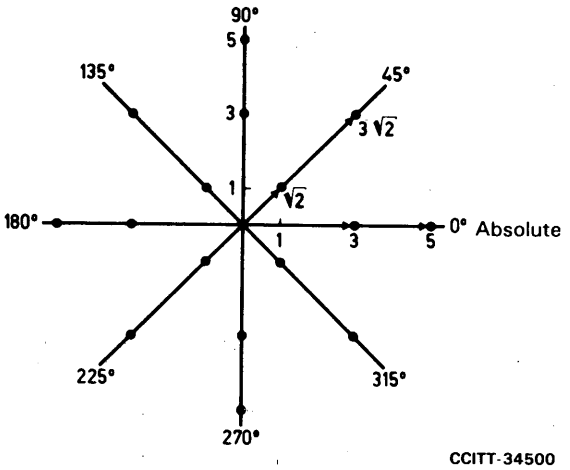


FIGURE 1/V.29

Signal space diagram at 9600 bit/s

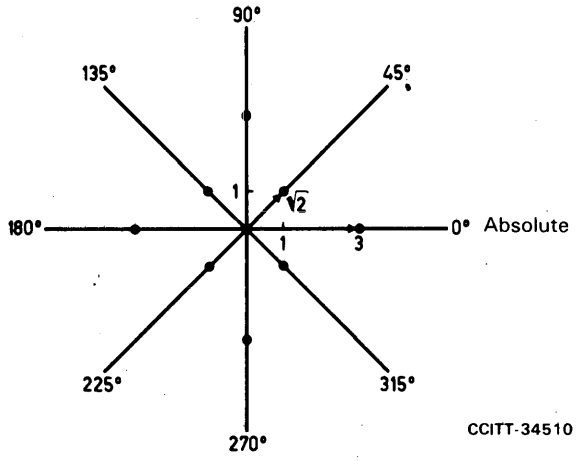


FIGURE 2/V.29

Signal space diagram at 7200 bit/s

TABLE 3/V.29

Data bits		Quadbits Q1	Q2	Q3	Q4	Phase change
0	0	0	0	0	1	0°
0	1	0	0	1	0	90°
1	1	0	1	1	1	180°
1	0	0	1	0	0	270°

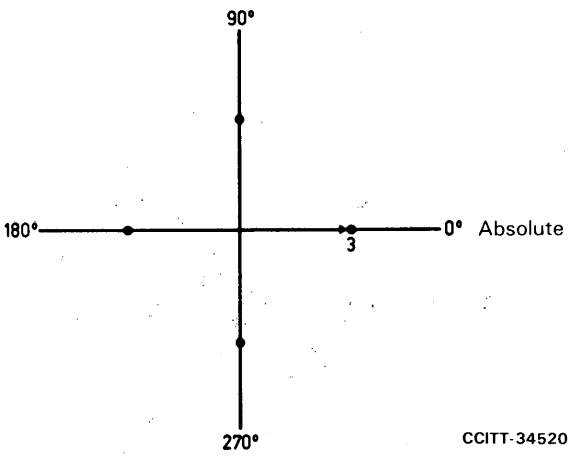


FIGURE 3/V.29

Signal space diagram at 4800 bit/s

3 Data signalling and modulation rates

The data signalling rates shall be 9600, 7200 and 4800 bits per second ± 0.01%. The modulation rate is 2400 bauds ± 0.01%.

4 Received signal frequency tolerance

The carrier frequency tolerance allowance at the transmitter is ± 1 Hz. Assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received signal frequency.

5 Interchange circuits

5.1 *List of interchange circuits* (Table 4/V.29)

TABLE 4/V.29

Interchange circuit (see Note 1)	
No.	Designation
102	Signal ground or common return
103	Transmitted data
104	Received data
105 (see Note 2)	Request to send
106	Ready for sending
107	Data set ready
109	Data channel received line signal detector
111 (see Note 3)	Data signalling rate selector (DTE source)
113	Transmitter signal element timing (DTE source)
114	Transmitter signal element timing (DTE source)
115	Receiver signal element timing (DCE source)
140 (see Note 4)	Loopback/Maintenance test
141 (see Note 4)	Local loopback
142	Test indicator

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordande with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 – Not essential for continuous carrier operation.

Note 3 – A manual selector shall be implemented which determines the two data signalling rates selected by circuit 111. The manual selector positions shall be designated 9600/7200, 9600/4800 and 7200/4800. The ON condition of circuit 111 selects the higher data signalling rate and the OFF condition of circuit 111 selects the lower data signalling rate.

Note 4 – Interchange circuits 140 and 141 are optional.

5.2 *Threshold and response times of circuit 109*

5.2.1 *Threshold*

- greater than −26 dBm: circuit 109 ON;
- less than −31 dBm: circuit 109 OFF.

The condition of circuit 109 for levels between −26 dBm and −31 dBm is not specified except that the signal detector shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

5.2.2 *Response times*

- ON to OFF: 30 ± 9 ms;
- OFF to ON:
  1) for initial equalization, circuit 109 must be ON prior to user data appearing on circuit 104;
  2) for re-equalization during data transfer, circuit 109 will be maintained in the ON condition; during this period, circuit 104 may be clamped to the binary 1 condition;
  3) after a line signal interruption that lasts more than the ON to OFF response time:
     a) when no new equalization is needed, 15 ± 10 ms,
     b) when a new equalization is needed, circuit 109 must be ON prior to user data appearing on circuit 104.

Response times of circuit 109 are the times that elapse between the connection or removal of a line signal to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuit 109.

Note – Circuit 109 ON to OFF response time should be suitably chosen within the specified limits to ensure that all valid data bits have appeared on circuit 104.

5.3 *Response time for circuit 106*

The time between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106 shall be optionally 15 ms ± 5 ms or 253.5 ms ± 0.5 ms.

The short delay is used when circuit 105 does not control the transmitter carrier. The long delay is used when circuit 105 controls transmitter carrier and a synchronizing signal is initiated by the OFF to ON transition of circuit 105.

The time between the ON to OFF transition of circuit 105 and the ON to OFF transition of circuit 106 shall be suitably chosen to ensure that all valid signal elements have been transmitted.

5.4 *Fault condition of interchange circuits*

(See Recommendations V.28, § 7 for association of the receiver failure detection types.)

5.4.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.4.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.4.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114, and receiver signal element timing, circuit 115. In this arrangement, the transmitter may either run as an independent timing source or with loopback timing (transmit timing slaved to receive timing). Loopback timing may be desirable in some network applications. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment and be transferred to the modem via interchange circuit 113.

8 Synchronizing signals

Transmission of synchronizing signals may be initiated by the modem or by the associated data terminal equipment. When circuit 105 is used to control the transmitter carrier the synchronizing signals are generated during the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106. When the receiving modem detects a circuit condition which requires resynchronizing, it shall turn circuit 106 OFF and generate a synchronizing signal.

The synchronizing signals for all data signalling rates are divided into four segments as in Table 5/V.29.

TABLE 5/V.29

	Segment 1	Segment 2	Segment 3	Segment 4	Total of Segments 1, 2, 3 and 4
Type of line signal	No transmitted energy	Alternations	Equalizer conditioning pattern	Scrambled all binary ONEs	Total synchronizing signal
Number of symbol intervals	48	128	384	48	608
Approximate time in ms [a]	20	53	160	20	253

[a] Approximate times are provided for information only. The segment duration is determined by the exact number of symbol intervals.

8.1 Segment 2 of the synchronizing signal consists of alterations between two signal elements. The first signal element (A) transmitted has a relative amplitude of 3 and defines the absolute phase reference of 180°. The second signal element (B) transmitted depends on the data signalling rate. Figure 4/V.29 shows the B signal element at each of the data signalling rates. Segment 2 alternates ABAB...ABAB for 128 symbol intervals.

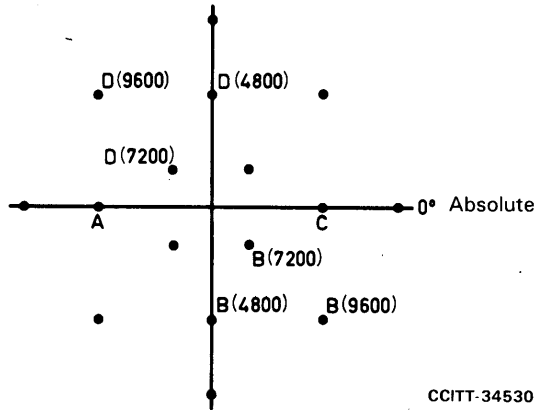


FIGURE 4/V.29

Signal space diagram showing synchronizing signal points

8.2 Segment 3 of the synchronizing signals transmits two signal elements according to an equalizer condition pattern. The first signal element (C) has a relative amplitude of 3 and absolute phase of 0°. The second signal element (D) transmitted depends on the data signalling rate. Figure 4/V.29 shows the D signal element at each of the data signalling rates. The equalizer conditioning pattern is a pseudo-random sequence generated by the polynomial:

$$1 + x^{-6} + x^{-7}$$

Each time the pseudo-random sequence contains a ZERO, point C is transmitted. Each time the pseudo-random sequence contains a ONE, the point D is transmitted. Segment 3 begins with the sequence CDCDCDC.... according to the pseudo-random sequence and continues for 384 symbol intervals. The detailed pseudo-random sequence generation is described in Appendix I.

8.3 Segment 4 commences transmission according to the encoding described in § 2.2 above with continuous binary ONEs applied to the input of the data scrambler. Segment 4 duration is 48 symbol intervals. At the end of Segment 4, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

9 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial $1 + x^{-18} + x^{-23}$, shall be included in the modem.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence. At the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix II.

10 Equalizer

An automatic adaptive equalizer shall be provided in the receiver.

The receiver shall incorporate a means of detecting loss of equalization and initiating a synchronizing signal sequence in its associated local transmitter.

The receiver shall incorporate a means of detecting a synchronizing signal sequence from the remote transmitter and initiating a synchronizing signal sequence in its associated local transmitter, which may be initiated at any time during the reception of the synchronizing signal sequence, regardless of the state of circuit 105.

Either modem can initiate the synchronizing signal sequence. The synchronizing signal is initiated when the receiver has detected a loss of equalization or when circuit 105 OFF to ON transition occurs in the carrier controlled mode, as described in § 5.3 above. Having initiated a synchronizing signal, the modem expects a synchronizing signal from the remote transmitter.

If the modem does not receive a synchronizing signal from the remote transmitter within a time interval equal to the maximum expected two-way propagation delay, it transmits another synchronizing signal. A time interval of 1.2 seconds is recommended.

If the modem fails to synchronize on the received signal sequence, it transmits another synchronizing signal.

If a modem receives a synchronizing signal when it had not initiated a synchronizing signal and the receiver properly synchronizes, it returns only one synchronizing sequence.

Note – Manufacturers should note that where there is a likelihood that double-hop satellite connections may be encountered, a more appropriate value for this timer may be in the range of 1.8 to 2.6 seconds.

11 The following information is provided to assist equipment manufacturers:

- The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.
- The transmitter energy spectrum shall be shaped in such a way that with continuous binary ONEs applied to the input of the scrambler the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 700 Hz to 2700 Hz and the energy density at 500 Hz and 2900 Hz shall be attenuated 4.5 dB ± 2.5 dB with respect to the maximum energy density between 500 Hz and 2900 Hz.

12 **Multiplexing** (see Table 6/V.29)

A multiplexing option may be included to combine 7200, 4800 and 2400 bits per second data subchannels into a single aggregate bit stream for transmission. Identification of the individual data subchannels is accomplished by assignment to the modulator quadbit as defined in § 2.2 above.

12.1 *List of interchange circuits concerned with multiplexer ports* (see Table 7/V.29)

12.2 *Transmit buffers*

In the transmitter of each multiplexer port, there shall be a data buffer of suitable capacity. In this way, both phase variations and, within certain limits, frequency deviations are absorbed. The buffer shall be initialized when the OFF to ON transition of circuit 105 occurs and may be repositioned in the event of the buffer overflow.

Note – The buffer may be initialized upon the DCE sending a synchronizing signal.

12.3 *Transmit port timing arrangements*

Table 8/V.29 shows all possible combinations of port and main DCE transmit timing clock arrangements.

12.4 *Port simulated circuit 105 to circuit 109 operation (optional)*

Simulated circuits 105 to 109 operation on an individual port interface may optionally be provided in accordance with Recommendation V.13.

Note – There may be equipment in the field that accomplishes simulated 105 to 109 operation in a different way. In this case the entire DCE shall operate in continuous carrier mode.

12.5 *Response times for circuit 106*

Circuit 105 to circuit 106 delays on individual ports of the multiplexer are not necessarily those specified in § 5.3. Other suitable delays may be needed to handle simulated circuit 105 to circuit 109 operations.

TABLE 6/V.29

Aggregate data rate	Multiplex configuration	Sub-channel data rate	Multiplex channel	Modulator bits			
				Q1	Q2	Q3	Q4
9600 bit/s	1	9600	A	X	X	X	X
	2	7200 2400	A B	X	X	X	 X
	3	4800 4800	A B	X	 X	X	 X
	4	4800 2400 2400	A B C	X	 X	X	 X
	5	2400 2400 2400 2400	A B C D	X	 X	 X	 X
7200 bit/s	6	7200	A		X	X	X
	7	4800 2400	A B		X	X	 X
	8	2400 2400 2400	A B C		X	 X	 X
4800 bit/s	9	4800	A		X	X	
	10	2400 2400	A B		X	 X	

Note – When more than one modulator bit is assigned to a sub-channel, the first bit in time of the sub-channel is assigned to the first bit in time (Q1) of the modulator.

TABLE 7/V.29

Interchange circuits (see Note 1)		Port A	Ports B, C, D
No.	Designation		
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105	Request to send	X (see Note 2)	X (see Note 2)
106	Ready for sending	X (see Note 3)	X (see Note 3)
107	Data set ready	X	X
109	Data channel received line signal detector	X	X
111	Data signalling rate selector (DTE source)	X (see Note 4)	
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
140	Loopback/Maintenance test	X (see Note 5)	X (see Note 5)
141	Local loopback	X (see Notes 5 and 6)	
142	Test indicator	X (see Note 7)	X (see Note 7)

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 – Circuit 105 is not necessary for continuous carrier transmission. The transmitted line signal will not be controlled by this interchange circuit. If needed, circuit 105 (when the multiplexer is present) is used to control circuit 109 at the remote DCE. See § 12.4 below.

Note 3 – During the synchronization process of the main DCE, the OFF condition of circuit 106 is signalled at all port interfaces.

Note 4 – Circuit 111 is optionally present on Port A. If present, circuit 111 is activated in multiplexer configurations 1, 6 and 9 in the same way as if no multiplexer were present.

Note 5 – Circuits 140 and 141 are optional.

Note 6 – Circuit 141 is present only on Port A. When used in multiplexer configurations other than configurations 1, 6 or 9, the looping occurs on all ports.

Note 7 – Circuit 142 is present on all ports of the multiplexer, but may be activated on an individual port basis for individual port tests. All are activated simultaneously for entire DCE tests.

TABLE 8/V.29

Source of port transmitter signal element timing (used to clock in circuit 103)	Source of DCE internal transmitter element timing (internal transmit clock)	Port transmit buffer
114 (DCE source)	Internal (Independent timing)	Not required
	External [a] (Circuit 113 of selected port)	Not required
	Receiver timing (Loopback timing)	Not required
113 (DTE source) [a]	Internal (Independent timing)	Required
	External [a] (Circuit 113 of selected port)	Required for all ports except port supplying circuit 113 to DCE
	Receiver timing (Loopback timing)	Required

[a] In these applications a source could also be another DCE.

APPENDIX I

(to Recommendation V.29)

Details of the pseudo-random sequence generator

The equalizer conditioning pattern is determined by a pseudo-random sequence generated by the polynomial $1 + x^{-6} + x^{-7}$. Figure I-1/V.29 shows a suitable implementation.

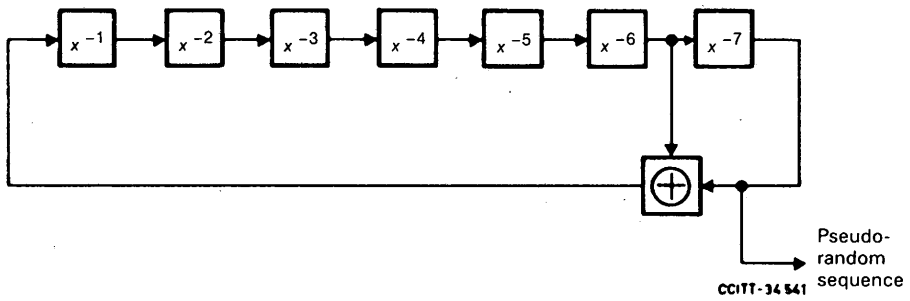


FIGURE I-1/V.29

The initial condition of the generator is 0101010. The generator clock is at the symbol rate (2400 symbols per second). The first four conditions of the generator are:

- initial condition: 0101010
- after first shift: 1010101
- after second shift: 1101010
- after third shift: 1110101

APPENDIX II

(to Recommendation V.29)

Detailed scrambling and descrambling process

II.1 *Scrambling*

The message polynomial is divided by the generating polynomial $1 + x^{-18} + x^{-23}$ (see Figure II-1/V.29). The coefficients of the quotient of this division taken in descending order form the data sequence to be transmitted. In order to ensure that proper starting sequence is generated, the shift register is fed with "0" during segments 1, 2 and 3. During segment 4 and normal data transmission it is fed with scrambled data D_s, (input data D_i being "1" during segment 4).

$$D_s = D_i \oplus D_s x^{-18} \oplus D_s x^{-23}$$

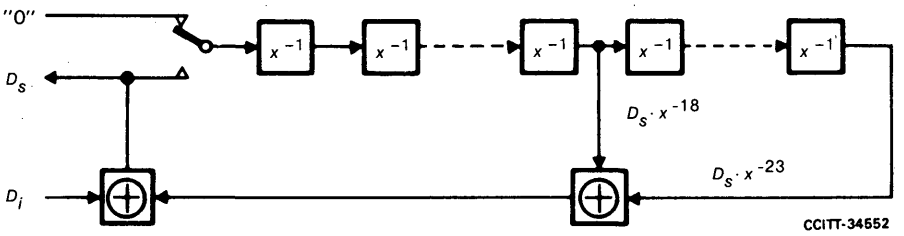


FIGURE II-1/V.29

II.2 *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial (Figure II-2/V.29) to form the recovered message polynomial. The coefficients of the recovered polynomial, taken in descending order, form the output data sequence D_o.

$$D_o = D_i = D_s (1 \oplus x^{-18} \oplus x^{-23})$$

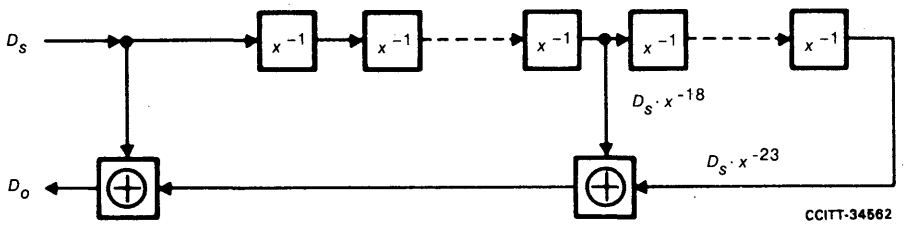


FIGURE II-2/V.29

II.3 *Elements of the scrambling process*

The polynomial $1 + x^{-18} + x^{-23}$ generates a pseudo-random sequence of length $2^{23} - 1 = 8{,}388{,}607$. This long sequence does not require the use of a guard polynomial to prevent the occurrence of repeat patterns and is particularly simple to implement with integrated circuits.

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with basic bandwidth conditioning*, Vol. IV, Rec. M.1025.

Recommendation V.31

ELECTRICAL CHARACTERISTICS FOR SINGLE-CURRENT INTERCHANGE CIRCUITS CONTROLLED BY CONTACT CLOSURE

(Geneva, 1972)

1 General

In general, the electrical characteristics specified in this Recommendation apply to interchange circuits operating at data signalling rates up to 75 bit/s.

Each interchange circuit consists of two conductors (go and return leads) which are electrically insulated from each other and from all other interchange circuits. A common return lead can be assigned to several interchange circuits of a group.

2 Equivalent circuit of interface

Figure 1/V.31 shows the equivalent interchange circuit, together with the electrical characteristics laid down in this Recommendation. Some electrical characteristics vary depending upon whether the signal receive side is located in the data circuit-terminating equipment or in the data side is located in the data circuit-terminating equipment or in the data terminal equipment. This fact is specially referred to below.

3 Signal source

The signal source must be isolated from ground or earth irrespective of whether it is located within the data circuit-terminating equipment or within the data terminal equipment.

If the signal receive side is in the data circuit-terminating equipment, the open-contact insulation resistance measured from either leg to ground or to any other interchange circuit shall not fall below 5 megohms and the capacitance measured between the same points shall not exceed 1000 picofarads.

Irrespective of the above, the following specifications apply to the signal source.

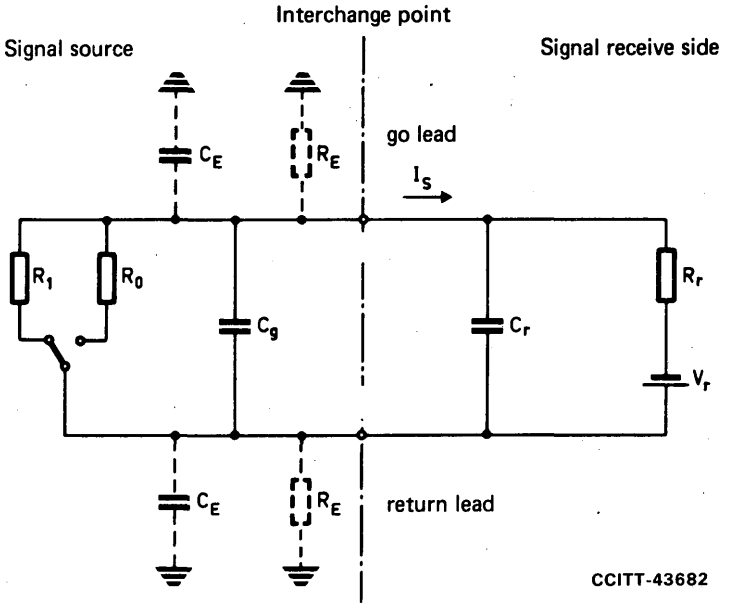
3.1 *Internal resistance of signal source R_1, R_0*

The d.c. resistance of the closed contact R_1, including the resistance of the interface cable, measured at the interface (see Figure 1/V.31), should not exceed 10 ohms within the current and voltage ranges of the signal receive side.

The d.c. resistance of the open contact R_0 including the insulation resistance of the interface cable should not fall below 250 kilohms when measured at the interface (see Figure 1/V.31) within the voltage range of the signal receive side.

3.2 *Capacitance of signal source C_g*

The capacitance of the signal source C_g including that of the interface cable, measured at the interface (see Figure 1/V.31), should not exceed 2500 picofarads.



R_1 = internal resistance of the signal source in the closed contact condition
R_0 = internal resistance of the signal source in the open contact condition
C_g = capacitance of signal source
C_r = capacitance of signal receive side
V_r = open circuit voltage of signal receive side
I_S = current in interchange circuit
R_r = internal resistance of signal receive side
R_E = insulation resistance of signal source if the latter is in the data terminal equipment
C_E = ground capacitance of signal source if the latter is in the data terminal equipment

FIGURE 1/V.31

Equivalent circuit of interface

4 Signal receive side

4.1 *Signal receive side in the data circuit-terminating equipment*

The signal receive side in the data circuit-terminating equipment can be floating or connected to ground at any single point.

4.1.1 *Open circuit voltage of the signal receive side V_r*

The open circuit voltage V_r on the signal receive side of the data-circuit terminating equipment, measured at the interface (see Figure 1/V.31), should not fall below 3 volts and should not exceed 12 volts.

4.1.2 *Current at interface I_s*

The current I_s supplied by the signal receive side in the data circuit-terminating equipment should not fall below 0.1 milliamp and should not exceed 15 milliamps, when measured at the interface (see Figure 1/V.31) in the closed contact condition, i.e. with an internal resistance of the signal source of $R_1 \leqslant 10$ ohms.

Note – Irrespective of the current I_s in the closed contact conditions, i.e. with an internal resistance of the signal source of $R_1 \leqslant 10$ ohms, the voltage at the interface should not exceed 150 millivolts, when measured between go and return leads.

4.1.3 *Internal resistance of signal receive side R_r*

The internal resistance R_r of the signal receive side of the data circuit-terminating equipment results from the limits for the open circuit voltage V_r of the signal receive side and the current I_s at the interface, which are specified under §§ 4.1.1 and 4.1.2 above.

Even if R_r has an inductive component, the voltage at the interface should not exceed the maximum of 12 volts specified under § 4.1.1 above.

Note – This item is subject to further study.

4.1.4 *Capacitance of signal receive side C_r*

The capacitance of C_r of the signal receive side in the data circuit-terminating equipment, including the capacitance of the cable up to the interface (see Figure 1/V.31), is not specified. It is only necessary to ensure that the signal receive side works satisfactorily, allowing for the capacitance of the signal source C_g.

4.2 *Signal receive side in the data terminal equipment*

The signal receive side in the data terminal equipment can be connected to ground at any single point.

4.2.1 *Open circuit voltage of the signal receive side V_r*

The open circuit voltage V_r of the signal receive side of the data terminal equipment, measured at the interface (see Figure 1/V.31), should not fall below 3 volts and should not exceed 52.8 volts.

4.2.2 *Current at the interface I_s*

The current I_s, supplied by the signal receive side in the data terminal equipment, should not fall below 10 milliamps and not exceed 50 milliamps, when measured at the interface (see Figure 1/V.31) in the closed contact condition, i.e. with an internal resistance of the signal source of $R_1 \leqslant 10$ ohms.

4.2.3 *Internal resistance of signal receive side R_r*

The internal resistance R_r of the signal receive side in the data terminal equipment is obtained from the limits for the open circuit voltage V_r of the signal receive side and the current I_s at the interface, which are specified under §§ 4.2.1 and 4.2.2 above.

Even if R_r has an inductive component, the voltage at the interface should not exceed the maximum of 52.8 volts, specified under § 4.2.1.

Note – This item is subject to further study.

4.2.4 *Capacitance of signal receive side C_r*

The capacitance of C_r of the signal receive side in the data terminal equipment including the capacitance of the cable is not specified. It is only necessary to ensure that the signal receive side works satisfactorily, allowing for the capacitance of the signal source C_g.

5 Signal allocation

Table 1/V.31 shows allocations of digital signals for data, control and timing circuits.

TABLE 1/V.31

	Closed contact $R_1 \leqslant 10\ \Omega$	Open contact $R_0 \geqslant 250\ k\Omega$
Data circuits	"1" condition	"0" condition
Control and timing circuits	ON condition	OFF condition

Recommendation V.31 *bis*

ELECTRICAL CHARACTERISTICS FOR SINGLE-CURRENT INTERCHANGE CIRCUITS USING OPTOCOUPLERS

(Malaga-Torremolinos, 1984)

1 General

In general, the electrical characteristics specified in this Recommendation apply to interchange circuits operating at data signalling rates up to 75 bit/s, which have been covered in Recommendation V.31, and also to interchange circuits operating at data signalling rates up to 1200 bit/s.

The electrical characteristics are specified to provide compatibility with existing equipment according to Recommendation V.31 which meet the voltage and current values given in Table 1/V.31 *bis*. The resistance values defined in Recommendation V.31 are converted into current and voltage values to meet the optocouplers requirements.

Each interchange circuit consists of two conductors (go and return leads) which are electrically insulated from each other and from all other interchange circuits. A common return lead can be assigned to several interchange circuits of a group.

2 Equivalent circuit of interface

Figure 1/V.31 *bis* shows the equivalent interchange circuit, together with the electrical characteristics laid down in this Recommendation. Some electrical characteristics vary depending upon whether the signal receive side is located in the data circuit-terminating equipment (DCE) or in the data terminal equipment (DTE). This fact is specially referred to below.

3 Signal source

The signal source must be isolated from ground or earth irrespective of whether it is located within the data circuit-terminating equipment or within the data terminal equipment.

If the signal receive side is in the data circuit-terminating equipment, the insulation resistance in the ON or OFF condition measured from either leg to ground or to any other interchange circuit shall not fall below 5 megohms and the capacitance measured between the same points shall not exceed 1000 picofarads.

Irrespective of the above, the following specifications apply to the signal source.

3.1 *Internal resistance of signal source R_1, R_0*

The d.c. resistance of the signal source in the ON (or 1) condition R_1 depends on V_s, V_r and I_1 (see Figure 1/V.31 *bis*). The d.c. resistance of the signal source in the OFF (or 0) condition R_0 depends on V_r and I_0 (see Figure 1/V.31 *bis*).

3.2 *Current at the interface I_0*

The current I_0, which represents the reverse current of the optocouplers in the OFF condition, should not exceed 10 μA (see Figure 1/V.31 *bis*).

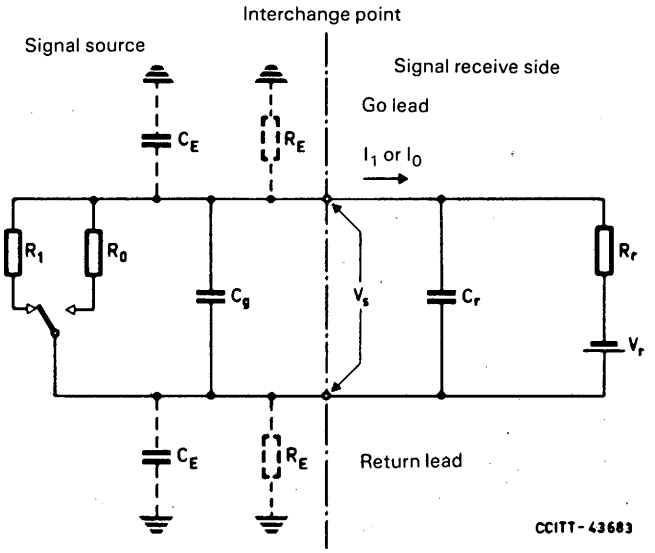
3.3 *Capacitance of signal source*

The capacitance of the signal source C_g including that of the interface cable, measured at the interface (see Figure 1/V.31 *bis*), should not exceed 2500 pF.

4 Signal receive side

4.1 *Signal receive side in the DCE*

The signal receive side in the DCE can be floating or connected to ground at any single point.



R_1 Internal resistance of the signal source in the ON (or 1) condition.
R_0 Internal resistance of the signal source in the OFF (or 0) condition.
C_g Capacitance of signal source.
C_r Capacitance of signal receive side.
V_r Open circuit voltage of signal receive side.
I_1 Current in interchange circuit in the ON (or 1) condition.
I_0 Current in the interchange circuit in the OFF (or 0) condition.
R_r Internal resistance of signal receive side.
R_E Insulation resistance of signal source if the latter is in the data terminal equipment.
C_E Ground capacitance of signal source if the latter is in the data terminal equipment.
V_s Voltage between the two leads of the interchange circuit in the ON (or 1) condition.

FIGURE 1/V.31 *bis*

Equivalent circuit of interface

4.1.1 *Open circuit voltage of the signal receive side V_r*

The open circuit voltage V_r on the signal receive side of the DCE, measured at the interface (see Figure 1/V.31 *bis*), should not fall below 3 V and should not exceed 25 V. The polarity of V_r has to be chosen for the current direction DTE to DCE in the go lead and DCE to DTE in the return lead.

4.1.2 *Current at the interface I_1*

The current I_1 supplied by the receive side in the DCE should not fall below 0.1 mA and should not exceed 5 mA, when measured at the interface in the ON (or 1) condition.

4.1.3 *Voltage at the interface V_s*

The voltage at the interface V_s, measured between the go and return leads in the ON (or 1) condition, should not exceed 1 V.

4.1.4 *Internal resistance of signal receive side R_r*

The internal resistance R_r of the signal receive side of the DCE results from the limits for the open circuit voltage V_r of the signal receive side and the current I_1 at the interface, which are specified under §§ 4.1.1 and 4.1.2 above.

Even if R_r has an inductive component, the voltage at the interface should not exceed the maximum of 25 V specified under § 4.1.1 above.

4.1.5 *Capacitance of signal receive side C_r*

The capacitance of C_r, of the signal receive side in the DCE, including the capacitance of the cable up to the interface (see Figure 1/V.31 *bis*), is not specified. It is only necessary to ensure that the signal receive side works satisfactorily, allowing for the capacitance of the signal source C_g.

4.2 *Signal receive side in the DTE*

The signal receive side in the DTE can be connected to ground at any single point.

4.2.1 *Open circuit voltage of the signal receive side V_r*

The open circuit voltage V_r of the signal receive side of the DTE, measured at the interface (see Figure 1/V.31 *bis*), should not fall below 3 V and should not exceed 25 V. The polarity of V_r has to be chosen for the current direction DTE to DCE in the go lead and DCE to DTE in the return lead.

4.2.2 *Current at the interface I_1*

The current I_1, supplied by the signal receive side in the DTE, should not fall below 0.1 mA and should not exceed 15 mA, when measured at the interface (see Figure 1/V.31 *bis*), in the ON (or 1) condition.

4.2.3 *Voltage at the interface V_s*

The voltage at the interface V_s, measured between the go and return leads in the ON (or 1) condition, should not exceed 1.5 V.

4.2.4 *Internal resistance of signal receive side R_r*

The internal resistance R_r of the signal receive side of the DTE results from the limits for the open circuit voltage V_r of the signal receive side and the current I_1 at the interface, which are specified under §§ 4.2.1 and 4.2.2 above.

4.2.5 *Capacitance of signal receive side C_r*

The capacitance of C_r of the signal receive side in the DTE including the capacitance of the cable is not specified. It is only necessary to ensure that the signal receive side works satisfactorily, allowing for the capacitance of the signal source C_g.

5 Signal allocation

Table 1/V.31 *bis* shows allocations of digital signals for data, control and timing circuits.

TABLE 1/V.31 *bis*

	0.1 mA $\leqslant I_1 \leqslant$ 5 mA (15 mA) $V_s \leqslant$ 1 V (1.5 V)	$I_0 \leqslant$ 10 μA
Data circuits	1 condition	0 condition
Control and timing circuits	ON condition	OFF condition

A FAMILY OF 2-WIRE, DUPLEX MODEMS OPERATING AT DATA SIGNALLING RATES OF UP TO 9600 bit/s FOR USE ON THE GENERAL SWITCHED TELEPHONE NETWORK AND ON LEASED TELEPHONE-TYPE CIRCUITS

(Malaga-Torremolinos, 1984, amended at Melbourne, 1988)

1 Introduction

This family of modems is intended for use on connections on general switched telephone networks (GSTNs) (see Note 1) and on point-to-point leased telephone-type circuits. The principal characteristics of the modems are as follows:

a) Duplex mode of operation on GSTN and 2-wire point-to-point leased circuits (see Note 2).

b) Channel separation by echo cancellation techniques.

c) Quadrature amplitude modulation for each channel with synchronous line transmission at 2400 bauds.

d) Any combination of the following data signalling rates may be implemented in the modems:

9600 bit/s synchronous,

4800 bit/s synchronous,

2400 bit/s synchronous (for further study).

e) At 9600 bit/s, two alternative modulation schemes, one using 16 carrier states and one using trellis coding with 32 carrier states, are provided for in this Recommendation. However, modems providing the 9600 bit/s data signalling rate shall be capable of interworking using the 16-state alternative.

f) Exchange of rate sequences during start-up to establish the data rate, coding and any other special facilities.

g) Optional provision of an asynchronous mode of operation in accordance with Recommendation V.14.

Note 1 – On international GSTN connections that utilize circuits that are in accord with Recommendation G.235 (16-channel terminal equipments), it may be necessary to employ a greater degree of equalization within the modem than would be required for use on most national GSTN connections.

Note 2 – The transmit and receive rates in each modem shall be the same. The possibility of asymmetric working remains for further study.

2 Line signals

2.1 *Carrier frequency*

The carrier frequency is to be 1800 ± 1 Hz. No separate pilot tones are to be provided. The receiver must be able to operate with received frequency offsets of up to ± 7 Hz.

2.2 *Transmitted spectrum*

The transmitted power level must conform to Recommendation V.2. With continuous binary ones applied to the input of the scrambler, the transmitted energy density at 600 Hz and 3000 Hz should be attenuated 4.5 ± 2.5 dB with respect to the maximum energy density between 600 Hz and 3000 Hz.

2.3 *Modulation rate*

The modulation rate shall be 2400 bauds ± 0.01%.

2.4 *Coding*

2.4.1 *Signal element coding for 9600 bit/s*

Two alternatives are defined:

2.4.1.1 *Nonredundant coding*

The scrambled data stream to be transmitted is divided into groups of 4 consecutive data bits. The first two bits in time $Q1_n$ and $Q2_n$ in each group, where the subscript n designates the sequence number of the group, are differentially encoded into $Y1_n$ and $Y2_n$ according to Table 1/V.32. Bits $Y1_n$, $Y2_n$, $Q3_n$ and $Q4_n$ are then mapped into the coordinates of the signal state to be transmitted according to the signal space diagram shown in Figure 1/V.32 and as listed in Table 3/V.32.

2.4.1.2 *Trellis coding*

The scrambled data stream to be transmitted is divided into groups of 4 consecutive data bits. As shown in Figure 2/V.32, the first two bits in time $Q1_n$ and $Q2_n$ in each group, where the subscript n designates the sequence number of the group, are first differentially encoded into $Y1_n$ and $Y2_n$ according to Table 2/V.32. The two differentially encoded bits $Y1_n$ and $Y2_n$ are used as input to a systematic convolutional encoder which generates a redundant bit $Y0_n$. This redundant bit and the 4 information-carrying bits $Y1_n$, $Y2_n$, $Q3_n$ and $Q4_n$ are then mapped into the coordinates of the signal element to be transmitted according to the signal space diagram shown in Figure 3/V.32 and as listed in Table 3/V.32.

2.4.2 *Signal element coding for 4800 bit/s*

The scrambled data stream to be transmitted is divided into groups of 2 consecutive data bits. These bits, denoted $Q1_n$ and $Q2_n$, where $Q1_n$ is the first in time, and the subscript n designates the sequence number of the group, are differentially encoded into $Y1_n$ and $Y2_n$ according to Table 1/V.32. Figure 1/V.32 shows the subset A, B, C and D of signal states used for 4800 bit/s transmission.

2.4.3 *Signal element coding for 2400 bit/s*

(For further study.)

3 Interchange circuits

3.1 *List of interchange circuits*

These are listed in Table 4/V.32 below.

3.2 *Transmit data*

The modems shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or 114.

3.3 *Receive data*

The modems shall pass synchronous data to the DTE on circuit 104 under the control of circuit 115.

3.4 *Timing arrangements*

Clocks shall be included in the modems to provide the DTE with transmitter signal element timing on circuit 114 and receiver signal element timing on circuit 115. The transmitter timing may originate in the DTE and be transferred to the modem via circuit 113. In some applications it may be necessary to slave the transmitter timing to the receiver timing inside the modem.

3.5 *Data rate control*

Data rate selection may be by switch (or similar means) or alternatively by circuit 111. In cases where three different data signalling rates are implemented in a modem, a manual selector may be provided which determines the two data signalling rates selected by circuit 111.

The ON condition of circuit 111 selects the higher data signalling rate and the OFF condition of circuit 111 selects the lower data signalling rate.

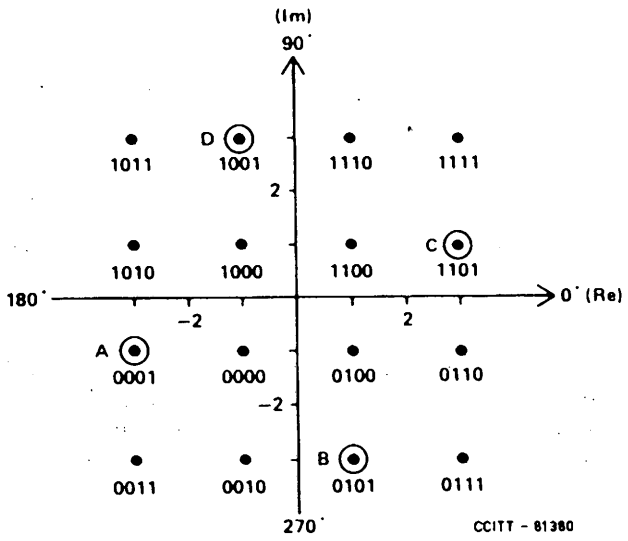
3.6 *Circuit 106*

After the start-up and retrain sequences, circuit 106 must follow the state of circuit 105 within 2 ms.

TABLE 1/V.32

Differential quadrant coding for 4800 bit/s and for nonredundant coding at 9600 bit/s

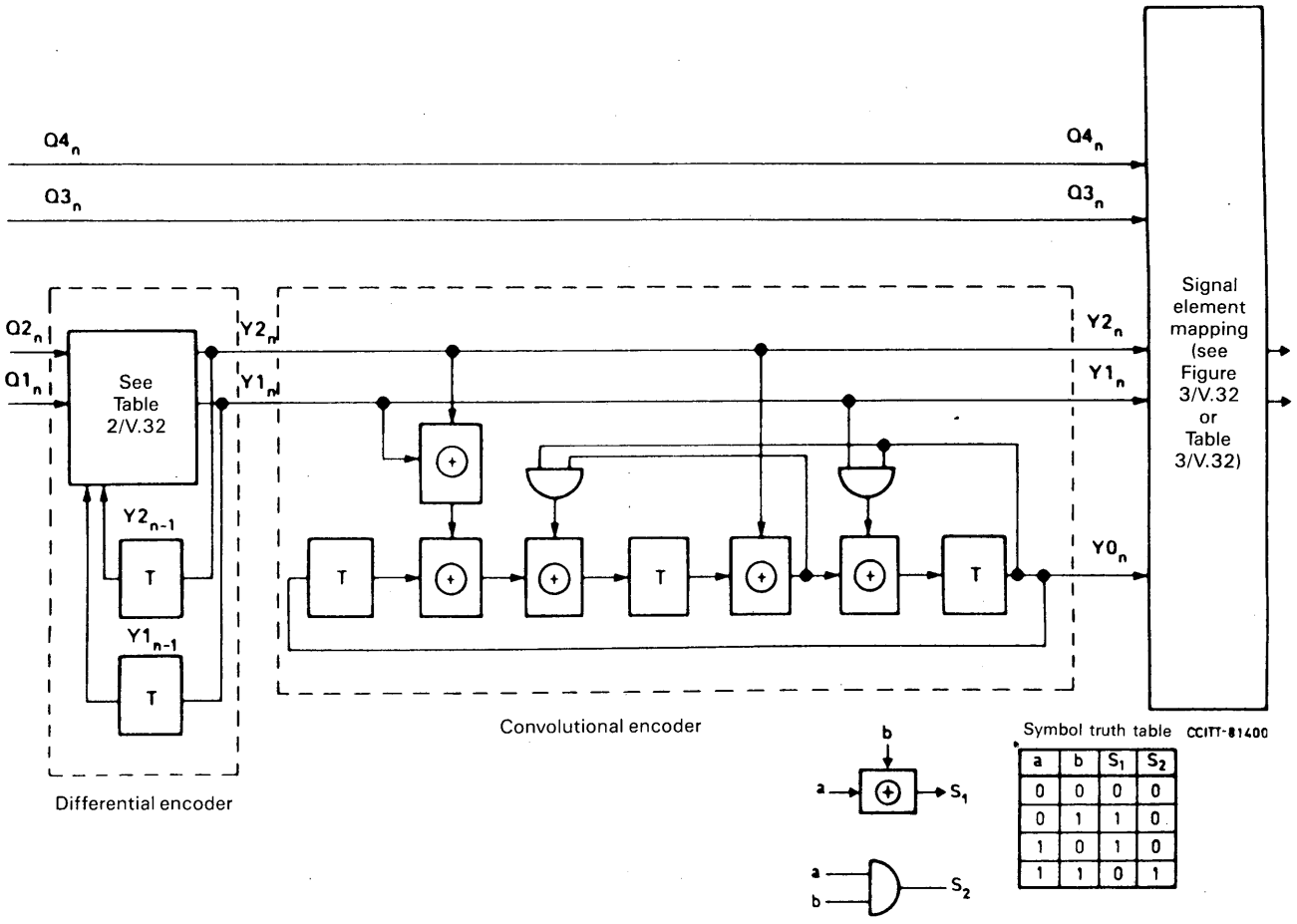
Inputs		Previous outputs		Phase quadrant change	Outputs		Signal state for 4800 bit/s
$Q1_n$	$Q2_n$	$Y1_{n-1}$	$Y2_{n-1}$		$Y1_n$	$Y2_n$	
0	0	0	0	+ 90°	0	1	B
0	0	0	1		1	1	C
0	0	1	0		0	0	A
0	0	1	1		1	0	D
0	1	0	0	0°	0	0	A
0	1	0	1		0	1	B
0	1	1	0		1	0	D
0	1	1	1		1	1	C
1	0	0	0	+180°	1	1	C
1	0	0	1		1	0	D
1	0	1	0		0	1	B
1	0	1	1		0	0	A
1	1	0	0	+270°	1	0	D
1	1	0	1		0	0	A
1	1	1	0		1	1	C
1	1	1	1		0	1	B



The binary numbers denote $Y1_n\ Y2_n\ Q3_n\ Q4_n$

FIGURE 1/V.32

16-point signal structure with nonredundant coding for 9600 bit/s and subset A B C D of states used at 4800 bit/s and for training



a	b	S_1	S_2
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FIGURE 2/V.32

Trellis coding at 9600 bit/s

TABLE 2/V.32

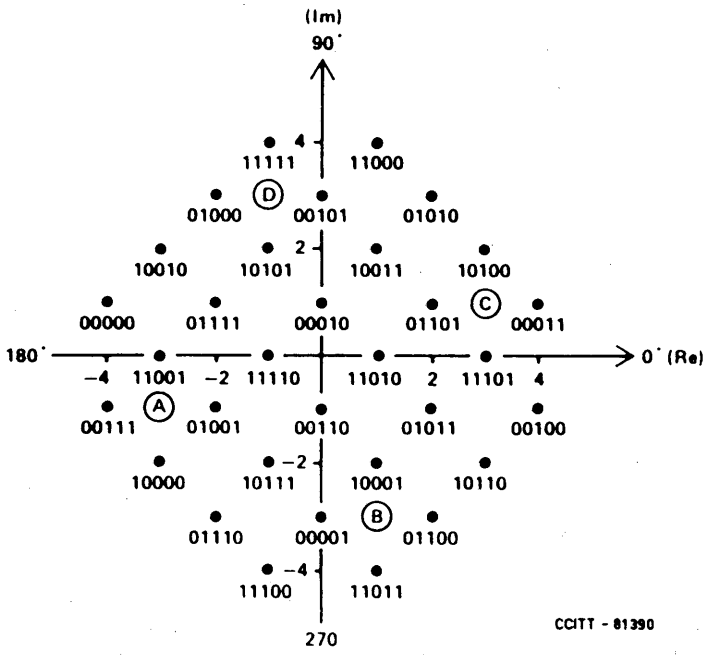
Differential encoding for use with trellis coded alternative at 9600 bit/s

Inputs		Previous outputs		Outputs	
$Q1_n$	$Q2_n$	$Y1_{n-1}$	$Y2_{n-1}$	$Y1_n$	$Y2_n$
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	1	0	1

TABLE 3/V.32

The two alternative signal-state mappings for 9600 bit/s

Coded inputs (see Table 1/V.32 or Table 2/V.32 with Figure 2/V.32)					Nonredundant coding		Trellis coding	
(Y0)	Y1	Y2	Q3	Q4	Re	Im	Re	Im
0	0	0	0	0	−1	−1	−4	1
	0	0	0	1	−3	−1	0	−3
	0	0	1	0	−1	−3	0	1
	0	0	1	1	−3	−3	4	1
	0	1	0	0	1	−1	4	−1
	0	1	0	1	1	−3	0	3
	0	1	1	0	3	−1	0	−1
	0	1	1	1	3	−3	−4	−1
	1	0	0	0	−1	1	−2	3
	1	0	0	1	−1	3	−2	−1
	1	0	1	0	−3	1	2	3
	1	0	1	1	−3	3	2	−1
	1	1	0	0	1	1	2	−3
	1	1	0	1	3	1	2	1
	1	1	1	0	1	3	−2	−3
	1	1	1	1	3	3	−2	1
1	0	0	0	0			−3	−2
	0	0	0	1			1	−2
	0	0	1	0			−3	2
	0	0	1	1			1	2
	0	1	0	0			3	2
	0	1	0	1			−1	2
	0	1	1	0			3	−2
	0	1	1	1			−1	−2
	1	0	0	0			1	4
	1	0	0	1			−3	0
	1	0	1	0			1	0
	1	0	1	1			1	−4
	1	1	0	0			−1	−4
	1	1	0	1			3	0
	1	1	1	0			−1	0
	1	1	1	1			−1	4



The binary numbers denote YO_n $Y1_n$ $Y2_n$ $Q3_n$ $Q4_n$

FIGURE 3/V.32

32-point signal structure with trellis coding for 9600 bit/s and states A B C D used at 4800 bit/s and for training

TABLE 4/V.32

Interchange circuit (see Note 1)		Notes
No.	Description	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	
106	Ready for sending	
107	Data set ready	
108/1 or	Connect data set to line	2
108/2	Data terminal ready	2
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	3
112	Data signalling rate selector (DCE source)	3
113	Transmitter signal element timing (DTE source)	5
114	Transmitter signal element timing (DCE source)	6
115	Receiver signal element timing (DCE source)	6
125	Calling indicator	4
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 – All interchange circuits which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.8).

Note 2 – This circuit shall be capable of operation as circuit 108/1 or circuit 108/2 depending on its use. Operation of circuits 107 and 108/1 shall be in accordance with § 4.4 of Recommendation V.24.

Note 3 – This circuit is not essential when only one data signalling rate is implemented in the modem.

Note 4 – This circuit is for use with the general switched telephone network only.

Note 5 – When the modem is not operating in a synchronous mode at the interface, any signals on this circuit shall be disregarded. Many DTEs operating in an asynchronous mode do not have a generator connected to this circuit.

Note 6 – When the modem is not operating in a synchronous mode at the interface, this circuit shall be clamped to the OFF condition. Many DTEs operating in an asynchronous mode do not terminate this circuit.

3.7 *Circuit 109*

OFF to ON and ON to OFF transitions of circuit 109 should occur solely in accordance with the operating sequences defined in § 5. Thresholds and response times are inapplicable because a line signal detector cannot be expected to distinguish wanted received signals from unwanted talker echoes.

3.8 *Electrical characteristics of interchange circuits*

3.8.1 Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.9 *Fault condition on interchange circuits*

See § 7 of Recommendation V.28 for association of the receiver failure detection types.

3.9.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.9.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.9.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Scrambler and descrambler

A self-sychronizing scrambler/descrambler shall be included in the modem. Each transmission direction uses a different scrambler. The method of allocating the scramblers/descramblers is described in § 4.1. According to the direction of transmission, the generating polynomial is:

Call mode modem generating polynomial: (GPC) $= 1 + x^{-18} + x^{-23}$, or

Answer mode modem generating polynomial: (GPA) $= 1 + x^{-5} + x^{-23}$

At the transmitter, the scrambler shall effectively divide the message data sequence by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. At the receiver the received data sequence shall be multiplied by the scrambler generating polynomial to recover the message sequence.

4.1 *Scrambler/descrambler allocation*

4.1.1 *General switched telephone network (GSTN)*

On the general switched telephone network, the modem at the calling data station (call mode) shall use the scrambler with the GPC generating polynomial and the descrambler with the GPA generating polynomial. The modem at the answering data station (answer mode) shall use the scrambler with the GPA generating polynomial and the descrambler with the GPC generating polynomial. In some situations, however, such as when calls are established on the GSTN by operators, bilateral agreement on call mode/answer mode allocation will be necessary.

4.1.2 *Point-to-point leased circuits*

Scrambler/descrambler allocation and call mode and answer mode designation on point-to-point leased circuits will be by bilateral agreement between Administrations or users.

5 Operating procedures

5.1 *Recommendation V.25 automatic answering sequence*

The Recommendation V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted on point-to-point leased circuits or on national connections on the GSTN where permitted by Administrations. In this event, the answer mode modem shall initiate transmission as in the retrain procedure specified in § 5.5.

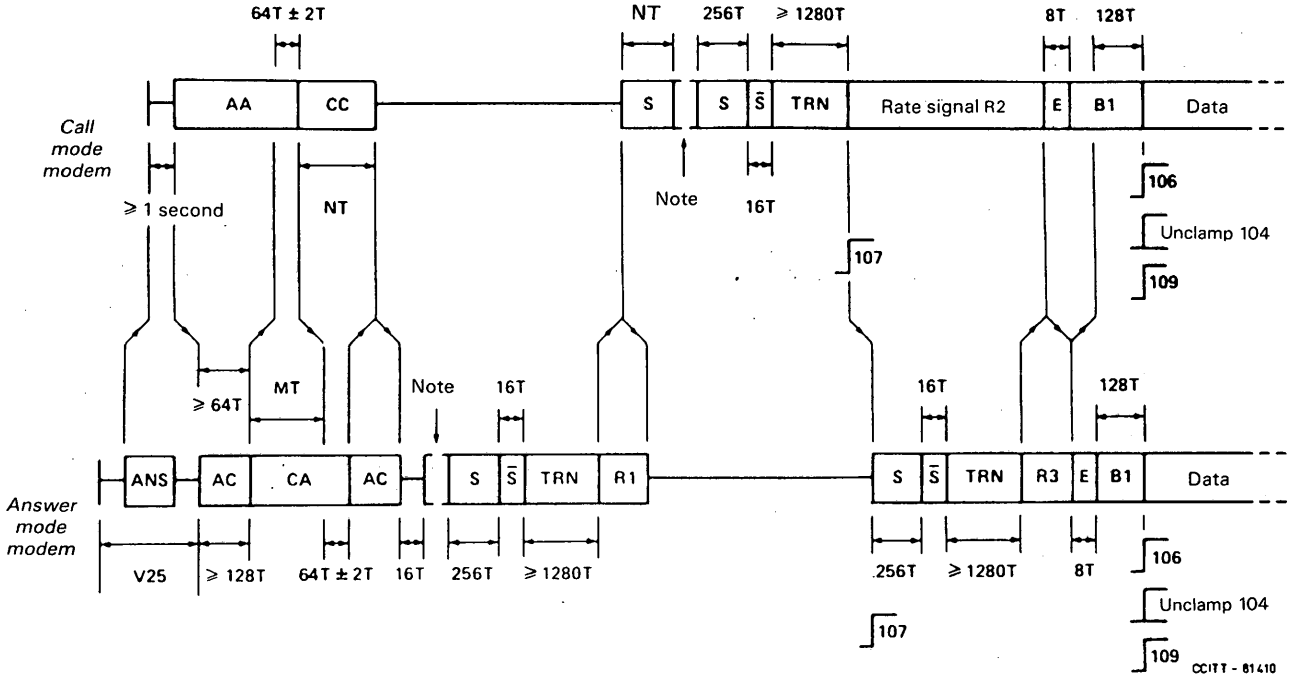
5.2 *Receiver conditioning signal*

The receiver conditioning signal shall be used in the start-up and retrain procedures defined in §§ 5.4 and 5.5 below. The signal consists of three segments:

5.2.1 Segment 1, denoted by S in Figures 4/V.32 and 5/V.32, consists of alternations between states A and B as shown in Figure 1/V.32, for a duration of 256 symbol intervals.

5.2.2 Segment 2, denoted by $\bar{S}$ in Figures 4/V.32 and 5/V.32, consists of alternations between states C and D as shown in Figure 1/V.32, for a duration of 16 symbol intervals.

The transition from segment 1 to segment 2 provides a well-defined event in the signal that may be used for generating a time reference in the receiver.

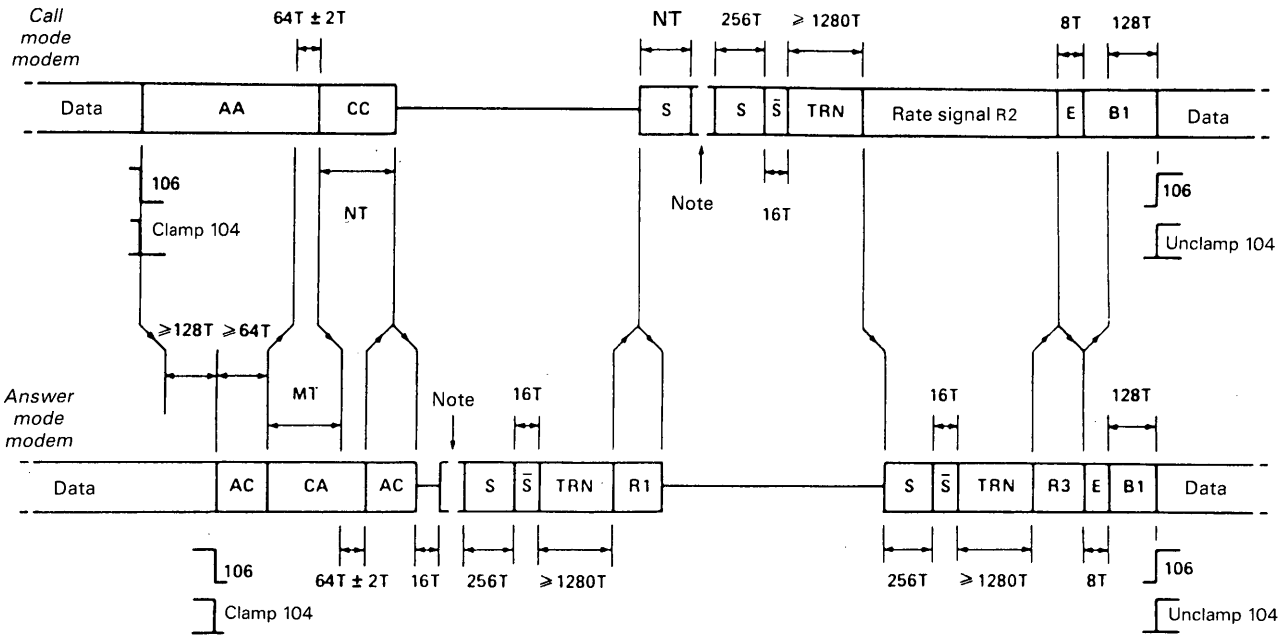


AC Signal states ACAC..AC for an even number of symbol intervals T; similarly with CA, AA and CC.
MT, NT Round-trip delays observed from answer and call modems respectively, including 64T ± 2T modem turn round delay.
S, $\bar{S}$ Signal states ABAB..AB, CDCD..CD.
TRN Scrambled ones at 4800 bit/s with dibits encoded directly to states A, B, C and D as defined in § 5.2.3.
R1, R2, R3 Each a repeated 16-bit rate sequence at 4800 bit/s scrambled and differentially encoded as in Table 1/V.32.
E A single 16-bit sequence marking and following the end of a whole number of 16-bit rate sequences in R2 and R3.
B1 Binary ones scrambled and encoded as for the subsequent transmission of data.

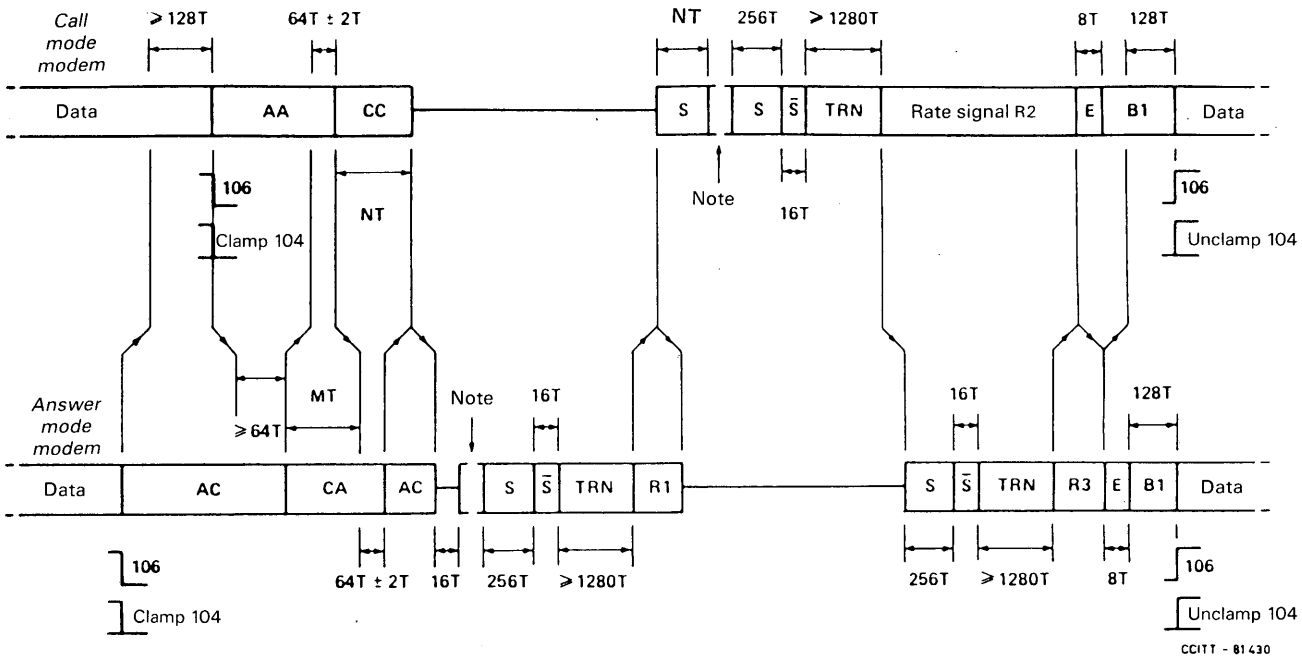
Note — The inclusion of a special echo canceller training sequence at this point is optional (see § 5.4, Note 3).

FIGURE 4/V.32

Start-up procedure



a) Retrain initiated by the calling modem



b) Retrain initiated by the answering modem

AC Signal states ACAC..AC for an even number of symbol intervals T; similarly with CA, AA and CC.
MT, NT Round-trip delays observed from answer and call modems respectively, including 64T ± 2T symbol intervals modem turn round delay.
S, $\bar{S}$ Signal states ABAB..AB, CDCD..CD.
TRN Scrambled ones at 4800 bit/s with dibits encoded directly to states A, B, C and D as defined in § 5.2.3.
R1, R2, R3 Each a repeated 16-bit rate sequence at 4800 bit/s scrambled and differentially encoded as in Table 1/V.32.
E A single 16-bit sequence marking and following the end of a whole number of 16-bit rate sequences in R2 and R3.
B1 Binary ones scrambled and encoded as for the subsequent transmission of data.

Note — The inclusion of a special echo canceller training sequence at this point is optional (see § 5.4, Note 3).

FIGURE 5/V.32

5.2.3 Segment 3, denoted by TRN in Figures 4/V.32 and 5/V.32, is a sequence derived by scrambling binary ones at a data rate of 4800 bit/s with the scrambler defined in § 4. During the transmission of this segment, the differential quadrant encoding shall be disabled. The initial state of the scrambler shall be all zeros, and a binary one applied to the input for the duration of segment 3. Successive dibits are encoded onto transmitted signal states.

The first 256 transmitted signal states are determined from the state of the first bit occurring (in time) in each dibit. When this bit is ZERO, signal state A is transmitted; when this bit is ONE, signal state C is transmitted. Depending on whether the modem is in call or answer mode, the scrambler output patterns and corresponding signal states will then begin as below, where the bits and the signal states are shown in time sequence from left to right.

Call mode modem:

GPC: 11 11 11 11 11 11 11 11 11 00 00 01 11 11 11
C C C C C C C C C A A A C C C

Answer mode modem:

GPA: 11 11 10 00 00 11 11 10 00 00 11 10 01 11 11
C C C A A C C C A A C C A C C

Immediately after 256 such symbols, successive scrambled dibits are encoded onto transmitted signal states in accordance with Table 5/V.32 directly without differential encoding for the remainder of segment 3. The duration of segment 3 shall be at least 1280 and not exceed 8192[1] symbol intervals.

Segment 3 is intended for training the adaptive equaliser in the receiving modem and the echo canceller in the transmitting modem.

TABLE 5/V.32

Encoding for TRN segment after the first 256 symbols

Dibit	Signal state
00	A
01	B
11	C
10	D

Note – Signal states A, B, C and D are shown in Figure 1/V.32.

5.3 *Rate signal*

The rate signal consists of a whole number of repeated 16-bit binary sequences, as defined in Table 6/V.32, scrambled and transmitted at 4800 bit/s with dibits differentially encoded as in Table 1/V.32. The differential encoder shall be initialized using the final symbol of the transmitted TRN segment.

The first two bits and each successive dibit of the rate sequence shall be encoded to form the transmitted signal states.

The first transmitted octet, B0-B7, is fully defined in Table 6/V.32 and shall be interpreted by all Recommendation V.32 modems; the second octet, B8-B15, includes some codes defined in the table, some to be defined later and others to be left undefined for use by manufacturers.

[1] The maximum duration of 8192 symbol intervals is for further study.

TABLE 6/V.32

Coding of the 16-bit rate sequence

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	10	11	12	13	14	15	B0	B1	B2	B3	B4	etc.
0	0	0	0	–	–	–	1	–	–	–	1	–	–	–	1	0	0	0	0	–	

B0-3, B7, 11, 15	For synchronizing on a received rate signal
B4	1 denotes ability to receive data at 2400 bit/s
B5	1 denotes ability to receive data at 4800 bit/s
B6	1 denotes ability to receive data at 9600 bit/s
B4-6	0 0 0 calls for a GSTN cleardown
B8	1 denotes availability of trellis coding/decoding at the highest data rate indicated in B4-6
B9-14	0 0 1 0 0 0 denotes absence of special operational modes

Note – The remaining codes may be allocated within Recommendation V.32 in the future.

5.3.1 *Detecting a rate signal*

The minimum requirement for detection is the receipt of two consecutive identical 16-bit sequences each with bits B0-3, B7, 11 and 15 conforming to Table 6/V.32.

5.3.2 *Ending the rate signal*

In order to mark the end of transmission of any rate signal other than R1 (Figure 4/V.32), the modem shall first complete the transmission of the current 16-bit rate sequence, and then transmit one 16-bit sequence E, coded as shown in Table 7/V.32.

TABLE 7/V.32

Coding of signal E

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	10	11	12	13	14	15
1	1	1	1	–	–	–	1	–	–	–	1	–	–	–	1

B4-14	As in Table 6/V.32, except that the only data rate and coding to be indicated shall relate to the transmission of scrambled binary ones immediately following signal E

5.4 *Start-up procedure*

The procedure for achieving synchronism between the calling modem and the answering modem on international GSTN connections is shown in Figure 4/V.32. The procedure includes the estimating of round-trip delay from each modem, the training of echo cancellers and receivers initially with half-duplex transmissions, and the exchanging of rate signals for automatic bit-rate and mode selection.

5.4.1 *Call mode modem*

After receiving the answer tone for a period of at least 1 s as specified in Recommendation V.25, the modem shall be connected to line (see Note 1 below) and shall condition the scrambler and descrambler in accordance with § 4.1.

The modem shall repetitively transmit carrier state A as shown in Figure 1/V.32.

The modem shall be conditioned to detect (see Note 2 below) one of two incoming tones at frequencies 600 ± 7 Hz and 3000 ± 7 Hz, and subsequently to detect a phase reversal in that tone.

On detection of one such phase reversal, the modem shall be conditioned to detect a second phase reversal in the same tone, start a counter/timer and change to repetitively transmitting state C as shown in Figure 1/V.32. The time delay between the reception of this phase reversal at the line terminals and the transmitted AA to CC transition appearing at the line terminals shall be 64 ± 2 symbol periods.

On detection of a second phase reversal in the same incoming tone, the modem shall stop the counter/timer and cease transmitting.

When the modem detects an incoming S sequence (see § 5.2), it shall proceed to train its receiver, and then seek to detect at least two consecutive identical 16-bit rate sequences as defined in Table 6/V.32.

On detection of the rate signal (R1), the modem shall transmit an S sequence for a period NT already estimated by the counter/timer.

After this period has expired (see Note 3 below), the modem shall transmit the receiver conditioning signal as defined in § 5.2, starting with an S sequence for 256 symbol intervals.

Transmission of the TRN segment of the receiver conditioning signal may be extended in order to ensure a satisfactory level of echo cancellation (see Note 4 below).

After the TRN segment, the modem shall apply an ON condition to circuit 107 and transmit a rate signal (R2) in accordance with § 5.3 to indicate the currently available data rates and whether trellis coding and/or other special operational modes are available. R2 shall exclude rates and operational modes not appearing in the previously received rate signal R1. It is recommended that R2 should also take account of the likely receiver performance with the particular GSTN connection. If it appears that satisfactory performance cannot be attained at any of the available data rates, then R2 should be used to call for a GSTN cleardown in accordance with Table 6/V.32.

Transmission of R2 shall continue until an incoming rate signal R3 is detected. The modem shall then, after completing its current 16-bit rate sequence, transmit a single 16-bit sequence E in accordance with § 5.3.2 indicating the data rate, coding and any special operational modes called for in R3. If, however, R3 is calling for a GSTN cleardown in accordance with Table 6/V.32, then the call modem shall disconnect from line and effect a cleardown.

The modem shall then transmit continuous scrambled binary ones at the data rate and with the coding called for in R3, and apply the appropriate condition to circuit 112. If trellis coding according to § 2.4.1.2 is to be used, the initial states of the delay elements of the convolution encoder shown in Figure 2/V.32 should be set to zero.

On detecting an incoming 16-bit E sequence as defined in § 5.3.2, the modem shall condition itself to receive data at the rate and with the coding indicated by the incoming E sequence. After a delay of 128 symbol intervals, it shall apply an ON condition to circuit 109, and unclamp circuit 104.

The modem shall then enable circuit 106 to respond to the condition of circuit 105 and be ready to transmit data.

5.4.2 *Answer mode modem*

On connection to line, the modem shall condition the scrambler and descrambler in accordance with § 4.1, and transmit the Recommendation V.25 answer sequence. Means, defined in Recommendation V.25, of disabling network echo cancellers and/or truncating the answer tone may be employed.

After the Recommendation V.25 answer sequence, the modem shall transmit alternate carrier states A and C as shown in Figure 1/V.32.

After alternate states A and C have been transmitted for an even number of symbol intervals greater than or equal to 128 *and* an incoming tone has been detected at 1800 ± 7 Hz for 64 symbol periods (see Note 5 below), the modem shall be conditioned to detect a phase reversal in the incoming tone, start a counter/timer, and change to transmitting alternate carrier states C and A for an even number of symbol intervals.

On detecting a phase reversal in the incoming tone, the modem shall stop the counter/timer and, after transmitting a state A, revert to transmitting alternate states A and C. The time delay between the reception of this phase reversal at the line terminals and the transmitted CA to AC transition appearing at the line terminals shall be 64 ± 2 symbol periods.

When an amplitude drop is detected in the incoming tone, the modem shall cease transmitting for a period of 16 symbol intervals and then (see Note 3) transmit the receiver conditioning signal as defined in § 5.2.

Transmission of the TRN segment of the receiver conditioning signal may be extended in order to ensure a satisfactory level of echo cancellation (see Note 4).

After the TRN segment, the modem shall transmit a rate signal (R1) in accordance with § 5.3 to indicate the data rates, coding and any special operational modes currently available in the answer modem and associated DTE.

On detection of an incoming S sequence, the modem shall cease transmitting.

The modem shall wait for a period MT already estimated by the counter/timer and then, if an incoming S sequence persists, or when an S sequence reappears (see Note 3), the modem shall proceed to train its receiver.

After training its receiver, the modem shall seek to detect at least two consecutive identical incoming 16-bit rate sequences as defined in § 5.3.

On detection of a rate signal (R2), the modem shall apply an ON condition to circuit 107 and transmit a second receiver conditioning signal as defined in § 5.2.

After the TRN segment, the modem shall transmit a second rate signal (R3) in order to indicate the data rate, coding and any special operational modes to be used by both modems. The data rate and operational modes selected by R3 shall be within those indicated by R2. It is recommended that R3 should also take account of the likely performance of the answer modem receiver with the particular GSTN connection established. If R2 is calling for a GSTN cleardown (see Table 6/V.32) and/or if it appears that satisfactory performance cannot be attained by the answer modem at any of the available data rates, then R3 should call for a GSTN cleardown, in accordance with Table 6/V.32.

When the modem detects an incoming 16-bit E sequence as defined in § 5.3.2, it shall condition itself to receive data at the rate and with the coding indicated by the E sequence.

The modem shall complete the current 16-bit rate sequence and then transmit a single 16-bit E sequence indicating the data rate and coding to be used in the subsequent transmission of scrambled binary ones. If trellis coding according to § 2.4.1.2 is to be used, then the initial states of the delay elements of the convolution encoder shown in Figure 3/V.32 should be set to zero.

The modem shall transmit scrambled binary ones for 128 symbol intervals, then enable circuit 106 to respond to the condition of circuit 105 and be ready to transmit data.

The modem shall also apply an ON condition to circuit 109 and unclamp circuit 104.

Note 1 – Once an incoming tone is detected at 600 ± 7 Hz or 3000 ± 7 Hz, the calling modem should proceed with the start-up sequence even if no 2100 Hz tone has been detected.

Note 2 – In some cases, the incoming tones may be preceded by a special pattern which may last up to 294 ms (see Appendix I).

Note 3 – The TRN segment in the receiver conditioning signal is suitable for training the echo canceller in the transmitting modem. Alternatively, it is acceptable to precede the receiver conditioning signal by a sequence which can be used specifically for training the echo canceller, but which need not be defined in detail in the Recommendation. The echo cancellation sequence (if used) must maintain energy transmitted to line to hold network echo control devices disabled (as required). In order to avoid confusion with Segments 1 or 2 of the receiver conditioning signal defined in § 5.2, the echo cancellation sequence shall produce a transmitted signal such that the sum of its power in the three 200 Hz bands centred at 600 Hz, 1800 Hz and 3000 Hz is at least 1 dB less than its power in the remaining bandwidth. This applies for the relative power averaged over any 6 ms time interval. The duration of this signal must not exceed 8192[2)] symbol intervals.

Note 4 – Manufacturers are cautioned that a period of 650 ms is needed for training any network echo cancellers conforming to Recommendation G.165, that may be encountered on GSTN connections.

[2)] The maximum duration of 8192 symbol intervals is for further study.

Note 5 – The answering modem may disconnect from the line if the 1800 ± 7 Hz tone is not detected following transmission of the segment AC. However, to assure compatibility with manual originating data stations, it shall not disconnect for at least 3 seconds after the segment AC has been transmitted.

5.5 *Retrain procedure*

A retrain may be initiated during data transmission if either modem incorporates a means of detecting unsatisfactory signal reception. Figure 5a/V.32 shows a retrain event initiated by the calling modem and Figure 5b/V.32 shows a retrain event initiated by the answering modem. The procedure is as follows:

5.5.1 *Call mode modem*

Following detection of unsatisfactory signal reception or detection of one of two tones at frequencies 600 ± 7 Hz and 3000 ± 7 Hz for more than 128 symbol intervals, the modem shall turn OFF circuit 106, clamp circuit 104 to binary one and repetitively transmit carrier state A as shown in Figure 1/V.32. It shall then proceed in accordance with § 5.4.1 beginning with the third paragraph (see Note in § 5.5.2).

5.5.2 *Answer mode modem*

Following detection of unsatisfactory signal reception or detection of a tone of frequency 1800 ± 7 Hz for more than 128 symbol intervals, the modem shall turn OFF circuit 106, clamp circuit 104 to binary one and transmit alternate carrier states A and C for an even number of symbol intervals not less than 128. It shall then proceed in accordance with § 5.4.2 beginning with the third paragraph (see Note).

Note – During a retrain, circuit 107 should remain ON.

(The need for a shorter duplex retrain procedure to provide for rapid training of the modem receivers is for further study.)

5.5.3 *Operation of circuit 109 during retrain procedure*

Circuit 109 shall be maintained in the ON condition except that the OFF condition may optionally be applied if transmission of the AA segment in the Call modem or of the first AC segment in the Answer modem continues for a period exceeding 45 seconds. If the retrain procedure is subsequently completed, the ON condition shall be re-applied to circuit 109 at the time that circuit 104 is unclamped.

6 Testing facilities

Test loops 2 and 3 as defined in Recommendation V.54 should be provided. Provision for test loop 2 shall be as specified for point-to-point circuits.

7 Asynchronous to synchronous conversion protocol – Modes of operation

The modem can be configured for the following modes of operation (modes 2 and 4 are optional):

Mode 1 9600 bit/s ±0.01% synchronous

Mode 2 9600 bit/s start-stop 8, 9, 10 or 11 bits per character

Mode 3 4800 bit/s ±0.01% synchronous

Mode 4 4800 bit/s start-stop 8, 9, 10 or 11 bits per character

7.1 *Transmitter*

7.1.1 In the synchronous modes of operation, the modem shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or circuit 114. The data shall then be scrambled in accordance with § 4 and then passed to the modulator for encoding in accordance with § 2.4.

7.1.2 In the start-stop modes, the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of 9600 or 4800 bit/s per second. The start-stop data to be transmitted shall be converted in conformity with Recommendation V.14 to a synchronous data stream suitable for transmission in accordance with § 7.1.1.

7.2 *Receiver*

Demodulated data shall be decoded in accordance with § 2.4, then descrambled in accordance with § 4 and then passed to the converter in conformity with Recommendation V.14 for regaining the data stream of start-stop characters.

The intracharacter signalling rate provided to the DTE over circuit 104 shall be in the ranges given in Table 8/V.32 when operating in the basic, or in the extended signalling rate ranges, respectively.

TABLE 8/V.32

Intracharacter signalling rate range

Data rate	Signalling rate range	
	Basic	Extended
9600 bit/s 4800 bit/s	9600 to 9696 bit/s 4800 to 4848 bit/s	9600 to 9821 bit/s 4800 to 4910 bit/s

APPENDIX I

(to Recommendation V.32)

Interworking procedure for echo cancelling modems

Considering

– that the V.26 *ter* modem at 2400 bit/s and the V.32 modems at 9600 bit/s and 4800 bit/s are based on the same technique, referred to as echo cancellation;

– that the 1800 Hz carrier frequency is the same for the two modems;

– that there may be a need for a modem, referred to as multimode, able to interwork with V.26 *ter* and V.32 modems;

– that the determination of round-trip delay may be useful in some cases,

the handshaking operating sequence defined in the following paragraphs is provided for the information of manufacturers.

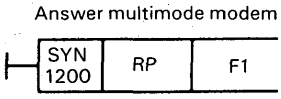
I.1 *Interworking of echo cancelling modems*

The V.32 modems at 9600 bit/s and 4800 bit/s and the V.26 *ter* modems at 2400 bit/s could interwork with a dedicated multimode modem implementing both V.32 and V.26 *ter* capabilities, as illustrated in Table I-1/V.32.

TABLE I-1/V.32

Handshaking compatibility

Calling \ Answering	V.26 *ter*	V.32	M (Multimode)
V.26 *ter*	SYN 1200 / SYN 1200	F1 Disconnect / No energy	SYN 1200 then F1 (Note) / SYN 1200
V.32	F2 Wait at least T1 = 300 ms / SYN 1200 disconnect	F1 / F2	SYN 1200 then F1 (Note)
M (Multimode)	SYN 1200 / SYN 1200	F1 / Detected transmit F2	SYN 1200 then F1 (Note) / F2 or SYN 1200



CCITT - 85680

F1 : tones at 600 ± 7 Hz and 3000 ± 7 Hz generated by alternately transmitting carrier states A and C.
F2: tone at 1800 ± 7 Hz generated by repetitively transmitting carrier state A.

Note — The modem M is distinguished by a special rate pattern.

I.1.1 *Operation of the calling multimode modem*

The modem will recognize:

- A V.26 *ter* modem by detecting the 1200 baud synchronization signals followed by a rate pattern and then will proceed as defined in V.26 *ter* (see Figure I-1/V.32).
- V.32 modems by the detection of one of two incoming tones at frequencies 600 ± 7 Hz and 3000 ± 7 Hz (see Figure I-2/V.32). It will then proceed as defined in § 5.4.1.
- A multimode modem by the detection of a special rate pattern assigned to the multimode modem. It will transmit, as shown in Figure I-3/V.32, repetitively carrier state A or the synchronizing signals followed by the rate pattern, according to the selected mode of operation: V.32 or V.26 *ter* respectively.

I.1.2 *Operation of the answering multimode modem*

After the V.25 sequence, the modem will transmit the 1200 baud synchronizing signals followed by its special rate pattern, and then alternate carrier states A and C as defined in Recommendation V.32.

It will recognize during the transmission of these alternate carrier states A and C:

- a V.26 *ter* modem by the detection of the 1200 baud synchronizing signals followed by a rate pattern. It will stop transmitting alternate carrier states A and C and proceed according to Recommendation V.26 *ter* (see Figure I-4/V.32);
- V.32 modems by recognizing a tone at 1800 ± 7 Hz and will then proceed as defined in Recommendation V.32 (see Figure I-5/V.32).

The case of multimode modems on both answering and calling sides has been considered in § I.1.1.

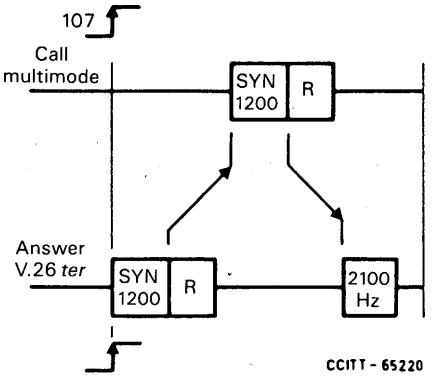


FIGURE I-1/V.32

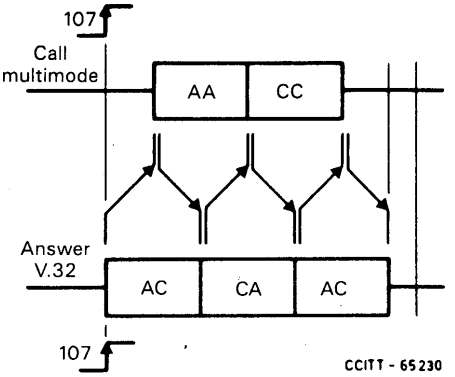


FIGURE I-2/V.32

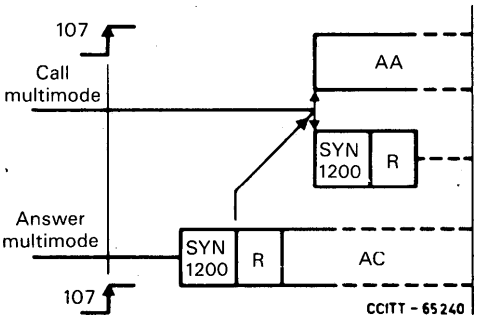


FIGURE I-3/V.32

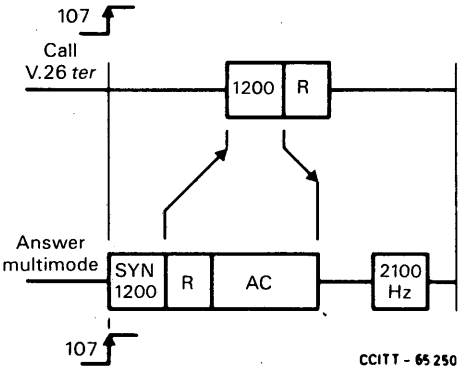


FIGURE I-4/V.32

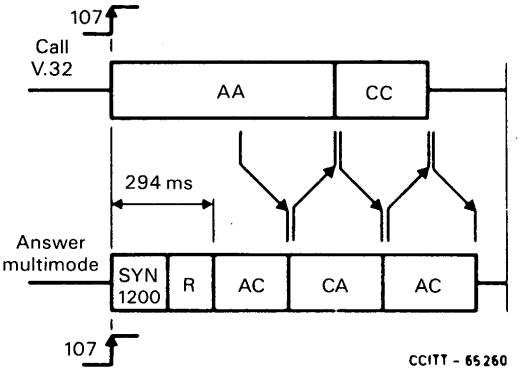


FIGURE I-5/V.32

14 400 BITS PER SECOND MODEM STANDARDIZED FOR USE ON POINT-TO-POINT 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Melbourne, 1988)

1 Introduction

This modem is intended to be used primarily on special quality leased circuits, e.g. Recommendation M.1020 [1] or M.1025 [2] circuits but this does not preclude the use of this modem over circuits of lower quality at the discretion of the administration concerned (see Notes 1 and 2).

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the administrations and users, this Recommendation in no way restricts the use of any other modems.

The principal characteristics of this modem are as follows:

a) fallback rate of 12 000 bits per second;

b) capable of operating in a duplex mode with continuous carrier;

c) combined amplitude and phase modulation with synchronous mode of operation;

d) inclusion of an eight state trellis coded modulation;

e) optional inclusion of a multiplexer for combining data rates of 12 000, 9600, 7200, 4800 and 2400 bits per second (see Note 3).

Note 1 – The principal use of this recommended modem is on 4-wire leased circuits. Other applications, such as stand-by operation on the switched telephone network, half duplex or multipoint operation are for further study. Circuits should be of the special quality type, e.g. M.1020 [1] or M.1025 [2]. However, administrations and users may wish to note that modems conforming to this Recommendation, even assuming proper implementations, will not necessarily operate satisfactorily on all circuits conforming to M.1020 and M.1025; particularly where noise is at or near the specified limiting magnitude.

Note 2 – Attention should be given to the selection of appropriate equalization techniques in the modem implementation, if acceptable performance on circuits conforming to Recommendation M.1025 is desired.

Note 3 – When the multiplexer option is installed, provisions in section 10 may supersede provisions given in other sections.

2 Line signals

2.1 The carrier frequency is to be 1800 ± 1 Hz. The power levels used will conform to Recommendation V.2.

2.2 *Signal space coding*

2.2.1 At 14 400 bits per second, the scrambled data stream to be transmitted is divided into groups of six consecutive data bits. As shown in Figure 1/V.33, the first two bits in time $Q1_n$ and $Q2_n$ in each group, are first differentially encoded into Y1 and Y2 according to Table 1A/V.33. The two differentially encoded bits $Y1_n$ and $Y2_n$ are used as input to a systematic convolutional encoder which generates a redundant bit $Y0_n$. This redundant bit and the six information-carrying bits $Y1_n$, $Y2_n$, $Q3_n$, $Q4_n$, $Q5_n$ and $Q6_n$ are then mapped into the coordinates of the signal element to be transmitted according to the signal space diagram shown in Figure 2/V.33.

2.2.2 At the fallback rate of 12 000 bit/s, the scrambled data stream to be transmitted is divided into groups of five consecutive data bits. The trellis coding scheme shown in Figure 1/V.33, is used with the modification that first, the line designated by $Q6_n$ is removed and second, the signal element mapping is now as shown in Figure 3/V.33.

2.2.3 Table 1B/V.33 describes the differential encoding used for the 4800 bit/s rate signal in segment 3 of synchronizing signals (§ 8.3).

TABLE 1A/V.33

Differential encoding for use with trellis coding

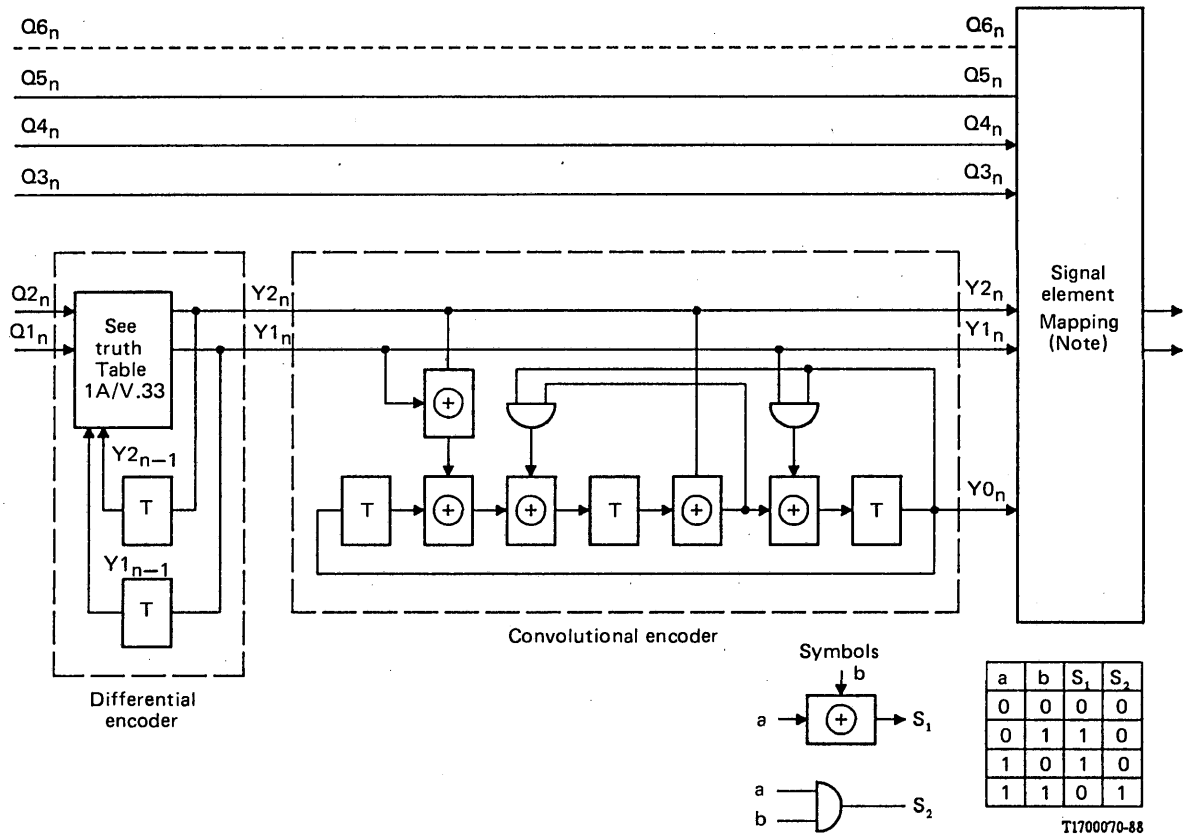
Inputs		Previous outputs		Outputs	
$Q1_n$	$Q2_n$	$Y1_{n-1}$	$Y2_{n-2}$	$Y1_n$	$Y2_n$
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	1	0	1

TABLE 1B/V.33

Differential quadrant coding for 4800 bit/s rate signal

Inputs		Previous outputs		Phase quadrant	Outputs		Signal element for 4800 bit/s	Coordinates	
$Q1_n$	$Q2_n$	$Y1_{n-1}$	$Y2_{n-1}$		$Y1_n$	$Y2_n$		Re	Im
0	0	0	0	+90°	0	1	D	−2	+6
0	0	0	1		1	1	A	−6	−2
0	0	1	0		0	0	C	+6	+2
0	0	1	1		1	0	B	+2	−6
0	1	0	0	0°	0	0	C	+6	+2
0	1	0	1		0	1	D	−2	+6
0	1	1	0		1	0	B	+2	−6
0	1	1	1		1	1	A	−6	−2
1	0	0	0	+180°	1	1	A	−6	−2
1	0	0	1		1	0	B	+2	−6
1	0	1	0		0	1	D	−2	+6
1	0	1	1		0	0	C	+6	+2
1	1	0	0	+270°	1	0	B	+2	−6
1	1	0	1		0	0	C	+6	+2
1	1	1	0		1	1	A	−6	−2
1	1	1	1		0	1	D	−2	+6

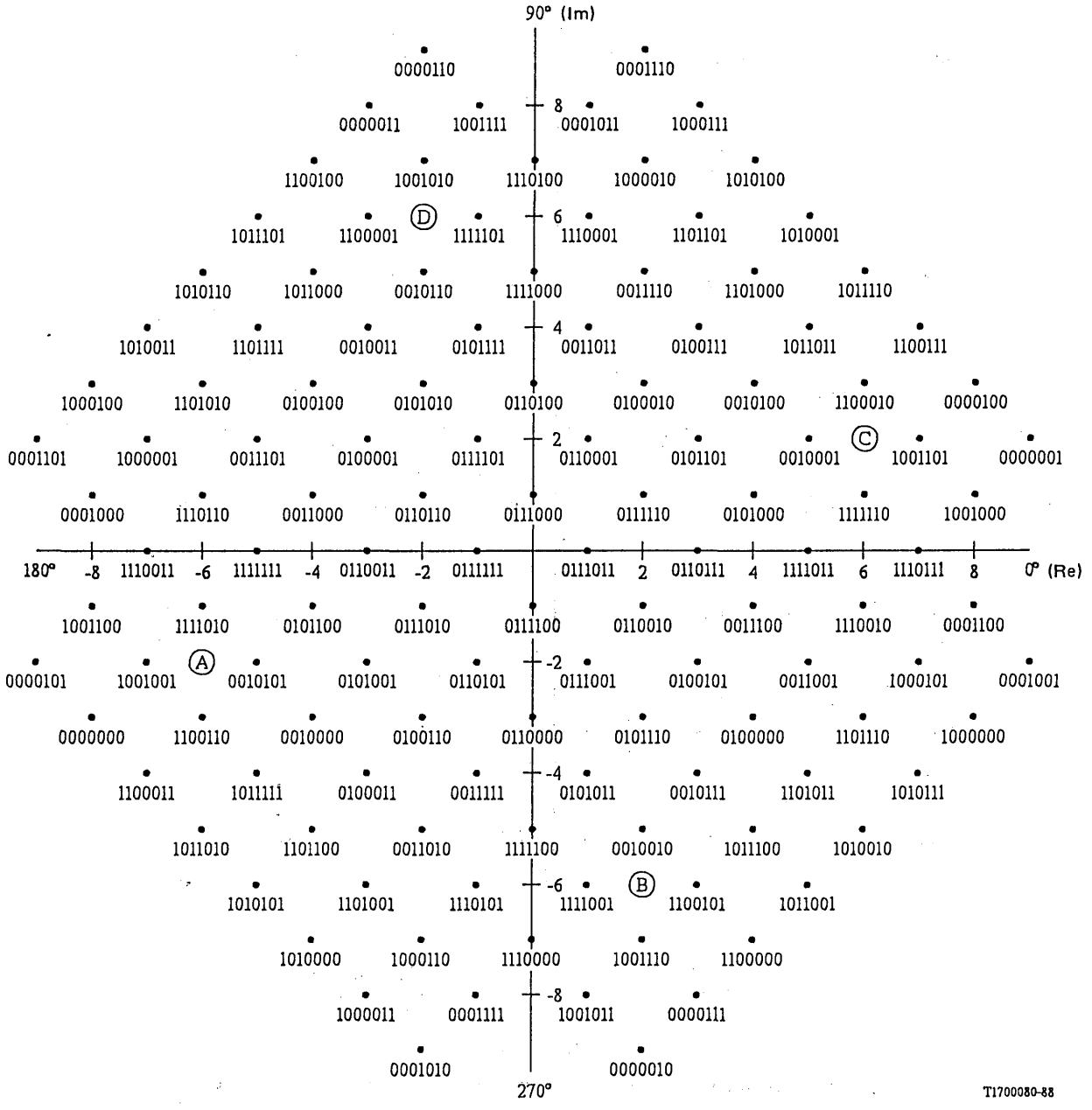
Note – Q1 is the first bit in time.



Note – See Figure 2/V.33 for 14 400 bit/s rate, Figure 3/V.33 for 12 000 bit/s.

FIGURE 1/V.33

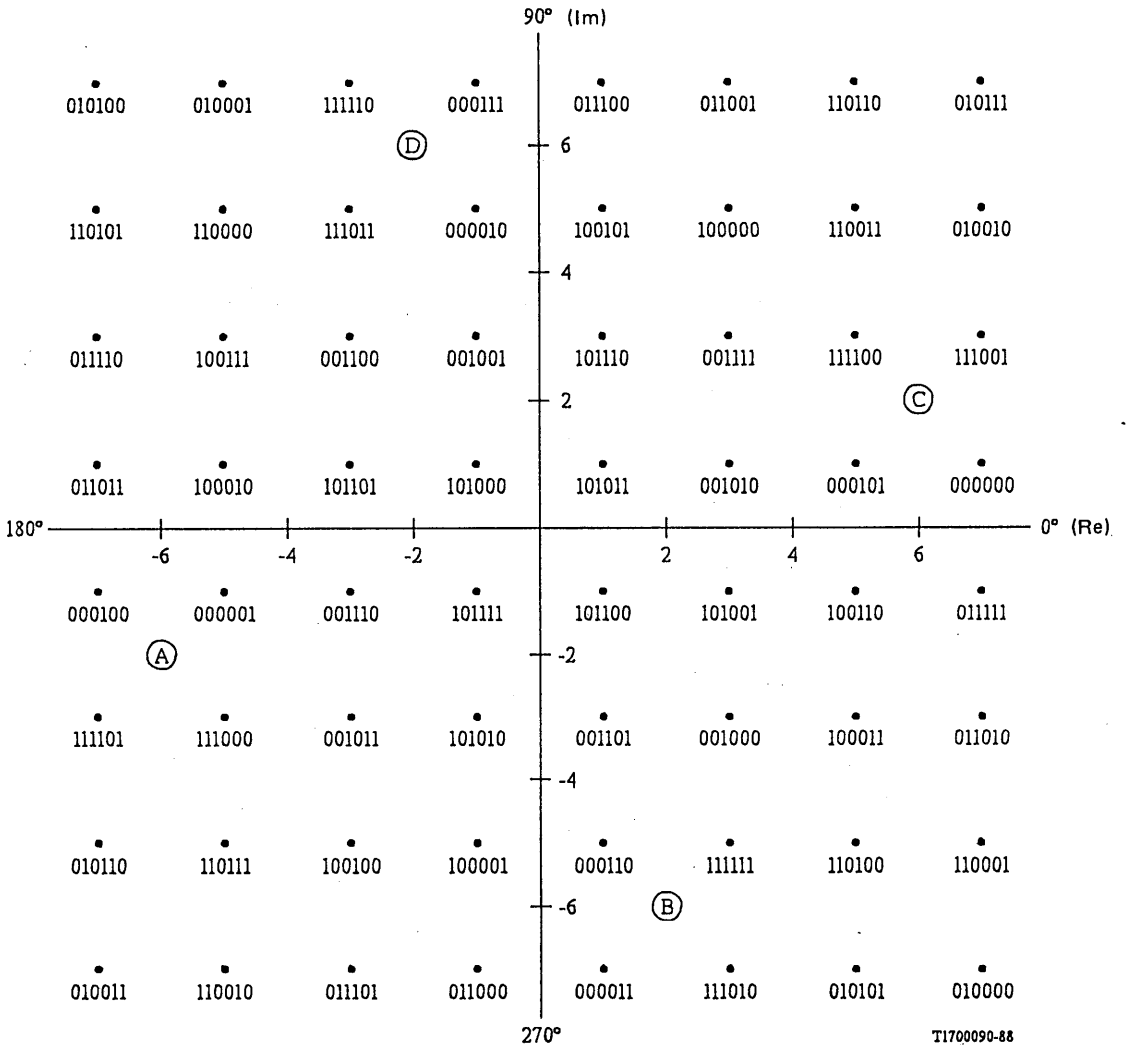
Trellis coder at 14 400 bit/s and 12 000 bit/s



Binary numbers refer to $Q6_n$, $Q5_n$, $Q4_n$, $Q3_n$, $Y2_n$, $Y1_n$, $Y0_n$,
A, B, C, D refer to synchronizing signal elements

FIGURE 2/V.33

Signal space diagram and mapping for trellis-coded modulation at 14 400 bit/s



Binary numbers refer to $Q5_n$, $Q4_n$, $Q3_n$, $Y2_n$, $Y1_n$, $Y0_n$,
A, B, C, D refer to synchronizing signal elements

FIGURE 3/V.33

Signal space diagram and mapping for trellis-coded modulation at 12 000 bit/s

3 Data signalling and modulation rates

The data signalling rates shall be 14 400 and 12 000 bit/s ± 0.01%. The modulation rate is 2400 bauds ± 0.01%.

4 Received signal frequency tolerance

The carrier frequency tolerance allowance at the transmitter is ± 1 Hz. Assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received signal frequency.

5 Interchange circuits

5.1 *List of interchange circuits* (Table 2/V.33)

TABLE 2/V.33

Interchange circuit(see Note 1)

No.	Designation	Notes
102	Signal ground or commun return	
103	Transmitted data	
104	Received data	
105	Request to send	Note 2
106	Ready for sending	
107	Data set ready	
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	
112	Data signalling rate selector (DCE source)	
113	Transmitter signal element timing (DTE source)	
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
140	Loopback/Maintenance test	Note 3
141	Local loopback	Note 3
142	Test indicator	

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 – Not essential for continuous carrier operation.

Note 3 – Interchange circuits 140 and 141 are optional.

5.2 *Threshold and response times of circuit 109*

5.2.1 *Threshold*

- greater than −26 dBm: circuit 109 ON
- less than −33 dBm: circuit 109 OFF

The condition of circuit 109 for levels between −26 dBm and −33 dBm is not specified except that the signal detector shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

5.2.2. *Response times*

- ON to OFF: 40 ± 10 ms:
- OFF to ON:
  1) for initial equalization, circuit 109 must be ON prior to user data appearing on circuit 104;
  2) for re-equalization during data transfer, circuit 109 will be maintained in the ON condition; during this period, circuit 104 may be clamped to the binary 1 condition;

3) after a line signal interruption that lasts more than the ON to OFF response time:

a) when no new equalization is needed, 25 ± 10 ms;

b) when a new equalization is needed, circuit 109 must be ON prior to user data appearing on circuit 104.

Response times of circuit 109 are the times that elapse between the connection or removal of a line signal, generated by applying binary one to circuit 103, to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuit 109.

Note – Circuit 109 ON to OFF response time should be suitably chosen within the specified limits to ensure that all valid data bits have appeared on circuit 104.

5.3 *Response time for circuit 106*

Following the complete training procedure, the time between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106 shall be 15 ms ± 5 ms.

The time between the ON to OFF transition of circuit 105 and the ON to OFF transition of circuit 106 shall be suitably chosen to ensure that all valid signal elements have been transmitted.

6 Electrical characteristics of interchange circuits

6.1 Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110 [3].

6.2 *Fault condition on interchange circuits*

(See § 7 of Recommendation V.28 for association of the receiver failure detection types).

6.2.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

6.2.2 The DCE should interpret a fault condition on circuit 105 as an OFF condition using failure detection type 1.

6.2.3 All other circuits not referred to above may use failure detection types 0 or 1.

6.3 *Timing arrangements*

Clocks shall be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114, and receiver signal element timing, circuit 115. In this arrangement, the transmitter may either run as an independent timing source or with loopback timing (transmit timing slaved to receive timing). Loopback timing may be desirable in some network applications.

Alternatively, the transmitter signal element timing may be originated in the data terminal equipment and be transferred to the modem via interchange circuit 113.

7 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial $1 + x^{-18} + x^{-23}$, shall be included in the modem.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence. At the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in the Annex.

8 Synchronizing signals

Transmission of synchronizing signals may be initiated by the modem. When the receiving modem requires resynchronizing, it shall turn circuit 106 OFF and generate a synchronizing signal sequence.

The synchronizing signals for all data signalling rates are divided into four segments as in Table 3/V.33.

TABLE 3/V.33

	Segment 1	Segment 2 TRN	Segment 3	Segment 4	Total
Type of line signal	Alternations ABAB	Equalizer condition pattern	Rate sequence	Scrambled all binary ONEs	Total synchronizing signal time
Number of symbol intervals	256	2976	64	48	3344
Approximate time in ms	106	1240	27	20	1393

8.1 Segment 1 consists of alternations between states A and B as shown in Figures 2 and 3/V.33 for a duration of 256 symbol intervals.

8.2 *Segment 2: Equalizer conditioning pattern*

The segment consists of the sequential transmission of four signal elements A, B, C and D. These signal elements are shown in Figures 2/V.33 and 3/V.33. The equalizer conditioning pattern is a pseudo-random sequence at 4800 bit/s generated by the $1 + x^{-18} + x^{-23}$ data scrambler. During segment 2 any differential quadrant encoding is disabled and the scrambled dibits are encoded as follows:

$$00 = C \quad 01 = D \quad 11 = A \quad 10 = B$$

With a binary 1 applied to the input, the initial state of the scrambler shall be selected to produce the following scrambler output pattern and corresponding signal elements:

00	01	00	01	00	01	00	01	00	01	00	01	10	01	10	01
C	D	C	D	C	D	C	D	C	D	C	D	B	D	B	D

Segment 2 continues for 2976 symbol intervals.

8.3 *Segment 3: Rate signal*

The rate signal consists of a 16-bit binary sequence repeated 8 times. The sequence is defined in Table 4/V.33, scrambled and transmitted at 4800 bit/s with dibits differentially encoded as in Table 1B/V.33. The differential encoder shall be initialized using the final symbol of the previous segment.

The first two bits and subsequent dibits of each rate sequence shall be encoded as one signal state.

The rate signal may be used for establishing the data signalling rate between the modems, and providing information regarding multiplexer configuration, or other configuration information (subject to further study). When B14 = 0, only data signalling rate information is conveyed according to Table 4A/V.33. When B14 = 1, the bit assignment of Table 4B/V.33 applies.

The minimum requirement for detection is the receipt of two consecutive identical 16-bit sequences each with bits B0-3, B7, B11 and B15 conforming with Table 4/V.33. Following the detection of the rate sequence, the receiver shall be conditioned to receive data at the highest common rate with the indicated multiplexer configuration.

TABLE 4A/V.33

Bit designations

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0				1				1			0	1

B0-3, B7, B11, B15		For synchronizing on a received rate signal
B4-6		Not yet defined (for further study)
B8	1	Denotes ability to transmit and receive data at 12 000 bit/s (Note)
B9	1	Denotes ability to transmit and receive data at 14 400 bit/s (Note)
B10, B12, B13		Not yet defined (for further study)

Note – When transmitting a rate signal, the modem will transmit bits B8 B9 equal to 11 or 01 when the data signalling rate of segment 4 equals 14.4 kbit/s and B8 B9 = 10 when the data signalling rate of segment 4 equals 12 kbit/s.

TABLE 4B/V.33

Bit designations

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0				1				1			0	1

B0-3, B7, B11, B15		For synchronizing on a received rate signal
B4, B5	00	Denotes that B6, B10, B12, B13 define multiplexer configuration select (Note 1)
B8	1	Denotes ability to transmit and receive data at 12 000 bit/s (Notes 1 and 3)
B9	1	Denotes ability to transmit and receive data at 14 400 bit/s (Notes 1 and 3)
B6, B10, B12, B13		Multiplexer configuration select (see Note 2 and Tables 5A, 5B/V.33)

Note 1 – Other combinations of B4, B5 may be used to denote that B6, B8, B9, B10, B12 and B13 define other configuration information (for further study).

Note 2 – a) B6, B10, B12, B13 = all ZEROs: Manual Mode;

b) B6, B10, B12, B13 Binary representation of 1 through 11 (B6 = MSB, most significant bit) denotes desired multiplexer configuration as shown in Tables 5A and 5B/V.33;

c) B6, B10, B12, B13 = all ONEs: Remotely Programmable Mode. If a modem is so configured it will always transmit this pattern.

d) B6, B10, B12, B13 The unused combinations are available for use as manufacturer's option;

e) It is recommended that either both modems be configured with the identical multiplexer Mode or one modem be configured in the remotely programmable multiplexer Mode.

Note 3 – When transmitting a rate signal, the modems will transmit bits B8 B9 equal to 11 or 01 when the data signalling rate of segment 4 equals 14.4 kbit/s and B8 B9 = 10 when the data signalling rate of segment 4 equals 12 kbit/s.

8.4 *Segment 4*

The differential encoding to be used during this segment is defined in Table 1A/V.33. The differential encoder shall be initialized using the first symbol of the previous segment. Segment 4 shall begin with the initial states of the delay elements of the convolutional encoder shown in Figure 1/V.33 set to zero.

This segment initiates transmission at the highest rate indicated by segment 3 according to the encoding described in § 2.2 above with continuous binary ONEs applied to the input of the data scrambler. The duration of segment 4 is 48 symbol intervals. At the end of segment 4, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

9 Training-retraining procedure

An automatic adaptive equalizer shall be provided in the receiver.

The receiver shall incorporate a means of detecting loss of equalization and initiating a synchronizing signal sequence in its associated local transmitter.

The receiver shall incorporate a means of detecting a synchronizing signal and the rate sequence from the remote transmitter and initiating a synchronizing signal sequence in its associated local transmitter, which may be initiated at any time during the reception of the synchronizing signal sequence, regardless of the state of circuit 105.

Either modem may initiate a synchronizing signal sequence. The synchronizing signal is initiated when the receiver has detected a loss of equalization, or upon detecting a change in data rate or multiplexer configuration selection (made by a switch or by circuit 111). Having initiated a synchronizing signal, the modem expects a synchronizing signal from the remote transmitter.

Following the end of the transmitted synchronizing signal sequence, if the modem does not receive a synchronizing signal from the remote transmitter within a time interval equal to the maximum expected two-way propagation delay, it transmits another signal. A time interval of 1.2 seconds is recommended.

If the modem fails to synchronize on the received signal sequence, or fails to detect the rate signal, or is unable to provide the requested rate, or is transmitting at a rate higher than the requested rate, it transmits another synchronizing signal with rate sequence and data signalling rate conforming with the highest common rate, provided that it had not been sending a synchronizing sequence within the last 1.2 seconds.

If the modem receives a synchronizing signal when it had not initiated a synchronizing signal and the receiver properly synchronizes, it returns only one synchronizing sequence.

Note – When a synchronizing sequence is initiated due to loss of equalization, the previous multiplexer configuration should be maintained.

10 Multiplexing (See Tables 5A/V.33 and 5B/V.33)

A multiplexing option may be included to combine 12 000, 9600, 7200, 4800, and 2400 bit/s data subchannels into a single aggregate bit stream for transmission. Identification of the individual modulator bits is accomplished by assignment to the modulator as defined in § 2.2 above.

TABLE 5A/V.33

Aggregate data rate (bit/s)	Multiplex configuration	Sub-channel data rate (bit/s)	Multiplex channel	Modulator bits					
				Q1	Q2	Q3	Q4	Q5	Q6
14 400	1	14 400	A	X	X	X	X	X	X
14 400	2	12 000 2 400	A B	X	X	X	X	X	 X
14 400	3	9 600 4 800	A B	X	X	 X	X	X	 X
14 400	4	9 600 2 400 2 400	A B C	X	X	 X	X	X	 X
14 400	5	7 200 7 200	A B	X	 X	X	 X	X	 X
14 400	6	7 200 4 800 2 400	A B C	X	 X	X	 X	X	 X
14 400	7	7 200 2 400 2 400 2 400	A B C D	X	 X	X	 X	X	 X
14 400	8	4 800 4 800 4 800	A B C	X	 X	 X	X	X	 X
14 400	9	4 800 4 800 2 400 2 400	A B C D	X	 X	 X	X	X	 X
14 400	10	4 800 2 400 2 400 2 400 2 400	A B C D E	X	 X	 X	X	 X	 X
14 400	11	2 400 2 400 2 400 2 400 2 400 2 400	A B C D E F	X	 X	 X	 X	 X	 X

Note – When more than one modulator bit is assigned to a sub-channel, the first bit in time of the sub-channel is assigned to the first available bit in time of the modulator.

TABLE 5B/V.33

Aggregate data rate (bit/s)	Multiplex configuration	Sub-channel data rate (bit/s)	Multiplex channel	Modulator bits					
				Q1	Q2	Q3	Q4	Q5	Q6
12 000	1	12 000	A	X	X	X	X	X	
12 000	2	9 600 2 400	A B	X	X	X	X	X	
12 000	3	7 200 4 800	A B	X	X	X	X	X	
12 000	4	7 200 2 400 2 400	A B C	X	X	X	X	X	
12 000	5	4 800 4 800 2 400	A B C	X	X	X	X	X	
12 000	6	4 800 2 400 2 400 2 400	A B C D	X	X	X	X	X	
12 000	7	2 400 2 400 2 400 2 400 2 400	A B C D E	X	X	X	X	X	

Note – When more than one modulator bit is assigned to a sub-channel, the first bit in time of the sub-channel is assigned to the first available bit in time of the modulator.

10.1 *List of interchange circuits concerned with multiplexer ports*

TABLE 6/V.33

Interchange circuits (see Note 1)		Port A	Port B, C, D, E and F	Notes
No.	Designation			
102	Signal ground or common return	X	X	
103	Transmitted data	X	X	
104	Received data	X	X	
105	Request to send	X	X	Note 2
106	Ready for sending	X	X	Note 3
107	Data set ready	X	X	
109	Data channel received line signal detector	X	X	
111	Data signalling rate selector (DTE source)	X		Note 4
113	Transmitter signal element timing (DTE source)	X	X	
114	Transmitter signal element timing (DCE source)	X	X	
115	Receiver signal element timing (DCE source)	X	X	
140	Loopback/Maintenance test	X	X	Note 5
141	Local loopback	X		Notes 5 & 6
142	Test indicator	X	X	Note 7

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 – Circuit 105 is not necessary for continuous carrier transmission. The transmitted line signal will not be controlled by this interchange circuit. If needed, circuit 105 (when the multiplexer is present) is used to control circuit 109 at the remote DCE. See § 10.4 below.

Note 3 – During the synchronization process of the main DCE the OFF condition of circuit 106 is signalled at all port interfaces.

Note 4 – Circuit 111 is optionally present on port A. If present, circuit 111 is activated in multiplexer configuration 1 in the same way as if no multiplexer were present.

Note 5 – Circuits 140 and 141 are optional.

Note 6 – Circuit 141 is present only on port A. When used in multiplexer configurations other than configuration 1, the looping occurs on all ports.

Note 7 – Circuit 142 is present on all ports of the multiplexer, but may be activated on an individual port basis for individual port tests. All are activated simultaneously for entire DCE test.

10.2 *Transmit buffers*

In the transmitter of each multiplexer port, there shall be a data buffer of suitable capacity. In this way, both phase variations and, within certain limits, frequency deviations are absorbed. The buffer shall be initialized when the OFF to ON transition of circuit 105 occurs and may be repositioned in the event of the buffer overflow.

Note – The buffer may be initialized upon the DCE sending a synchronizing signal.

10.3 *Transmit port timing arrangements*

Table 7/V.33 shows all possible combinations of port and main DCE transmit timing clock arrangements.

TABLE 7/V.33

Source of port: transmitter signal element timing (used to clock in circuit 103)	Source of DCE: internal transmitter element timing (internal transit clock)	Port transmit buffer
114 (DCE source)	Internal (Independent timing)	Not required
	External [a] (circuit 113 of selected port)	Not required
	Receiver timing (loopback timing)	Not required
113 (DTE [a] source)	Internal (Independent timing)	Required
	External [a] (Circuit 113 of selected port)	Required for all ports except port supplying circuit 113 to DTE
	Receiver timing (loopback timing)	Required

[a] In these applications a source could also be another DCE.

10.4 *Port simulated circuit 105 to circuit 109 operation* (optional)

Simulated circuits 105 to 109 operation on an individual port interface may optionally be provided in accordance with Recommendation V.13.

ANNEX A

(to Recommendation V.33)

Detailed scrambling, descrambling and pseudo-random sequence generation processes

A.1 *Scrambling*

The message polynomial is divided by the generating polynomial $1 + x^{-18} + x^{-23}$ (see Figure A.1/V.33). The coefficients of the quotient of this division taken in descending order form the data sequence to be transmitted. The shift register shall be preconditioned to produce the output pattern defined in § 8.2 (the initial state of the scrambler required to generate that pattern is: 1010, 1011, 1011 0011, 0111, 010). The scrambler shall be clocked at 4 800 Hz during segments 2 and 3 and shall be clocked at the data rate during segment 4. During segments 2, 3 and 4 and during normal data transmission, the shift register is fed with scrambled data D_s:

$$D_s = D_i + D_s\, x^{-18} + D_s\, x^{-23}$$

where D_i is binary one during segments 2 and 4 and the rate sequence during segment 3.

A.2 *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial (Figure A.2/V.33) to form the recovered message polynomial. The coefficients of the recovered polynomial, taken in descending order, form the output data sequence D_o:

$$D_o = D_i = D_s (1 + x^{-18} + x^{-23})$$

A.3 *Elements of the scrambling process*

The polynomial $1 + x^{-18} + x^{-23}$ generates a pseudo-random sequence of length $2^{23} - 1 = 8{,}388{,}607$. This long sequence does not require the use of a guard polynomial to prevent the occurrence of repeated patterns and is particularly simple to implement with integrated circuits.

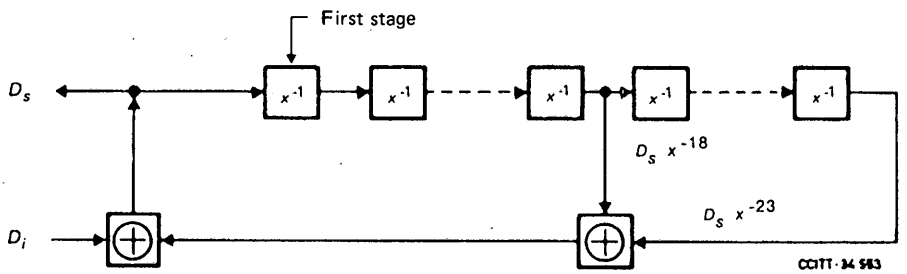


FIGURE A-1/V.33

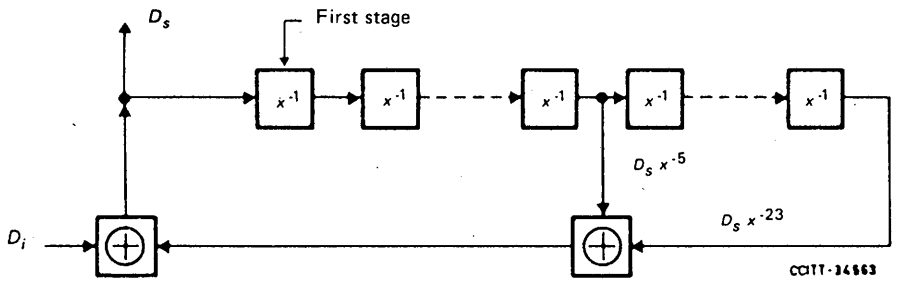


FIGURE A-2/V.33

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Fascicle IV.2, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with basic bandwidth conditioning*, Vol. IV, Fascicle IV.2, Rec. M.1025.

[3] Data communication – *25-pin DTE/DCE interface connector and pin assignments*, ISO Standard 2110.

SECTION 3

WIDEBAND MODEMS

Recommendation V.35

DATA TRANSMISSION AT 48 KILOBITS PER SECOND USING 60-108 kHz GROUP BAND CIRCUITS

(Mar del Plata, 1968; amended at Geneva, 1972 and 1976)

(For the text of this Recommendation, see Red Book Volume VIII – Fascicle VIII.1)

Note – It is the opinion of the CCITT that the information contained in Recommendation V.35 is out of date. Therefore it is not recommended to use the techniques described in this Recommendation for new designs. Alternative techniques are described in Recommendations V.36 and V.37. It should be noted that other Recommendations make reference to the electrical characteristics described in Appendix II to this Recommendation. As these characteristics are expected to allow interworking with V.11 characteristics, use of V.11 circuits is recommended in those cases.

(Melbourne, 1988)

Recommendation V.36

MODEMS FOR SYNCHRONOUS DATA TRANSMISSION USING 60-108 kHz GROUP BAND CIRCUITS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984 and Melbourne, 1988)

On leased circuits, considering that there exist and will come into being other modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

The only group reference pilot frequency which can be used in conjunction with this modem is 104.08 kHz.

1 Scope

The family of modems covered by this Recommendation should be applicable to the following uses:

a) transmission of data between customers on leased circuits;

b) transmission of a multiplex aggregate bit stream for public data networks;

c) extension of a PCM channel at 64 kbit/s over analogue facilities;

d) transmission of a common channel signalling system for telephony and/or public data networks;

e) extension of Single-Channel-Per-Carrier (SCPC) circuit from a satellite earth station;

f) transmission of a multiplex aggregate bit stream for telegraph and data signals.

Principal recommended characteristics to be used for simultaneous both-way synchronous operation are the following:

2 Data signalling rates

2.1 *Application a)*

The recommended data signalling rate (equals the customer signalling rate) for international use is synchronous at 48 kbit/s. For certain national applications or with bilateral agreement between Administrations, the following data signalling rates are applicable: 56, 64 and 72 kbit/s.

2.2 *Applications b), c) and d)*

For these applications, the recommended data signalling rate is synchronous at 64 kbit/s.

For those synchronous networks requiring the end-to-end transmission of both the 8 kHz and 64 kHz timing together with the data at 64 kbit/s, a data signalling rate of 72 kbit/s on the line is suggested.

The corresponding data format should be obtained by inserting one extra bit E just before the first bit of each octet of the 64 kbit/s data stream. The bits E convey alignment and housekeeping information, according to the pattern shown in Figure 1/V.36.

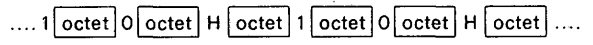


FIGURE 1/V.36

The use of the housekeeping bits H is determined with bilateral agreement between Administrations. When not used, these bits should be assigned the value 1. A framing strategy is not specified in this Recommendation.

When the transmission of the 8 kHz timing is not required, the data signalling rate on the line may be 64 kbit/s.

2.3 *Application e)*

The recommended data signalling rate (equals the customer signalling rate) for international use is synchronous at 48 kbit/s. For certain national applications or with bilateral agreement between Administrations the data signalling rate of 56 kbit/s is applicable.

2.4 *Application f)*

The recommended data signalling rate is synchronous at 64 kbit/s.

2.5 The permitted tolerance for all the data signalling rates mentioned above is $\pm 5 \times 10^{-5}$ bit/s.

Note – There are equipments in service which will only work successfully with a maximum tolerance of the data signalling rate of $\pm$ 1 bit/s.

3 Scrambler/descrambler

In order to be bit sequence independent and to avoid high amplitude spectral components on the line, the data should be scrambled and descrambled by means of the logical arrangements described in Appendix I.

4 Baseband signal

The equivalent baseband signal shaping process is based upon the binary coded partial response pulse, often referred to as class IV, whose time and spectral function are defined by:

$$g(t) = \frac{2}{\pi} \cdot \frac{\sin \frac{\pi}{T} t}{\left(\frac{t}{T}\right)^2 - 1}$$

and

$$G(f) = \begin{cases} 2\,Tj \sin 2\pi\, Tf, & |f| \leqslant \dfrac{1}{2\,T} \\ 0, & |f| > \dfrac{1}{2 \cdot T} \end{cases}$$

respectively, where $1/T$ denotes the data signalling rate.

This shaping process should be effected in such a way that the decoding can be achieved by full wave rectification of the demodulated line signal.

The reference to equivalent baseband signals recognizes that the modem implementation may be such that the binary signal at the input and output of the modem is converted to and from the line signal without appearing as an actual baseband signal.

5 Line signal in 60-108 kHz band (at the line output of the modem)

5.1 In the 60-108 kHz band the line signal should correspond to a single sideband signal with its carrier frequency at 100 kHz ± 2 Hz.

5.2 The relationship between the binary signals at the real or hypothetical output of the scrambler and the transmitted line signal states shall be in accordance with the amplitude modulation case of Recommendation V.1, i.e., tone ON for binary 1 and tone OFF for binary 0.

In a practical case this means that the voltage or no voltage conditions which will result from the full wave rectification of the demodulated line signal will correspond with the binary 1 and binary 0 signals respectively at the output of the scrambler.

5.3 The amplitude of the theoretical line signal spectrum, corresponding to binary symbol 1 appearing at the output of the scrambler, is to be sinusoidal, with zeros and maxima at the frequencies listed below:

Data signalling rate (kbit/s)	Zeros at (kHz)	Maxima at (kHz)
64	68 and 100	84
48	76 and 100	88
56	72 and 100	86
72	64 and 100	82

5.4 In the 60-108 kHz band, amplitude distortion of the real spectrum relative to the theoretical spectrum as defined under § 5.3 above is not to exceed ± 1 dB; the group delay distortion is not to exceed 8 microseconds. These two requirements are to be met for each frequency band centred on one of the maxima mentioned in § 5.3 and whose width is equal to 80% of the frequency band used.

5.5 The nominal level of the line data signal should be −6 dBm0. The actual level should be within ± 1 dB of the nominal level.

5.6 A pilot carrier at the same frequency as the modulated carrier at the transmitter and with a level of −9 ± 0.5 dB relative to the actual level mentioned under § 5.5 above, should be added to the line signal. The relative phase between the modulated carrier and the pilot carrier at the transmitter should be time invariant.

6 Group reference pilot

6.1 Provision should be made for facilitating the injection of a group reference pilot of 104.08 kHz from a source external to the modem.

6.2 The protection of the group reference pilot should conform to Recommendation H.52 [1].

7 Voice channel

7.1 The service speech channel is an integral part of the applications a) and e) of this system and is used on an optional basis. The channel corresponds to channel 1 of a 12-channel SSB-AM system in the 104-108 kHz band (virtual carrier at 108 kHz). It can transmit continuous voice at a mean level of maximum −15 dBm0 or pulsed signalling tones according to the individual specifications.

To avoid overloading of the system by peak signals a limiter shall be used with cut-off levels above +3 dBm0.

To avoid stability problems the channel shall be connected to 4-wire equipment only.

For operator-to-operator signalling Recommendation Q.1 [2] shall be followed, but instead of 500/20 Hz a non-interrupted tone of 2280 Hz at a level of −10 dBm0 shall be used.

For other signalling purposes [application e)] the R1 or R2 inband signalling, described in Recommendations Q.322 [3], Q.323 [4] and Q.454 [5], Q.455 [6] respectively, is preferred.

The transmit filter shall be such that any frequency applied to the transmit input terminals at a level of −15 dBm0 will not cause a level exceeding:

a) −73 dBm0p in the adjacent group,

b) −61 dBm0 in the vicinity (± 25 Hz) of the pilot 104.08 kHz,

c) −55 dBm0 in the data band between 64 and 101 kHz,

d) the values specified in Recommendation Q.414 [7] to protect the nearest low level signalling path.

The voice band is sufficiently protected if the same filter is used in the receive direction of the channel. The attenuation/frequency characteristic, measured between the voice-frequency input and the group band output or the group band input and the voice-frequency output, with respect to the value at 800 Hz is limited by:

−1 dB over the 300-3400 Hz band,

+2 dB between 540 and 2280 Hz.

7.2 The voice channel is inapplicable to applications b), c), d) and f). It is used on an optional basis for applications a) and e).

Note – When the modem is installed at the repeater station, the voice channel should be extended to the renter's premises.

8 Adjacent channel interference

In the bands 36-60 kHz and 108-132 kHz, the adjacent channel interference should conform to Recommendation H.52 [1].

9 Line characteristics

The modem is intended to operate satisfactorily over group links according to reference [8] at data signalling rates of 48 up to 64 kbit/s.

For group links, comprising more than three group sections, or where a data signalling rate of 72 kbit/s is required, the characteristics given in reference [8] are not adequate.

Furthermore, compliance of a group link with reference [8] does not necessarily guarantee proper operation of the modem, nor does noncompliance imply improper operation.

In Annex A a method is presented to calculate the suitability of a group link for data transmission using a modem according to this Recommendation.

When an automatic adaptive equalizer is included in the modem, proper operation over a circuit of similar construction as the hypothetical reference circuit as specified in reference [9] will be possible at data signalling rates up to 64 kbits.

Note 1 – Reference [9] specifies a maximum number of 8 through-group filters, but this figure is subject to further study and possible amendment.

Note 2 – The modem may allow operation at 72 kbit/s over a circuit having a maximum of 5 through-group filters. This value is left for further study.

10 Interface

10.1 *Interface for applications a), e) and f) indicated in § 1*

10.1.1 *List of interchange circuits* (See Table 1/V.36)

TABLE 1/V.36

Interchange circuit (see Note 1)		Remark
102	Signal ground or commun return	See Note 2
102a	DTE common return	See Note 3
102b	DCE common return	See Note 3
103	Transmitted data	
104	Received data	
105	Request to send	
106	Ready for sending	
107	Data set ready	
109	Data channel received line signal detector	
113	Trasmitter signal element timing (DTE source)	
114	Trasmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
140	Loopback/Maintenance test	See Note 2
141	Local loopback	See Note 2
142	Test indicator	See Note 2

Note 1 – When the modem is installed at the repeater station, this interface should appear at the customer's premises without restrictions regarding the data signalling rate and the provision of the voice channel. The method to achieve this is subject to national regulations.

Note 2 – Equipment may be in service that does not implement these circuits.

Note 3 – Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 are used.

10.1.2 *Electrical characteristics*

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended together with the use of the connector and pin assignment plan specified by ISO 4902.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

ii) In the case of circuits 105, 106, 107 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1 or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies with receivers configured as specified by Recommendation V.10 for category 2.

Note – For an interim period the connector and contact-assignment plan specified in ISO 2593 and commonly referred to as the "V.35 interface" may optionally be used. In this case electrical characteristics may be either V.11 for circuits 103, 104, 113, 114 and 115 together with V.10 (receivers configured as specified in category 2) for all other circuits, or V.35 Appendix II together with V.28 respectively.

10.2 *Interface for applications b), c) and d) indicated in § 1*

For applications b), c) and d) the interface may comply with the functional requirements given in reference [10] for the 64 kbit/s interface. In these cases, the electrical characteristics may comply with reference [11].

If an end-to-end transmission of the 8 kHz timing signal is not used, an 8 kHz timing signal across the interface will not be supplied nor utilized by the modem.

Alternatively the interface according to § 10.1 may be used for these applications.

11 Threshold and response time of circuit 109

11.1 *Threshold*

For a data line signal level greater than −13 dBm0, circuit 109 is ON. For data line signal level less than −18 dBm0, circuit 109 is OFF.

Note – The corresponding levels for the pilot carrier are −22 dBm0 and −27 dBm0 respectively.

The condition of circuit 109 for levels between the above levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition. To measure the thresholds of the detector, a modulated data signal with its pilot carrier at the level specified in § 5.6 should be used.

11.2 *Response time*

From OFF to ON: 15 ms to 150 ms,

From ON to OFF: 5 ms to 15 ms.

The response times of circuit 109 are the time intervals between the appearance or disappearance of the line signal at the reception input terminal of the modem and the occurrence of the corresponding ON or OFF condition on circuit 109.

The line signal level should be within the range from 3 dB above the actual threshold of the line signal detector at reception and the maximum permissible level of the signal at reception.

12 Error performance

12.1 For a hypothetical reference circuit, 2500 km in length, with characteristics in accordance with Recommendation H.14 [8], and with not more than two through-group connection equipments, the performance objective in terms of error rate should be not worse than 1 error per 10^7 bits transmitted. This is based on an assumed Gaussian noise power of 4 pW per km/per 4 kHz band psophometrically weighted (this figure corresponds to 4 pW0p/km).

13 Additional information for the designer

13.1 *Input level variation*

The step-change in the input level is, under normal conditions, smaller than ± 0.1 dB. The gradual input level change is smaller than ± 6 dB and includes the tolerance of the transmitter output level.

13.2 *Interference from adjacent group bands*

A sinusoidal signal of +10 dBm0 in the frequency bands of 36-60 kHz and 108-132 kHz can appear together with the data line signal at the input of the receiver.

ANNEX A

(to Recommendation V.36)

Line characteristics

For proper operation of the modem, the line characteristic of a group link shall comply with:

$$\varepsilon = \sqrt{\frac{c^2}{a^2 + b^2} - \frac{1}{2}} < 0.08$$

where

$$a = \frac{2}{T} \int_{f_t - \frac{1}{2T}}^{f_t} |G(f)|^2 \cdot |H(f)| \cos [\theta(f) + 2\pi f\tilde{\tau}] \, df,$$

$$b = \frac{2}{T} \int_{f_t - \frac{1}{2T}}^{f_t} |G(f)|^2 \cdot |H(f)| \sin [\theta(f) + 2\pi f\tilde{\tau}] \, df,$$

$$c^2 = \frac{2}{T} \int_{f_t - \frac{1}{2T}}^{f_t} |G(f)|^2 \cdot |H(f)|^2 \, df,$$

$|H(f)|$ is the attenuation characteristic of the link,

$\theta(f)$ is the phase characteristic of the link,

$G(f)$ is the spectral function of the transmitted line signal $= 2jT \sin \{2\pi (f_t - f)T\}$,

$\tilde{\tau}$ represents a constant time delay which should be chosen in such a way as to minimize ε, and

f_t is 100 kHz.

APPENDIX I

(to Recommendation V.36)

Scrambling process

I.1 *Definitions*

I.1.1 **applied data bit**

The data bit which has been applied to the scrambler but has not affected the transmission at the time of consideration.

I.1.2 **next transmitted bit**

The bit which will be transmitted as a result of scrambling the applied data bit.

I.1.3 **earlier transmitted bits**

Those bits which have been transmitted earlier than the next transmitted bit. They are numbered sequentially in reverse time order, i.e. the first earlier transmitted bit is that immediately preceding the next transmitted bit.

I.1.4 **adverse state**

The presence of any one of certain repetitive patterns in the earlier transmitted bits.

I.2 *Scrambling process*

The binary value of the next transmitted bit shall be such as to produce odd parity when considered together with the twentieth and third earlier transmitted bits and the applied data bit unless an adverse state is apparent, in which case the binary value of the next transmitted bit shall be such as to produce even instead of odd parity.

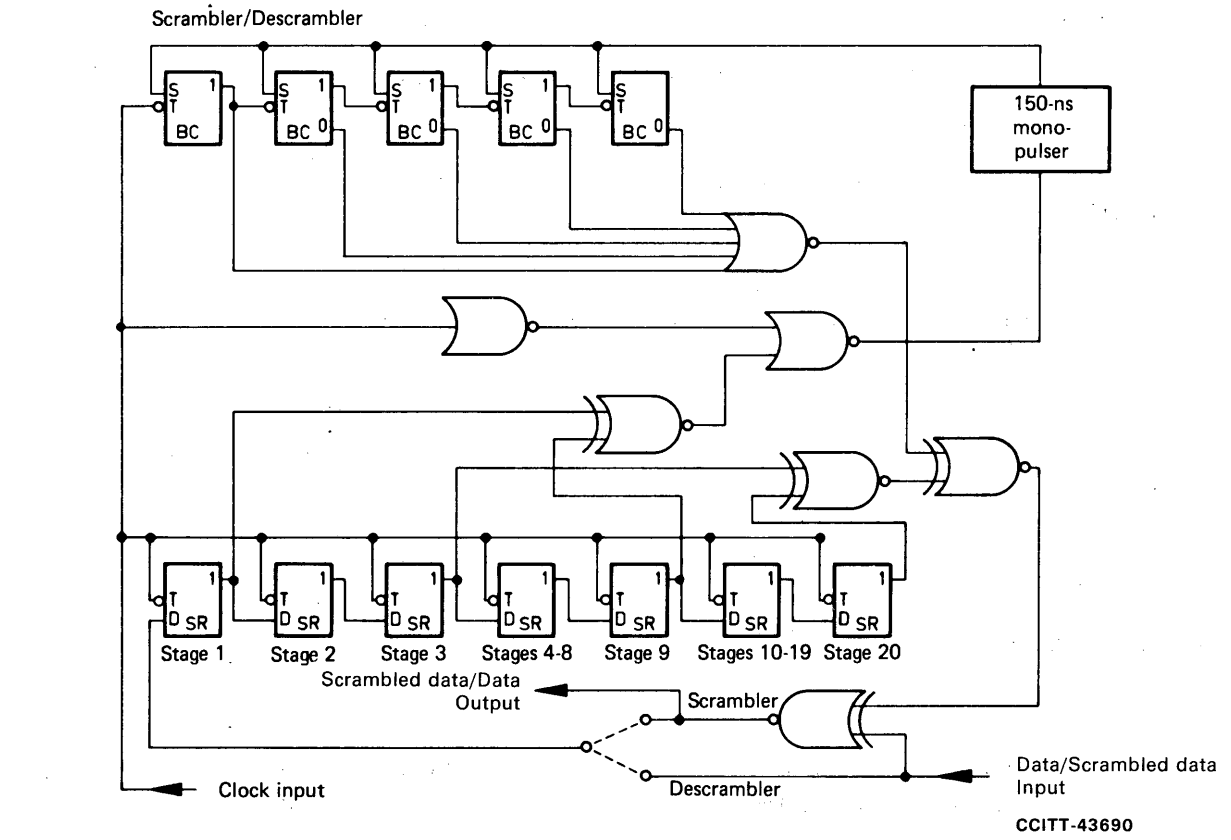
An adverse state shall be apparent only if the binary values of the p^{th} and $(p+8)^{th}$ earlier transmitted bits have not differed from one another when p represents all the integers from 1 to q inclusive. The value of q shall be such that, for $p = (q + 1)$, the p^{th} and $(p+8)^{th}$ earlier transmitted bits had opposite binary values and $q = (31 + 32\ r)$, r being 0 or any positive integer.

At the time of commencement, i.e. when no earlier bits have been transmitted, an arbitrary 20-bit pattern may be assumed to represent the earlier transmitted bits. At this time also it may be assumed that the p^{th} and $(p+8)^{th}$ earlier transmitted bits have had the same binary value when p represents all the integers up to any arbitrary value. Similar assumptions may be made for the descrambling process at commencement.

Note 1 – From this it can be seen that received data cannot necessarily be descrambled correctly until at least 20 bits have been correctly received and any pair of these bits, separated from each other by seven other bits, have differed in binary value from one another.

Note 2 – It is not possible to devise a satisfactory test pattern to check the operation of the Adverse State Detector (ASD) because of the large number of possible states in which the 20 state shift register can be at the commencement of testing. For those modems in which it is possible to bypass the scrambler and the descrambler and to strap the scrambler to function as a descrambler, the following method may be used. A 1 : 1 test pattern is transmitted with the ASD of the scrambler bypassed. If the ASD of the descrambler is functioning correctly the descrambled test pattern will contain a single element error every 32 bits, i.e. 90 000 errors per minute for a modem operating at 48 kbit/s indicates that the descrambler is functioning correctly. The operation of the ASD of the scrambler may be checked in a similar manner with the scrambler strapped as a descrambler and the descrambler bypassed.

I.3 Figure I-1/V.36 is given as an indication only, since with another technique this logical arrangement might take another form.



Symbol truth tables

Or

A	B	C
0	0	1
0	1	0
1	1	0
1	0	0

Or-Not

A	B	C
0	0	1
0	1	0
1	1	0
1	0	0

Exclusive or-not

A	B	C
0	0	1
0	1	0
1	1	1
1	0	0

Inverter

A	C
1	0
0	1

Shift register

T	D	1 output	0 output
1	Q	–	–
0	–	Q	$\bar{Q}$

Q is either 0 or 1

Binary counter

T	1 output	0 output
1	Q	$\bar{Q}$
0	$\bar{Q}$	Q

S	1 output	0 output
0	Q	$\bar{Q}$
1	1	0

(Reset)

Note – Negative-going transitions of clocks (i.e. 1 to 0 transitions) coincide with data transitions. This is self-synchronizing.

FIGURE I-1/V.36

An example of scrambler and descrambler circuitry

References

[1] CCITT Recommendation *Transmission of wide-spectrum signals (data, facsimile, etc.) on wideband group links*, Vol. III, Rec. H.52.

[2] CCITT Recommendation *Signal receivers for manual working*, Vol. VI, Rec. Q.1.

[3] CCITT Recommendation *Multifrequency signal sender*, Vol. VI, Rec. Q.322.

[4] CCITT Recommendation *Multifrequency signal receiving equipment*, Vol. VI, Rec. Q.323.

[5] CCITT Recommendation *The sending part of the multifrequency signalling equipment*, Vol. VI, Rec. Q.454.

[6] CCITT Recommendation *The receiving part of the multifrequency signalling equipment*, Vol. VI, Rec. Q.455.

[7] CCITT Recommendation *Signal sender*, Vol. VI, Rec. Q.414.

[8] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals*, Vol. III, Rec. H.14, § 2.

[9] *Ibid.*, § 3.

[10] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces*, Vol. III, Rec. G.703, § 1.

[11] *Ibid.*, § 1.2.

Recommendation V.37

SYNCHRONOUS DATA TRANSMISSION AT A DATA SIGNALLING RATE HIGHER THAN 72 kbit/s USING 60-108 kHz GROUP BAND CIRCUITS

(Geneva, 1980; amended at Malaga-Torremolinos, 1984 and at Melbourne, 1988)

1 Introduction

On leased circuits, considering that there exist and will come into being other modems with features designed to meet the requirements of Administrations and users, this Recommendation in no way restricts the use of any other modems.

The only group reference pilot frequency which can be used in conjunction with this modem is 104.08 kHz.

The modem is intended to be used on group band circuits not necessarily conforming to [1].

Principal characteristics:

a) transmission of any type of high-speed synchronous data in duplex constant carrier mode on 4-wire (60-108 kHz) group band circuits;

b) primary data signalling rates up to 144 kbit/s;

c) inclusion of an automatic adaptive equalizer;

d) class IV partial response pulse amplitude single sideband signalling and modulation;

e) optional inclusion of an overhead-free multiplexer combining existing data signalling rates;

f) optional voice channel.

2 Data signalling rates

2.1 The recommended synchronous data signalling rates are 96 kbit/s, 112 kbit/s, 128 kbit/s and 144 kbit/s. For some applications with agreement from the Administration, data signalling rates up to 168 kbit/s are applicable. (See the Note to § 7.)

2.2 The permitted tolerance for all data signalling rates is $\pm 5 \times 10^{-5}$.

3 Scrambler/descrambler

In order to be bit sequence independent, to avoid high amplitude spectral components on the line, and to allow the automatic equalizer to remain converged, the data should be scrambled and descrambled by means of the logical arrangements described in Appendix I.

4 Encoding method

The binary bit stream A, delivered by the scrambler, to be transmitted is divided into consecutive groups of 2 bits A_1 and A_2 (dibits), A_1 being the first in time delivered by the scrambler.

An amplitude level B is assigned to each dibit (A) as shown in Table 1/V.37.

TABLE 1/V.37

A_1	A_2	Equivalent B amplitude level
0	0	0
0	1	+1
1	1	+2
1	0	+3

A pre-encoder circuit converts the stream B into another quaternary stream C which conforms to the relation:

$$C_i = B_i \oplus C_{i-2}$$

where

$\oplus$ represents the modulo 4 sum

and the subscript i represents the i^{th} element of B or C.

The resulting quaternary stream C can be processed to form a baseband signal.

5 Baseband signal shaping

The equivalent baseband signal shaping process is based upon the binary coded partial response pulse, often referred to as class IV, whose time and spectral function are defined by:

$$g(t) = \frac{2}{\pi} \cdot \frac{\sin \frac{\pi}{T} t}{\left(\frac{t}{T}\right)^2 - 1}$$

and

$$G(f) = \begin{cases} 2\,T j \sin 2\pi\, Tf\,, & |f| \leqslant \dfrac{1}{2\,T} \\ 0\,, & |f| > \dfrac{1}{2\,T} \end{cases}$$

respectively, where $1/T$ denotes the modulation rate.

The reference to equivalent baseband signals recognizes that the modem implementation may be such that the binary signal at the input and output of the modem is converted to and from the line signal without appearing as an actual baseband signal.

The baseband signal formed by the processes described above will present 7 levels (see Table 2/V.37).

The baseband signal shaping is performed in the transmitter.

TABLE 2/V.37

Level	Bit value	
	A_1	A_2
+3	1	0
+2	1	1
+1	0	1
0	0	0
−1	1	0
−2	1	1
−3	0	1

6 **Line signal in the 60-108 kHz band** (at the line output of the modem)

6.1 In the 60-108 kHz band, the line signal should correspond to a single sideband signal with its carrier frequency pilot and timing pilot at frequencies as specified in Table 3/V.37.

6.2 The amplitude of the theoretical line signal spectrum, corresponding to a quaternary symbol (+1) appearing at the output of the encoder, is sinusoidal. The zeros and maxima of the theoretical line spectrum are shown in Table 3/V.37.

TABLE 3/V.37

Data rate (kbit/s)	Zeros at (kHz)	Maxima at (kHz)	Pilot carrier frequency	Timing pilot frequency
144	64 and 100	82	100 kHz	64 kHz
128	68 and 100	84	100 kHz	68 kHz
112	72 and 100	86	100 kHz	72 kHz
96	76 and 100	88	100 kHz	76 kHz
168 (optional)	62 and 104	83	104 kHz	62 kHz

6.3 In the 60-108 kHz band, amplitude distortion of the real spectrum relative to the theoretical spectrum as defined under § 6.2 above is not to exceed ± 1 dB; the group-delay distortion is not to exceed 15 μs. These two requirements are to be met for each frequency band centred on one of the maxima mentioned in § 6.2 and whose width is equal to 80% of the frequency band used.

6.4 The nominal level of the line data signal should be −6 dBm0. The actual level should be within ± 1 dB of the nominal level.

6.5 A pilot carrier at the same frequency as the modulated carrier (100 kHz ± 2 Hz) at the transmitter and with a level of −9 ± 0.5 dB relative to the actual level mentioned under § 6.4 above, should be added to the line signal. The relative phase between the modulated carrier and the pilot carrier at the transmitter should be time invariant.

Note – For the optional data signalling rate of 168 kbit/s, the pilot carrier should be 104 kHz ± 2 Hz.

6.6 A timing pilot at a frequency difference from the carrier equal to half the modulation rate at the transmitter with a level of −12 ± 0.5 dB relative to the actual level mentioned under § 6.4 above, should be added to the line signal.

The relationship between the timing pilot and the pilot carrier should remain time invariant at the transmitter.

7 Group reference pilot

7.1 Provision should be made for facilitating the injection of a group reference pilot of 104.08 kHz from an external source.

7.2 The protection of the group reference pilot should conform to Recommendation H.52 [2].

Note – Group reference pilot must be removed from the channel for operation at 168 kbit/s.

8 Optional voice channel

The service speech channel may be an integral part of the application of this system and is used on an optional basis. The channel corresponds to channel 1 of a 12 channel SSB-AM system in the 104-108 kHz band (virtual carrier at 108 kHz). It can transmit continuous voice at a mean level of maximum −15 dBm0 or pulsed signalling tones according to the individual specifications.

To avoid overloading of the system by peak signals, a limiter shall be used with cut-off levels above +3 dBm0.

To avoid stability problems, the channel shall be connected to 4-wire equipment only.

The transmit filter shall be such that any frequency applied to the transmit input terminals at a level of −15 dBm0 will not cause a level exceeding:

a) −73 dBm0p in the adjacent group;

b) −61 dBm0 in the vicinity (± 25 Hz) of the pilot 104.08 kHz;

c) −55 dBm0 in the data band between 64 and 101 kHz. When the 168 kbit/s data signalling rate is used this requirement applies between 62 and 104 kHz.

The voiceband is sufficiently protected if the same filter is used in the receive direction of the channel. The attenuation/frequency characteristic, measured between the voice-frequency input and the group band output or the group input and the voice-frequency output, with respect to the value at 800 Hz is limited by:

−1 dB over the 300-3400 Hz band,

+2 dB between 540 and 2280 Hz.

Note – When the modem is installed at the repeater station, the voice channel should be extended to the customer's premises.

9 Adjacent channel interference

In the bands 36-60 kHz and 108-132 kHz the adjacent channel interference should conform to Recommendation H.52 [2].

10 Line characteristics

The modem will allow proper operation of data signalling rates up to 128 kbit/s over a circuit of similar construction as the Hypothetical Reference Circuit as specified in reference [3].

Note 1 – Reference [3] specifies a maximum number of 8 through-group filters, but this figure is subject to further study and possible amendment.

Note 2 – The modem will allow operation over a circuit having a maximum number of 5 through-group filters at 144 kbit/s.

Note 3 – The line characteristics for operation at 168 kbit/s are not specified.

11 Synchronizing signals

Transmission of synchronizing signals is initiated by the modem. When the receiving modem detects a condition which requires resynchronizing, it shall turn circuit 106 OFF and generate synchronizing signals.

The synchronizing signals for all data signalling rates are divided into three segments as indicated in Table 4/V.37.

TABLE 4/V.37

	Segment 1	Segment 2	Segment 3	Total of segments 1, 2 and 3	
Type of line signals	Only carrier and timing pilots	Carrier and timing pilots and alternation of levels (± 2)	Carrier and timing pilots and scrambled all binary ONEs	Data signalling rates (kbit/s)	Approximate time (s)
Number of symbol intervals	10 240	4096	262 144	96	5.76
				112	4.93
				128	4.32
				144	3.84
				168	3.29

11.1 Segment 1 transmits the carrier pilot, the timing pilot and data signal corresponding with the dibits (0, 0) applied at the input of the encoder.

11.2 Segment 2 consists of the carrier pilot, the timing pilot and an alternation between two signal levels (+2) and (−2) corresponding with the dibits (1, 1) applied at the input of the encoder.

11.3 Segment 3 consists of the carrier pilot, the timing pilot and scrambled all binary ONEs.

At the beginning of this segment:

- the scrambler shift register must be set to all 0s (see Appendix I);
- the adverse state detector counter must be set to all 1s (see Appendix I);
- the pre-encoder must be set to all 0s.

The equivalent baseband signal processed at the beginning of Segment 3 consists of a succession of 15 levels (0) followed by levels (+1), (0), (−1), (+1), (0), (−1), (+1), (0), (−1), (+1), (+1), (−1) . . . .

11.4 Circuit 106 is turned ON at the end of segment 3 and the user's data may appear at the input of the scrambler.

12 Optional multiplexing

Multiplexing options shall be separately available to combine nominally available group band data rates of 48, 56, 64 or 72 kbit/s into a single aggregate bit stream for transmission as shown in Table 3/V.37. These multiplexers should be of a synchronous, overhead-free, bit interleave design. Using modem internal processing signals, multiplexers shall require no framing, allowing each subchannel to be a full one-half of the composite bit rate.

The two port multiplexer uses the bits from port A and B for bits A_1 and A_2 respectively of the dibits defined in § 4.

12.1 *Transmit buffers*

In the transmitter of each multiplex port, there shall be a data buffer of suitable capacity. In this way, both phase variations and, within certain limits, frequency deviations are absorbed. The buffer shall be initialized when an OFF to ON condition of circuit 105 occurs and may be repositioned in the event of a buffer overflow.

Note – The buffer may reinitialize upon a DCE resynchronization signal.

12.2 *Transmit port timing arrangements*

Table 5/V.37 shows all possible combinations of port and main DCE transmit timing clock arrangements.

TABLE 5/V.37

Source of port transmitter signal element timing (used to clock in circuit 103)	Source of DCE internal transmitter element timing (internal transmit clock)	Port transmit buffer
114 (DCE source)	Internal (Independent timing)	Not required
	External [a] (Circuit 113 of selected port)	Not required
	Receiver timing (Loopback timing)	Not required
113 (DTE source) [a]	Internal (Independent timing)	Required
	External [a] (Circuit 113 of selected port)	Required for all ports except port supplying circuit 113 to DCE
	Received timing (Loopback timing)	Required

[a] In these applications a source could also be another DCE.

13 Digital interface requirements

13.1 *List of interchange circuits* (see Table 6/V.37)

The interchange circuit table is valid for the main channel or the subchannel interfaces.

TABLE 6/V.37

Interchange circuit (see Note 1)		Remark
102	Signal ground or common return	See Note 2
102a	DTE commun return	See Note 3
102b	DCE common return	See Note 3
103	Transmitted data	
104	Received data	
105	Request to send	See Note 4
106	Ready for sending	See Notes 4 and 5
107	Data set ready	
109	Data channel received line signal detector	
113	Transmitter signal element timing (DTE source)	See Note 4
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
128	Receiver signal element timing (DTE source)	
140	Loop-back/Maintenance test	
141	Local loop-back	See Note 4
142	Test indicator	See Note 6

Note 1 – When the modem is installed at the repeater station, this interface should appear at the customer's premises without restrictions regarding the data signalling rate and the provision of the voice channel. The method to achieve this is subject to national regulations.

Note 2 – The provision of this conductor is optional.

Note 3 – Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 are used.

Note 4 – Not essential in subchannel.

Note 5 – During the synchronization process of the main modem, the OFF condition of circuit 106 is signalled at all port interface.

Note 6 – Circuit 142 is present on all ports of the multiplexer, but may be activated on an individual port basis for individual port tests. All are activated simultaneously for entire modem test.

13.2 *Electrical characteristics*

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended together with the use of the connector and pin assignment plan specified by ISO 4902.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

ii) In the case of circuits 105, 106, 107 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1, or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies, with receivers configured as specified by Recommendation V.10 for category 2.

Note – For an interim period the connector and contact-assignment plan specified in ISO 2593 and commonly referred to as the "V.35 interface" may optionally be used. In this case electrical characteristics may be either V.11 for circuits 103, 104, 113, 114 and 115 together with V.10 (receivers configured as specified in category 2) for all other circuits, or V.35 Appendix II together with V.28 respectively.

14 Optional PCM interface alternative

The recommended data signalling rate is synchronous at 64 kbit/s.

For those synchronous networks requiring the end-to-end transmission of both the 8 kHz and 64 kHz timing together with the data at 64 kbit/s, an internal data signalling rate of 72 kbit/s is suggested.

The corresponding data format shall be obtained by inserting one extra bit (E) just before the first bit of each octet of the 64 kbit/s data stream.

The bits E convey alignment and housekeeping information, according to the pattern shown in Figure 1/V.37.

FIGURE 1/V.37

The use of the housekeeping bits H is determined with bilateral agreement between Administrations. When not used these bits should be assigned the value 1. A framing strategy is not specified in this Recommmendation.

When the transmission of the 8 kHz timing is not required, the data signalling rate may be 64 kbit/s.

The interfaces shall comply with the functional requirements given in Recommendation G.703 [4] for the 64 kbit/s interface. The electrical characteristics may comply with reference [5].

If an end-to-end transmission of an 8 kHz timing signal is not used, an 8 kHz timing across the interface will not be supplied nor utilized by the modem.

15 Threshold and response times of circuit 109

15.1 *Threshold*

For a data line signal level greater than −13 dBm0, circuit 109 is ON. For a data line signal level less than −18 dBm0, circuit 109 is OFF.

Note – The corresponding levels for the pilot carrier are −22 dBm0 and −27 dBm0 respectively.

The condition of circuit 109 for levels between the above levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition. To measure the thresholds of the detector, a modulated data signal with its carrier and timing pilots at the levels specified in §§ 6.5 and 6.6 above should be used.

15.2 *Response times*

ON to OFF: 15 to 50 ms.

OFF to ON:

1) For initial equalization, circuit 109 must be ON prior to user data appearing on circuit 104.

2) For re-equalization during data transfer, circuit 109 will be maintained in the ON condition. During this period, circuit 104 may be clamped to the binary 1 condition.

3) After a line signal interruption that lasts more than the ON to OFF response time:

   a) when no new equalization is needed, the exact figure is under study;

   b) when a new equalization is needed, circuit 109 must be ON prior to user data appearing in circuit 104.

The response times of circuit 109 are the time intervals between the appearance or disappearance of the line signal at the reception input terminals of the modem and the occurrence of the corresponding ON or OFF condition on circuit 109.

The line signal level should be within the range from 3 dB above the actual threshold of the line signal detector at reception and the maximum permissible level of the signal at reception.

16 Response times of circuit 106

ON to OFF response time less than or equal to 2 ms

OFF to ON response time less than or equal to 2 ms.

17 Equalizer

An automatic adaptive equalizer shall be provided in the receiver.

The receiver shall incorporate a means of detecting loss of equalization and initiating a synchronizing signal sequence in its associated local transmitter.

The receiver shall incorporate a means of detecting a synchronizing signal sequence from the remote transmitter and initiating a synchronizing signal sequence in its associated local transmitter, which may be initiated at any time during the reception of the synchronizing signal sequence.

Either modem can initiate the synchronizing signal sequence. The synchronizing signal is initiated when the receiver has detected a loss of equalization. Having initiated a synchronizing signal, the modem expects a synchronizing signal from the remote transmitter.

If the modem does not receive a synchronizing signal from the remote transmitter within a time interval equal to the maximum expected two-way propagation delay plus twice the synchronizing signal detection time, it transmits another synchronizing signal.

If the modem fails to synchronize on the received signal sequence, it transmits another synchronizing signal.

If a modem receives a synchronizing signal when it has not initiated a synchronizing signal and the receiver properly synchronizes, it returns only one synchronizing sequence.

18 Additional information for the designer

18.1 *Input level variation*

The step-change in the input level is, under normal conditions, smaller than ± 0.1 dB. The gradual input level change is smaller than ± 6 dB and includes the tolerance of the transmitter output level.

18.2 *Interference from adjacent group bands*

A sinusoidal signal of +10 dBm0 in the frequency bands of 36-60 kHz and 108-132 kHz can appear together with the data line signal at the input of the receiver.

APPENDIX I

(to Recommendation V.37)

Scrambling process

I.1 *Definitions*

I.1.1 applied data bit

The data bit which has been applied to the scrambler but has not affected the transmission at the time of consideration.

I.1.2 next transmitted bit

The bit which will be transmitted as a result of scrambling the applied data bit.

I.1.3 earlier transmitted bits

Those bits which have been transmitted earlier than the next transmitted bit. They are numbered sequentially in reverse time order, i.e. the first earlier transmitted bit is that immediately preceding the next transmitted bit.

I.1.4 adverse state

The presence of any one of certain repetitive patterns in the earlier transmitted bits.

I.2 *Scrambling process*

The binary value of the next transmitted bit shall be such as to produce odd parity when considered together with the twentieth and third earlier transmitted bits and the applied data bit unless an adverse state is apparent, in which case the binary value of the next transmitted bit shall be such as to produce even instead of odd parity.

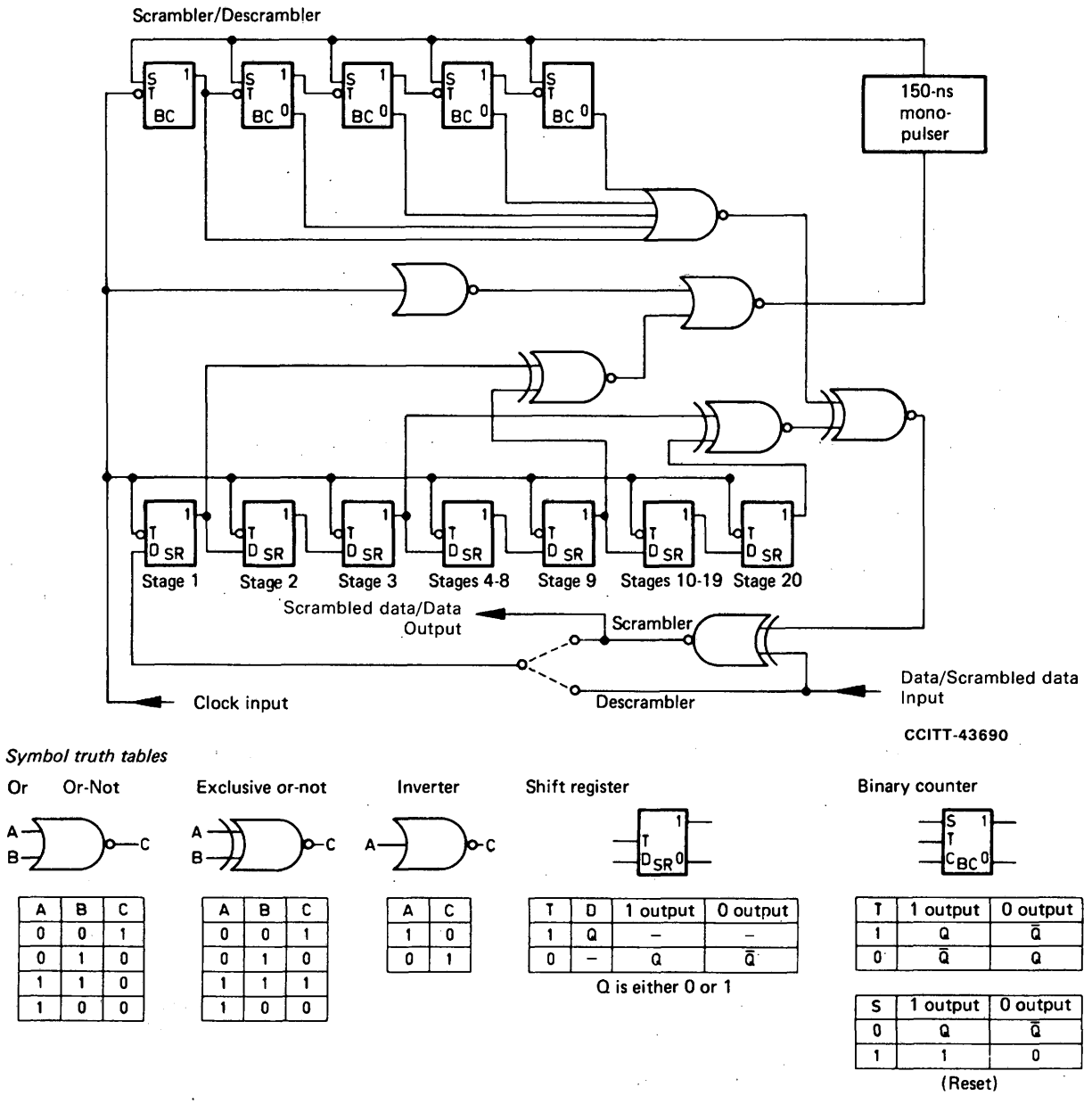
An adverse state shall be apparent only if the binary values of the p^{th} and $(p + 8)^{th}$ earlier transmitted bits have not differed from one another when p represents all the integers from 1 to q inclusive. The value of q shall be such that, for $p = (q + 1)$, the p^{th} and $(p + 8)^{th}$ earlier transmitted bits had opposite binary values and $q = (31 + 32\ r)$, r being 0 or any positive integer.

At the time of commencement, i.e. when no earlier bits have been transmitted, an arbitrary 20-bit pattern may be assumed to represent the earlier transmitted bits. At this time also it may be assumed that the p^{th} and $(p + 8)^{th}$ earlier transmitted bits have had the same binary value when p represents all the integers up to any arbitrary value. Similar assumptions may be made for the descrambling process at commencement.

Note 1 – From this it can be seen that received data cannot necessarily be descrambled correctly until at least 20 bits have been correctly received and any pair of these bits, separated from each other by seven other bits have differed in binary value from one another.

Note 2 – It is not possible to devise a satisfactory test pattern to check the operation of the Adverse State Detector (ASD) because of the large number of possible states in which the 20 state shift register can be at the commencement of testing. For those modems in which it is possible to bypass the scrambler and the descrambler and to strap the scrambler to function as a descrambler, the following method may be used. A 1 : 1 test pattern is transmitted with the ASD of the scrambler bypassed. If the ASD of the descrambler is functioning correctly the descrambled test pattern will contain a single element error every 32 bits, i.e. 180 000 errors per minute for a modem operating at 96 kbit/s indicates that the descrambler is functioning correctly. The operation of the ASD of the scrambler may be checked in a similar manner with the scrambler strapped as a descrambler and the descrambler bypassed.

I.3 Figure I-1/V.37 is given as an indication only, since with another technique this logical arrangement might take another form.



A	B	C
0	0	1
0	1	0
1	1	0
1	0	0

A	B	C
0	0	1
0	1	0
1	1	1
1	0	0

A	C
1	0
0	1

T	D	1 output	0 output
1	Q	–	–
0	–	Q	$\bar{Q}$

T	1 output	0 output
1	Q	$\bar{Q}$
0	$\bar{Q}$	Q

S	1 output	0 output
0	Q	$\bar{Q}$
1	1	0

Note – Negative-going transitions of clocks (i.e. 1 to 0 transitions) coincide with data transitions. This is self-synchronizing.

FIGURE I-1/V.37

An example of scrambler and descrambler circuitry

References

[1] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals*, Vol. III, Fascicle III.4, Rec. H.14, § 2.

[2] CCITT Recommendation *Transmission of wide-spectrum signals (data, facsimile, etc.) on wideband group links*, Vol. III, Fascicle III.4, Rec. H.52.

[3] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals*, Vol. III, Fascicle III.4, Rec. H.14, § 3.

[4] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces*, Vol. III, Fascicle III.3, Rec. G.703, § 1.

[5] *Ibid.*, § 1.2.

SECTION 4

ERROR CONTROL

Recommendation V.40

ERROR INDICATION WITH ELECTROMECHANICAL EQUIPMENT

(Mar del Plata, 1968)

If use is made of a code providing for the introduction into each character signal of an extra unit for the parity check, it is possible with electromechanical equipment to detect errors not only in the transmission channel but also in part of the mechanical translation or transmission equipment.

It might be possible therefore, when an error is detected in a character signal, to arrange for an error indication to be given on the position where the error is found.

This indication could take the form of an extra perforation in the tapes of the perforated tape equipment or a special printout with direct printing equipment.

Such devices would however be either very costly or only partially effective (for example, many character signals of the International Alphabet No. 5 do not correspond to any printout so that for these characters the normal sign cannot be replaced by an "error" sign).

For these reasons, the CCITT *unanimously recommends*

that use of an alarm or error-counting device is the best method if a local indication is required for an error detected in a character signal.

Recommendation V.41

CODE-INDEPENDENT ERROR-CONTROL SYSTEM

(Mar del Plata, 1968, amended at Geneva, 1972)

1 General

This Recommendation is primarily intended for error control when implemented as an intermediate equipment which may be provided either with data terminal equipment or with the data circuit-terminating equipment. The appropriate interfaces are shown in Figures 1/V.41 and 2/V.41. The system is not primarily intended for use with multi-access computing systems. The Recommendation does not exclude the use of any other error-control system that may be better adapted to special needs.

The modems used must provide simultaneous forward and backward channels. The system uses synchronous transmission on the forward channel and asynchronous transmission on the backward channel. When modems to Recommendation V.23 are used with data signalling rates of 1200 or 600 bit/s in the general switched telephone network, Recommendation V.5 applies, the error-control equipment being classed as communication equipment. The margin of the synchronous receiver should be at least ± 45%.

The system employs block transmission of information in fixed units of 240, 480, 960 or 3840[1] bits and is therefore most suited to the transmission of medium or long data messages, but a fast starting procedure is incorporated to improve the transmission efficiency for shorter messages.

Error control is achieved by means of automatic repetition of a block upon request (ARQ) from the data receiver. If storage is provided at the receiver, detected errors can be removed before the system output (clean copy). Storage for at least two data blocks must be provided at the transmitter.

The forward bit stream is divided into blocks each consisting of four service bits, the information bits, and 16 error-detection (or check) bits in that order, the check bits being generated in a cyclic encoder. Thus each block transmitted to line contains 260, 500, 980 or 3860[1] bits.

The system will detect:

a) all odd numbers of errors within a block;

b) any error burst not exceeding 16 bits in length and a large percentage of other error patterns.

Assuming a distribution of errors as recorded in reference [1], the error-rate improvement factor has been indicated by a computer simulation to be of the order of 50 000 for a block size of 260 bits.

The fixed block system employed limits the use of the system to those lines having a loop propagation time not greater than the figures given in Table 1/V.41. Allowances of 40 ms for total modem delay and 50 ms for the detection of the RQ signal have been made.

TABLE 1/V.41

Maximum permissible line loop propagation times (ms)

Block size (bits) \ Data signalling rate (bit/s)	200	600	1200	2400	3600	4800
260	1 210	343	127	18	–	–
500	2 410	743	327	118	49	14
980	4 810	1543	727	318	182	114
3860	19 210	6343	3127	1518	982	714

2 Encoding and checking process

The service bits and information bits, taken in conjunction, correspond to the coefficients of a message polynomial having terms from x^{n-1} (n = total number of bits in a block or sequence) down to x^{16}. This polynomial is divided, modulo 2, by the generating polynomial $x^{16} + x^{12} + x^5 + 1$. The check bits correspond to the coefficients of the terms from x^{15} to x^0 in the remainder polynomial found at the completion of this division. The complete block, consisting of the service and information bits followed by the check bits, corresponds to the coefficients of a polynomial which is integrally divisible in modulo 2 fashion by the generating polynomial.

[1] This block length is suitable for circuits provided by means of geostationary orbit satellites.

At the transmitter the service bits and information bits are subjected to an encoding process equivalent to a division by the generator polynomial. The resulting remainder is transmitted to line immediately after the information bits, commencing with the highest order bits.

At the receiver, the incoming block is subjected to a decoding process equivalent to a division by the generator polynomial which in the absence of errors will result in a zero remainder. If the division results in other than a zero remainder, errors are indicated.

The above processes may conveniently be carried out by a 16-stage cyclic shift register with appropriate feedback gates (see Figures I-1/V.41 and I-2/V.41) which is set to the all 0 position before starting to process each block; at the receiver the all 0 condition after processing a block indicates error-free reception.

Use of scramblers – Where self-synchronizing scramblers (i.e. scramblers which effectively divide the message polynomial by the scrambler polynomial at the transmitter and multiply the received polynomial by the scrambler polynomial at the receiver) are used, in order to ensure satisfactory performance of the error-detecting system, the scrambler polynomial and the Recommendation V.41 generating polynomial must have no common factors. Where this condition cannot be maintained, the scrambling process must precede the error detection encoding process and the descrambler process must follow the error detection decoding process. Where additive (i.e. non-self-synchronizing) scramblers are used, this precaution need not be observed.

3 The service bits

3.1 *Block sequence indication*

The four service bits at the beginning of each block transmitted to the line indicate the block sequence and convey control information external to the message information. One of these control functions is to ensure that the information block order can be checked during repetitions, thus ensuring that information is not lost, gained or transposed. Three block sequence indicators A, B and C are used cyclically in that order.

Once a sequence indicator has been attached to an information block it remains with that block until the block is received correctly. Examination of the sequence indication is an additional part of the checking process.

3.2 *Allocation of service bits*

The allocation of the 16 possible combinations of the four service bits is given in Tables 2/V.41 and 3/V.41. Table 2/V.41 lists essential and therefore mandatory combinations and Table 3/V.41 optional combinations.

TABLE 2/V.41

Essential combinations

Group	Combination	Function
a	0011	Block A sequence indicator
b	1001	Block B sequence indicator
c	1100	Block C sequence indicator
d	0101	Synchronizing sequence prefix

Note – The digit on the left occurs first.

TABLE 3/V.41

Optional combinations

Group	Combination	Function
e	0110	Hold block
f	1000	End of transmission (this block contains no data)
g	0001	Start of message 1 (five-unit codes)
h	1010	Start of message 2 (six-unit codes)
j	1011	Start of message 3 (seven-unit codes)
k	0010	Start of message 4 (eight-unit codes)
l	0100	End of message (this block contains no data)
m	0111	Data link escape (general control block)
n	1101	To be allocated by bilateral agreement
p	1110	
q	1111	
r	0000	

3.3 *Control functions*

Synchronization is the only essential control function catered for in the service bits.

The optional *Data link escape* (general control) block contains data which are special in some way agreed to by the users.

Additional optional functions are *Start of message 1* (or for five-unit codes), *Start of message 2* (or for six-unit codes), *Start of message 3* (or for seven-unit codes), *Start of message 4* (or for eight-unit codes), *End of message*, and *End of transmission.*

Four additional service bit combinations are available for allocation by bilateral agreement.

The message information part of the non-data blocks (*Hold, End of transmission* and *End of message*) is of no significance, but such blocks will still be checked at the receiver.

When the optional facilities groups g to k are not used, the first data block following the OFF to ON transition of *Ready for sending* is automatically prefixed *Block A sequence indicator, group a.* Data blocks BCABC, etc. then follow sequentially unless one (or more) of the other types of block are inserted.

When the optional facilities groups g to k are used, the first data block is prefixed by one of the *Start of message indicators* 1, 2, 3 or 4 (groups g to k), depending on the number of bits per character which will be used during transmission. Data blocks ABCAB, etc. then follow. Should an interruption to a leased type connection occur during transmission or should an operator interrupt the transmission to change to the speech mode, the transmission will be resumed with the sequence indicator following that of the last block to be accepted before the interruption. A *Start of message* indicator should not be used after such an interruption.

In the case of switched connections, special measures may be necessary to ensure that an interrupted message is not continued by a new message without appropriate indication.

4 Correction procedure

A binary 1 condition on the backward channel (the supervisory channel) indicates the need for repetition of information (RQ). Conversely, a binary 0 implies acceptance of the transmitted information. The rules governing the transmission and reception of these conditions are given in the following and §§ 5 and 6 below.

4.1 *Data transmitter sequence*

Starting and resynchronizing conditions are given in §§ 5 and 6 below, only normal operations being dealt with here.

Data are transmitted block by block, but the contents of each transmitted block together with its service bits are held in store at the transmitter until correct reception has been ensured. Storage for at least two blocks must be provided.

During transmission of a block the condition of the backward channel (circuit 119) is monitored for a period of 45-50 milliseconds immediately prior to transmission of the last check bit. If any RQ is found within this period the block is rendered invalid by inverting this last bit. The transmitter then recommences transmission from the beginning of the previous block by reference to the store. During the retransmission of the block which follows the detection of the RQ signal, the state of the backward channel is ignored.

4.2 *Receiver procedure*

In normal operation a binary 0 is maintained on the backward channel as long as blocks are received with correct check bits and permissible service combinations. Any data contained in these blocks are passed to the receiver output. If a clean copy output is required, data storage for at least one block should be provided since a block cannot be checked until it has been completely received.

When a block has been received which does not meet the error check condition, binary 1 is transmitted on the backward channel and the expected service bit combination is noted in the receiver.

Usually, the first received data block in the repetition cycle having correct check bits also will have an acceptable service bit combination and any data within it will be processed. Occasionally the first block which checks correctly may bear an abnormal service bit combination due to a line transmission error in the backward channel (causing either a mutilated or imitated binary 0 signal). In either case the data in this first block are discarded. In the case that the block checks correctly but the service bit combination indicates the block preceding the expected block, a binary 0 should be applied to the backward channel.

If the next block checks correctly and bears an acceptable service bit combination, its data should be processed and normal operation resumed. In the case that the service bit combination indicates an invalid block, a binary 1 should be applied; moreover, if the service bit combination indicates the block following the expected block, it is implied that a binary 0 has been imitated for the whole of the 45 ms period specified in § 4.1 above and an alarm must be given since it is not possible to recover from this (rare) condition automatically.

5 Starting procedures

5.1 *Transmitter procedures and synchronizing pattern*

During the delay between *Request to send* and *Ready for sending*, line idle conditions (binary 1) are emitted by the modem. The first data signals, after the modem is ready for sending, are the synchronizing sequence prefix (0101), followed by the synchronizing filler, followed by the synchronizing pattern. The filler may be of any length provided it includes at least 28 transitions and does not include the synchronizing pattern. The synchronizing pattern is 0101000010100101 starting from the left-hand digit (see Appendix I for a possible derivation). The 28 transitions are provided for bit synchronization purposes. These synchronizing signals are followed by *Block A* or a *Start of message* block (groups g to k in Table 3/V.41). During the whole of this sequence from the beginning of the synchronizing prefix the transmitter ignores the condition of the backward channel, acting as though binary 0 were present. The condition of the backward channel then assumes its normal significance (see § 4 above). Should this be binary 1 during the examination period of the second block, this block must be completed with the last bit inverted and the starting procedure must be recommenced from the beginning of the synchronizing sequence prefix.

5.2 *Receiver procedures*

Binary 1 is emitted on the backward channel at the receiving terminal until the synchronizing pattern (0101000010100101) is detected, at which time binary 0 is emitted and block timing is established. The only acceptable service bit combinations to follow the synchronizing pattern are the *Block A* sequence indicator or a *Start of message* indicator (when used). If other service bit combinations are received, binary 1 is returned and the search for the synchronizing pattern is resumed.

6 Resynchronization procedure

6.1 *Recovery of synchronization*

Should the receiver fail to recognize an acceptable block within a reasonable time, then it must examine the incoming bit stream continuously to find the synchronization pattern. When this pattern is found, block timing is re-established and the binary 0 condition applied to the backward channel; the procedure is identical to the starting procedure except that the expected service bit combination is that following the last sequence indicator to have been accepted.

6.2 *Emission of synchronization pattern*

If the normal repetition cycle has continued for a number of times consecutively (typically 4 or 8) the transmitter must assume that resynchronization is necessary. The normal repetition cycle is replaced by a three-block cycle including a synchronization block and the two blocks previously repeated. The synchronization block contains the synchronization sequence prefix, filler and pattern as described in § 5.1 above.

Note – A short filler should result in quicker resynchronization, particularly when long blocks are used. However, the short filler has the disadvantage that correct synchronization can be lost if the prefix is imitated or disturbed by noise or should the synchronization pattern be disturbed. The use of the longer filler, making the block the same length as the data block, overcomes this difficulty. There is the option to choose either length, both lengths being compatible.

6.3 *Use of synchronization block for delay in transmission*

The information flow may be suspended by the insertion of a synchronizing "block". In the case of the short filler it is essential that the receiving terminal should recognize the synchronizing prefix and change itself immediately into the synchronizing search mode, otherwise synchronization will be lost. In the case of the filler which produces a normal block length it is desirable to change into the search mode without abandoning block timing, a backward binary 0 being returned at the end of the block if the prefix is recognized and the check bits correspond to the synchronization pattern.

It may happen that the transmitter emits a resynchronization cycle before the receiver has changed into the synchronization search condition. The procedure at the receiver is identical to that just described for the use of a synchronization block for suspending the information flow.

7 Interfaces

7.1 *Modem interfaces*

In the normal case where the modems are not an integral part of the data terminal, the modem interfaces are as shown at points A-A in Figures 1/V.41 and 2/V.41. Where synchronous modems are employed, the appropriate signal element timing circuits will also be included in these interfaces.

7.2 *Data terminal interfaces*

Where the error control equipment (including stores) is not an integral part of the data terminal, the error control equipments are interposed between the data terminals and the modem. The data terminal interfaces are then as indicated at B-B and C-C in Figures 1/V.41 and 2/V.41 respectively. A signal element timing circuit is included in each of these interfaces.

7.2.1 In the case of the transmitting terminal all the interchange circuits perform their usual functions but *ready-for-sending* also takes advantage of the final paragraph of its definition in Recommendation V.24 and performs in the following manner:

Ready-for-sending circuit (see Figure 1/V.41)

This circuit, in conjunction with the signal element timing circuit, will inform the data terminal equipment when data are required in response to the *request-to-send* circuit. The *ready-for-sending* circuit will go to the ON condition when data are required and to the OFF condition when data are not required (in general this will be during the service and check bit transmissions and any repetition). This circuit will not go to the ON condition until the *request-to-send* circuit has gone to the ON condition. All transitions of this circuit will coincide with the signal element timing transition from ON to OFF. The transition from ON to OFF will thus coincide with the signal element timing transition from ON to OFF during the 240th, 480th, 960th or 3840th bit of the information within a block, as appropriate.

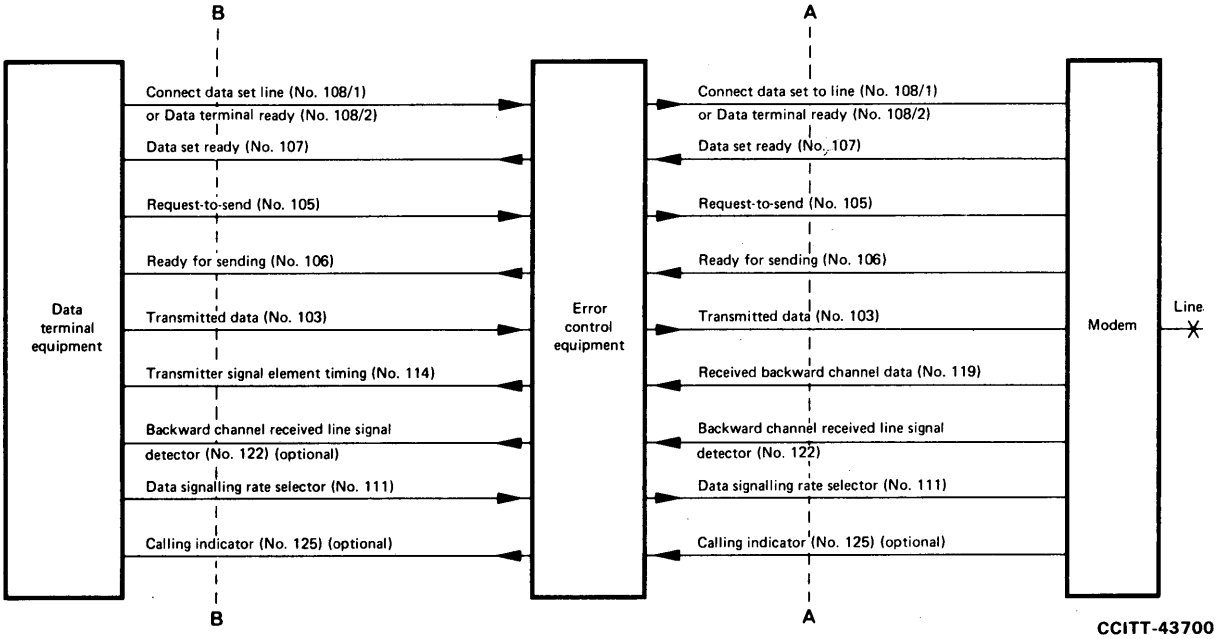


FIGURE 1/V.41

Interchange circuits – Transmitting terminal

7.2.2 In the case of the receiving terminal two new circuits are introduced, but since two (or more) of the modem interface circuits are not used in this interface, the number of circuits is not increased. Circuit 118 – *Transmitted backward channel data* is not available at this interface.

A *Ready for receiving* function must be provided to inform the error control equipment of the status of the data terminal. This function may be performed by circuit 108, in which case a connection on the switched telephone network will be released when the circuit goes from ON to OFF. Alternatively, a separate function control circuit may be provided in order to retain the line connection for short periods when the data terminal is unable to accept data. This new circuit may be assumed to take the place of circuit 120 and functions in the following manner:

Ready-for-receiving (see Figure 2/V.41)

Direction: to error control equipment from data terminal equipment

The data terminal equipment shall maintain the ON condition on this circuit when the data terminal equipment is ready to receive data. Since the error control equipment will receive data in blocks, the data terminal equipment must be capable of receiving data also in blocks. Therefore, the data terminal equipment shall change this circuit to the ON condition only if the data terminal equipment is capable of accepting a block of data (240, 480, 960 or 3840 elements) and shall return to the OFF condition if the data terminal equipment cannot accept another block within 15 element intervals after the end of the previous block of transferred data.

Note – If this *Ready for receiving* circuit is OFF at the end of this 15-element period, an RQ condition will be generated.

The other new circuit performs the function of responding to the ready-for-receiving function and is therefore analogous to circuit 121 – *Backward channel ready.* This new circuit functions as below:

Received-data-present (see Figure 2/V.41)

Direction: from error control equipment to data terminal equipment

This circuit, in conjunction with the signal element timing circuit, will inform the data terminal equipment when data are going to be output in response to the receive data terminal's connect data set to line (and separate *Ready for receiving* circuit when provided) and the incoming data from the distant end being adjudged correct. The *Received data present* circuit will go to the ON condition when data are going to be output and to the OFF condition at all other times. All transitions of this circuit will coincide with the signal element timing transition from ON to OFF. The transition from ON to OFF will thus coincide with the signal element timing transition from ON to OFF during the 240th, 480th, 960th or 3840th bit of information within a block as appropriate.

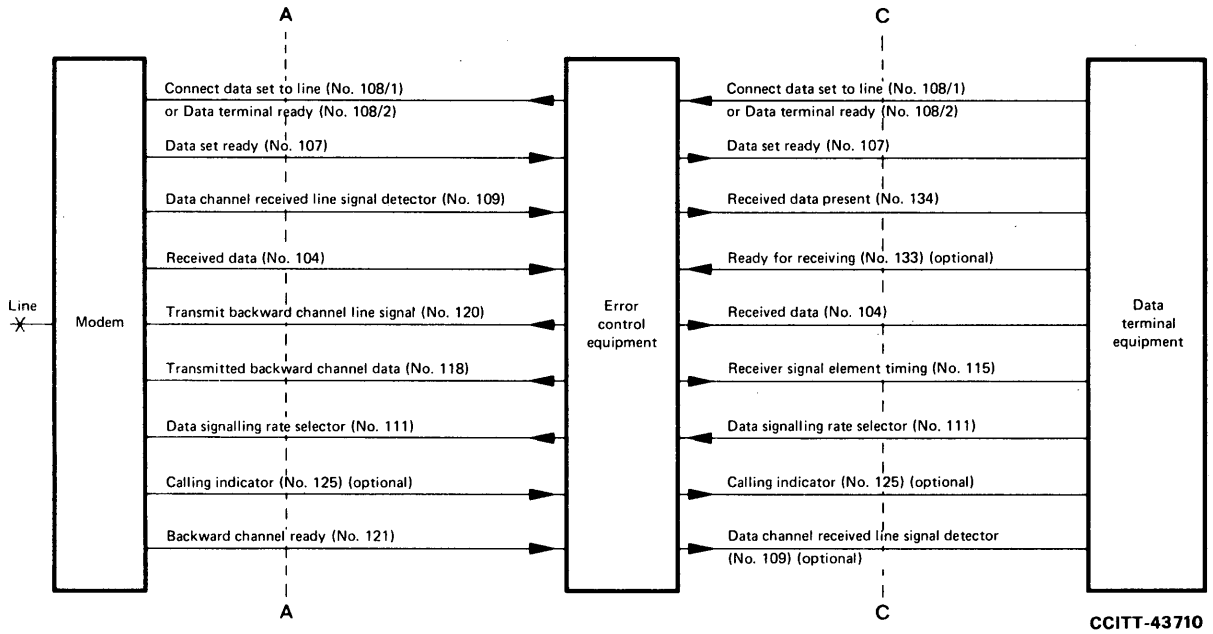


FIGURE 2/V.41

Interchange circuits – Receiving terminal

7.2.3 Additional interchange circuits may be provided at the data terminal interface by bilateral agreement of the users. These additional circuits may be used to introduce service bit control functions other than those provided as a basic necessity. Such circuits should not interfere with the operation of the recommended circuits.

8 Use of service functions

Data link escape is included in Table 3/V.41 as an optional indicator and its use is left to be agreed between operators. It may, for instance, be used to signal to a receiving station that the sending station wishes to speak over the connection. In this case the receiving equipment would operate a bell or similar calling device and transfer the line from the modem to a telephone. Alternatively, it may cause a short message to be printed on a teleprinter for the attention of an operator.

End of transmission is envisaged as giving a positive indication to the receiver that the transmission has ended and that the connection may be released. This is an alternative to the data terminal equipment interpreting the received data to know when to release the connection.

The optional start of message indicators together with the end of message indicator may be used to route messages to different destinations or terminal equipment at the receiving end, which may include the selection of equipment appropriate to the code used.

The hold block need not be used at a transmitter since synchronization sequences may be used as packing between data blocks in the event of data not being ready at the transmitting data terminal equipment, but if required a hold block may be used for this purpose.

APPENDIX I

(to Recommendation V.41)

Encoding and decoding realization for cyclic code system

I.1 *Encoding*

Figure I-1/V.41 shows an arrangement for encoding using the shift register. To encode, the storage stages are set to zero, gates A and B are enabled, gate C is inhibited and k service and information bits are clocked into the input. They will appear simultaneously at the output.

After the bits have been entered, gates A and B are inhibited and gate C is enabled, and the register is clocked a further 16 counts. During these counts the required check bits will appear in succession at the output.

Generation of the synchronizing pattern may be achieved by making $k = 4$, the four bits being 0101. Clocking is suspended for the duration of the synchronizing filler.

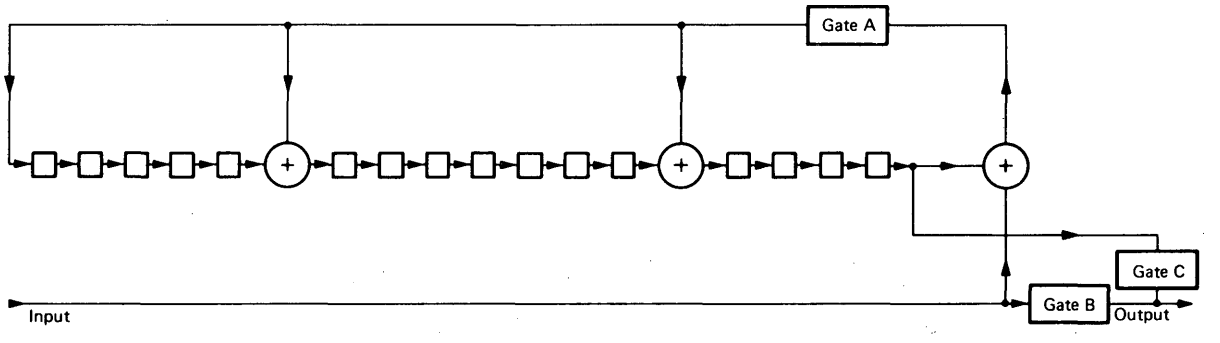


FIGURE I-1/V.41

Encoder

I.2 *Decoding*

Figure I-2/V.41 shows an arrangement for decoding using the shift register. To decode, gates A, B and E are enabled, gate D is inhibited and the storage stages are set to zero.

The k information or prefix bits are then clocked into the input and after k counts gate B is inhibited, the 16 check bits are then clocked into the input and the contents of the storage stages are then examined. For an error-free block the contents will be zero. A non-zero content indicates an erroneous block.

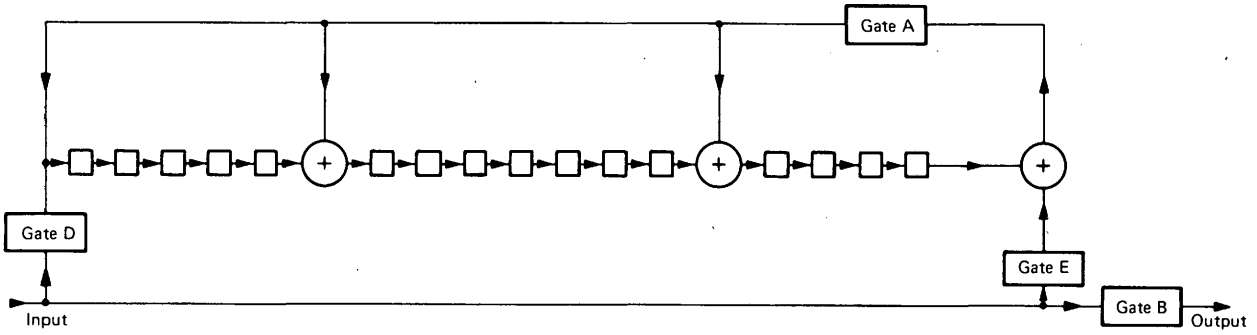


FIGURE I-2/V.41

Decoder

I.3 *Synchronizing at receiver*

For block synchronizing gate D is enabled (Figure I-2/V.41 and gates A, B and E are inhibited and the register is examined in successive bit intervals for the required 16-bit pattern. When the pattern is recognized the register and bit counter are set to zero and decoding proceeds normally.

Reference

[1] *Measurements on switched and leased telephone lines transmitting data at speeds of 250, 800 and 1000 bauds*, Blue Book, Vol. VIII, Supplement No. 22, ITU, Geneva, 1964.

Recommendation V.42

ERROR-CORRECTING PROCEDURES FOR DCES USING ASYNCHRONOUS-TO-SYNCHRONOUS CONVERSION

(Melbourne, 1988)

The CCITT,

considering

(a) that the use of high-speed DCEs for transmission of asynchronous data on the GSTN is increasing;

(b) that there is a demand for an improved error performance on such connections by the use of an error-correcting protocol;

(c) that there is a need to interwork with DCEs not providing such a protocol,

declares

that the error-correcting procedures to be followed by DCEs using asynchronous-to-synchronous conversion are as specified in this Recommendation.

CONTENTS

1 Scope

1.1 *General*

This Recommendation describes error-correcting protocols for use with V-Series duplex DCEs to accept start-stop data from the DTE and transmit in synchronous mode. Use in half-duplex DCEs is for further study.

The Recommendation contains an HDLC-based protocol referred to as the Link Access Procedure for Modems, LAPM. Additionally, an alternative procedure is defined in Annex A.

Note – There are DCEs currently in operation that implement the protocol defined in Annex A.

Compliance with this Recommendation requires implementation of both protocols. However, unless otherwise specified by user options, two V.42 DCEs will communicate using LAPM. A V.42 DCE dialing or dialled by DCEs currently in operation that only use the protcol in Annex A will communicate using that protocol.

It is the intention of CCITT to further enhance and extend the LAPM protocol. Several topics for further study are listed in Appendix V. It is not intended to further enhance the protocol defined in Annex A.

The principal characteristics of the protocols are as follows:

a) interworking in the non-error-correcting mode with V-Series DCEs that include asynchronous-to-synchronous conversion according to Recommendation V.14;

b) error detection through the use of a cyclic redundance check;

c) error correction through the use of automatic retransmission of data;

d) synchronous transmission through the conversion of start-stop data;

e) an initial handshake in start-stop format which minimizes disruption to the DTEs.

1.2 *Relationship to other international standards*

The error-correcting protocol defined in the main body of this Recommendation can be specified in terms of the High-level Data Link Control (HDLC) formats and procedures. In particular, it makes use of the Balanced asynchronous Class (BAC) of HDLC procedures. The basic mode (i.e. without options) of this protocol makes use of HDLC "Optional Functions" 1, 2, 4, 7 8 and 10. (This mode is identical to CCITT Recommendations Q.920/Q.921.) When using optional procedures of this error-correcting protocol, HDLC "Optional Functions" 3 (for selective retransmission), 12 (for loop-back test), and 14 (for 32-bit FCS) are added.

2 Definitions

An error-correcting protocol may be used with a signal converter to create an error-correcting DCE.

2.1 DCE

In this Recommendation, a DCE, when used without further qualification, consists primarily of three sections: interchange circuits for the interface to the DTE and signal converters for transmission over telephone circuits. A control function is used to provide a user interface and to coordinate the operation of the interchange circuits. A control function is used to provide a user interface to coordinate the operation of the interchange circuits and the signal converter. The structure of a DCE is shown in Figure 1/V.42.

a) The DTE exchanges data with the DCE through a V.24 interface. The data is exchanged in start-stop format.

b) The signal converter provides the modulation and demodulation of signals exchanged on the GSTN, or two-wire point-to-point leased circuits.

c) The control function provides overall control and coordination between each of the DCE components. Further, the controller provides the specific operational configuration for the DCE selected by the user. The user interface to the controller is implementation dependent.

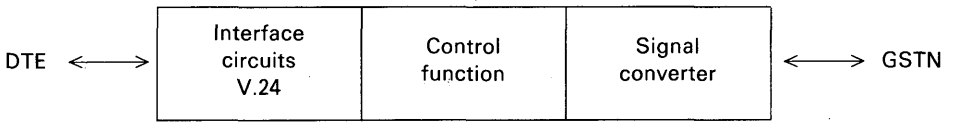


FIGURE 1/V.42

DCE

2.2 error-Correcting DCE

The logical structure of an error-correcting DCE is shown in Figure 2/V.42. The error control functions implements the error-correcting protocols of this Recommendation.

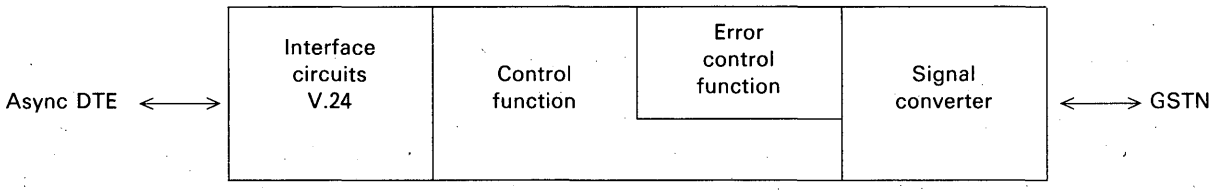


FIGURE 2/V.42

Error-Correcting DCE

3 Abbreviations

Abbreviations used in this Recommendation are:

ADP	Answerer detection pattern
C/R	Command/response bit
CRC	Cyclic redundance check
DCE	Data circuit-terminating equipment
DISC	Disconnect (frame)
DLCI	Data link connection identifier
DM	Disconnected mode (frame)
DTE	Data terminal equipment
FCS	Frame check sequence
FI	Format identifier
FRMR	Frame reject (frame)
GI	Group identifier
GL	Group length
GSTN	General switched telephone network
HDLC	High-level data link control (protocol)
I	Information (frame)
LA	Link acknowledgement (frame of the alternative error-correcting procedure)
LAPM	Link access procedure for modems
LD	Link disconnect (frame of the alternative error-correcting procedure)
LN	Link attention (frame of the alternative error-correcting procedure)
LNA	Link attention acknowledgment (frame of the alternative error-correcting procedure)
LR	Link request (frame of the alternative error-correcting procedure)
LT	Link transfer (frame of the alternative error-correcting procedure)
ODP	Originator detection pattern
P/F	Poll/Final (bit)
PI	Parameter identifier
PL	Parameter length
PV	Parameter value
REJ	Reject (frame)
RNR	Receive not ready (frame)
RR	Receive ready (frame)
SABME	Set asynchronous balanced mode extended (frame)
SREJ	Selective reject (frame)
UA	Unnumbered acknowledgement (frame)
XID	Exchange identification (frame)

4 Establishing an error-corrected connection

A connection over which the DCE's error-correcting protocol operates is established in two phases. Initially, a physical connection is established between the peer signal converters, as specified by the appropriate V-Series Recommendation. After the physical connection has been established, the signal converter is in the data mode.

Error-correcting DCEs shall provide a mechanism for enabling or disabling establishment of the error-correcting protocol. This mechanism may be used in situations where the attempt to establish the error-correcting protocol interferes with operation of the remote DTE or when error-correction between DCEs is not desired or needed (such as when the DTEs provide higher-layer error control). The ability to initiate or terminate the erro-correction protocol independent of the physical connection (i.e. while a physical connection is already in progress or retained) may optionally be provided, but coordination of protocol initiation at times other than immediately following establishment of the physical connection is not a subject of this Recommendation.

If establishment of the error-correcting protocol is enabled, then after the signal converter is in the data mode, the peer error control functions will establish the error-corrected connection.

5 Interchange circuits affected by error correction

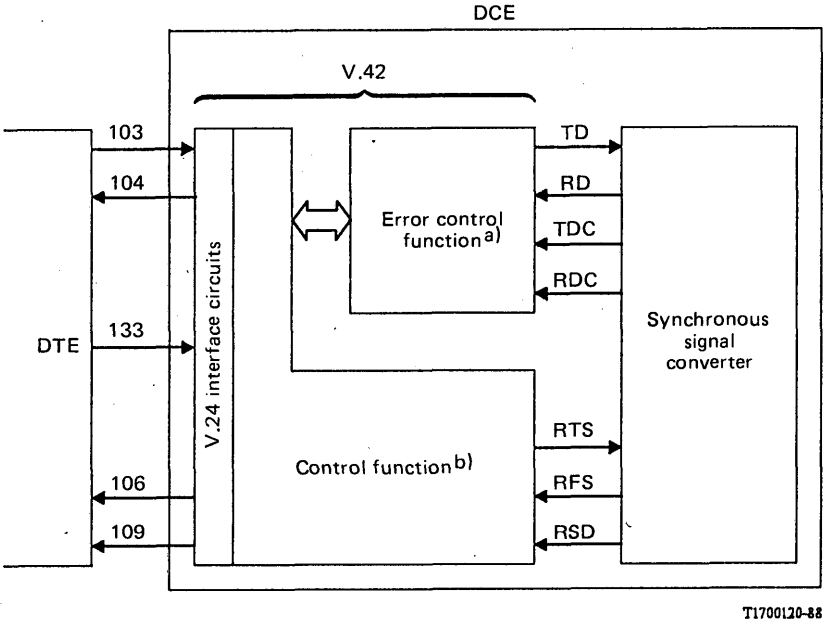
The affected circuits are listed in Table 1/V.42.

The interconnection of the functional elements of an error-correcting DCE is shown in Figure 3/V.42.

TABLE 1/V.42

Interchange circuits affected by error control

No.	Description
103	Transmitted data
104	Received data
106	Ready for sending
109	Data channel received line signal detector
133	Ready for receiving



a) See § 8 and Annex A.

b) See § 7.

FIGURE 3/V.42

Circuits affected by error control

6 Overview of error-correcting DCE operation

6.1 *General*

An error-correcting DCE, as depicted in Figure 2/V.42, contains four components:

a) V.24 interface circuits;

b) a signal converter;

c) a control function;

d) an error control function.

While the first three components are also found in the DCE depicted in Figure 1/V.42, the control function in an error-correcting DCE is enhanced beyond the functionality of a control function in a DCE. For example, the control function in an error-correcting DCE shall be capable of determining whether the remote DCE is an error-correcting DCE or a non-error-correcting DCE. The error control function is unique to an error-correcting DCE.

Paragraph 7 provides a detailed description of the control function. Paragraph 8 and Annex A provide detailed descriptions of the error-correcting protocols and their interactions with the control function.

Note – The decomposition of the functionality of an error-correcting DCE into a control function and an error control function, as well as the description of their interaction, is not meant to imply a particular method of implementation.

The remainder of § 6 gives an overview of the control function and the error control function.

6.2 *Overview of the control function*

The control function shall be responsible for the overall coordination of functions within a DCE. When realized in an error-correcting DCE, the control function shall be responsible for the following additional aspects of operation:

a) conducting an initial handshake to determine whether the remote DCE is also a V.42 error-correcting DCE;

b) falling back to a non-error-correcting mode to interwork with V-Series DCEs that include asynchronous-to-synchronous conversion according to Recommendation V.14;

c) coordinating the negotiation and/or indication of any necessary parameters;

d) coordinating the negotiation of optional procedures;

e) coordinating the establishment of an error-corrected connection after the establishment of the physical connection with a peer error-correcting DCE;

f) coordinating the delivery of data between the V.24 interface and the error control function so that data loss, to the extent possible, does not occur due to congestion on the DTE/DCE or DCE/DCE interface (this includes inspection of the characters received from the V.24 interface to determine whether the DTE has invoked flow control);

g) converting data received on the V.24 interface with start-stop framing to a format suitable for synchronous transmission;

h) converting data received on the DCE/DCE interface in synchronous format for delivery with start-stop framing on the V.24 interface;

i) processing a break (spacing) signal received on the V.24 interface for synchronous transmission;

j) processing a break indication received on the DCE/DCE interface;

k) coordinating a loop-back test;

l) re-negotiating parameters if conditions warrant it; and

m) releasing the error-corrected connection in an orderly fashion.

6.3 *Overview of the error control function*

The error control function shall be responsible for the operation of the protocol that realizes the error-corrected connection. The protocol shall have the following functional capabilities:

a) negotiation and/or indication of appropriate operational parameters;

b) negotiation of optional procedures;

c) establishment of an error-corrected connection;

d) transmission and reception of data;

e) error detection and correction;

f) transmission and reception of a break signal;

g) initiation of and responding to loop-back testing; and

h) orderly release of an error-corrected connection.

6.4 *Communication between the control function and the error control function*

Communication between the control function and error control function is modeled as a set of abstract primitives, which represents the logical exchange of information and control to accomplish a task or service. In the context of this Recommendation, the control function is viewed as the "service-user" while the error control function is viewed as the "service-provider".

A primitive is of the general form

X-NAME TYPE

where:

X designates a particular pair of communicating entities;

NAME designates the service being invoked;

TYPE designates the initiator of the communication.

Table 2/V.42 shows the services expected by the control function (i.e. the values that "NAME" can take on).

There are four "TYPES" of primitives. These are:

a) a request primitive, which is used by the service-user to request a service;

b) an indication primitive, which is used by the service-provider to notify the service-user of a request for a service or an action initiated by the service-provider;

c) a response primitive, which is used by the service-user to respond to a request for a service; and

d) a confirm primitive, which is used to indicate that a service request has been completed.

TABLE 2/V.42

Services expected by the control function

Service	Primitive	§
Establish an error-corrected connection between peer error-correcting entities	L-ESTABLISH	7.2.2
Transfert data	L-DATA	7.3
Release an error-corrected connection	L-RELEASE	7.2.2, 7.7
Transfer a break signal	L-SIGNAL	7.4, 7.5
Negotiate/indicate parameter values and optional procedures	L-SETPARM	7.6
Conduct a loop-back test between error-correcting entities	L-TEST	7.8

7 Operation of the control function

Paragraph 6.2 provided an overview of the control function. This section details the operation of the control function, which completely controls all phases of error control function operation.

7.1 *Physical handshake*

The procedures for establishing a physical connection are specified by the appropriate V-Series Recommendation. After the physical connection has been established, the control function shall be aware of the following information:

a) whether the DCE is the originating or answering DCE;

b) various aspects concerning the transmission facility (e.g. speed); and

c) the character format used by the DTE.

The method for determining the above information is beyond the scope of this Recommendation. This information is used to govern some aspects of error-correcting-DCE operation.

7.2 *Phases of error-correcting protocol establishment*

Upon receipt of an indication that the signal converter element has completed carrier handshake and that the physical connection is ready for communications, the control function initiates error-correcting protocol operation. This process has been divided into two phases:

a) the detection phase determines whether the remote DCE is also an error-correcting DCE; and

b) the protocol establishment phase determines parameter values and optional procedures to be used, as necessary, and establishes the error-corrected connection.

The detection phase has been designed to avoid the potential disruption to the called DTE that could occur if the control function immediately entered the protocol establishment phase and the remote DCE was *not* an error-correcting DCE. However, the detection phase may optionally be disabled by the user if, for example, the answering DCE is known to be of a compatible type. The error-correcting DCE does not transmit any data received on the V.24 interface to the remote DCE in error-correcting mode until the successful establishment of the error-corrected connection. At that time, the control function adjusts the V.24 interface to inform the DTE that DTE-to-DTE data transfer may commence.

7.2.1 *Detection phase*

This phase allows the control function to verify the presence of a remote error-correcting DCE.

Considerations for interworking between an error-correcting DCE and a non-error-correcting DCE are given in Appendix I.

7.2.1.1 *Determination of role*

The success of the detection phase depends on both control functions knowing their roles as originating DCE (hereinafter called the *originator*) or answering DCE (*answerer*). The role is determined by the frequencies used for communication or the role assumed during carrier handshake as assigned in the particular modulation Recommendations. In the situation where no phone call is placed (such as in a "leased line" connection) or where, because of the nature of the modulation, there is no clear differentiation between originator and answerer, the roles must be determined by parameterization (stapping options or other user indication of desired role to the control function).

7.2.1.2 *Originator actions*

The detection phase actions by the originator may be disabled by the user. In this case, the originator moves directly to the protocol establishment phase (see § 7.2.2).

If the detection phase is enabled, when circuits RFS and RSD go ON, indicating a successful connection between the signal converters, the originator shall then send the originator detection pattern (ODP). The ODP is defined as the following pattern of bits (listed left to right in order of transmission):

0 1000 1000 1 11...11 0 1000 1001 1 11...11

This pattern represents DC1 with even parity, followed by 8 to 16 one's, followed by DC1 with odd parity, followed by 8to 16 one's. The ODP is transmitted for the period of the detection phase timer, T400 (see § 9.1.1) or until the answerer detection pattern (ADP), which is defined in § 7.2.1.3, is received.

All transmissions are sent using the scrambling function of the signal converter (if any) and in synchronization with the derived carrier clock signal (i.e. without use of any inherent asynchronous speed-matching capability of the signal converter that would otherwise be used in an asynchronous non-error-correcting DCE).

The originator shall examine the incoming bit stream from the receiver signal element for the presence of the ADP. Correct receipt of the characters from at least two adjacent ADPs shall be required for the originator to determine that the pattern is being observed.

If the ADP is *not* observed within the period of T400 (see § 9.1.1), following completion of the transmission of the last repetition of the ODP the originator shall decide that the answerer does not possess V.42 error-correcting capability. In this case, the originator may fall back to non-error-correcting mode or may attempt to detect the presence of an alternative error-correcting capability, such as that described in Annex A.

If the ADP is observed within the period of T400, the originator stops transmission of the ODP and takes the appropriate action based upon the ADP received (e.g. if "EC" is received, initiate LAPM).

7.2.1.3 *Answerer actions*

Upon indication of successful establishment of a connection between the signal converters, the control function of the answerer shall transmit 1-bits (mark) until termination of the detection phase, receipt of the ODP, or detection of the start of the protocol phase (the start of the protocol phase is indicated by receipt of continuous flags, or of a LAPM or alternative procedure protocol frame).

The answerer shall examine the incoming bit stream from the signal converter for the presence of the ODP, which is defined in § 7.2.1.2. Correct receipt of at least four DC1's of alternating parity shall be required for the answerer to determine that the ODP is being observed.

If, after establishment of the physical connection, the ODP is *not* observed within the period of T400 (see § 9.1.1) and the start of the protocol establishment phase is not observed within the same period, then the answerer shall decide that the originator is not capable of V.42 error-correcting operation and shall fall back to non-error-correcting operation.

If the ODP is observed, the answerer interprets this as an indication from the originator that the originator is capable of error-correcting operation and desires to continue into the protocol establishment phase. The answerer shall immediately send one of the answerer detection patterms (ADPs) defined in Table 3/V.42 ten times.

All transmissions are sent using the scrambling function of the signal converter and in synchronization with the derived carrier clock signal.

TABLE 3/V.42

Answerer detection patterns

Type	Meaning
0 1010 0010 1 11...11 0 1100 0010 1 11...11 (E) and (C) separated by 8 to 16 one's	V.42 supported
0 1010 0010 1 11...11 0 0000 0000 1 11...11 (E) and (Null) separated by 8 to 16 one's	No error-correcting protocol desired
0 1010 0010 1 11...11 0 0000 XXXX 1 11...11	The remaining 15 code points are reserved for study and assignment

Note – The above bit patterns are listed left to right in order of transmission (i.e., low-order bit transmitted first).

7.2.2 *Protocol establishment phase*

The protocol establishment phase is initiated by the originating DCE upon successful completion of the detection phase if enabled. The purpose of this phase is to:

a) negotiate and/or indicate the parameters and any optional procedures that govern the subsequent operation of the DCE; and

b) establish the error-corrected connection.

Negotiation/indication may be omitted if default parameter values and procedures are satisfactory. When needed, the control function shall follow the procedures in § 7.6 for the negotiation/indication of parameter values and optional procedures.

After the negotiation/indication process has been completed, the originating DCE initiates establishment of the error-corrected connection. The control function in the originating DCE instructs its error control function to initiate connection establishment by issuing an L-ESTABLISH request primitive.

Upon receiving an L-ESTABLISH indication primitive from its error control function, a control function must determine whether it wishes to accept the request for error-corrected connection establishment. If it wishes to accept the request,. it issues an L-ESTABLISH response primitive; data may now be transmitted over the error-corrected connection. Otherwise, the control function issues an L-RELEASE request primitive to the error control function. The control function may fall back to operation in a non-error-control mode or it may release the physical connection.

After having issued an L-ESTABLISH request primitive, the control function, upon receipt of an L-ESTABLISH confirm primitive, considers the establishment of the error-corrected connection to be completed and may transmit data over it. If the control function receives an L-RELEASE indication primitive (e.g. as a result of a failure to set up the error-corrected connection or the remote control function refusing to accept error-corrected connection setup), then it may fall back to operation in a non-error-correcting mode or it may release the physical connection.

7.3 *Data transfer*

Upon completion of the protocol establishment phase, the control function shall request transmission by the error control function of data received on the V.24 interface. Regardless of the character format used, each character received on the V.24 interface shall be transmitted as an 8-bit character (without start and stop bits) across the DCE/DCE interface.

Annex B provides the mapping of various character formats to an 8-bit character format.

Note – It is beyond the scope of this Recommendation to specify how the control function determines when to request the error control function to transmit data. Some considerations are given in Appendix II.

To transmit data, the control function shall issue an L-DATA request primitive to the error control function. This primitive shall indicate the data to be transmitted.

Upon receipt of an L-DATA indication primitive, the control function shall deliver the received data to the V.24 interface. Each character shall contain the proper start-stop framing.

7.3.1 *Flow control across the DTE/DCE interface*

The control function will be capable of indicating to the DTE a temporary inability to accept data on Circuit 103 (DCE not-ready condition), and of recognizing a corresponding indication from the DTE (DTE not-ready condition). Upon receiving such an indication, the DCE shall and the DTE should complete transmission of any partially-transmitted character and then cease transmitting data on Circuit 104 (103) and clamp Circuit 104 (103) to binary 1. When the not-ready condition is cleared, the DCE (DTE) may resume the transmission of data on Circuit 104 (103).

The flow control indication may be performed in one of two ways:

a) using Circuit 133 and 106:

a DCE not-ready condition may be indicated by turning Circuit 106 OFF and cleared by turning Circuit 106 ON;

a DTE not-ready condition may be recognized by an ON-to-OFF transition and cleared by an OFF-to-ON transition of Circuit 133;

b) using DC1/DC3 characters (XON/XOFF functions):

a DCE not-ready condition may be indicated by transmitting a DC3 character and cleared by transmitting a DC1 character on Circuit 104;

a DTE not-ready condition may be recognized by the reception of a DC3 character and the condition cleared by the reception of a DC1 character on Circuit 103;

Optionally, DC1 and DC3 characters received from the DTE may remain in the data stream.

Both tehniques (a) and (b) shall be provided, however, the choice of technique is a user-configurable option.

The response times of the DCE of indication of a DTE not-ready condition and the DTE to indication of a DCE not-ready condition are for further study. These times should be kept as short as practical. DCEs should accommodate latency in DTE recognition of the DCE not-ready indication by accepting several characters on Circuit 103 after the indication is given.

7.4 *Transfer of break signal*

Upon receipt of a break signal on the V.24 interface, the control function shall determine:

a) how to handle data (discard or deliver) not yet transmitted across the V.24 interface or to the remote DCE; and

b) in what sequence (in sequence or preceding) the break signal shall be delivered to the remote V.24 interface with respect to data delivery.

The control function shall issue an L-SIGNAL request primitive to the error control function, indicating the break-handling option corresponding to the appropriate actions. The break-handling option and the actions to be followed are given in Table 4/V.42. The L-SIGNAL request primitive may also indicate the length of the break.

The control function shall not issue a subsequent L-SIGNAL request primitive before a prior one has been acknowledged by an L-SIGNAL confirm primitive from the error control function.

7.5 *Receipt of break*

The control function is informed of a break upon receipt of an L-SIGNAL indication primitive. It shall acknowledge this primitive with an L-SIGNAL response primitive as soon as possible. Actions to be taken on receipt of the break depend on the break-handling option, as shown in Table 5/V.42. If a break length is not indicated, a break of default length is delivered to the DTE.

7.6 *Negotiation/indication of parameter values and optional procedures*

During the protocol establishment phase (see § 7.2.2), negotiation and/or indication of parameter values and optional procedures in initiated by the control function in the originating DCE if default values are not satisfactory. It may also be initiated at any time thereafter by the control function in either DCE.

Note – The criteria by which the control function determines to change parameter values and optional procedures, once set during the protocol establishment phase, are beyond the scope of this Recommendation. Examples may include detection of changing transmission-line conditions.

The control function issues an L-SETPARM request primitive to instruct its error control function to initiate negotiation and/or indication of parameter values and optional functions.

Upon receipt of an L-SETPARM indication primitive fom its error control function, the control function shall perform the necessary negotiation (see §§ 9 and 10). It shall then issue an L-SETPARM response primitive to its error control function and complete the negotiation/indication process (see below).

Upon receipt of an L-SETPARM confirm primitive from its error control function, the control function completes the negotiation/indication process (see below).

Negotiation/indication of parameter values and optional procedures follow the prcedures in §§ 9 and 10. To complete the negotiation/indication process, the control function shall set the affected parameters to their new values and activate/deactivate the affected procedures.

Note – Some parameters are set independently of and without informing the remote DCE. In such cases, the control function sets these parameters to their new values without interacting with the error control function as described below.

TABLE 4/V.42

Transmitting DCE actions on receipt of break signal on the V.24 interface

Break handling option	With respect to data			
	Going to remote DCE	Going to local DTE	Coming from remote DCE	Coming from local DTE
Destructive/ expedited [a]	– Complete data transmission in progress, then transmit break – Discard data not yet transmitted	– Discard data not yet delivered	– Discard data until receive acknowledgement	– Hold data until receive acknowledgement
Non-destructive/ expedited	– Complete data transmission in progress, then transmit break – Hold data until receive acknowledgement	– Continue delivering data	– Continue receiving data	– Continue receiving data
Non-destructive/ non-expedited	– Wait for acknowledgement of data previsously transmitted, and then transmit break – Hold data until receive aknowledgement	– Continue delivering data	– Continue receiving data	– Continue receiving data

[a] All state variables pertaining to control function and error control function operation, except those pertaining to break transfer, are reset to their initial values.

TABLE 5/V.42

Receiving DCE actions on receipt of break from the remote DCE

Break handling option	With respect to data	
	Going to remote DCE	Going to local DTE
Destructive/expedited [a] [b]	– Discard data not yet transmitted	– Discard data not yet delivered – Deliver break signal
Non-destructive/expedited	– No effect	– Deliver break signal immediately – Resume normal data delivery
Non-destructive/non-expedited	– No effect	– Deliver break signal in sequence with respect to data

[a] All state variables pertaining to control function and error control function operation, except those pertaining to break transfer, are reset to their initial values.

[b] For all break options, acknowledgement should be returned as soon as possible.

7.7 *Orderly release of the error-corrected connection*

After prior establishment of an error-corrected connection, the control function may instruct its error control function to release the error-corrected connection in an orderly fashion by issuing an L-RELEASE request primitive. At this time, the control function considers the procedure completed. The control function also determines whether to release the physical connection.

Note – The stimuli by which the control function orders the error control function to release the error-corrected connection in an orderly fashion are beyond the scope of this Recommendation. The control function may disconnect the physical connection, without requesting an orderly release of the error-corrected connection, upon detection of the corresponding changes on the V.24 interface.

The control function is informed of an orderly release of the error-corrected connection when it receives an L-RELEASE indication primitive from its error control function. The control function may then release the physical connection and effect the corresponding changes on the V.24 interface.

7.8 *Loop-back test*

As an optional function agreed to during the protocol establishment phase, a control function may initiate a loop-back test with the remote control function.

Note – How a control function determines the need to conduct a loop-back test is for further study.

To initiate a loop-back test, the control function shall issue an L-TEST request primitive to its error control function. The control function is responsible for generating unique data to be returned by the remote control function to indicate a successful test.

A loop-back test may be initiated at any time after completion of the protocol establishment phase.

The test is considered terminated on receipt of L-TEST indication primitive containing the data sent with the L-TEST request primitive or when a locally-defined period of time has expired.

A control function receiving an L-TEST indication primitive without having issued a prior L-TEST request primitive (i.e. it needs to respond to a loop-back test from the remote control function) shall issue an L-TEST request primitive to its error control function. This primitive shall contain the data received in the L-TEST indication primitive to be returned to the test initiator.

8 Operation of the error control function: LAPM procedures

This section and Annex A describe the operation of the error control function.

Within LAPM, all messages are transmitted in *frames*, which are delimited by opening and closing *flags*. The frame structure and flag pattern are descrived in § 8.1.1 below.

The procedures in this Recommendation include functions for:

a) frame delimiting, alignment, and transparency;

b) transfer of user information (data and break);

c) sequence control;

d) detection of transmission, format, and operational errors;

e) recovery from detected transmission, format, and operational errors with notification of unrecoverable errors;

f) flow control;

g) negotiation/indication of parameter values and optional procedures; and

h) initialization and orderly release of the error-corrected connection.

In addition, LAPM makes provision for one or more "logical" error-corrected connections; discrimination between these connections is by means of a data link connection identifier (DCLI) contained in each frame.

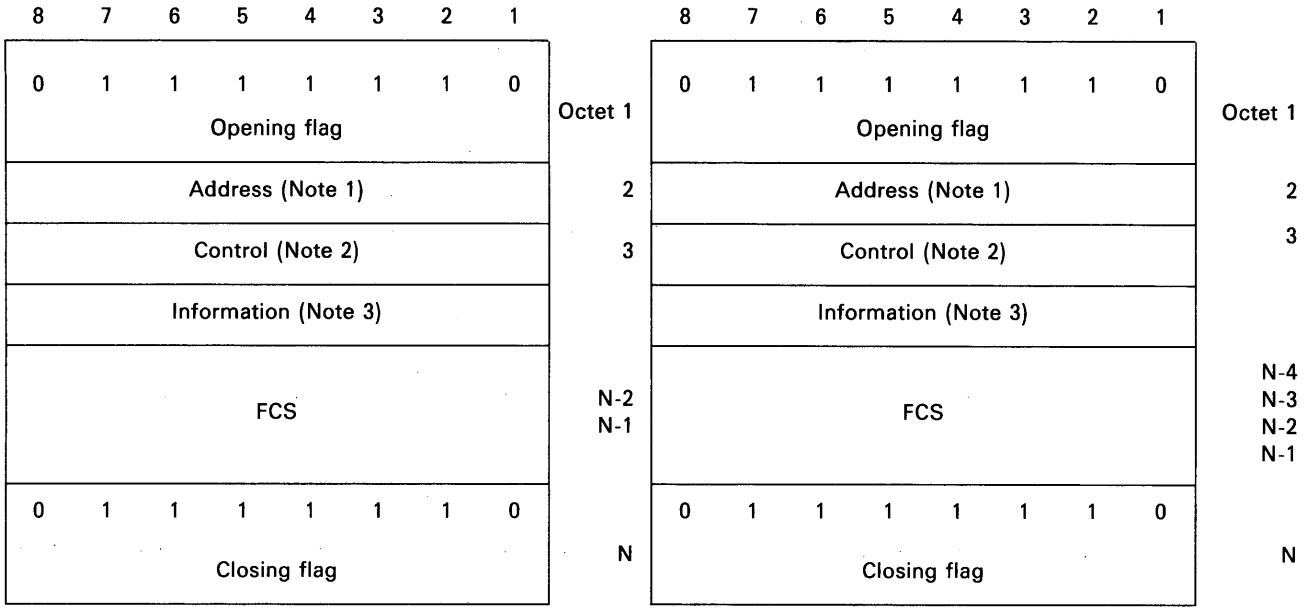
8.1 *General*

This section specifies the frame structure and procedures for the proper operation of the Link Access Procedure for Modems (LAPM).

8.1.1 *Frame structure and fields*

8.1.1.1 *Frame structure*

All DCE-to-DCE communications are accomplished using the frame structure shown in Figure 4/V.42.



a) 16-bit FCS *b) 32-bit FCS*

Note 1 – The maximum size of this field is limited to two octets.

Note 2 – The control field is two octets for frame types with sequence numbers and one octet for frame types without sequence numbers, see § 8.2.2.

Note 3 – Not all frame types have an information field

FIGURE 4/V.42

Frame structure

8.1.1.2 *Flag sequence and transparency*

All frames are delimited by the unique bit pattern "01111110", known as a *flag*. The flag preceding the address field is defined as the opening flag. The flag following the frame check sequence field is defined as the closing flag. The closing flag of one frame may also serve as the opening flag of the next frame.

Transparency is maintained by the transmitter's examinining the frame content between the opening and closing flags and inserting a "0" bit after all sequences of five contiguous "1" bits. The receiver examines the frame content between the opening and closing flags and discards any "0" bit that directly follows five contiguous "1" bits.

8.1.1.3 *Address field*

The primary purpose of the address field is to identify an error-corrected connection and the error-correcting entity associated with it. The format of this field is defined in § 8.2.1.

8.1.1.4 *Control field*

The control field is used to distinguish between different frame types. This field is further defined in § 8.2.2.

8.1.1.5 *Information field*

Depending on the frame type, an information field may also be present in the frame. The maximum number of octets in this field is governed by parameter N401 (see § 9.2.3).

8.1.1.6 *Frame check sequence (FCS) field*

This field uses a CRC polynomial to guard against bit errors.

8.1.1.6.1 *16-bit frame check sequence*

The FCS field shall be the sixteen-bit sequence preceding the closing flag. The 16-bit FCS shall be the ones complement of the sum (modulo 2) of:

a) the remainder of $x^k(x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^4 + x^3 + x^2 + x^1)$ divided (modulo 2) by the generator polynomial $x^{16} + x^{12} + x^5 + 1$, where k is the number of bits in the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency; and

b) the remainder of the division (modulo 2) by the generator polynomial $x^{16} + x^{12} + x^5 + 1$, of the product of x^{16} by the content of the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency.

As a typical implementation at the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all 1's and is then modified by division by the generator polynomial (as described above) of the address, control and information fields; the ones complement of the resulting remainder is transmitted as the sixteen-bit FCS.

As a typical implementation at the receiver, the initial content of the register of the device computing the remainder is preset to all 1's. The final remainder, after multiplication by x^{16} and then division (modulo 2) by the generator polynomial $x^{16} + x^{12} + x^5 + 1$ of the serial incoming protected bits and the FCS, will be "0001 1101 0000 1111" (x^{15} through X^0, respectively) in the absence of transmission errors.

8.1.1.6.2 *32-bit frame check sequence*

The FCS shall be the 32-bit sequence preceding the closing flag. The 32-bit FCS shall be the ones complement of the sum (modulo 2) of:

a) the remainder of $x^k(x^{31} + x^{30}1 + x^{29} + x^{28} + x^{27} + x^{26} + x^{25} + x^{24} + x^{23} + x^{22} + x^{21} + x^{20} + x^{19} + x^{18} + x^{17} + x^{16} + x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^4 + x^31 + x^2 + x^1 + 1)$ divided (modulo 2) by the generator polynomial $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$, where k is the number of bits in the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency; and

b) the remainder of the division (modulo 2) by the generator polynomial $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$, of the product of x^{32} by the content of the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency.

As a typical implementation at the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all 1's and is then modified by division by the generator polynomial (as described above) of the address, control and information fields; the ones complement of the resulting remainder is transmitted as the 32-bit FCS.

As a typical implementation at the receiver, the initial content of the register of the device computing the remainder is preset to all 1's. The final remainder, after multiplication by x^{32} and then division (modulo 2) by the generator polynomial $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ of the serial incoming protected bits and the FCS, will be "1100 0111 0000 0100 1101 1101 0111 1011) (x^{31} through x^0, respectively) in the absence of transmission errors.

8.1.2 *Format conventions*

8.1.2.1 *Numbering convention*

The basic convention used in this Recommendation is illustrated in Figure 5/V.42. The bits are grouped into octets. The bits of an octet are shown horizontally and are numbered from 1 to 8. Multiple octets are shown vertically and are numbered from 1 to n.

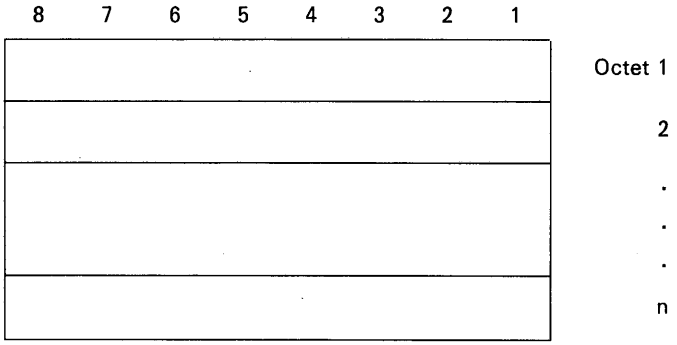


FIGURE 5/V.42

Format convention

8.1.2.2 *Order of bit transmission*

The octets are transmitted in ascending numerical order; inside an octet, bit 1 is the first bit to be transmitted.

8.1.2.3 *Field mapping convention*

When a field is contained within a single octet, the lowest bit number of the field represents the lowest-order value.

When a field spans more than one octet, the order of bit values within each octet progressively decreases as the octet number increases. The lowest bit number associated with the field represents the lowest-order value.

For example, a bit number can be identified as a couple (o,b) where o is the octet number and b is the relative bit number within the octet. Figure 6/V.42 illustrates a field that spans from bit (1,3) to bit (2,7). The high-order bit of the field is mapped on bit (1,3) and the low-order bit is mapped on bit (2,7).

An exception to the preceding field-mapping convention is the FCS field, which spans two or four octets. In this case, bit 1 of the first octet is the high-order bit; bit 8 of the second octet (for 16-bit FCS) or bit 8 of the fourth octet (for 32-bit FCS) is the low-order bit (Figure 7.V.42).

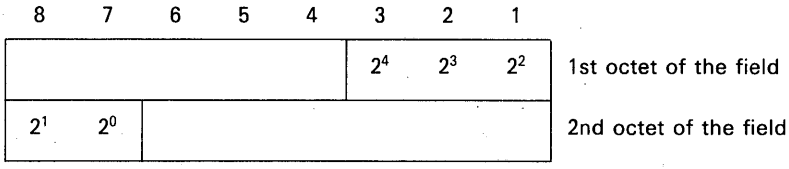


FIGURE 6/V.42

Field mapping convention

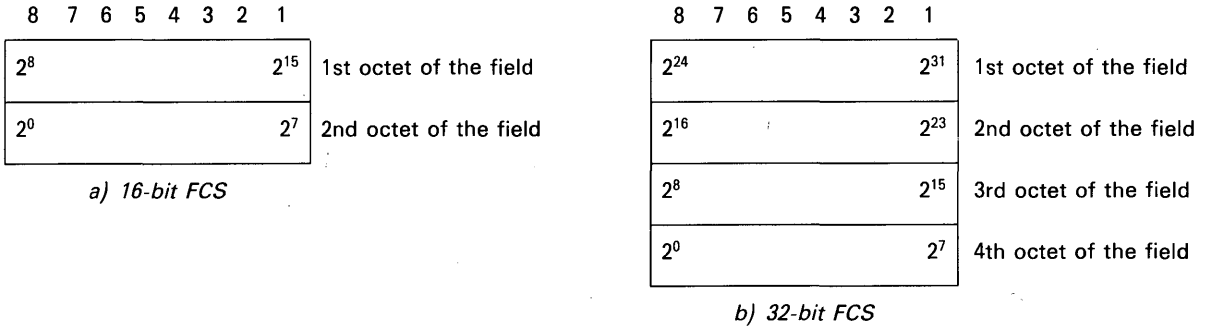


FIGURE 7/V.42

FCS mapping convention

8.1.3 *Invalid frames*

An invalid frame is one which:

a) is not properly bounded by two flags; or

b) for 16-bit FCS mode, has fewer than five octets between flags of frames that contain sequence numbers and fewer than four octets between flags of frames that do not contain sequence numbers; or

for 32-bit FCS FCS mode, has fewer than seven octets between flags of frames that contain sequence numbers and fewer than six octets between flags of frames that do not contain sequence numbers; or

c) does not consist of an integral number of octets prior to zero-bit insertion or following zero-bit extraction; or

d) contains a frame check sequence error; or

e) contains an address field with more than two octets or with a DLCI value not supported by the receiver.

Invalid frames shall be discarded without notification to the sender (however, see § 8.5.4). No action is taken as a result of having received the frame.

8.1.4 *Frame abort*

Receipt of seven or more contiguous 1 bits shall be interpreted as an abort and the error control function shall ignore the frame currently being received.

8.1.5 *Interframe time fill*

Interframe time fill is accomplished by transmitting contiguous flags between frames, i.e. multiple eight-bit flag sequences (see § 8.1.1.2).

8.2 *LAPM elements of procedures and field formats*

The elements of procedures define the comamnds and responses that are used on a LAPM error-corrected connection. Procedures, which are derived from these elements of procedures, are described in subsequent sections.

8.2.1 *Address field format*

The format of the address field is shown in Figure 8/V.42. The address field contains the data link connection identifier (DLCI), the C/R bit, and the address field extension (EA) bit.

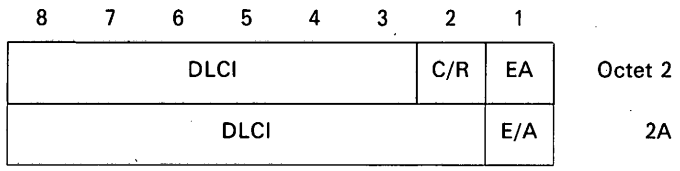


FIGURE 8/V.42

Address field format

8.2.1.1 *Data link connection identifier*

Within the scope of this Recommendation, two DLCI values are defined. One DLCI value is used to transfer information exchanged between V.24 interfaces. The other value, which is optional, is used as a control function-to-control function information connection; it is described in § 11. The value for each DLCI is defined in § 9.2.7 of this Recommendation.

When using the optional two-octet address field (see § 8.2.1.3), the DLCI also includes bits 8 through 2 of octet 2A.

8.2.1.2 *Command/response (C/R) bit field*

The C/R (command/response) bit identifies the frame as either a command or a response. In conformance with HDLC rules, a command frame contains the "address" of the error-correcting entity to which it is transmitted while a response frame contains the "address" of the error-correcting entity transmitting the frame. For a given error-corrected connection, the DLCI value of the address field remains the same but the C/R bit changes, as defined by Table 6/V.42.

TABLE 6/V.42

Command/response bit usage

Commande/response	Direction			C/R value
Command	Originator	⟶	Answerer	1
	Answerer	⟶	Originator	0
Response	Originator	⟶	Answerer	0
	Answerer	⟶	Originator	1

8.2.1.3 *Address field extension (EA) bit*

According to the rules of HDLC, the range of the address field may be extended by reserving the first transmitted bit of each octet of this field to indicate whether the octet is the last one of the field. Within the scope of this Recommendation, the address field is limited to a maximum of two octets.

When the EA bit is set to 1 in an octet, it signifies that this octet is the last octet of the address field. When the EA bit is set to 0, it signifies that another octet of the address field follows.

8.2.2 *Control field format*

The control field identifies the type of frame, which will be a command or response. The control field will contain sequence numbers, where applicable.

Three types of control-field formats are specified: numbered information transfer (I format), supervisory functions (S format), and unnumbered information transfers and control functions (U format). The control-field formats are shown in Table 7/V.42.

TABLE 7/V.42

Control field formats

Format	Control field bits (modulo 128) 8	7	6	5	4	3	2	1	
I format	N(S)							0	Octet 3
	N(R)							P	4
S format	X	X	X	X	S	S	0	1	3
	N(R)							P/F	4
U format	M	M	M	P/F	M	M	1	1	3

N(S) Transmitter send sequence number

N(R) Transmitter receive sequence number

S Supervisory function bit

M Modifier function bits

P/F Poll when issued as a command
Final bit when issued as a response

X Reserved and set to 0

8.2.2.1 *Information transfer (I) format*

The I format shall be used to perform an information transfer between error-correcting entities. The functions of N(S), N(R), and P are independent; that is, each I frame has an N(S) sequence number, an N(R) sequence number that may or may not acknowledge additional I frames received by error-correcting entity, and a P bit that may be set to 0 or 1.

8.2.2.2 *Supervisory (S) format*

The S format shall be used to perform supervisory control procedures on the error-corrected connection, such as acknowledge I frames, request retransmission of one or more I frames, and request temporary suspension of transmission of I frames. The functions of N(R) and P/F are independent; that is, each supervisory frame has an N(R) sequence number that may or may not acknowledge additional I frames received by the error-correcting entity, and a P/F bit that may be set to 0 or 1.

8.2.2.3 *Unnumbered (U) format*

The U format shall be used to provide additional connection control procedures and unnumbered information transfers. The U format does not include sequence numbers but does include a P/F bit that may be set to 0 or 1.

8.2.3 *Control field parameters and associated state variables*

The various parameters associated with the control-field formats are described in this section. The coding of the bits within these parameters is such that the lowest numbered bit within the parameter field is the least-significant bit.

8.2.3.1 *Poll/final (P/F) bit*

All frames contain the poll/final (P/F) bit. The P/F bit serves a function in both command frames and response frames. In command frames, the P/F bit is referred to as the P bit. In response frames, it is referred to as the F bit. The P bit set to 1 is used by an error-correcting entity to solicit (poll) a response frame from the peer error-correcting entity. The F bit set to 1 is used by an error-correcting entity to indicate the response frame transmitted as a result of a soliciting (poll) command.

8.2.3.2 *Variable and sequence numbers*

8.2.3.2.1 *Modulus*

Each I frame is sequentially numbered and may have the value 0 through n minus 1 (where n is the modulus of the sequence numbers). The modulus equals 128 and the sequence numbers cycle through the entire range, 0 through 127.

Note – All arithmetic operations on state variables and sequence numbers contained in this Recommendation are affected by the modulus operation.

8.2.3.2.2 *Send state variable V(S)*

Each connection shall have an associated V(S) when using I frame commands. V(S) denotes the sequence number of the next I frame to be transmitted. V(S) can take on the value 0 through n minus 1. The value of V(S) shall be incremented by 1 with each successive I frame transmission, and shall not exceed V(A) by more that the maximum number of outstanding I frames, k. The value of k may be in the range of $1 \leqslant k \leqslant 127$.

8.2.3.2.3 *Acknowledge state variable V(A)*

Each connection shall have an associated V(A) when using I frame commands and supervisory frame commands/response. V(A) identifies the last frame that has been acknowledged by its peer (V(A) – 1 equals the N(S) of the last acknowledged I frame). V(A) can take on the value 0 through n minus 1. The value of V(A) shall be updated by the valid N(R) values received from its peer (see § 8.2.3.2.6). A valid N(R) value is one that is in the range $V(A) \leqslant N(R) \leqslant V(S)$.

8.2.3.2.4 *Send sequence number (N(S)*

Only I frames contain N(S), the send sequence number of transmitted I frames. At the time that an in-sequence I frame is designated for transmission, the value of N(S) is set equal to V(S).

8.2.3.2.5 *Receive state variable V(R)*

Each connection shall have an associated V(R) when using I frame commands and supervisory frame commands/responses. V(R) denotes the sequence number of the next in-sequence I frame expected to be received. V(R) can take on the value 0 through n minus 1. The value of V(R) shall be incremented by one with the receipt of an error-free, in-sequence I frame whose N(S) equals V(R).

8.2.3.2.6 *Receive sequence number N(R)*

All I frames and supervisory frames contain N(R), the expected send sequence number of the next received I frame. At the time that a frame of the above types is designated for transmission, the value of N(R) is set equal to V(R). N(R) indicates that the error-correcting entity transmitting the N(R) has correctly received all I frames numbered up to and including N(R) – 1.

8.2.4 *Frame types*

8.2.4.1 *Commands and responses*

The command and response frames listed in Table 8/V.42 are used by either error-correcting entity. For purposes of the LAPM procedures, those frame types not identified in Table 8/V.42 are classified as undefined command and/or response control fields; the actions to be taken are specified in § 8.5.5.

The commands and responses in Table 8/V.42 are defined in §§ 8.2.4.2 through 8.2.4.14.

TABLE 8/V.42

Commands and Responses

Format	Commands	Responses	Encoding 8	7	6	5	4	3	2	1	
Information transferion	I (information)		N(S)							0	Octet 3
			N(R)							P	4
Supervisory	RR (receive ready)	RR (receive ready)	0	0	0	0	0	0	0	1	3
			N(R)							P/F	4
	RR (receive not ready)	RR (receive not ready)	0	0	0	0	0	1	0	1	3
			N(R)							P/F	4
	REJ (reject)	REJ (reject)	0	0	0	0	1	0	0	1	3
			N(R)							P/F	4
	SREJ (selective reject)	SREJ (selective reject)	0	0	0	0	1	1	0	1	3
			N(R)							P/F =0	4
Unnumbered	SABME (set asynchronous balanced mode extended)		0	1	1	P	1	1	1	1	3
		DM (disconnected mode)	0	0	0	F	1	1	1	1	3
	UI (unnumbered information)	UI (unnumbered information)	0	0	0	P/F	0	0	1	1	3
	DISC (disconnect)		0	1	0	P	0	0	1	1	3
		UA (unnumbered acknowledgement)	0	1	1	F	0	0	1	1	3
		FRMR (frame reject)	1	0	0	F	0	1	1	1	3
	XID (exchange identification)	XID (exchange identification)	1	0	1	P/F =0	1	1	1	1	3
	TEST (test)		1	1	1	P=0	0	0	1	1	3

8.2.4.2 *Information (I) command*

The function of the information (I) command is to transfer, across an error-corrected connection, sequentially numbered frames containing data received from the V.24 interface and provided by the control function.

8.2.4.3 *Set asynchronous balanced mode extended (SABME) command*

The SABME unnumbered command is used to place the addressed error-correcting entity into the *connected* state.

No information field is permitted with the SABME command. An error-correcting entity confirms acceptance of an SABME command by the transmission at the first opportunity of a UA response. Upon acceptance of this command, the error-correcting entity's V(S), V(A), and V(R) are set to 0. The transmission of an SABME command indicates the clearance of all exception conditions.

Previously-transmitted I frames that are unacknowledged when this command is processed remain unacknowledged and are discarded.

8.2.4.4 *Disconnect (DISC) command*

The DISC unnumbered command is used to return to the *disconnected* state.

No information field is permitted with the DISC command. The error-correcting entity receiving the DISC command confirms the acceptance of a DISC command by the transmission of a UA response. The error-correcting entity sending the DISC command terminates the error-corrected connection when it receives the acknowledging UA or DM response.

Previously-transmitted I frames that are unacknowledged when this command is processed remain unacknowledged and are discarded.

8.2.4.5 *Unnumbered information (UI) command/response*

Unnumbered information (UI) frames are used to convey control information outside the DTE information stream, which is carried by I frames. This control information may be associated with the DTE's information stream (e.g. a break signal). No sequence numbers are contained within the control field of a UI frame. The P/F bit of a UI frame is set to 0.

The encoding of this information field is given in § 12.3.

8.2.4.6 *Receive ready (RR) command/response*

The RR supervisory frame is used by an error-correcting entity to:

a) indicate it is ready to receive an I frame;

b) acknowledge previously received I frames numbered up to and including N(R) – 1 (as defined in § 8.4.3.1); and

c) clear a busy condition that was indicated by the earlier transmission of an RNR frame by that same error-correcting entity.

In addition to indicating the status of an error-correcting entity, the RR command with the P bit set to 1 may be used by the error-correcting entity to ask for the status of its peer error-correcting entity.

8.2.4.7 *Reject (REJ) command response*

The REJ supervisory frame is used by an error-correcting entity to request retransmission of I frames starting with the frame numbered N(R). The value of N(R) in the REJ frame acknowledges I frames numbered up to and including N(R) – 1. New I frames pending initial transmission shall be transmitted following the retransmitted I frame(s).

Only one REJ exception condition for a given direction of information transfer is established at a time. The REJ exception condition is cleared (reset) upon the receipt of an I frame with an N(S) equal to the N(R) of the REJ frame.

The transmission of an REJ frame shall also indicate the clearance of any busy condition within the sending error-correcting entity that was reported by the earlier transmission of an RNR frame by that same error-correcting entity.

In addition to indicating the status of an error-correcting entity, the REJ command with the P bit set to 1 may be used by the error-correcting entity to ask for the status of its peer error-correcting entity.

8.2.4.8 *Selective reject (SREJ) command/response*

Implementation of the selective reject (SREJ) frame is optional. When implemented, it is used by an error-correcting entity to request retransmission of the single I frame numbered N(R). Within the scope of this Recommendation, the P/F bit of a SREJ frame is always set to 0. In this case, the N(R) of the SREJ frame does not indicate acknowledgement of any I frames.

Each SREJ exception condition is cleared upon receipt of the I frame with an N(S) equal to the N(R) of the SREJ frame. An error-correcting entity may transmit one or more SREJ frames, each containing a different N(R), with the P/F bit set to 0 before one or more earlier SREJ exception conditions have been cleared.

I frames that may have been transmitted following the I frame indicated by the SREJ frame shall not be retransmitted as the result of receiving an SREJ frame. Additional I frames awaiting initial transmission may be transmitted following the retransmission of the specific I frame requested by the SREJ frame.

8.2.4.9 *Receive not ready (RNR) command/response*

The RNR supervisory frame is used by an error-correcting entity to indicate a busy condition; that is, a temporary inability to accept additional incoming I frames. The value of N(R) in the RNR frame acknowledges I frames numbered up to and including N(R) – 1.

In addition to indicating the status of an error-correcting entity, the RNR command with the P bit set to 1 may be used by the error-correcting entity to ask for the status of its peer error-correcting entity.

8.2.4.10 *Unnumbered acknowledgement (UA) response*

The UA unnumbered response is used by an error-correcting entity to acknowledge the receipt and acceptance of the mode-setting commands (SABME or DISC). Received mode-setting commands are not processed until the UA response is transmitted. No information field is permitted with the UA response. The transmission of the UA response indicates the clearance of any busy condition that was reported by the earlier transmission of an RNR frame by that same error-correcting entity.

8.2.4.11 *Disconnected mode (DM) response*

The DM unnumbered response is used by an error-correcting entity to report to its peer that the error-correcting entity is in the disconnected state and/or unable or unwilling to enter the connected state. No information field is permitted with the DM response.

8.2.4.12 *Frame reject (FRMR) response*

The FRMR unnumbered response may be received by an error-correcting entity as a report of an error condition not recoverable by retransmission of the identical frame, i.e. at least one of the following error conditions resulting from the receipt of a valid frame:

a) the receipt of a command or response control field that is undefined or not implemented;

b) the receipt of a supervisory or unnumbered frame with incorrect length;

c) the receipt of an invalid N(R); or

d) the receipt of an I frame with an information field which exceeds the maximum established length.

An undefined control field is any of the control-field encodings not identified in Table 8/V.42.

A valid N(R) value is one that is in the range $V(A) \leqslant N(R) \leqslant V(S)$.

An information field which immediately follows the control field and consists of five octets is returned with this response and provides the reason for the FRMR response. This information-field format is given in Figure 9/V.42.

8	7	6	5	4	3	2	1	
Rejected frame control field								Octet 5 6
V(S)							0	7
V(R)							C/R	8
0	0	0	0	Z	Y	X	W	9

Rejected frame control field is the control field of the received frame which caused the frame reject. When the rejected frame is an unnumbered frame, the control field of the rejected frame is positioned in octet 5, with octet 6 set to 0000 0000.

V(S) is the current send state variable value of the error-correcting entity reporting the rejection condition.

C/R is set to 1 if the frame rejected was a response and is set to 0 if the frame rejected was a command.

V(R) is the current receive state variable value of the error-correcting entity reporting the rejection condition.

W set to 1 indicates that the control field received and returned in octets 5 and 6 was undefined or not implemented.

X set no 1 indicates that the control field received and returned in octets 5 and 6 was considered invalid because the frame contained an information field which is not permitted with this frame or is a supervisory or unnumbered frame with incorrect length. Bit W must be set to 1 in conjunction with this bit.

Y set to 1 indicates that the information field received exceeded the maximum established information-field length (N401) of the error-correcting entity reporting the rejection condition.

Z set to 1 indicates that the control field received and returned in octets 5 and 6 contained an invalid N(R).

Octet 7, bit 1 and octet 9, bits 5 through 8 shall be set to 0.

FIGURE 9/V.42

FRMR information field format

8.4.2.13 *Exchange identification (XID) command/response*

XID frames are used to exchange general identification information. No sequence numbers are contained within the confrol field of an XID frame. The P/F bit of an XID frame is set to 0.

Within the scope of this Recommendation, the information field of XID frames is used for negotiation/indication of parameter values and optional procedures. The encoding of this information field is given in § 12.2.

8.2.4.14 *Test (TEST) command*

Implementation of the TEST command frame is optional. When implemented, it is used to conduct a loop-back test between the two control functions. No sequence numbers are contained within the control field of a TEST frame. the P bit of a TEST command frame is set to 0.

An information field, not specified by this Recommendation, is also included in the frame. The control function initiating a loop-back test chooses the contents of the information field. The control function responding to a loop-back test returns the information field received from the initiator.

8.2.5 *Use of timers*

For various functions in the following sections, timers are used to ensure proper operation of the protocol. In these sections, the following terminology is used to describe timer operations:

a) to *start* or *restart* a timer both imply that the timer is set to run from a predefined value;

b) to *stop* a timer implies that it no longer runs and that the value of the timer at the time it is stopped is of no significance.

8.3 *Establishment of the error-corrected connection*

8.3.1 *General*

The procedures in this section are used to establish the error-corrected connection (i.e. go from a disconnected to a connected state) to allow the transfer of user data from V.24 interface to V.24 interface.

On receipt of an L-ESTABLISH request primitive from its control function, the error control function shall attempt to establish the error-corrected connection. The L-ESTABLISH request primitive is also used to re-establish the error-corrected connection (see § 8.4.9). In either case, the error-correcting entity transmits an SABME frame. All frames other than unnumbered format frames received at this time shall be ignored.

8.3.2 *Detailed procedures*

8.3.2.1 *Establishment procedures*

A request to establish the error-corrected connection is initiated by the transmission of the SABME command. All existing exception conditions shall be cleared, the retransmission counter shall be reset, and timer T401 shall then be started (timer T401 is defined in § 9.2.1).

Note 1 – To avoid misinterpretation of a received DM response frame, the SABME frame shall always be transmitted with its P bit set to 1.

Note 2 – When sending the above frame as the first protocol frame following the detection phase (if used) or establishment of the physical connection (if the detection phase is not used), the originator shall first transmit flag patterns for a period of time sufficient to guarantee the transmission of at least 16 flag patterns.

Transmission of an SABME command as a result of receiving an L-ESTABLISH request primitive implies the discard of all data in queue.

Note – When an SABME frame is transmitted or received to establish or re-establish (see § 8.4.9) the error-corrected connection, any unacknowledged I frames remain unacknowledged with respect to the error control function. Responsibility for the contents of the information fields of such I frames reverts to the control function. Whether or not the contents of these information fields are reassigned to the error control function is decided by the control function.

An error-correcting entity receiving an SABME command, if it is able to establish the error-corrected connection (as indicated by receipt of an L-ESTABLISH response primitive from the control function in response to an L-ESTABLISH indication primitive), shall:

- respond with a UA response with the F bit set to the same binary value as the P bit in the received SABME command;
- set V(S), V(R), and V(A) to O;
- consider the error-corrected connection as established and enter the connected state;
- clear all existing exception conditions;
- clear any existing peer-receiver busy condition; and
- start timer T403 (timer T403 is defined in § 9.2.6) if implemented.

If the control function is unable to accept establishment of the error-corrected connection (as indicated by an L-RELEASE request primitive from the control function in response to an L-ESTABLISH indication primitive), the error-correcting entity shall respond to the SABME command with a DM response with the F bit set to the same binary value as the P bit in the received SABME command.

Upon receipt of the UA response with the F bit set to 1, the originator of the SABME command shall:

- stop timer T401;
- start timer T403 if implemented;
- set V(S), V(R), and V(A) to O; and
- consider the error-corrected connection as established (i.e. enter the connected state) and inform the control function by using the L-ESTABLISH confirm primitive.

Upon reception of a DM response with the F bit set to 1, the originator of the SABME command shall inform its control function of a failure to establish the error-corrected connection (by issuing an L-RELEASE indication primitive) and stop timer T401. DM responses with the F bit set to O shall be ignored in this case.

An L-RELEASE request primitive received during re-establishment initiated by the error-correcting entity shall be serviced on completion of the re-establishment procedure.

8.3.2.2 *Procedure on expiry of timer T401*

If timer T401 expires before the UA or DM response with the F bit set to 1 is received, the error-correcting entity shall:

- retransmit the SABME command as above;
- restart timer T401; and
- increment the retransmission counter (N400).

After retransmission of the SABME command N400 times and failure to receive a response, the error-correcting entity shall indicate this to the control function by means of the L-RELEASE indication primitive. Any data in queue shall be discarded.

The value of N400 is defined in § 9.2.2.

8.4 *Transfer of user data from the V.24 interface*

Having either transmitted the UA response to a received SABME command or received the UA response to a transmitted SABME command, information transfer may commence. This section deals with transfer of user data from the V.24 interface. Paragraph 8.6 deals with the transfer of control information.

8.4.1 *Transmitting I frames*

Data received by the error-correcting entity from the control function by means of an L-DATA request primitive shall be transmitted in an I frame. The control field parameters N(S) and N(R) shall be assigned the values V(S) and V(R), respectively. (V(S) shall be incremented by 1 at the end of the transmission of the I frame.

If timer T401 is not running at the time of transmission of an I frame, it shall be started. If timer T401 expires, the procedures defined in § 8.4.8 shall be followed.

If V(S) is equal to V(A) plus k (where k is the maximum number of outstanding I frames – see § 9.2.4), the error-correcting entity shall not transmit any new I frames, but may retransmit an I frame as a result of the error-recovery procedures as described in §§ 8.4.4 and 8.4.5.

When an error-correcting entity is in an own-receiver busy condition, it may still transmit I frames, provided that a peer-receiver busy condition does not exist.

Note – L-DATA request primitives received while in the timer-recovery condition (see § 8.5.3) shall be queued.

8.4.2 *Receiving I frames*

Independent of a timer-recovery condition, when an error-correcting entity is not in an own-receiver busy condition and receives a valid I frame whose N(S) is equal to the current V(R), the error-correcting entity shall:

- pass the information field of this frame to the control function using the L-DATA indication primitive;
- increment by 1 its V(R) and act as indicated below.

8.4.2.1 *P bit set to 1*

If the P bit of the received I frame was set to 1, the error-correcting entity shall respond to its peer in one of the following ways:

- if the error-correcting entity receiving the I frame is still not in an own-receiver busy condition, it shall send an RR response with the F bit set to 1;
- if the error-correcting entity receiving the I frame enters the own-receiver busy condition upon receipt of the I frame, it shall send an RNR response with the F bit set to 1.

8.4.2.2 *P bit set to 0*

If the P bit of the received I frame was set to 0 and:

a) if the error-correcting entity is still not in an own-receiver busy condition:
   - if no I frame is available for transmission or if an I frame is available for transmission but a peer-receiver busy condition exists, the error-correcting entity shall transmit an RR response with the F bit set to 0; or
   - if an I frame is available for transmission and no peer-receiver busy condition exists, the error-correcting entity shall transmit I frame with the value of N(R) set to the current value of V(R) as defined in § 8.4.1; or

b) if, on receipt of this I frame, the error-correcting entity is now in an own-receiver busy condition, it shall transmit an RNR response with the F bit set to 0.

When the error-correcting entity is in an own-receiver busy condition, it shall process any received I frame according to § 8.4.7.

8.4.3 *Sending and receiving acknowledgements*

8.4.3.1 *Sending acknowledgements*

Whenever an error-correcting entity transmits an I frame or an RR, RNR, or REJ supervisory frame, N(R) shall be set equal to V(R).

8.4.3.2 *Receiving acknowledgements*

On receipt of a valid I frame or an RR, RNR, or REJ supervisory frame, even in the own-receiver busy or the time-recovery condition, the error-correcting entity shall treat the N(R) contained in this frame as an acknowledgement for all the I frames it has transmitted with an N(S) up to and including the received N(R) – 1. V(A) shall be set to N(R). The error-correcting entity shall stop the timer T401 on receipt of a valid I frame or an RR, RNR, or REJ supervisory frame with the N(R) higher than V(A) (actually acknowledging some I frames), or an REJ frame with an N(R) equal to V(A). The error-correcting entity shall stop the timer T401 on receipt of an SREJ supervisory frame with an N(R) equal to or higher than V(A), even though there is no acknowledgement function associated with the N(R) contained in the SREJ frame.

Note 1 – If an RR, RNR, or REJ supervisory frame with P bit set to 1 has been transmitted and not acknowledged, timer T401 shall not be stopped.

Note 2 – Upon receipt of a valid I frame, timer T401 shall not be stopped if the error-correcting entity is in the peer-receiver busy condition (i.e. the remote error-correcting entity had indicated a busy condition).

If timer T401 has been stopped by the receipt of an I, RR, or RNR frame, and if there are outstanding I frames still unacknowledged, the error-correcting entity shall restart timer T401. If timer T401 then expires, the error-correcting entity shall follow the recovery procedure as defined in § 8.4.8 with respect to the unacknowledged I frames.

If timer T401 has been stopped by the receipt of an REJ frame, the error-correcting entity shall follow the retransmission procedures in § 8.4.4.

If timer T401 has been stopped by the receipt of an SREJ frame, the error-correcting entity shall follow the selective retransmission in § 8.4.5 and stop timer T401. If timer T401 then expires, the error-correcting entity shall follow the recovery procedure defined in § 8.4.8 with respect to the unacknowledged I frames.

8.4.4 *Receiving REJ frames*

On receipt of a valid REJ frame, the error-correcting entity shall act as follows:

a) if it is not in the timer-recovery condition:

- clear an existing peer-receiver busy condition;
- set its V(S) and its V(A) to the value of the N(R) contained in the REJ frame control field;
- stop timer T401;
- start timer T403 if implemented;
- if it was an REJ command frame with the P bit set to 1, transmit an appropriate supervisory response frame (see Note 2 in § 8.4.6) with the F bit set to 1;
- transmit the corresponding I frame as soon as possible, as defined in § 8.4.1, taking into account the items 1) to 3) below and the paragraph following items 1) to 3); and
- note that a protocol violation has occurred if the received frame was an REJ response frame with the F bit set to 1.

b) if it is the timer-recovery condition and it was an REJ response frame with the F bit set to 1:

- clear an existing peer-receiver busy condition;
- set its V(S) and its V(A) to the value of the N(R) contained in the control field of the REJ frame;
- stop timer T401;
- start timer T403 if implemented; and
- transmit the corresponding I frame as soon as possible, as defined in § 8.4.1, taking into account the items 1) to 3) below and the paragraph following items 1) to 3).

c) if it is in the timer-recovery condition and it was an REJ frame other than an REJ response frame with the F bit set to 1:

- clear an existing peer-receiver busy condition;
- set its V(A) to the value of the N(R) contained in the control field of the REJ frame; and
- if it was an REJ command frame with the P bit set to 1, transmit an appropriate supervisory response frame with the F bit set to 1 (see Note 2 in § 8.4.6).

Transmission of I frames shall take account of the following:

1) if the error-correcting entity is transmitting a supervisory frame when it receives the REJ frame, it shall complete that transmission before commencing transmission of the requested I frame;

2) if the error-correcting entity is transmitting an SABME command, a DISC command, a UA response, or a DM response when it receives the REJ frame, it shall ignore the request for retransmission; and

3) if the error-correcting entity is not transmitting a frame when the REJ is received, it shall immediately commence transmission of the requested I frame.

All outstanding unacknowledged I frames, commencing with the I frame identified in the received REJ frame shall be transmitted. Other I frames not yet transmitted may be transmitted following the retransmitted I frames.

8.4.5 *Receiving SREJ frames*

If the optional selective retransmission procedure has been agreed for use on the error-corrected connection, then receipt of an SREJ frame results in the retransmission of the I frame whose N(S) is equal to the N(R) in the SREJ frame. No other I frames shall be retransmitted as a result of receiving the SREJ frame (however, I frames pending initial transmission may be transmitted).

Transmission of I frames shall take account of the following:

1) if the error-correcting entity is transmitting a supervisory frame when it receives the SREJ frame, it shall complete that transmission before commencing transmission of the requested I frame;

2) if the error-correcting entity is transmitting an SABME command, a DISC command, a UA response, or a DM response when it receives the SREJ frame, it shall ignore the request for retransmission; and

3) if the error-correcting entity is not transmitting a frame when the SREJ is received, it shall immediately commence transmission of the requested I frame.

If the optional selective retransmission procedure has not been agreed for use, then receipt of an SREJ frame shall be treated as an unrecognized command/response control field (see § 8.5.5).

8.4.6 *Receiving RNR frames*

After receiving a valid RNR command or response, if the error-correcting entity is not engaged in a mode-setting operation (i.e. not transmitting an SABME or DISC frame), it shall set a peer-receiver busy condition and then:

- if it was an RNR command with the P bit set to 1, it shall respond with an RR response with the F bit set to 1 if the error-correcting entity is not in an own-receiver busy condition, and shall respond with an RNR response with the F bit set to 1 if the error-correcting entity is in an own-receiver busy condition; and
- if it was an RNR response with the F bit set to 1, an existing timer-recovery condition shall be cleared and the N(R) contained in this RNR response shall be used to update V(S).

The error-correcting entity shall take note of the peer-receiver busy condition and not transmit any I frames to the remote error-correcting entity.

Note 1 – The N(R) in any RR or RNR command frame (irrespective of the setting of the P bit) will not be used to update the send state variable V(S).

The error-correcting entity shall then:

- treat the N(R) contained in the received RNR frame as an acknowledgement for all the I frames that have been (re)transmitted with an N(S) up to and including N(R) minus 1, and set its V(A) to the value of the N(R) contained in the RNR frame; and
- restart timer T401 unless an RR, RNR, or REJ supervisory response frame with F bit set to 1 is still expected.

If timer T401 expires, the error-correcting entity shall:

- if it is not yet in a timer-recovery condition, enter the timer-recovery condition and reset the retransmission count variable; or
- if it is already in a timer-recovery condition, add one to its retransmission count variable.

The error-correcting entity shall then:

a) if the value of the retransmission count variable is less than N400:
   - transmit an appropriate RR, RNR, or REJ supervisory command (see Note 2 below) with P bit set to 1;
   - restart timer T401; and

b) if the value of the retransmission count variable is equal to N400, initiate a re-establishment procedure as defined in § 8.4.9.

The error-correcting entity receiving the RR, RNR, or REJ supervisory frame with the P bit set to 1 shall respond, at the earliest opportunity, with an RR, RNR, or REJ supervisory response frame (see Note 2 below) with the F bit set to 1 to indicate whether or not its own-receiver busy condition still exists.

Upon receipt of the RR, RNR, or REJ supervisory response with the F bit set to 1, the error-correcting entity shall stop timer T401, and:

- if the response is an RR or REJ response, the peer-receiver busy condition is cleared and the error-correcting entity may transmit new I frames or retransmit I frames as defined in § 8.4.1 or 8.4.4, respectively; or
- if the response is an RNR response, the error-correcting entity receiving the response shall proceed according to the first paragraph of this section.

If a supervisory command (RR, RNR, or REJ) with P bit set to 0 or 1, or a supervisory response frame (RR, RNR, or REJ) with the F bit set to 0 is received during the enquiry process, the error-correcting entity shall:

- if the supervisory frame is an RR or REJ command frame or an RR or REJ response frame, clear the peer-receiver busy condition and if the supervisory frame received was a command with the P bit set to 1, transmit the appropriate supervisory response frame (see Note 2 below) with the F bit set to 1. However, the transmission or retransmission of I frames shall not be undertaken until the appropriate supervisory response frame with the F bit set to 1 is received or until the expiry of timer T401; or
- if the supervisory frame is an RNR command frame or an RNR response frame, retain the peer-receiver busy condition and if the supervisory frame received was an RNR command with P bit set to 1, transmit the appropriate supervisory response frame (see Note 2 below) with the F bit set to 1.

Upon receipt of an SABME command, the error-correcting entity shall clear the peer-receiver busy condition.

Note 2 – If the error-correcting entity is not in an own-receiver busy condition and is in a reject-exception condition (that is, an N(S) sequence error has been detected and an REJ frame has been transmitted, but the requested I frame has not been received), the appropriate supervisory frame is the RR frame.

If the error-correcting entity is not in an own-receiver busy condition but is in an N(S) sequence error exception condition (that is, and N(S) sequence error has been detected but an REJ frame has not been transmitted), the appropriate supervisory frame is the REJ frame.

If the error-correcting entity is in its own-receiver busy condition, the appropriate supervisory frame is the RNR frame.

Otherwise, the appropriate supervisory frame is the RR frame.

8.4.7 *Own-receiver busy condition*

When the error-correcting entity enters an own-receiver busy condition, it shall transmit an RNR frame at the earliest opportunity.

The RNR frame may be either:

- an RNR frame with the F bit set to 0; or
- if this condition is entered on receiving a command frame with P bit set to 1, an RNR response with the F bit set to 1; or
- if this condition is entered on expiry of timer T401, an RNR command with the P bit set to 1.

All received I frames with the P bit set to 0 shall be discarded, after updating V(A).

All received RR, RNR, REJ supervisory frames with the P/F bit set to 0 shall be processed, including updating V(A).

All received SREJ supervisory frames with the P/F bit set to 0 shall be processed as specified in § 8.4.5.

All received I frames with the P bit set to 1 shall be discarded, after updating V(A). However, an RNR response frame with the F bit set to 1 shall be transmitted.

All received RR, RNR, REJ supervisory frames with the P bit set to 1 shall be processed, including updating V(A). An RNR response with the F bit set to 1 shall be transmitted.

To indicate to the peer error-correcting entity the clearance of the own-receiver busy condition, the error-correcting entity shall transmit an RR frame or, if a previously-detected N(S) sequence error has not yet been reported, an REJ frame with its N(R) set to the current value of V(R) or an SREJ frame (if agreed for use).

The transmission of an SABME command or a UA response (in reply to an SABME command) also indicates to the peer error-correcting entity the clearance of the own-receiver busy condition.

8.4.8 *Waiting acknowledgement*

The error-correcting entity shall maintain an internal retransmission count variable.

If timer T401 expires, the error-correcting entity shall:

- if it is not yet in the timer-recovery condition, enter the timer-recovery condition and reset the retransmission count variable; or
- if it is already in the timer-recovery condition, add one to its retransmission count variable.

The error-correcting entity shall then:

a) if the value of the retransmission count variable is less than N400, restart. Timer T401 and transmit an appropriate supervisory command (see Note 2 in § 8.4.6) with the P bit set to 1; or

b) if the value of the retransmission count variable is equal to N400, initiate a re-establishment procedure as defined in § 8.4.9.

The time-recovery condition is cleared when the error-correcting entity receives a valid RR, RNR, or REJ supervisory response frame with the F bit set to 1. If the received RR, RNR, or REJ supervisory frame N(R) is within the range from its current V(A) to its current V(S), inclusive, it shall set its V(S) to the value of the received N(R). Timer T401 shall be stopped if the received supervisory frame response is an RR or REJ response, and then the error-correcting entity shall resume with I frame transmission or retransmission, as appropriate. Timer T401 shall be stopped and restarted if the received supervisory response is an RNR response, to proceed with the enquiry process according to § 8.4.6.

8.4.9 *Re-establishment of the error-corrected connection*

8.4.9.1 *Criteria for re-establishment*

The criteria for re-establishing an error-corrected connection are defined in this section by the following conditions:

- the receipt, while in the connected state, of an SABME;
- the receipt of an L-ESTABLISH request primitive from the control function (see § 8.3.1);
- the occurrence of N400 retransmission failures while in the time-recovery condition (see § 8.4.8);
- the occurrence of a frame-rejection condition as identified in § 8.5.5;
- the receipt, while in the connected state, of an FRMR response frame (see § 8.5.6);
- the receipt, while in the connected state, of an unsolicited DM response with the F bit set to 0 (see § 8.5.7);
- the receipt, while in the time-recovery condition, of a DM response with the F bit set to 1.

8.4.9.2 *Procedures*

In all re-establishment situations, the error-correcting entity shall follow the procedures defined in § 8.3. All locally-generated conditions for re-establishment will cause the transmission of the SABME.

In the case of re-establishment initiated by either error-correcting entity, the error-correcting entity shall also, if V(S) > V(A) prior to re-establishment, issue an L-ESTABLISH indication primitive to the control function and discard all I frames in queue.

In the case of re-establishment initiated by the control function or if an L-ESTABLISH request primitive occurs pending re-establishment, the L-ESTABLISH confirm primitive shall be used.

8.5 *Exception condition reporting and recovery*

Exception conditions may occur as the result of errors on the physical connection or procedural errors by an error-correcting entity.

The error-recovery procedures that are available to effect recovery following the detection of an exception condition by an error-correcting entity are defined in this section.

8.5.1 *N(S) sequence error*

An N(S) sequence error exception condition occurs in the receiver when a valid I frame is received containing an N(S) value that is not equal to the V(R) at the receiver. The action of the receiver depends on whether or not the optional selective-retransmission procedure has been agreed for use on the error-corrected connection. If it has, the information field of I frames whose N(S) is not equal to the V(R) at the receiver shall be held for subsequent delivery to the control function until the expected I frame (i.e. the I frame with its N(S) = V(R) is received. If the selective-retransmission procedure has not been agreed for use, the information field of all I frames whose N(S) does not equal the V(R) shall be discarded.

In either case, the receiver shall not acknowledge (nor increment its V(R)) the I frame causing the sequence error, nor any I frames which may follow, until an I frame with the correct N(S) is received.

An error-correcting entity that receives one or more I frames having sequence errors but which are otherwise error-free, or subsequent RR, RNR, and REJ supervisory frames, shall use the N(R) and P/F bit setting contained in the control field to perform connection-control functions, for example, to receive acknowledgement of previously-transmitted I frames and to cause the error-correcting entity to respond if the P bit set to 1. Therefore, the retransmitted I frame may contain an N(R) value and P bit that are updated from, and therefore different from, the ones contained in the originally transmitted I frame.

Either the REJ frame or the SREJ frame is used by a receiving error-correcting entity to initiate an exception condition recovery (retransmission) following the detection of an N(S) sequence error.

Only one REJ exception condition for a given direction of information transfer shall be established at a time. Any number of SREJ exception conditions for a given direction of information transfer may be established at a time.

An error-correcting entity receiving an REJ command or response shall initiate sequential transmission (retransmission) of I frames starting with the I frame indicated by the N(R) contained in the REJ frame.

An error-correcting entity receiving an SREJ command or response frame shall initiate retransmission of the I frame indicated by the N(R) contained in the SREJ frame.

An REJ or SREJ exception condition is cleared when the requested I frame is received or when an SABME or DISC command is received.

Neither REJ or SREJ frames may be retransmitted (in case of loss of either, the expiration of timer T401 in the remote error-correcting entity will eventually cause resending of the requested I frame(s)). However, if examination of received I frames indicates that retransmission of the requested frame has occurred without having satisfied the reject condition, a new REJ or SREJ condition may optionally be established and the REJ or SREJ frame repeated.

8.5.2 *N(R) sequence error*

An N(R) sequence error exception condition occurs in the transmitter when a valid supervisory frame or I frame is received that contains an invalid N(R) value.

A valid N(R) is one that is in the range $V(A) \leqslant N(R) \leqslant V(S)$.

The information field contained in an I frame that is correct in sequence and format may be delivered to the control function by means of the L-DATA indication primitive.

The error-correcting entity shall initiate re-establishment according to § 8.4.9.2.

8.5.3 *Timer-recovery condition*

In an error-correcting entity, due to a transmission error, does not receive a single I frame or the last I frame(s) in a sequence of I frames, it will not detect an out-of-sequence exception condition and, therefore, will not transmit an REJ or SREJ frame.

The error-correcting entity that transmitted the unacknowledged I frame(s) shall, on the expiry of timer T401, take appropriate recovery action as defined in § 8.4.8 to determine at which I frame retransmission must begin.

8.5.4 *Invalid-frame condition*

Any frame received that is invalid (as defined in § 8.1.3) shall be discarded, and no action shall be taken as a result of that frame.

As an optional procedure in response to a received frame with an FCS error, an error-correcting entity may transmit an REJ frame rather than ignoring the frame without taking any action. In all other respects, the received frame shall be discarded, without any indication to the control function of its receipt.

8.5.5 *Frame-rejection condition*

A frame-rejection condition results from one of the conditions described in § 8.2.4.1 (first paragraph) or § 8.2.4.12, items b, c and d.

Upon occurrence of a frame-rejection condition, the error-correcting entity shall initiate re-establishment (see § 8.4.9.2).

Note – For satisfactory operation, it is essential that a receiver is able to discriminate between invalid frames, as defined in § 8.1.3, and I frames with an information field that exceeds the maximum established length (see item d) in § 8.2.4.12). An unbound frame may be assumed and thus, discarded if two times the longest-permissible frame plus two octets are received without a flag detection.

8.5.6 *Receipt of an FRMR response frame*

Upon receipt of an FRMR response frame in the connected state, the error-correcting entity shall initiate re-establishment (see § 8.4.9.2).

8.5.7 *Unsolicited response frames*

The action to be taken on the receipt of an unsolicited response frame is defined in Table 9/V.42.

TABLE 9/V.42

Actions taken on receipt of unsolicited response frame

Unsolicited response frame	Disconnected state	Awaiting connection establishment	Awaiting connection release	Connected state	
				Not in timer-recovery condition	In timer-recovery condition
UA response F = 1	Ignore *	(Solicited)	(Solicited)	Ignore *	Ignore *
UA response F = 0	Ignore *	Ignore *	Ignore *	Ignore *	Ignore *
DM response F = 1	Ignore	(Solicited)	(Solicited)	Ignore *	(Solicited)
DM response F = 0	Establish connection	Ignore	Ignore	Re-establish connection	Re-estabish connection
RR, RNR, REJ response: F = 1	Ignore	Ignore	Ignore	Ignore *	(Solicited)
RR, RNR, REJ response: F = 0	Ignore	Ignore	Ignore	(Solicited)	(Solicited)
SREJ response F = 1	Ignore	Ignore	Ignore	Re-establish connection	Re-establish connection
SREJ response F = 0	Ignore	Ignore	Ignore	(Solicited)	(Solicited)

Note 1 – For ignore-cases marked with an asterisk (*), the error-correcting entity may inform the control function of a protocol violation.

Note 2 – Cases marked as (*solicited*) represent proper protocol operation.

8.6 *Transfer of user-control information*

User-control information is transferred using the information field of UI frames. A UI frame has the same value of DLCI as that used for transferring user data.

In general, the transfer of user-control information can be done immediately or in sequence with respect to user data. In the first case, the UI frame shall be transmitted immediately after transmission of the current I frame, if any, is completed. In the second case, the UI frame is transmitted only after acknowledgement is received for all unacknowledged I frames. Whether subsequent transmission of I frames can resume immediately after the transmission of the UI frame or await some further event depends on the type of control information transmitted.

See § 8.13 for procedures for transmitting a break signal between V.24 interfaces.

8.7 *Orderly release of an error-corrected connection*

8.7.1 *General*

These procedures shall be used to return to the disconnected state.

The control function requests release of an error-corrected connection by use of the L-RELEASE request primitive.

All frames other than unnumbered frames received during the release procedurs shall be ignored.

All outstanding L-DATA and L-SIGNAL request primitives and all associated frames in queue shall be discarded.

8.7.2 *Release procedure*

An error-correcting entity shall initiate a request for release of the connection by transmitting the disconnect (DISC) command.

Note – To avoid misinterpretation of a received DM response frame, the DISC frame shall always be transmitted with its P bits set to 1.

Timer T401 shall then be started and the retransmission counter reset.

An error-correcting entity receiving a DISC command while in the connected state shall transmit a UA response with the F bit set to the same binary value as the P bit in the received DISC command. An L-RELEASE indication primitive shall be passed to the control function, and the disconnected state shall be entered.

If the originator of the DISC command receives either.

- a UA response with the F bit set to 1; or
- a DM response with the F bit set to 1, indicating that the peer error-correcting entity is already in the disconnected state,

it shall enter the disconnected state and stop timer T401.

The error-correcting entity that issued the DISC command is now in the disconnected state and will notify its control function by means of the L-RELEASE indication primitive. The conditions relating to this state are defined in § 8.8.

8.7.3 *Procedure on expiry of timer T401*

If timer T401 expires before a UA or DM response with its F bit set to 1 is received, the originator of the DISC command shall:

- retransmit the DISC command as defined in § 8.7.2;
- restart timer T401; and
- increment the retransmission counter.

If the error-correcting entity has not received the correct response as defined in § 8.7.2, after N400 attempts to recover, the error-correcting entity shall enter the disconnected state and notify its control function by means of the L-RELEASE indication primitive.

8.8 *Disconnected state*

While in the disconnected state:

- the receipt of a DISC command shall result in the transmission of a DM response with F bit set to the value of the received P bit;
- on receipt of an SABME command, the procedures defined in § 8.3 shall be followed;
- on receipt of an unsolicited DM response with the F bit set to 0, the error-correcting entity shall, if it is able to and the control function is willing, initiate the error-correction establishment procedures by the transmission of an SABME (see § 8.3.2.1); otherwise, the DM shall be ignored; and
- all other frame type shall be discarded.

8.9 *Collision of unnumbered commands and responses*

8.9.1 *Identical transmitted and received set-mode commands*

If transmitted and received unnumbered set-mode commands (SABME or DISC) are the same, the error-correcting entities shall send the UA response at the earliest possible opportunity. The indicated state (the connected state if the commands were SABMEs, or the disconnected state if they were DISCs) shall be entered after receiving the UA response. The error-correcting entity shall notify its control function by means of the appropriate primitive.

8.9.2 *Different transmitted and received set-mode commands*

If the transmitted and received unnumbered set-mode commands (SABME or DISC) are different, the error-correcting entities shall issue a DM response at the earliest possible opportunity. Upon receipt of a DM response with the F bit set to 1, the error-correcting entity shall enter the disconnected state and notify its control function by means of an L-RELEASE indication primitive.

8.9.3 *Unsolicited DM response and SABME or DISC command*

A DM response with its F bit to 0 colliding with an SABME or DISC command shall be ignored.

8.10 *Negotiation/indication of parameter values and optional procedures*

8.10.1 *General*

Upon receipt of an L-SETPARM request primitive from its control function, an error-correcting entity shall initiate procedures using XID frames to negotiate/indicate parameter values and optional procedures with the remote DCE. If data transfer is possible (i.e. the error-corrected connection is in the connected state), then the error-correcting entity shall first transmit an RNR command frame with its P bit set to 1 (see § 8.4.7) to its peer and cease transmission of I frames.

Note – This is necessary since parameters/procedures to be negotiated/indicated may affect the procedures governing I frame transmission.

Upon completion of the negotiation/indication process, the affected parameter values/procedure settings shall be recorded. If a busy condition had been initiated as part of the process of changing parameter values/procedure settings (see above), then an indication of busy-condition clearance shall be transmitted.

Paragraphs 9 and 10 indicate which parameters and procedures, respectively, may be negotiated/indicated while § 12.2 indicates the encoding of the information field of the XID frame.

8.10.2 *Negotiation/indication procedure*

Upon receipt of an L-SETPARM request primitive, the error-correcting entity shall transmit an XID command frame. The information field of this frame shall be used to convey the parameters/procedures to be negotiated/indicated to the remote error-correcting entity. Timer T401 shall then be started and the retransmission counter, N400, reset.

Note – When sending the above frame as the first protocol frame following the detection phase (if used) or establishment of the physical connection (if the detection phase is not used), the originator shall first transmit flag patterns for a period of time sufficient to guarantee the transmission of at least 16 flag patterns.

On receipt of an XID command frame used for parameter/procedure negotiation/indication, the error control function shall issue an L-SETPARM indication primitive to its control function, passing it the contents of the information field.

On receipt of an L-SETPARM response primitive from its control function, an error control function shall return the indicated parameter values/procedure settings in the information field of an XID response frame.

If 32-bit FCS is requested and agreed during the protocol establishment phase (see § 7.2.2), a called DCE shall be capable of checking subsequent frames against both the 16-bit FCS (see § 8.1.1.6.1) and the 32-bit FCS (see § 8.1.1.6.2) simultaneously (a frame shall be discarded only if it fails both FCS checks). Until a SABME frame is received, the called DCE transmits frames with a 16-bit FCS. Receipt of a SABME frame with 16- or 32-bit FCS indicates use of the corresponding FCS for all subsequent frames (and checking of frames against both the 16-bit and 32-bit FCS may be disabled). Receipt of another XID command frame, with a 16-bit FCS, shall be responded to according to the negotiation/indication rules using an XID response frame with a 16-bit FCS.

On receipt of an XID response frames used for parameter/procedure negotiation/indication, the error control function shall inform its control function by an L-SETPARM confirm primitive of the values contained in the information field.

8.10.3 *Procedure on expiry of timer T401*

If timer T401 expires before receipt of the XID response frame, the error-correcting entity shall:

- retransmit the XID command as above;
- restart timer T410; and
- increment the retransmission counter (N400).

After retransmission of the XID command N400 times and failure to receive an XID response, the error-correcting shall notify the control function that the negotiation/indication procedure did not complete.

The value of N400 is defined in § 9.2.2.

8.11 *Loop-back test*

Upon receipt of an L-TEST request primitive from its control function, the error-correcting entity shall transmit a TEST command frame with its P bit set to 0. The information field of the TEST frame shall be used to convey the information provided by the control function. An L-TEST request primitive may be received at any time after completion of the protocol establishment phase. Its receipt does not affect the flow of other frames.

On receipt of a TEST command frame with its P bit set to 0, the error-correcting entity shall issue an L-TEST indication primitive to its control function that also conveys the contents of the information field from the received TEST frame.

8.12 *Monitoring functions*

8.12.1 *General*

The procedural elements defined in the earlier parts of § 8 allow for the supervision of the error-corrected connection. This section describes procedures that may be used to provide this supervision function. The use of this function is optional.

8.12.2 *Supervision during the connected state*

The connection verification is a service provided by the error-correcting entity to its control function. This implies that the control function is informed in case of a failure only. Furthermore, the procedure may be incorporated in the "normal" exchange of information and may become more efficient than a procedure based on the involvement of the control function.

The procedure is based on supervisory command frames (RR command, RNR command) and timer T403, and operates during the connected state as follows.

If there are no frames being exchanged on the error-corrected connection (neither new nor outstanding I frames, nor supervisory frames with a P bit set to 1), there is no means to detect a faulty error-corrected connection condition. Timer T403 represents the maximum time allowed without frames being exchanged.

If timer T403 expires, a supervisory command with a P bit set to 1 is transmitted. Such a procedure is protected against transmission errors by making use of timer T401 and the N400 retransmission count.

8.12.3 *Connection verification procedures*

8.12.3.1 *Start timer T403*

The timer T403 is started:

- when the connected state is entered; and
- in the connected state whenever timer T401 is stopped.

Upon receiving an I or supervisory frame, timer T403 will be restarted if timer T401 is not to be started.

8.12.3.2 *Stop timer T403*

The timer T403 is stopped

- when, in the connected state, the timer T401 is started; and
- upon leaving the connected state.

8.12.3.3 *Expiry of timer T403*

If timer T403 expires, the error-correcting entity will act as follows (it should be noted that timer T401 is neither running nor expired):

a) set the retransmission count variable to 0;

b) enter the timer-recovery condition (see § 8.5.3);

c) transmit a supervisory command with the P bit set to 1 as follows:
   - if there is not an own-receiver busy condition, transmit an RR command; or
   - if there is an own-receiver busy condition, transmit an RNR command;

d) start timer T401; and

e) inform the control function after N400 retransmissions.

8.13 *Transfer of break*

8.13.1 *General*

Upon receipt of an L-SIGNAL request primitive from its control function, an error-correcting entity shall transmit a UI command frame with its P bit set to 0. The information field of the UI command frame shall be encoded to indicate a break (BRK) message and shall contain the break-handling option as indicated by the control function. If the L-SIGNAL request primitive includes a break length, it shall also be encoded in the information field of the UI frame. (See § 12.3 on the encoding of UI frames for transferring a break signal.) Actions taken by the DCE (including the error-correcting entity) are specified in Table 4/V42.

On receipt of a UI command frame indicating a BRK, the error-correcting entity shall issue an L-SIGNAL indication primitive to its control function, conveying the break-handling option and, if present, the break length and follow the actions specified in Table 5/V.42. On receipt of an L-SIGNAL response primitive from its control function, an error-correcting entity shall transmit a UI response frame as soon as possible with its F bit set to the same binary value as the received UI command frame. The information field of the UI response frame shall be encoded to indicate a break acknowledgement (BRKACK) message.

On receipt of a UI response frame with a BRKACK message in reply to a UI command frame conveying a BRK message, an error-correcting entity shall issue an L-SIGNAL confirm primitive to its control function.

Note – The exchange of UI frames, in and of itself, does not provide a confirmed service. The confirmed nature of the L-SIGNAL service provided to the control function, as described here, comes about through the association and interpretation of the contents of the information fields of the UI frames exchanged and not the association of a UI response frame with a previously-transmitted UI command frame.

8.13.2 *State variables and parameters*

8.13.2.1 *Send and receive sequence numbers*

To distinguish between unique and duplicate UI frames carrying break information, an error-correcting entity shall perform a sequencing operation, modulo 2, on the information field of the UI frame. Bit 8 of the first octet of the information field shall be used for this purpose. As such, bit 8 serves as a break send sequence number, N(SB), in BRK message while it serves as a break receive sequence number, N(RB), in BRKACK messages.

8.13.2.2 *Send state variable V(SB)*

The error-correcting entity shall maintain the break send state variable V(SB). V(SB) denotes the value of N(SB) in the next BRK message sent as a result of receiving an L-SIGNAL request primitive from the control function. V(SB) is complemented each time a transmitted BRK message is correctly acknowledged by a BRKACK message. Initially, when the physical connection has been established, V(SB) is set to zero; it is not reset even if the error-corrected connection is re-established per § 8.4.9.

8.13.2.3 *Receive state variable V(RB)*

The error-correcting entity shall maintain the break receive state variable V(RB). V(RB) denotes the expectd value of N(SB) in the nest BRK message to be received. If N(SB) in the next received BRK message is equal to V(RB), then V(RB) shall be complemented prior to sending the BRKACK message. Initially, when the physical connection has been established, V(RB) is set to zero; it is not reset even if the error-corrected connection is re-established per § 8.4.9.

8.13.3 *Break procedures*

8.13.3.1 *Transmitting a BRK message*

On receipt of an L-SIGNAL request primitive, the error-correcting entity shall transmit a BRK message in a UI command frame with its P bit set to 0. The error-correcting entity shall set N(SB) to the current value of V(SB), start the acknowledgement timer T401 (see § 9.2.1) and set the retransmission counter N400 (see § 9.2.2) to zero.

8.13.3.2 *Receiving a BRK message*

When receiving a BRK message in a UI command frame, the error-correcting entity shall check whether N(SB) is equal to the current value of V(RB). If it is, the error-correcting entity shall issue an L-SIGNAL indication primitive to the control function, passing it the break-handling option and, if present, the length of break information. The error-correcting entity shall also complement the value of V(RB).

Upon receipt of an L-SIGNAL response primitive, the error-correcting entity shall transmit a BRKACK message in a UI response frame with N(RB) equal to the value of V(RB). The F bit of the UI response frame shall be set to the same binary value as the received UI command frame.

If N(SB) in the received BRK message is not equal to V(RB), then the error-correcting entity shall discard the BRK message and retransmit the previous BRKACK message with N(RB) equal to the current value of V(RB). No L-SIGNAL indication primitive shall be issued to the control function.

8.13.3.3 *Receiving a BRKACK message*

When receiving a BRKACK message in a UI response frame, the error-correcting entity shall check whether N(RB) is equal to V(SB) + 1. If it is, the error-correcting entity shall complement V(SB), stop the acknowledgement timer T401, and issue an L-SIGNAL confirm primitive to the control function. If N(RB) is not equal to V(SB) + 1, the error-correcting entity shall ignore the BRKACK message.

8.13.3.4 *Expiration of the acknowledgement timer*

If T401 expires before a BRKACK message is received to acknowledge the last BRK message transmitted, the error-correcting entity shall retransmit the BRK message with N(SB) equal to the current value of V(SB). No more than N400 retransmissions shall occur. Failure to receive a BRKACK after N400 retransmissions shall be reported to the control function.

9 System parameters

This section specifies the parameters needed for proper operation. For each parameter, it indicates:

a) whether the parameter is used by the control function or the error control function;

b) the definition of the parameter;

c) whether information about the parameter is carried in XID frames and, if so, whether the information is for negotiation or indication purposes;

d) for those parameters that are negotiated by XID frames, what the negotiation rules are; and

e) what the default value of the parameter is.

9.1 *Parameters of the control function*

9.1.1 *Detection phase timer (T400)*

The detection phase timer governs the amount of time that a control function in an originating or answering DCE waits for the ADP or the ODP, respectively (see § 7.2.1). Information about this timer is *not* carried in XID frames. The default value shall be 750 ms. (This is the estimated maximum propagation delay of all required transmissions including a single satellite link, plus sufficient time for the required transmissions at the data rate used in any V-Series modem that uses asynchronous-to-synchonous conversion.)

Note – Implementations may provide a mechanism for the user to set a value different from the default.

9.2 *Parameters of the error control function*

9.2.1 *Acknowledgement timer (T401)*

The acknowledgement timer governs the amount of time that an error-correcting entity will wait for an acknowledgement before resorting to other action (e.g. transmitting a frame). Information about this timer is *not* carried in XID frames. The two error-correcting entities associated with an error-corrected connection may operate with a different value of T401.

Note – This timer should be regarded as a logical parameter. That is, there can be one acknowledgement timer associated with each LAPM function (e.g. transmitting an I frame, transmitting a BRK message) that requires an acknowledgement to be received before expiration of this timer. This does not necessarily imply separate timer circuits.

Appendix IV shows the various factors that influence T401.

9.2.2 *Maximum number of retransmissions (N400)*

N400 governs the maximum number of times that an error-correcting entity will re-attempt a procedure requiring a response. Information about this counter is *not* carried in XID frames. The two error-correcting entities associated with an error-corrected connection may operate with a different value of N400. While no default value is specified for N400, it shall have a minimum value of 1.

9.2.3 *Maximum number of octets in an information field (N401)*

N401 governs the maximum number of octets that can be carried in the information field of an I frame, an XID frame, a UI frame, or a TEST frame transmitted by an error-correcting entity. The default value of N401 shall be 128 octets for both directions of data transmission. If the default is not satisfactory to the negotiation initiator, then a different value may be negotiated separately for each direction by use of the XID frame. The

initiator of the negotiation shall indicate the N401 value it wishes to use for each direction (absence of a value indicates use of the default). The responder to the negotiation indicates the N401 value it wishes to use for each direction. The value chosen by the responder shall be between the value chosen by the initiator and the default value, inclusive, and shall be the value used during the operation of the error-corrected connection (unless overridden by a subsequent negotiation).

9.2.4 *Window size (k)*

k governs the maximum number of I frames that an error-correcting entity can have outstanding (i.e. unacknowledged). The default value of k shall be 15 for both directions of data transmission. If the default is not satisfactory to the negotiation initiator, then a different value may be negotiated separately for each direction by use of the XID frame. The initiator of the negotiation shall indicate the k value it wishes to use for each direction (absence of a value indicates use of the default). The responder to the negotiation indicates the k value it wishes to use for each direction. The value chosen by the responder shall be between the value chosen by the initiator and the default value, inclusive, and shall be the value used during the operation of the error-corrected connection (unless overridden by a subsequent negotiation).

9.2.5 *Reply delay timer (T402) – optional*

T402 is the maximum amount of time the error-correcting entity may wait, following receipt of any frame requiring a reply, before it initiates transmission of an appropriate reply in order to ensure that the reply frame is received by the remote error-correcting entity prior to expiration of the remote error-correcting entity's T401 timer. Information about this timer is *not* carried in XID frames. If this timer expires, then the reply that would have been returned prior to its expiration shall not be sent.

Note – The necessity for and operation of such a timer remains for further study.

9.2.6 *Inactivity timer (T403) – optional*

T403 represents the maximum amount of time an error-correcting entity will allow to elapse without frames being exchanged on the error-corrected connection. Information about this timer is *not* carried in XID frames. The two error-correcting entities associated with an error-corrected connection may operate with a different value of T403. While no default value is specified for T403, it should take on relatively small values so that faults can be detected early.

9.2.7 *DLCI values*

The DLCI value in the address field of a frame transmitted by the error control function serves to identify the connection between two peer error-correcting entities. Information about these values is not carried in XID frames. DLCI values are defined in Table 10/V.42.

TABLE 10/V.42

Allocation of DLCI values

DLCI value	Used for
0	DTE-to-DTE (V.24 interfaces) data
1-31	Reserved for future use by this Recommendation
32-62	Not reserved for use by this Recommendation
63	Reserved for control-function to control-function information (for further study)

Note – The DLCI assignments above are use with an address field consisting of a single octet (see § 8.2.1). Allocation of DLCI values that make use of optional octet 2A (see Figure 8/V.42) is for further study.

10 Negotiation of optional procedures

Within the scope of this Recommendation, there are three procedures that are optional for error control function operation. These are:

a) selective retransmission, using an SREJ frame to request retransmission of only a single frame;

b) loop-back test, where a control function can determine whether its peer is operational; and

c) extended FCS, where a 32-bit FCS (rather than a 16-bit FCS) is used.

Use of any optional procedure requires agreement by both control functions using the mechanisms in § 8.10. The negotiation-initiator can choose whether to request use of a particular procedure. The procedure is used only if the negotiation-initiator requests its use and the responder agrees to its use.

11 Control function-to-control function connection

An error-corrected connection, with a DLCI value of 63, has been reserved for use as a control function-to-control function connection. The protocol used between two control functions is for further study.

12 Encoding of information fields

12.1 *Information fields in I frames*

The encoding of the information field of I frames is determined by the use of the error-corrected connection (e.g. when used to carry data received from the V.24 interface).

12.2 *Information fields in XID frames*

12.2.1 *General*

The general structure of the information field of an XID frame is based on the encoding in ISO Standard 8885 and is shown in Figure 10/V.42 below. The information field is composed of a number of subfields. These subfields are a format identifier subfield, zero or more data link layer subfields, and, possibly, a user data subfield.

When an octet encoding is shown for any of the subfields, it is shown with the right-most bit being the low-order bit and the bit transmitted first.

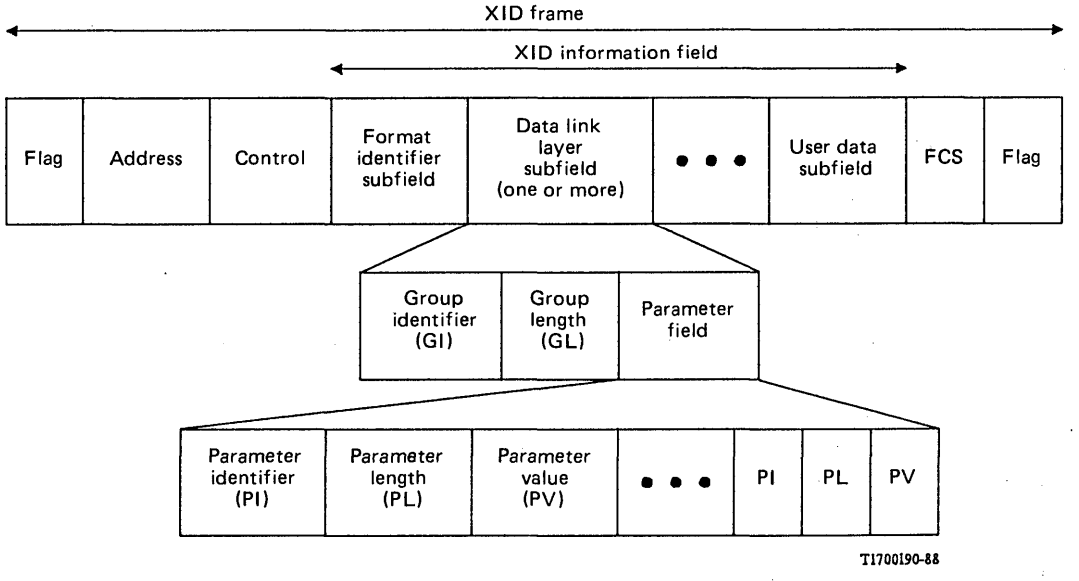


FIGURE 10/V.42

General format of XID information field

12.2.1.1 *Format identifier subfield*

Format identifier (FI) subfield is one octet in length and is the first octet of the information field of the XID frame. In general, the FI is encoded such that it can designate 128 different formats standardized by ISO and 128 different formats defined by users. Each ISO-standardized format is associated with a different FI value. The only such format defined at this time is the "general purpose" format.

12.2.1.2 *Data link layer subfields*

Data link layer subfields are used to specify various data link layer characteristics, such as operational parameters. In terms of Figure 10/V.42, a data link layer subfield consists of a group identifier (GI) one octet in length, a group length (GL) two octets in length, and a parameter field (whose length is given by GL). The parameter field, in turn, is similarly decomposed into one or more sets of a parameter identifier (PI), a parameter length (PL), and a parameter value (PV) (the parameter length, however, is only one octet in length).

12.2.1.3 *User data subfield*

A GI has been defined to specify a user data subfield used in conjunction with the "general purpose" FI. This subfield follows all data link layer subfields, as Figure 10/V.42 shows. The subsequent information is bounded by the frame's FCS field.

For the purposes of this Recommendation, this subfield is also divided into sets of PIs, PLs, and PVs.

12.2.2 *Encoding for negotiation/indication of parameter values and optional procedures*

The information field shall be encoded as specified below. Fields that are not recognized are ignored.

Format identifier subfield

For negotiation/indication of parameter values and optional procedures, the FI subfield shall be encoded as "10000010" to indicate the ISO-standardized "general purpose" FI.

Data link layer subfields

Only the data link layer subfield associated with "parameter negotiation" shall be present. This subfield has a GI value of "10000000". The length of this subfield (GL) is dependent on the actual information to be transmitted.

Each item to be negotiated and/or indicated is identified by a PI. Table 11/V.42 shows the items and their PI values.

User data subfield

The user data subfield may be present independently of whether negotiation and/or indication is performed. This subfield has a GI value of "11111111".

The only parameter within this subfield defined in this Recommendation at this time is a "manufacturer ID". This parameter shall be identified by a PI value of "11111111". The encoding of the associated PV subfield is manufacturer-specific. The high-order bit of the first octet of the PV field is used as follows:

- bit = 0: Manufacturer IDs not assigned by CCITT;
- bit = 1: CCITT-assigned manufacturer IDs (the assignment of these identifiers is for further study)

When receiving a manufacturer ID that is not recognized, the manufacturer ID field is ignored.

12.3 *Information fields in UI frames*

In the encodings below, bit 1 is the low-order bit and is transmitted first.

The first octet of the information field of a UI frame shall be encoded to indicate the usage of the field, as given in Table 12/V.42.

TABLE 11/V.42

Parameter/Procedures

PI		Parameter/procedure	Units
Decimal	Binary		
3	00000011	HDLC optional functions	(Note 1)
5	00000101	Maximum length of information field (N401): transmit direction	bits (Note 2)
6	00000110	Maximum length of information fiel (N401): receive direction	bits (Note 2)
7	00000111	Window size (k): transmit direction	Frames
8	00001000	Window size (k): receive direction	Frames

Note 1 – The length of this item is 3 octets (i.e., PL = 3). The bits in these octets constitute a 24-bit mask, each for a particular HDLC optional function. Bit 1 of this mask is the low-order bit octet 1 and is transmitted first; bit 9 is the low-order bit of octet 2; etc. The bits corresponding to the optional procedures used within this Recommendation are as follows:

– 3 Selective retransmission procedure (SREJ frame)
– 14 Loop-back test procedure (TEST frame)
– 17 Extended FCS procedure (32-bit FCS).

A bit position set to 1 indicates request/agreement to use the procedure. A bit position set to 0 indicates no request/no agreement to use the procedure.

For conformance with the encoding rules in ISO Standard 8885, the transmitter of an XID command frame shall set bit positions 2, 4, 8, 9, 12 et 16 to 1. The transmitter of an XID response frame shall also set these bit positions to 1, except bit position 16 shall be set to 0 if bit position 17 is set to 1. A receiver of these frames should ignore these bit positions.

Note 2 – N401 is expressed in octets. However, for negotiation purposes, units of "bits" shall be used.

Note 3 – The value of PL shall be the smallest number of octets needed to express the value of the parameter.

Note 4 – Parameter values for PI equal to 5, 6, 7, and 8 shall be encoded in binary. Within an octet, the first bit transmitted shall be the lowest-order bit. Where multiple octets are needed to express a parameter value, the first octet transmitted shall contain the higher-order bits.

TABLE 12/V.42

Encoding of octet 1 of the information field in a UI frame

Message type	Bits 8	7	6	5	4	3	2	1
BRK	x	1	0	0	0	0	0	0
BRKACK	x	1	1	0	0	0	0	0

Note 1 – Encodings not shown in the table are reserved.

Note 2 – The value of x is set as discussed below.

12.3.1 *Encoding of BRK message*

The encoding of a BRK message is shown in Figure 11/V.42. Bit 8 of octet 1 is used as a sequence number, modulo 2 (see § 8.13.2.1).

Break-handling option

The break-handling option is encoded as "DS", where:

- the "D" bit (bit 8 of octet 2) shall indicate whether data previously accumulated but not yet delivered should be discarded:

  D = 0 indicates no discarding of data

  D = 1 indicates discarding of data

- the "S" bit (bit 7 of octet 2) shall indicate whether the break should be delivered in sequence:

  S = 0 indicates that the break shall be delivered in sequence with respect to data generated before the break.

  S = 1 indicates that the break shall precede all data previously received but not yet delivered

Break length

The break length, which is optional, is binary-encoded in octet 3 in units of 10 ms where bit 1 is the low-order bit. The value of "11111111" shall be used to indicate a break longer than 2.54 seconds. Absence of a break length in a received BRK message shall be interpreted as a break of default length.

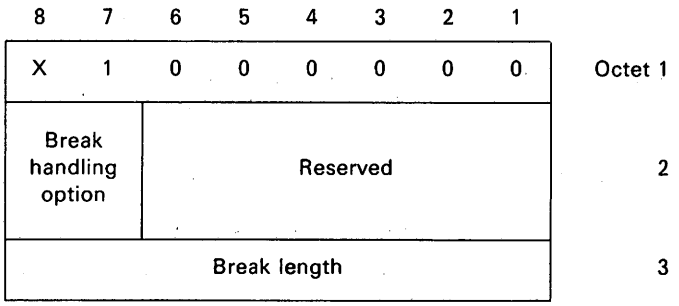


FIGURE 11/V.42

Format of UI information field for break

12.3.2 *Encoding of BRKACK message*

A BRKACK message contains only one octet. Bit 8 of octet 1 is used as a sequence number, modulo 2 (see § 8.13.2.1).

12.4 *Information fields in TEST frame*

The information fields in a TEST frame is used by the control function as part of a loop-back test. While specification of a particular encoding of this field is outside the scope of this Recommendation, the control function should ensure that the field is unique so that it can determine when a test has completed successfully.

References

[1] CCITT Recommendation Q.920, *ISDN user-network interface data link layer – general aspects*

[2] CCITT Recommendation Q.921, *ISDN user-network interface – data link layer specification*

[3] CCITT Recommendation V.14, *Transmission of start-stop characters over synchronous bearer channels*

[4] CCITT Recommendation V.24, *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment*

[5] CCITT Recommendation X.3, *Packet assembly/disassembly facility (PAD) in a public data network*

[6] ISO 3309, *Data communication – High-level data link control procedures – Frame structure*

[7] ISO 4335, *Data communication – High-level data link control elements of procedures*

[8] ISO 7809, *Data communication – High-level data link control procedures – Consolidation of classes of procedures*

[9] ISO 8885, *Data communication – High-level data link control procedures – General purpose XID frame information field content and format*

ANNEX A

(to Recommendation V.42)

Operation of the error control function – Alternative procedure

A.1 *General*

This Annex specifies the frame structure and procedures for the proper operation of the alternative error-correcting procedure for DCEs.

A.2 *Format conventions*

See § 8.1.2.

A.3 *Start-stop, octet-oriented framing mode*

In this mode, the error-correcting entities operate on an octet data stream. The framing format for start-stop, octet-oriented framing mode is shown in Figure A-1/V.42. This framing mode requires the use of four special octet values (SYN, DLE, STX, and ETX) for transparency. The transparency method is described in § A.3.4 below.

Each octet is transmitted with a start and stop bit.

A.3.1 *Start-flag field*

All frames shall begin with the three-octet, start-flag sequence SYN-DLE-STX. The values for the flag sequence are shown in Figure A-1/V.42.

A.3.2 *Header field*

The contents of the header field are described in §§ A.6.2 and A.6.3.

A.3.3 *Information field*

The information field of a frame, when present, contains transparent user data.

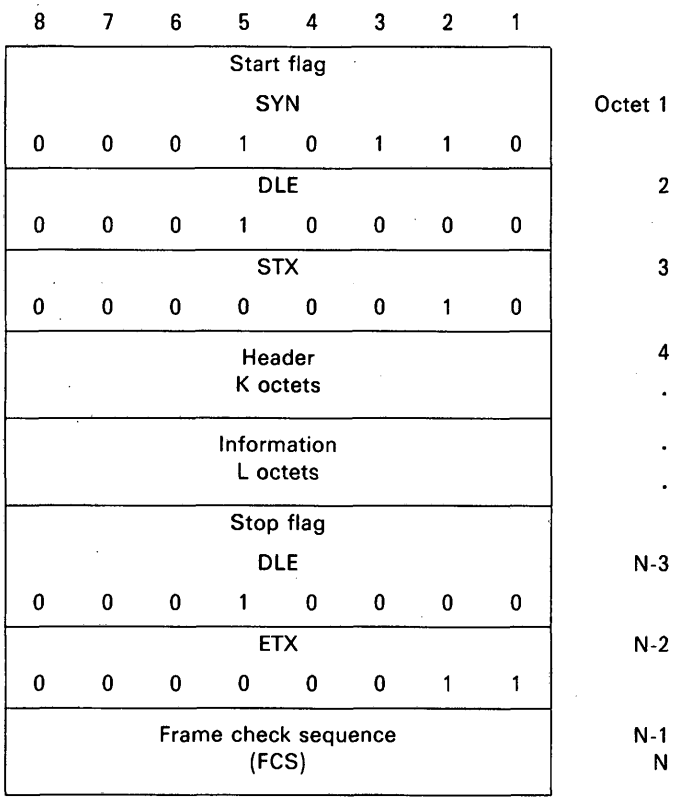


FIGURE A-1/V.42

Frame format for start-stop, octet-oriented mode

A.3.4 *Transparency*

The transmitting error-correcting entity shall examine the frame body (consisting of the header and information fields) and insert a DLE octet immediately following any occurrence of a DLE octet in the frame body octet stream. The receiving error-correcting entity shall examine the frame body and discard the second DLE of a two-octet DLE-DLE sequence. The first DLE is considered part of the frame body field. The DLE used in the start and end flag to delimit the STX and ETX control octets shall not be doubled, so that they shall be recognized as framing fields.

A.3.5 *End-flag field*

All frames shall end with the two-octet, end-flag sequence DLE-ETX (followed by the FCS field). The values for the flag sequence are shown in Figure A-1/V.42.

A.3.6 *Frame check sequence (FCS) field*

The FCS is a 16-bit sequence generated by the cyclic redundancy chech (CRC) polynomial $x^{16} + x^{15} + x^2 + 1$. The frame body and ETX octet of the stop flag are included in the FCS calculation. The start flag and all DLE octets used to maintain data transparency (§ A.3.4) are excluded from the FCS calculation.

Note – The CRC polynomial used in this frame mode differs from that specified in § 8.1.1.6.1.

A.4 *Bit-oriented framing mode*

In this mode, the error-correcting entities operate on a bit data stream. The framing format for bit-oriented mode is shown in Figure A-2/V.42.

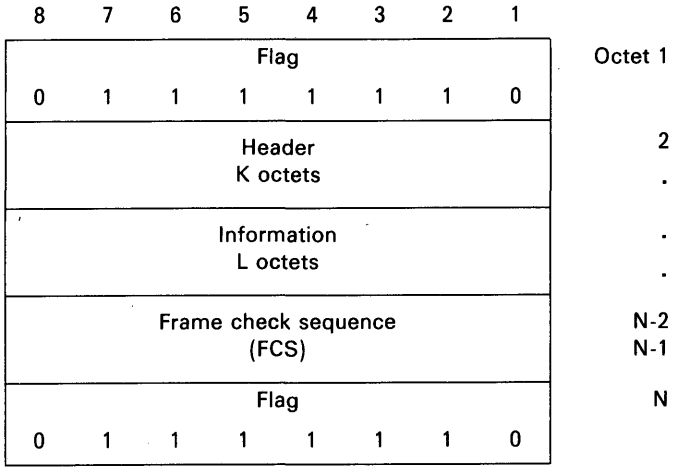


FIGURE A-2/V.42

Frame format for bit-oriented mode

A.4.1 *Flag sequence and transparency*

See § 8.1.1.2.

A.4.2 *Header field*

The contents of the header field are defined in §§ A.6.2 and A.6.3.

A.4.3 *Information field*

The information field of a frame, when present, contains transparent user data. The contents of the information field shall consist of an integer number of octets.

A.4.4 *Frame check sequence (FCS) field*

See § 8.1.1.6.1.

A.5 *Invalid frames*

For octet-oriented framing mode, see § 8.1.3, item d). For bit-oriented framing mode, see § 8.1.3, items a) to d).

A.6 *Alternative elements of procedure and field formats*

A.6.1 *General*

The elements of procedure define the message formats that are used on an alternative error-corrected connection.

A.6.2 *Header field – format*

The header field consists of fixed-length and variable-length parameters. Fixed-length parameters, or fixed parameters, have a predetermined length defined by the value of the type indication. Variable-length parameters, or variable parameters, have a length of three or more octets.

All valid header fields shall have a length indication (fixed parameter 0) and a type indication (fixed parameter 1) to identify the encoding for the remaining portion of the header field. The format is illustrated in Figure A-3/V.42.

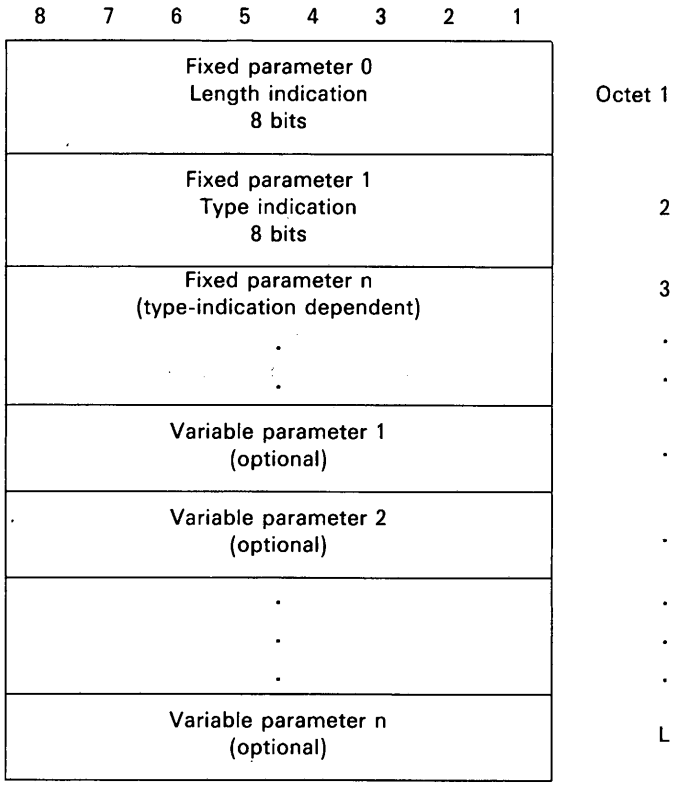


FIGURE A-3/V.42

Header field format

A.6.2.1 *Fixed parameter 0 – length indication*

The length indication shall be the first octet of the header field. The value of the length indication determines the total length of the header field, in octets. This length value does not include the length indication itself.

The value of 255 shall be used to indicate that the next two octets constitute a 16-bit extended length indication. The length indication requires three octets to represent lengths over 254 octets.

A.6.2.2 *Fixed parameter 1 – type indication*

The type indication shall be the second octet of the header field. The type indication identifies the header-field type and encoding for the remainder of the header field. The header-field types are shown in Table A-1/V.42.

TABLE A-1/V.42

Header field types

Type indication		Value
Link request	LR	1
Link disconnect	LD	2
Link transfer	LT	4
Link acknowledgement	LA	5
Link attention	LN	6
Link attention acknowledgement	LNA	7

A.6.2.3 *Fixed parameter 2 through n*

The presence of fixed parameters 2 through n is dependent on the header-field type.

A.6.2.4 *Variable parameters*

All variable parameters shall have three parts:

a) parameter-type indication,

b) parameter-length indication,

c) parameter values.

The structure of a variable parameter is shown in Figure A-4/V.42.

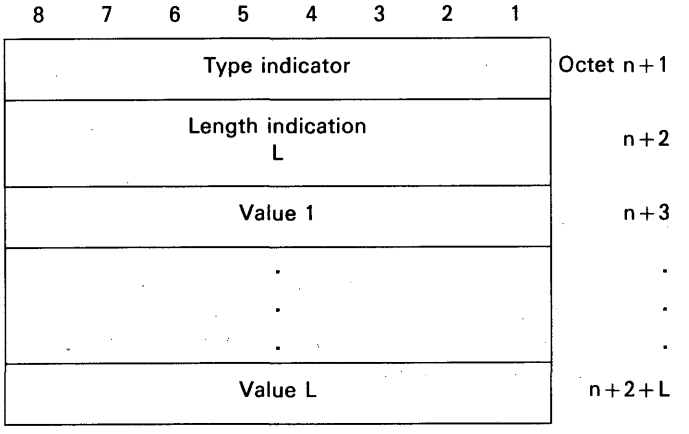


FIGURE A-4/V.42

Variable parameter format

A.6.2.4.1 *Variable parameter type indication*

The variable parameter-type indication shall consist of one octet, containing a value in the range from 1 to 254. For each header-field type, there is a separate and independent numbering sequence for variable parameter types.

A.6.2.4.2 *Variable parameter length indication*

The variable parameter-length indication shall be a single octet which specifies the number of octets contained in the variable parameter value.

A.6.4.2.3 *Variable parameter value*

The variable parameter field shall consist of one or more octets; the number of octets is specified by the parameter length indication.

A.6.3 *Header field – parameters*

A.6.3.1 *Modulus*

Each LT frame and LN frame is sequentially numbered and may have the value 0 through modulus minus 1 (where modulus is the modulus of the sequence numbers). The modulus is 256 and the sequence numbers cycle through the entire range.

A.6.3.2 *Send state variable V(S)*

The send state variable V(S) denotes the sequence number of the next in-sequence LT frame to be transmitted. V(S) can take on the values 0 through modulus minus 1. The value of V(S) is incremented by 1 with each successive LT frame transmission, but cannot exceed N(R) of the last received LA frame by more than the maximum number of outstanding LT frames (k). The value of k is defined in §§ A.6.4.1.6 and A.7.5.7.

Upon data phase initialization, V(S) is set to 1.

A.6.3.3 *Send sequence number N(S)*

Only LT frames contain N(S), the send sequence number of transmitted LT frames. At the time that an in-sequence LT frame is designated for transmission, the value of N(S) is set equal to the value of the send state variable V(S).

A.6.3.4 *Receive state variable V(R)*

The receive state variable V(R) denotes the sequence number of the next in-sequence LT frame expected to be received. V(R) can take on the values 0 through modulus minus 1. The value of V(R) is incremented by 1 by the receipt of an error-free, in-sequence LT frame whose send sequence number N(S) equals the receive state variable V(R).

Upon data phase initialization, V(R) is set to 1.

A.6.3.5 *Receive sequence number N(R)*

All LA frames contain N(R), the send sequence number of the last received LT frame. At the time that an LA frame is designated for transmission, the value of N(R) is set equal to the current value of the receive state variable V(R) – 1. N(R) indicates that the error-correcting entity transmitting the N(R) has received correctly all LT frames numbered up to and including N(R).

A.6.3.6 *Attention send state variable V(SA)*

The attention send state variable V(SA) denotes the sequence number of the next in-sequence LN frame to be transmitted. V(SA) can take on the values 0 through modulus minus 1. The value of V(SA) is incremented by 1 with each successive transmission of an LN frame.

Upon data phase initialization, V(SA) is set to 1.

A.6.3.7 *Attention send sequence number N(SA)*

Only LN frames contain N(SA), the attention send sequence number of transmitted LN frames. At the time that an in-sequence LN frame is designated for transmission, the value of N(SA) is set equal to the value of the attention send state variable V(SA).

A.6.3.8 *Attention receive state variable V(RA)*

The attention receive state variable V(RA) denotes the sequence number of the next in-sequence LN frame expected to be received. V(RA) can take on the values 0 through modulus minus 1. The value of V(RA) is incremented by 1 by the receipt of an error-free, in-sequence LN frame whose attention send sequence number N(SA) equals the attention receive state variable V(RA).

Upon data phase initialization, V(RA) is set to 1.

A.6.3.9 *Attention receive sequence number N(RA)*

The LNA frame contains N(RA), the attention send sequence number of the last received LN frame. At the time that an LNA frame is designated for transmission, the value of N(RA) is set equal to the current value of the receive state variable V(RA) − 1. N(RA) indicates that the error-correcting entity transmitting the N(RA) has received correctly all LN frames numbered up to and including N(RA).

A.6.3.10 *Receive credit state variable R(k)*

The receive credit state variable R(k) denotes the number of LT frames the receiver is able to receive. The number of received LT frames not acknowledged plus R(k) can not be greater than k (the maximum number of outstanding LT frames). System parameter k is defined in § A.7.5.7.

When the error-correcting entity enters the data phase, R(k) is set equal to k. During the data phase, R(k) is updated by the error-correcting entity as often as is required to accurately represent the receiver's ability to accept LT frames.

A.6.3.11 *Receive credit number N(k)*

Only LA frames contains N(k). At the time that an LA frame is designated for transmission, the value of N(k) is set equal to the value of the receive credit state variable R(k). N(k) indicates that the error-correcting entity transmitting the N(k) can properly receive LT frames numbered up to and including N(R) + N(k).

A.6.3.12 *Send credit state variable S(k)*

The send credit state variable S(k) denotes the number of LT frames the sender is able to transmit without receiving additional credit from the receiver. The number of LT frames not acknowledged plus S(k) can not be greater than k (the maximum number of outstanding LT frames). System parameter k is defined in § A.7.5.7.

Upon data phase initialization, S(k) is set to k.

A.6.4 *Protocol establishment phase*

The alternative error-correcting procedure begins operation in the protocol establishment phase. In this phase, the error-correcting entity attempts to initialize an error-corrected connection for exchanging data.

The protocol messages in the connection establishment message exchange shall be transmitted in start-stop, octet-oriented mode. The framing mode for the subsequent phases of error-corrected connection operation is determined during the protocol establishment phase.

A.6.4.1 *Link request (LR) frame*

The link request (LR) frame is used to establish an error-corrected connection between two error-correcting entities with an active physical connection. The LR frame is also used to negotiate operational parameters to be in effect for the duration of the error-corrected connection (see § A.7.1.5).

The header-field parameters of the LR frame are shown in Table A-2/V.42. No information field is permitted with the LR frame.

TABLE A-2/V.42

Link request header field parameters

Parameter name	F V	M O	Value name	Value
Length indication	F	M	–	Variable
Type indication	F	M	LR	1
Constant parameter 1	F	M	–	2
Constant parameter 2	V	M	Type Length – – – – – –	1 6 1 0 0 0 0 255
Framing mode	V	M	Type Length Mode (see § A.6.4.1.5)	2 1 2 ou 3
Maximum number of outstanding LT frames, k	V	M	Type Length k	3 1 Variable
Maximum information field length, N401	V	M	Type Length Max length (two octets)	4 2 Variable
Data phase optimization	V	M	Type Length Facilities (see § A.6.4.1.8)	8 1 Variable

F Fixed parameter

M Mandatory parameter

V Variable parameter

O Optional parameter

A.6.4.1.1 *Fixed parameter 0 – length indication*

The value of the length indication shall be a computed value equal to the length of the header field, excluding the length indicator.

A.6.4.1.2 *Fixed parameter 1 – type indication*

The value of the type indication shall be an octet value of 1.

A.6.4.1.3 *Fixed parameter 2 – constant parameter 1*

This constant parameter shall be the third octet of the header field. The value of this constant is an octet value of 2.

A.6.4.1.4 *Variable parameter 1 – constant parameter 2*

This constant parameter shall be an octet sequence of value (1,6,1,0,0,0,0,255).

A.6.4.1.5 *Variable parameter 2 – framing mode parameter*

The framing mode parameter defines the framing mode to be used on the error-corrected connection.

Two-way simultaneous, start-stop, octet-oriented framing mode shall be represented by framing mode 2.

Two-way simultaneous, bit-oriented framing mode shall be represented by framing mode 3.

An error-correcting entity that supports framing mode 3 must also support framing mode 2.

The responding error-correcting entity sends a response LR with the framing mode parameter set to the lesser of the framing-mode values for the framing mode that is supported by the responding entity or the framing mode parameter value received in the initiating LR frame. The framing mode represented by the framing mode parameter value in the response LR determines the framing mode used on the error-corrected connection after the protocol establishment phase is completed.

A.6.4.1.6 *Variable parameter 3 – Maximum number of outstanding LT frames parameter, k*

The maximum number of outstanding LT frames parameter, k, defines the maximum number of LT frames with a maximum-length information fields that an error-correcting entity may send at a given time without waiting for an acknowledgement. The value of k shall never exceed the sequence number modulus minus 1.

Any value of k less than or equal to the maximum value may be used.

A.6.4.1.7 *Variable parameter 4 – maximum information field length parameter N401*

The maximum information-field length parameter, N401, defines the maximum length of user data, in octets, that can be sent in the information field of the link transfer (LT) frame.

A.6.4.1.8 *Variable parameter 8 – data phase optimization*

The data phase optimization parameter defines optional facilities may be supported on an error-corrected connection to improve data throughput.

The value of this parameter is a bit map that indicates protocol facilities to be used, as follows:

bit 1 1 = maximum information-field length of 256 octets

bit 2 1 = fixed field LT and LA frames

bit 3-8 reserved

Reserved bits are set to 0 on transmission and ignored upon receipt.

The responding error-correcting entity sends a response LR with a data phase optimization parameter if it agrees to use any data phase optimization facility. The facilities represented by the bit values in the response LR determine the facilities to be used on the error-corrected connection during the data phase.

A.6.4.2 *Link acknowledgement (LA) frame*

The link acknowledgement (LA) frame is used to confirm the completion of the protocol establishment phase of the alternative error-correcting procedure. The confirming LA is sent by the error-correcting entity that sent the initiating LR frame.

Upon sending or receiving the confirming LA of the connection-establishment, three-message exchange, the error-correcting correcting entity enters the data phase.

The header-field parameters of the link acknowledgement frame are shown in Table A-3a/V.42 and A-3b/V.42. No information field is permitted in the LA frame.

TABLE A-3a/V.42

Link acknowledgement header field parameters (non-optimized data phase)

Parameter name	F V	M O	Value name	Value
Length indication	F	M	–	7
Type indication	F	M	LA	5
Receive sequence number, N(R)	V	M	Type Length N(R)	1 1 8 bits
Receive credit number, N(k)	V	M	Type Length Credit	2 1 8 bits

F Fixed parameter

M Mandatory parameter

V Variable parameter

O Optional parameter

TABLE A-3b/V.42

Link acknowledgement header field parameters (optimized data phase)

Parameter name	F V	M O	Value name	Value
Length indication	F	M	–	3
Type indication	F	M	LA	5
Receive sequence number, N(R)	F	M	N(R)	8 bits
Receive credit number, N(k)	F	M	N(k)	8 bits

F Fixed parameter

M Mandatory parameter

V Variable parameter

O Optional parameter

A.6.4.2.1 *Fixed parameter 0 – length indication*

The value of the length indication shall be an octet value of 7 in a non-optimized data phase (see Table A-3a/V.42) and 3 in an optimized data phase (see Table A-3b/V.42).

A.6.4.2.2 *Fixed parameter 1 – type indication*

The value of the type indication shall be an octet value of 5.

A.6.4.2.3 *Variable parameter 1 – receive sequence number (non-optimized data phase)*

The receive sequence number parameter contains the value of the receive number, N(R), of the last correctly received LT frame. The value used for the receive sequence number in the protocol establishment phase confirming the LA shall be 0.

A.6.4.2.4 *Variable parameter 2 – receive credit number (non-optimized data phase)*

The receive credit number parameter contains the value of the maximum number of LT frames that can be sent by an error-correcting entity before it must suspend sending LT frames and wait for an acknowledgement.

The value used for the receive credit for the confirming LA is the value received as the receive credits in the response LR.

A.6.4.2.5 *Fixed format for variable parameters 1 and 2 (optimized data phase)*

When the fixed format LA frame facility is in effect during an optimized data phase, the receive sequence number and the receive credit number are included in the fixed part of the frame header field.

The received sequence number value octet is fixed parameter 2.

The received credit number value octet is fixed parameter 3.

The header-field parameter of the LA frame in an optimized data phase is shown in Table A-3b/V.42.

A.6.5 *Disconnect phase*

The alternative error-correcting procedure terminates operation in the disconnect phase. The disconnect phase may be entered from any other phase of error-corrected connection operation. The disconnect phase shall use the same framing mode as used in the phase prior to the disconnect phase.

A.6.5.1 *Link disconnect (LD) frame*

The link disconnect (LD) frame is used to terminate operation of an active error-corrected connection, or to reject an attempt to establish an error-corrected connection.

The header-field parameters of the LD frame are shown in Table A-4/V.42. No information field is permitted in the LD frame.

A.6.5.1.1 *Fixed parameter 0 – length indication*

The value of the length indication shall be an octet value of 4 for LD frames without variable parameter 2 and 7 for LD frames with variable parameter 2.

A.6.5.1.2 *Fixed parameter 1 – type indication*

The value of the type indication shall be an octet value of 2.

A.6.5.1.3 *Variable parameter 1 – reason code*

The reason-code parameter defines the reason for disconnection when sent in an LD frame on an active error-corrected connection, or the reason for failure to establish when sent in an LD frame in response to a connection attempt.

The reason codes are listed in Table A-5/V.42. Reason codes 1, 2 and 3 are used if the disconnect phase is the result of failure in the protocol establishment phase.

TABLE A-4/V.42

Link disconnect header field parameters

Parameter name	F V	M O	Value name	Value
Length indication	F	M	–	4 or 7 (see § A.6.5.1.1)
Type indication	F	M	LD	2
Reason code	V	M	Type Length Value	1 1 Variable (see § A.6.5.1.3)
User code	V	O	Type Length Value	2 1 Variable

F Fixed parameter

M Mandatory parameter

V Variable parameter

O Optional parameter

TABLE A-5/V.42

Link disconnect reason code

Code	Reason
1	Protocol establishment phase error, LR expected but not received
2	LR constant parameter 1 contains an unexpected value
3	LR received with incompatible or unknown parameter value
4-254	Reserved
255	User-initiated disconnect

Note – Code 3 is only used during the protocol establishment phase by the establishment initiator.

A.6.5.1.4 *Variable parameter 2 – user code*

The user code parameter is an optional parameter. If this parameter is present, this parameter defines the error-correcting user's reason for releasing the connection.

A.6.6 *Data transfer phase*

The alternative error-correcting procedure transfers user data in the data transfer phase.

A.6.6.1 *Link transfer (LT) frame*

The function of the LT transfer (LT) frame is to transfer user data across the error-corrected connection in sequentially numbered information fields. The header-field parameters of the link transfer frame are shown in Table A-6a/V.42 and Table A-6b/V.42. The information field shall contain one or more octets of user data up to the maximum information-field length negotiated during the protocol establishment phase. A null (zero octets) information field is not allowed.

A.6.6.1.1 *Fixed parameter 0 – length indication*

The value of the length indication shall be an octet value of 4 in a non-optimized data phase (see Table A-6a/V.42) and 2 in an optimized data phase (see Table A-6b/V.42).

A.6.6.1.2 *Fixed parameter 1 – type indication*

The value of the type indication shall be an octet value of 4.

A.6.6.1.3 *Variable parameter 1 – send sequence number parameter (non-optimized data phase)*

The send sequence number parameter defines the order of this frame and its information field in the data-sequence phase. At the time that an LT frame is designated for transmission, the value of this parameter is set equal to the send state variable V(S). The send state variable is initially 1, and is incremented modulo 256 with each successive LT frame transmission.

A.6.6.1.4 *Fixed format for variable parameter 1 (optimized data phase)*

When the fixed format LT frame facility is in effect during an optimized data phase, the send sequence number is included in the fixed part of the frame header field.

The send sequence number value octet is fixed parameter 2.

This format is shown in Table A-6b/V.42.

A.6.6.2 *Link acknowledgement (LA) frame*

The link acknowledgement (LA) frame is used to confirm the receipt of LT frames up to and including N(R). A single LA frame may acknowledge multiple LT frames.

A.6.6.2.1 *Header field parameters*

The header-field parameters of the LA frame are shown in Table A-3a/V.42 and Table A-3b/V.42; the parameters are described in §§ A.6.4.2.1 through A.6.4.2.5. No information field is permitted in the LA frame.

A.6.6.2.2 *LT frame credit*

The LT frame credit parameter contains the value that represents the number of LT frames with maximum-length information fields that the receiver is able to accept at the moment of LA frame transmission. A credit value of zero serves to halt the transmission of LT frames by the sender. Transmission of LT frames from the sender shall resume when an LA frame with a non-zero credit value is sent.

A.6.7 *Transfer of break*

The attention frame provides a reliable mechanism for signalling between error-correcting entities a break condition on the DTE/DCE interface.

TABLE A-6a/V.42

Link transfer header field parameters
(non-optimized data phase)

Parameter name	F V	M O	Value name	Value
Length indication	F	M	–	4
Type indication	F	M	LT	4
Send sequence number, N(S)	V	M	Type Length N(S)	1 1 8 bits

F Fixed parameter

M Mandatory parameter

V Variable parameter

O Optional parameter

TABLE A-6b/V.42

Link transfer header field parameters
(optimized data phase)

Parameter name	F V	M O	Value name	Value
Length indication	F	M	–	2
Type indication	F	M	LT	4
Send sequence number, N(S)	F	M	N(S)	8 bits

F Fixed parameter

M Mandatory parameter

V Variable parameter

O Optional parameter

A.6.7.1 *Link attention (LN) frame*

The header-field parameters of the link attention (LN) frame are shown in Table A-7/V.42. No information field is permitted in the LN frame.

TABLE A-7/V.42

Link attention header field parameters

Parameter name	F V	M O	Value name	Value
Length indication	F	M	–	7
Type indication	F	M	LN	6
Attention send sequence number, N(SA)	V	M	Type Length N(SA)	1 1 8 bits
Attention type	V	M	Type Length Break	2 1 1 = D&E 2 = non-D&E 3 = non-D&non-E

F Fixed parameter

M Mandatory parameter

D Destructive break

V Variable parameter

O Optional parameter

E Expedited break

A.6.7.1.1 *Fixed parameter 0 – length indication*

The value of the length indication shall be an octet value of 7.

A.6.7.1.2 *Fixed parameter 1 – type indication*

The value of the type indication shall be an octet value of 6.

A.6.7.1.3 *Variable parameter 1 – attention send sequence number*

The attention send sequence number, N(SA), parameter defines the order of this frame in the attention sequence space. At the time that an LN frame is designated for transmission, the value of this parameter is set equal to the attention send state variable V(SA). The attention send state variable is initially 1, and is incremented modulo 256 with each successive LN frame transmission.

A.6.7.1.4 *Variable parameter 2 – attention type*

The attention type parameter defines error-correcting entity handling of the break condition relative to the user data.

If destructive break handling is specified, the error-correcting entity shall flush all data transmitted or received before the break signal that is in transit to the correspondent entity or not delivered to the user.

If expedited break handling is specified, the error-correcting entity shall process the break signal immediately and ahead of any user data pending transmission.

See §§ 7.4 and 7.5.

A.6.7.2 *Link attention acknowledgement (LNA) frame*

The link attention acknowledgement (LNA) frame is used to acknowledge successful receipt of an LN frame. The header-field parameters of the LNA frame are shown in Table A-8/V.42. No information field is permitted in the LNA frame.

TABLE A-8/V.42

Link attention acknowledgement header field parameters

Parameter name	F V	M O	Value name	Value
Length indication	F	M	–	4
Type indication	F	M	LNA	7
Attention receive sequence number, N(RA)	V	M	Type Length N(RA)	1 1 8 bits

F Fixed parameter

M Mandatory parameter

V Variable parameter

O Optional parameter

A.6.7.2.1 *Fixed parameter 0 – length indication*

The value of the length indication shall be an octet of value 4.

A.6.7.2.2 *Fixed parameter 1 – type indication*

The value of the type indication shall be an octet of value 7.

A.6.7.2.3 *Variable parameter 1 – attention receive sequence number*

The attention receive sequence number parameter is used to acknowledge the receipt of LN frames up to and including N(RA).

A.7 *Description of the error-correcting procedure*

A.7.1 *Protocol establishment phase procedure*

A.7.1.1 *Initiating the establishment procedure*

The protocol establishment phase begins after a physical connection is established. The originating DCE's error-correcting entity (the initiator) begins the procedures of the protocol establishment phase. The answering DCE's error-correcting entity (the responder) shall be ready to respond to protocol messages immediately after the physical connection is established.

A.7.1.2 *Initiator procedure*

The initiator shall begin connection establishment by transmitting an LR frame to the responder entity and starting its timer T401 in order to determine when too much time has elapsed waiting for a reply. When a reply LR is received, the initiator performs parameter negotiation (see § A.7.1.5) to determine the parameter values which will characterize the error-corrected connection.

If negotiation is successful, the initiator transmits an LA frame and enters the data phase.

The initiator shall resend the initial LR if:

a) timer T401 expires while waiting for the LR response, or

b) a protocol message arrives with an incorrect frame check sequence.

After resending the initial LR, the initiator restarts its timer T401 and waits for a reply. If the timer T401 again expires or another protocol message arrives with an invalid frame check sequence, the initiator may reject the connection establishment. However, the initiator may also repeat this procedure.

A.7.1.3 *Responder procedure*

The responder shall begin a connection establishment attempt by starting timer T401. When an LR is received, the responder performs parameter negotiation (see § A.7.1.5) to determine the parameter values which will characterize the error-corrected connection.

If negotiation is successful, the responder transmits an LR to the initiator and starts its timer T401 in order to determine when too much time has elapsed waiting for an acknowledgement. When an acknowledgment LA is received, the responder enters the data phase.

The responder shall resend the response LR if:

a) timer T401 expires while waiting for the LA response,

b) a protocol message arrives with an incorrect frame check sequence, or

c) another LR arrives.

After resending the response LR, the responder restarts timer T401 and waits for a reply. If the timer T401 again expires or if another protocol message arrives with an invalid frame check sequence, the responder rejects the connection establishment.

A.7.1.4 *Establishment rejection*

If the responder a) receives an LR with parameters that the responder is not prepared to accept, or b) does not receive an expected reply, then the responder shall enter the disconnect phase.

If the initiator a) receives an LR with parameters that fail the parameter negotiation, or b) does not receive an expected reply, then the initiator shall enter the disconnect phase.

A.7.1.5 *Parameter negotiation*

The error-correcting entity examines the parameters and parameter values of the LR it receives and compares them to its internal parameters. The negotiation rules are used to resolve parameter differences. If the negotiation rules can not resolve the parameter differences, then negotiation fails.

A.7.1.5.1 *Constant parameter 1*

Fixed parameter 1 shall always be of value 2. If another value is used, negotiation fails.

A.7.1.5.2 *Constant parameter 2*

This parameter must always be present. The negotiation rule accepts any value for constant parameter 2 and always produces the constant parameter value (see § A.6.4.1.3) as a result.

A.7.1.5.3 *Framing mode*

The negotiation rule selects the lower of the two values.

A.7.1.5.4 *Maximum number of outstanding LT frames, k*

The value for the maximum number of outstandling LT frames, k, will be the lower of the two values. If the resultant value is an unsupported number, then negotiation fails.

A.7.1.5.5 *Maximum information field length, N401*

The maximum information-field length, N401, will be the smaller of the two values. If the resultant value is an unsupported size, then negotiation fails.

A.7.1.5.6 *Unknown parameters*

During negotiation, the responder shall ignore all known parameters. When the responder sends its response LR, it includes only those parameters which it both received and understood.

A.7.2 *Disconnect phase procedures*

The LD frame is used to terminate a connection between two error-correcting entities. When an LD frame is received by an error-correcting entity, the entity shall terminate all protocol procedures.

A.7.2.1 *User initiated disconnect*

At the end of user data transfer, the user may initiate disconnection of the error-corrected connection. The interface between the user and the error-correcting entity is beyond the scope of this Recommendation.

A user-initiated disconnect shall cause the error-correcting entity to send an LD to terminate the error-corrected connection. After sending the LD, the error-correcting entity shall terminate the physical connection.

A.7.2.2. *Establishment rejection*

During the protocol establishment phase, both negotiation initiator and responder entities may reject the attempt to establish an error-corrected connection.

If the disconnect phase is initiated by a failure of the negotiation rules, the error-correcting entity shall send an LD to terminate the error-corrected connection. After sending the LD, the error-correcting entity shall terminate the physical connection.

If the disconnect phase is initiated by the expiration of timer T401 and the receipt of protocol messages with an invalid frame check sequence, the error-correcting entity shall send an LD to terminate the error-corrected connection. After sending the LD, the error-correcting entity shall terminate the physical connection.

If the disconnect phase is initiated by the expiration of timer T401 and no protocol messages were received, the error-correcting entity shall terminate operation without sending an LD. The physical connection shall continue to operate and data from the DTE interface will be directly presented to the Signal Converter for transmission over the physical connection in start-stop data transmission without error correction.

A.7.2.3 *Protocol errors*

If the error-correcting entity receives unexpected protocol messages or no response from the remote error-correcting entity, the local entity will release the connection by sending an LD to terminate the error-corrected connection. After sending the LD, the error-correcting entity shall terminate the physical connection.

A.7.2.4 *Executive retransmissions*

If the error-correcting entity repeats transmission of a frame and exceeds N400, the maximum number of attempts to complete a transmission, the local entity will release the connection by sending an LD to terminate the error-corrected connection. After sending the LD, the error-correcting entity shall terminate the physical connection.

A.7.3 *Data phase procedures*

The data phase is entered once the physical connection is established and the protocol establishment phase is completed. Th procedures that apply to the transmission of user data frames and acknowledgments during the information phase are described below.

The LT and LA frames are used to transfer data across an error-corrected connection.

A.7.3.1 *Sending an LT frame*

When an error-correcting entity has user data to transmit, the entity will transmit an LT with an N(S) equal to its current send state variable V(S). Each LT shall contain no more than N401 user octets in the information field. At the end of transmission of the LT frame, the error-correcting entity will increment, modulo 256, its send state variable V(S) by 1 and decrement S(k) by 1.

If timer T401 is not running at the time of transmission of an LT frame, it will be started. When k = 1, the timer is started after the error-correcting entity completes LT frame transmission. When k > 1, the timer is started when the error-correcting entity begins LT frame transmission.

If S(k) = 0, the error-correcting entity will not transmit any LT frames until S(k) is updated to a non-zero value through the receipt of an LA frame.

A.7.3.2 *Receiving an LT frame*

When an error-correcting entity receives a valid LT frame whose send sequence number N(S) is equal to the local receive state variable V(R), the error-correcting entity will accept the information field of this frame and increment by one, modulo 256, its receive state variable V(R).

Reception of an LT frame will start timer T402 if timer T402 is not already running.

Reception of an LT frame may also cause transmission of an acknowledgment (LA) frame (see § A.7.3.3).

A.7.3.2.1 *Reception of invalid frames*

When an error-correcting entity receives an invalid frame (see § A.5), it shall discard this frame.

A.7.3.2.2 *Reception of out-of-sequence LT frames*

When an error-correcting entity receives a valid LT frame whose send sequence number N(S) is not equal to the current receive state variable V(R), the error-correcting entity shall discard the information field of the LT frame and transmit an LA frame as described in § A.7.3.3.

The first reception of an LT frame with N(S) = V(R) − 1, however, is ignored and does not cause transmission of an LA frame.

A.7.3.2.3 *Reception of LT frames without receive credit*

When an error-correcting entity receives a valid LT frame when the receive credit R(k) = 0, the error-correcting entity shall discard the information field of the LT frame and transmit an LA frame as described in § A.7.3.3.

A.7.3.3 *Sending of an LA frame*

An error-correcting entity sends an LA frame to acknowledge successful reception of one or more LT frames or to signal the correspondent entity of a condition which may require retransmission of one or more LT frames. The LA frame also communicates the receiver's ability to accept additional LT frames.

The transmission of an LA frame can occur under two sets of conditions grouped according to the value of k.

A.7.3.3.1 *k = 1*

When k = 1, an LA frame shall be sent if one of the following conditions occur. The conditions are listed in declining order of precedence.

a) An invalid frame is received (§ A.5).

b) An LT frame is received out-of-sequence (§ A.7.3.2.2).

c) An LT frame is received without receive credit (§ A.7.3.2.3).

d) An LT frame is properly received.

A.7.3.2.2 *k > 1*

When k > 1, an LA frame shall be sent if one of the following conditions occur. The conditions are listed in declining order of precedence.

a) An invalid frame is received (§ A.5).

b) An LT frame is received out-of-sequence (§ A.7.3.2.2).

c) An LT frame is received without receive credit (§ A.7.3.2.3).

d) Timer T404 expires.

e) One or more correctly received LT frames have not yet been acknowledged and there is no user data to transmit.

f) One or more correctly received LT frames have not yet been acknowledged, there is user data to transmit, and the number of correctly received but unacknowledged LT frames is equal to or greater than k/2.

g) One or more correctly received LT frames have not yet been acknowledged, there is user data to transmit, and the number of correctly received but unacknowledged LT frames is less than k/2, and timer T402 expires.

Timer T404 shall be started when an error-correcting entity enters the data phase. Timer T404 shall be restarted whenever an LA frame is sent.

A.7.3.4 *Receiving an LA frame*

When an LA frame is received, the receiving error-correcting entity will consider the N(R) contained in this frame as an acknowledgement for all LT frames it has transmitted with an N(S) up to and including the received N(R). Timer T401 will be stopped if no additional LT frames remain unacknowledged, i.e., the received LA frame acknowledges all outstanding LT frames. Timer T401 will be restarted if additional LT frames remain unacknowledged.

An error-correcting entity that receives an LA frame uses the N(k) contained in the frame, minus the number of still unacknowledged LT frames in transit, as the new S(k) value.

A.7.3.5 *Retransmission of LT frames*

An error-correcting entity will initiate retransmission of LT frames when it has sent LT frames that have been acknowledged and one of the following conditions occurs:

a) An LA frame is received with an N(R) value equal to the N(R) of the last received LA frame.

b) Timer T401 expires.

Retransmission starts with the first LT frame in sequence which has not yet been acknowledged.

If S(k) = 0, the error-correcting entity will not retransmit any LT frame until S(k) is updated to a non-zero value through the receipt of an LA frame.

Timer T401 shall be restarted at the time of retransmission of the first LT frame in sequence. When k = 1, the timer is started after the error-correcting entity completes LT frame transmission. When k > 1, the timer is started when the receiving entity begins LT frame transmission.

During retransmission, the receipt of an LA frame may acknowledge some of the LT frames pending retransmission; any unacknowledged LT frames are not retransmitted.

A.7.3.6 *Link failure detection*

A transmitting error-correcting entity maintains a count of the number of times a particular LT frame is retransmitted. If this count for any LT frame reaches N400, failure of the connection is assumed and the error-correcting entity enters the disconnect phase.

A.7.4 *Break-signalling procedures*

The error-correcting entity in the data phase shall use the break-signalling procedures when it receives a break signal from the user at the V.24 interface. The break signal shall cause the transmission of link attention (LN) frame. The procedures that apply to the transmission of the LN frame are described below.

The link attention (LN) frame and link attention acknowledgement (LNA) frames are used to transfer break signals across an error-corrected connection.

A.7.4.1 *Sending an LN frame*

When an error-correcting entity has a break signal to transmit, the entity will transmit an LN frame with an N(SA) equal to its current attention send state variable V(SA). Timer T401 shall be started after the LN is sent.

An LN frame can only be transmitted if there is no outstanding LN frame which has not yet been acknowledged.

If an expedited LN frame is specified, the LN frame shall be transmitted immediately if no transmission is in progress, or immediately following the transmission in progress, if any. Non-expedited LN frames are sent after the acknowledgement of any LT frames pending transmission or retransmission at the time of the LN request, but before any subsequent user data.

A.7.4.2 *Effect of a transmitted LN frame on data*

See Table 4/V.42.

A.7.4.3 *Receiving an LN frame*

An error-correcting entity shall begin the break-signalling procedures when the entity receives a valid LN frame whose attention send sequence number N(SA) is equal to the attention receive state variable V(RA). The error-correcting entity shall accept this frame and increment its attention receive state variable V(RA) by one, modulo 256. If a valid LN frame is received with N(SA) less than V(RA), the error-correcting entity shall ignore the break signal of the LN frame.

Reception of any valid LN frame shall cause transmission of an attention acknowledgement (LNA) frame by the error-correcting, as described in § A.7.4.5.

A.7.4.4 *Effect of a received LN frame on data*

See Table 5/V.42.

A.7.4.5 *Sending an LA frame*

An error-correcting entity uses an LNA frame to acknowledge successful reception of an LN frame. It is transmitted in response to receipt of a valid LN frame. The LNA frame shall contain an N(RA) value equal to the N(SA) value contained in the received LN frame.

A.7.4.6 *Receiving an LNA frame*

A received LNA frame that contains N(RA) shall be the acknowledgment for the LN frame transmitted with an N(SA) equal to the received N(RA). If the received N(RA) is equal to N(SA) for the outstanding LN frame, timer T401 will be stopped and the attention send state variable V(SA) be incremented by 1, modulo 256.

After proper receipt of the LNA frame to acknowledge the outstanding LN frame, the break-signalling procedure is completed and the error-correcting entity resumes the sending of user data.

A.7.4.7 *Retransmission of LN frames*

At the expiration of timer T401, the error-correcting entity will retransmit the unacknowledged LN frame. The unacknowledged LN frame will also be retransmitted if an LNA frame is received with an N(RA) value less than N(SA).

Timer T401 shall be restarted at the time of transmission of the LN frame.

A.7.4.8 *Link failure protection*

A transmitting error-correcting entity shall maintain a count of the number of times a particular LN frame is retransmitted. If this count for any LN frame reaches N400, failure of the connection is assumed and the error-correcting entity enters the disconnect phase.

A.7.5 *List of error-correction system parameters*

A.7.5.1 *Timer T401 – acknowledgment timer*

The period of timer T401, at the end of which retransmission of a frame may be initiated, shall take into account whether T401 is started at the beginning or the end of the transmission of a frame.

The period of timer T401 in the protocol establishment phase shall be in the range 0.5-9 seconds.

The period of timer T401 for transmission of LT and LN frames is dependent on the transmission speed of the physical connection and shall be determined by the following formula:

$$T401 \geqslant \frac{2\,((k/2) \times L_b(L_f + L_{lt} + N401) + L_b(L_f + L_{la}))}{bps} + T_{rt}$$

where

L_b is the number of bits (framing mode 2 = 10, framing mode 3 = 8)

L_r is the length of frame overhead (octet-oriented framing mode = 7, bit-oriented framing mode = 4)

L_{lt} is the length of LT header field (non-optimized data phase = 5, optimized data phase = 3)

L_{la} is the length of LA header field (non-optimized data phase = 8, optimized data phase = 4)

T_{rt} is the round trip propagation delay (including remote processing and queuing delay)

bps is the physical connected speed in bits per second.

Typical values are shown in Table A-9/V.42.

TABLE A-9/V.42

Timer T401 values for transmission of LT and LN frames

Physical connection speed (in bit/s)	Period (in seconds) for N401 = 64	Period (in seconds for N401 = 256
1200	6	16
2400	4	9

A.7.5.2 *Timer T402 – LA timer*

The period of timer T402, at the end of which an acknowledgement must be sent, shall indicate the maximum amount of time available to the error-correcting entity between transmission of the acknowledging frames in order to ensure receipt of acknowledgments by the correspondent entity, prior to timer T401 expiring at the correspondent entity (timer T402 = 0.5 timer T401).

A.7.5.3 *Timer T403 – inactivity timer*

The error-correcting entity may, optionally, support a timer T403 with a period of at least 59 seconds. The period of timer T 403 shall be used by an error-correcting entity to detect a half-open connection condition in which the correspondent entity is non-active and non-operational.

T403 is started upon entering the data phase and is restarted upon receipt of any valid frame.

If T403 is enabled and expires, the observing entity shall enter the disconnect phase and terminate the connection.

A.7.5.4 *Timer T404 – flow control timer*

The period of timer T404, at the end of which transmission of an acknowledgment frame is sent, shall be used during the data phase of an error-corrected connection. The period of timer T404 shall be dependent on the transmission rate of the physical connection and shall be determined by the Table A-10/V.42.

TABLE A-10/V.42

Timer T404 values

Physical connection speed (in bit/s)	Period (in seconds)
1200	7
2400 or faster	3

A.7.5.5 *Maximum number of retransmissions (N400)*

The value of N400 shall indicate the maximum number of attempts made by the error-correcting entity to complete the successful transmission of a frame to the correspondent entity.

The value of N400 shall be 12.

A.7.5.6 *Maximum number of octets in an information field (N401)*

The value of N401 shall indicate the maximum number of octets in the information field, excluding DLE octets (in start-stop, octet-oriented framing mode) or 0 bits (in bit-oriented framing mode) inserted for transparency, that an error-correcting entity is willing to accept from the correspondent entity.

The value of N401 shall be determined during the protocol establishment phase by LR variable parameter 4 (§ A.6.4.1.7).

Note – Applications should support a value of N401 = 64.

A.7.5.7 *Maximum number of outstanding LT frames (k)*

The value of k shall indicate a maximum number of sequentially numbered LT frames that the error-correcting entity may have outstanding (i.e., unacknowledged).

The value of k shall be determined during the protocol establishment phase by LR variable parameter 3 (§ A.6.4.1.6).

The value of k shall never exceed 255.

Note – Applications should support a value of k = 8.

ANNEX B

(to Recommendation V.42)

Mapping of character formats to 8-bit format

This Annex presents the mapping for converting between character formats used on the DTE/DCE interface and those used on the control function/error control function interface. Only support of the 10-bit DTE-to-DCE format is mandatory; support of the other formats shown here is optional. Character formats other than those listed below are not supported.

DTE/DCE: Total bits per character	Specific formats of octets supported	Control function to error control function formatting of octets)
11	Start/ 8 data/ 2 stop Start/ 8 data/ parity/ stop	8 data (parity or second stop bit is independently generated on each DTE/DCE interface
10	Start/ 8 data/ stop	8 data
	Start/ 7 data/ 2 stop	7 data plus 0-bit pad in high-order bit
	Start/ 7 data/ parity/ stop	7 data plus parity as high-order bit
9	Start/ 7 data/ stop	7 data plus 0-bit pad in high-order bit
	Start/ 6 data/ 2 stop	6 data plus two 0-bit pads in two highest-order bits
	Start/ 6 data/ parity/ stop	6 data plus parity in next-to-high-order bit plus 0-bit pad in high-order bit
8	Start/ 6 data/ stop	6 data plus 0-bit pad in two highest-order bits
	Start/ 5 data/ 2 stop	5 data plus three 0-bit pads in three highest-order bits
	Start/ 5 data/ parity/ stop	5 data plus parity in third highest-order bit plus two 0-bit pads in two highest-order bits

APPENDIX I

(to Recommendation V.42)

Interworking with a non-error correcting DCE

This Appendix presents some considerations for interworking between an error-correcting DCE and a non-error-correcting DCE.

I.1 *Interworking with a non-error-correcting answerer*

A non-error-correcting answering DCE will pass the ODP through to its attached DTE. When passed through the asynchronous-to-synchronous converter of a DCE, the ODP produces a bit sequence that is interpreted by a large majority of DTEs as a series of IA5 characters of alternating parity (assuming that the DTE is using the following data format: one start bit, seven data bits, parity, one stop bit). The sequence may interfere with automatic baud rate or character format detection mechanisms of the Answerer or cause the inadvertent bypassing of prompts necessary to the establishment of non-error-corrected DTE-to-DTE communications. In this event, it will be necessary for the Originator to disconnect, manually disable error correction, and reattempt the call.

I.2 *Interworking with a non-error-correcting originator*

An error-correcting answerer called by a non-error-correcting originator will send only mark bits, which cause no observable effect at the originating DTE (since mark-idle is the "normal" state for an asynchronous DTE). After the detection phase timeout period, the error-correcting answerer will revert to non-error-correcting-DCE operation (i.e., non-error-correcting mode).

I.3 *Disposition of unrecognized bits*

If the detection phase is successful (i.e., the error-control DCEs each recognize the error-control capabilities of the other and move into the protocol establishment phase), none of the bits received during the detection phase (i.e., the ODP and the ADP) are delivered to the DTE.

If the detection phase fails, an error-correcting DCE reverts to the non-error-correcting-DCE operation. While the bits received during the failed detection phase were of no value to the error control function, they may indeed have been of value to the DTEs, since the non-error-control DCE will have already given its attached DTE the go-ahead to begin transmitting. There are several possible options for handling these bits, as discussed below; other possibilities also exist.

a) The error-correcting DCE may discard the bits received during the detection phase timeout period. This disposition is the minimal implementation. If the DTE attached to the non-error-correcting DCE did transmit data during the timeout period, it would be necessary, in this case, for the transmission to be repeated if, indeed, the fact that the bits were discarded is recognizable (perhaps because the transmission was meant to evoke some type of response, which fails to materialize).

b) The error-correcting DCE could buffer bits received during the detection phase and, upon termination of the detection phase, forward all of these bits to the DTE. Because of the possibility of continuous transmission from the other DTE, this optional mode of operation would likely require the implementation of fully buffered operation (i.e., every character received is held for forwarding after previously-received characters have been forwarded). While the non-error-correcting-DCE Recommendations do not require this mode of operation, the error-correcting DCE Recommendation does require fully buffered operation any way (as well as DTE/DCE flow control) because of the possibility of retransmission in the event of errors. Buffered and flow-controlled operation without error control could thus be considered a recognized subset of the error-correcting Recommendation that manufacturers could choose to implement and make available to users. This not only overcomes possible lost data during the detection phase, but also supports a constant-speed DTE/DCE interface during non-error-correcting operation. This Recommendation does not require this mode of operation to be available, however.

APPENDIX II

(to Recommendation V.42)

Data forwarding conditions

The control function is responsible for determining when to initiate data transfer for the purpose of transmitting the data received on the V.24 interface to the remote DCE. While it is beyond the scope of this Recommendation to specify when the control function initiates data transfer, several data-forwarding criteria are possible. These include the following:

a) *Data forwarding character* (this corresponds to parameter 3 of Recommendation X.3): The control function may trigger transmission of data received based on reception across the V.24 interface of a pre-designated character or character sequence.

b) *Idle timer* (this corresponds to Parameter 4 of Recommendation X.3): With this method, the control function starts a timer whenever a new character is received across the V.24 interface. If a pre-determined period passes without receipt of a further character, the control function instructs its error control function to transmit the accumulated characters.

c) *Interval timer*: With this method, the control function accumulates characters from the V.24 interface for a period of time. When this time has elapsed, the control function instructs its error control function to transmit the accumulated characters.

d) *Stream mode*: Upon receipt of a character from the V.24 interface, the control function instructs its error control function to commence transmission of data. As the error control function is transmitting an I frame to carry this data and prior to appending the FCS field to close out the I frame, the control function may provide to the error control function additional characters received from the V.24 interface for inclusion in the I frame.

e) *Block mode*: The control function may accumulate a pre-determined number of characters before requesting their transmission by the error control function.

Other data-forwarding criteria may also be used by the control function. The control function may use several methods at the same time.

APPENDIX III

(to Recommendation V.42)

Cross-reference with CCITT Recommendations Q.920 and Q.921

The concepts and procedures used in the main body of this Recommendation are based mostly on CCITT Recommendations Q.920 and Q.921. This Appendix provides a complete cross-reference of sections of Q.920/Q.921 applicable to this Recommendation. In particular, this Appendix indicates, for each section of Q.920 and Q.921, whether:

- it is not applicable to this Recommendation (indicated by a "No" entry in the tables below);
- it is applicable in a general way (indicated by only a "Yes" entry in the tables below); or
- it is applicable in a direct fashion whereby the concepts and/or procedures are nearly similar or identical (indicated by a "Yes" entry in the tables below followed by the applicable V.42 section).

Section of Rec. Q.920	Applicable here?	Section of Rec. Q.920	Applicable here?
1	Yes	4.2	No
2	Yes (§ 6.4)	4.2.1	No
3	Yes	4.2.2	Yes
3.1	Yes (§ 8)	4.3	No
Figure 6	only *a)*	4.4	No
Figure 7	No	4.5	Yes
3.2	No	4.5.1	Yes
3.3	Yes	4.5.2	No
3.4.1	Yes	Table 1	Yes for only point-to-point acknowledged
3.4.2	Yes	4.6	No
3.4.3	No	5	TEI related procedures: No Other procedures: Yes
3.4.4	Yes	5.1	Yes
4	Yes	5.2	Yes
4.1	Yes	5.3	Yes

Section of Rec. Q.921	Applicable here?	Section of Rec. Q.921	Applicable here?
1	Yes	4.2	Yes
2	Yes (§ 8.1)	4.2.1	Yes
3	Yes	4.2.2	Yes
3.1	Yes	5	Yes
3.2	Yes (§ 8.2.1)	5.1	Yes
3.3	Yes	5.1.1	No
3.3.1	Yes (§ 8.2.1.3)	5.1.2	Yes
3.3.2	Yes (§ 8.2.1.2)	5.2	Yes
3.3.3	Yes	5.3	No
3.3.4	Yes	5.4	Yes
3.3.4.1	No	5.5	Yes (§ 8.3, 8.7-8.9)
3.3.4.2	No	5.6	Yes (§ 8.4.1-8.4.8)
3.4	Yes (§ 8.2.2)	5.7	Yes (§ 8.4.9)
3.5	Yes (§ 8.2.3)	5.8	Yes, except 5.8.8: (§ 8.5)
3.6	Yes (§ 8.2.4)	5.9	Yes
4	Yes	5.9.1	Yes (§ 9.2.1)
4.1	Yes (§ 6.4)	5.9.2	Yes (§ 9.2.2)
4.1.1	Yes	5.9.3	Yes (§ 9.2.3)
4.1.1.1	Yes	5.9.4	No
4.1.1.2	Yes	5.9.5	Yes (§ 9.2.4)
4.1.1.3	Yes	5.9.6	No
4.1.1.4	No	5.9.7	No
4.1.1.5	No	5.9.8	Yes (§ 9.2.5)
4.1.1.6	No	5.10	Yes (§ 8.12)
4.1.1.7	No	5.10.1	Yes (§ 8.12.1)
4.1.1.8	No	5.10.2	Yes (§ 8.12.2)
4.1.1.9	Yes	5.10.3	Yes (§ 8.12.3)
4.1.1.10	No	Annex A	No
4.1.1.11	No	Annex B	Yes
4.1.1.12	No	Annex C	No
4.1.1.13	No	Annex D	Yes
4.1.1.14	No	Appendix I	Yes
4.1.1.15	No	Appendix II	No
4.1.2	Yes (§ 6.4)	Appendix III	No
4.1.3	No	Appendix IV	Yes (§ 12.2.1)

APPENDIX IV

(to Recommendation V.42)

Factors for determining the acknowledgment timer

Several procedures of the error control function utilize an acknowledgment timer (T401) to ensure timely receipt of the acknowledgment from the remote error control function. To ensure receipt of such an acknowledgment before the transmitter's T401 expires, the two communicating error control functions must take into account the following time factors:

a) the propagation delay involved in transmitting the frame requiring acknowledgment – (T_a)

b) the time needed for the remote DCE to process the received frame and formulate the acknowledgment – (T_b)

c) the maximum time allowed to complete transmission of those frames in the remote DCE's "transmit queue" (e.g., a frame already in progress of being transmitted or a frame that can not be displaced) – (T_c)

d) the time needed to transmit the acknowledging frame – (T_d)

e) the propagation delay involved in transmitting the acknowledging frame – (T_e)

f) the processing time needed by the error control function to recognize the acknowledging frame – (T_f)

Given values for the above time limits, the value of the acknowledgement timer used by the transmitting error control function should then be set as follows:

$$\text{T401} \geqslant T_a + T_b + T_c + T_d + T_e + T_f$$

APPENDIX V

(to Recommendation V.42)

Potential enhancements to LAPM protocol

During the development of V.42, several issues were raised that may lead to enhancements to the LAPM protocol (defined in the main body of V.42) or modifications to related V-Series Recommendations during the 1989-1992 Study Period. This Appendix briefly reviews these issues so that manufacturers are aware of the likely development path of V.42. Unless otherwise specified, the enhancements would be implemented as optional features.

V.1 *Data compression*

The performance of the error-correcting DCE may be enhanced considerably through the use of data compression on the character stream received from the DTE prior to transmission by the error control function.

V.2 *Forward error correction*

In certain applications of V-series modems, the bit error rate occurring over the physical connection may be sufficiently high to seriously reduce the throughput obtained by the error control function. An example of this type of application is the use of modems for data transmission over cellular radio links. Under these conditions, performance may be improved if the output of the error control function is encoded using a forward error-correction code prior to transmission over the physical connection.

V.3 *Statistical multiplexing*

Multiplexing of several streams of user data over a single physical connection may be performed in two ways. The procedures described in the LAPM definition are able to support multiple logical connections; therefore, a separate DLCI could be associated with each data stream. Alternatively, a single logical connection may be used to transport data from several DTEs that would require some means of structuring the information field of an I frame.

V.4 *End-to-end transport of interface state information*

A common requirement related to § V.3 is the ability to replicate the state of a subset of the V.24 interface leads at the remote DTE/DCE interface as, for example, described in Recommendation V.110. This could be accomplished by using a UI frame (see §§ 8.6 and 12.3) and encoding the interface circuit states within the information field, or by adding a header to each I frame.

V.5 *Issues related to control function-to-control function information exchange*

a) A DLCI value has been reserved for the transport of control function-to-control function information between the peer-DCE control functions. The protocol for this information exchange has been left for further study.

b) Loop-back testing between control functions is possible using the procedures defined within LAPM.

V.6 *Rate negotiation*

The DCE control functions may communicate information relating to the available transmission speeds and modulation schemes over the DLCI discussed in § V.5 so that a fallback/fall-forward strategy may be agreed. This has particular application in multi-standard DCEs where the ability to switch between, for example, V.32 and V.22 during the call may result in performance improvements due to poor line quality.

V.7 *Operation over an asymmetric or half-duplex physical connection*

Several issues were raised relating to operation over an asymmetric or half-duplex connection. The performance of the error-correcting protocol may be optimized for use over a specific physical connection; however, the means by which this is accomplished are for further study. One possible technique is described in § V.8 below. Another possible technique is given in Recommendation X.32 and is known as LAPX for operation on half-duplex connections.

V.8 *Multiple frame reject*

The selective reject mechanism defined for LAPM permits several I frames to be individually rejected; however, a control frame – SREJ – must be transmitted for each frame rejected (i.e., for each frame for which retransmission is requested). In certain applications, for example, for use with a half-duplex physical connection, performance would be significantly improved if a single control frame could be used to request retransmission of several I frames, not necessarily consecutive. The control frame (MREJ) could contain an information field with a bit map of length k bits, in which the state of each bit indicates the acknowledgment or rejection of the corresponding frame within the k-frame window of outstanding frames.

V.9 *Character format indication/negotiation*

While it is possible for the start-stop mode character format to be associated at each end with the DTE/DCE interface (i.e., that the format used by the DTE at each end of the connection may be different), certain inconsistencies would not be permitted. In the case of differences in the use of parity or the number of stop bits, it is sufficient that the data bits are carried end-to-end. If the character formats at the two DTE/DCE interfaces differ in the number of data bits, the call must be cleared or the DCEs negotiate a common format. This is for further study.

V.10 *Preservation of framing/parity errors*

When an 11-bit character format is used, there is no mechanism defined by which the state of the parity bit may be indicated to the remote DTE. In addition, other character-format errors detected at the DTE/DCE interface would not be signaled. There are two alternative options; to remove the requirement for octet alignment and, hence, allow a ninth or subsequent bits to be sent, or to send subsidiary information when an error is detected.

V.11 *Encryption*

The use of encryption within an error-correcting DCE has some advantages, specifically when used in conjunction with data compression. If encrypted data is received from the DTE, the properties that would normally be used to obtain data compression may be affected by the encryption process and, hence, poor compression achieved. The effectiveness of encryption employed after the data is compressed is higher, due to the lower redundancy within the encoded stream.

V.12 *ISDN compatibility*

Some advantage may be obtained from compatibility with ISDN access protocols in applications involving ISDN/GSTN interworking, i.e., where dial-up access to ISDN services or subscribers is required. LAPD-based protocols have been proposed for several applications within ISDN, for example, terminal adaption.

SECTION 5

TRANSMISSION QUALITY AND MAINTENANCE

Recommendation V.50

STANDARD LIMITS FOR TRANSMISSION QUALITY OF DATA TRANSMISSION

(Mar del Plata, 1968)

One of the most important factors affecting data transmission quality – similarly to telegraph transmission quality – is the distortion in time of the significant instants (known as "telegraph distortion" [1]; the degree of signal distortion must be kept within certain limits, the ultimate objective being that the degree of distortion on received signals should be compatible with the margin of the receiving equipment.

This distortion on received signals arises from the composition of:

a) the sending distortion;

b) the distortion introduced by the transmission channel.

Hence, limits must be fixed for the degree of sending distortion and for the degree of distortion due to the transmission channel.

The limits contemplated for the transmission channel are specified in Recommendation V.53; these limits, which are not yet final, are recalled below:

Channel with modem V.21: 20-25%

Channels with modem V.23:

600 bauds – leased circuits: 20-30%

1200 bauds – leased circuits: 25-35%

600 bauds – switched circuit: 25-30%

1200 bauds – switched circuit: 30-35%

(when this mode of operation is possible)

These figures are expressed provisionally in maximum degrees of individual distortion and apply to the circuit including the modems. The limits for the degree of sending distortion must be fixed so that a reasonable margin is left for the receiving equipment, making allowance for the distortion introduced by the circuit.

In view of the foregoing, the CCITT *unanimously issues the recommendation that*:

1 with regard to the *quality of transmission signals* (signals at point A – Figure 1/V.51), it is preferable, given the wide range of possible modulation rates, to adopt a single standard for each type of modem.

2 when a Recommendation V.21 modem is used, the duration of a unit element should be at least 90% of the duration of the unit element at 200 bauds [i.e. (1/200) × (90/100) second, or 4.5 milliseconds].

3 when a Recommendation V.23 modem is used, the duration of a unit element should be at least 95% of the duration of the unit element either at 1200 bauds [(1/1200) × (95/100) second, or 0.791 millisecond] or at 600 bauds [(1/600) × (95/100) second, or 1.583 millisecond].

4 if a system sends signals of which the sending distortion is systematically well below the limits specified above for the category concerned, the permissible margin for receivers of that system may be reduced.

5 the values indicated above could be revised when a more accurate plan for transmission quality has been drawn up.

Note – The receive margin limits will be studied in liaison with the ISO.

Reference

[1] CCITT Definition: *Telegraph distortion*, Volume I, Fascicle I.3 (Terms and Definitions).

Recommendation V.51

ORGANIZATION OF THE MAINTENANCE OF INTERNATIONAL TELEPHONE-TYPE CIRCUITS USED FOR DATA TRANSMISSION

(Mar del Plata, 1968)

(For the text of this Recommendation, see Recommendation M.729, Volume IV, Fascicle IV.1.)

Recommendation V.52

CHARACTERISTICS OF DISTORTION AND ERROR-RATE MEASURING APPARATUS FOR DATA TRANSMISSION

(Mar del Plata, 1968; amended at Geneva, 1972)

(Replaced by Recommendation O.153, Melbourne, 1988; see Volume IV, Fascicle IV.4 of the Blue Book.)

Recommendation V.53

LIMITS FOR THE MAINTENANCE OF TELEPHONE-TYPE CIRCUITS USED FOR DATA TRANSMISSION

(Mar del Plata, 1968)

For data transmission maintenance purposes, the following limits are recommended for the essential parameters indicating the quality of a transmission channel.

1 Telegraph distortion limits

Limits for the *degree of distortion on a transmission channel* between the interfaces (i.e. including the modems) vary with the data transmission system. The following values are recommended, these same limits applying to the backward channel:

System with Recommendation V.21 modem: 20-25%

Systems with Recommendation V.23 modem:

600 bauds – leased circuits: 20-30%

1200 bauds – leased circuits: 25-35%

600 bauds – switched circuit: 25-30%

1200 bauds – switched circuit: 30-35%

(when this mode of operation is possible).

These figures express provisionally maximum degrees of individual distortion. They will be converted into degrees of isochronous distortion once a method for determining the reference ideal instant has been studied, specifying a synchronization procedure for the distortion-measuring receiver.

2 Limits for error rates

2.1 *Bit error rate*

The limits in Table 1/V.53 are recommended; when they are exceeded the maintenance services should consider the transmission channel defective. The period of measurement is about 15 minutes (more precisely, the period corresponding to the transmission of the total number of sequences which is closest to 15 minutes).

TABLE 1/V.53

Modulation rate (bauds)	Connection	Maximum bit error rate
1200	switched (when possible)	10^{-3}
1200	leased	$5 \cdot 10^{-5}$
600	switched	10^{-3}
600	leased	$5 \cdot 10^{-5}$
200	switched	10^{-4}
200	leased	$5 \cdot 10^{-5}$

Note – These values are not intended for use in planning circuits, but for the information of maintenance services.

2.2 *Block error rate*

Information on the error rate for sequences of 511 bits would be given in a form similar to that for the bit error rate, the two measurements being made simultaneously. However, no limit for the sequence error rate can be recommended for the time being.

Note – To enable Administrations to appreciate the value of sequence error-rate measurement, Table 2/V.53 shows the *maximum and minimum theoretic values* of error rates for sequences of 511 bits corresponding to different values of bit error rate.

These theoretic values do not depend on the modulation rate. For the purposes of this table, a modulation rate of 1200 bauds has been taken as an example.

Modulation rate: 1200 bauds
Period of measurement: 15 minutes = 900 seconds
Number of bits transmitted: 1 080 000
Length of sequence: 511 bits
Number of sequences transmitted: 2113

3 Limit of uniform-spectrum random noise

See Recommendation G.153 [1].

TABLE 2/V.53

Bit error rate	Number of erroneous bits	Erroneous sequences			
		Maximum number [a]	Maximum rate in %	Minimum number [b]	Minimum rate in %
$2 \cdot 10^{-3}$	2160	2113	100	5	0.24
10^{-3} [c]	1080	1080	51.1	3	0.15
$5 \cdot 10^{-4}$	540	540	25.5	2	0.10
10^{-4}	108	108	5.1	1	0.05
$5 \cdot 10^{-5}$	54	54	2.5	1	0.05

[a] The *maximum* number of erroneous sequences corresponds to a *uniform* distribution of erroneous bits (one bit per sequence).

[b] The *minimum* number of erroneous sequences corresponds to a *grouped* distribution of erroneous bits (sets of 511 bits affecting the sequences).

[c] It will be seen that for a bit error rate of 10^{-3}, the sequence error rate can vary between 0.15% and 51.1%. (This shows the value of sequence error-rate measurement, not only for users, but also for Administrations, which can thus obtain useful information on the causes of bit and sequence error).

4 Limits for impulsive noise

4.1 Bearing in mind the following two points:

- that Recommendation V.2 demands a maximum data signal level of −10 dBm0 for a simplex transmission and −13 dBm0 for duplex transmission,
- that there has been considerable experience of using the threshold −18 dBm0 and −22 dBm0,

the threshold settings should be −18 dBm0 for telephone-type circuits and −21 dBm0 for the special quality circuits mentioned in Recommendation M.1020 [2], the standard measuring instrument (see Recommendation O.71, [3]) being adjustable to thresholds 3 dB apart (see Note 1).

4.2 For counting the number of impulses, the instrument shall be used in the "flat" bandwidth condition (see Note 2).

On a leased circuit, the admissible limit should be 70 impulse counts per hour; but in realizing that error rate measurements are conducted for periods of 15 minutes each, the recommended maintenance limit should be 18 counts in 15 minutes for leased circuits (see Note 3). The measurements should be made during peak hours.

At the time of measurement the line should be terminated at both ends by impedances of 600 ohms. The modem may be used for this purpose if it complies with this impedance.

4.3 For the general switched telephone network, there should be no recommended maintenance limits for impulse counts, but the instrument might be useful as a diagnostic aid at the discretion of the Administrations. This is because the impulse count results taken on any one connection vary considerably with time and even greater differences appear between various connections.

4.4 The correlation between the bit error rate and the number of impulse counts thus determined has not yet been established.

Note 1 – Levels should be expressed in dBm0, because

a) the difference between the various national transmission plans is taken into account, and

b) the level value is related to the value of the data signal level to a close degree.

Note 2 – Owing to lack of experience, no external filter should be used for present maintenance purposes. However, the study of the use of external filters should continue. By means of additional filters the instrument may provide other optional bandwidths (see the Recommendation cited in [4]).

Note 3 – These values are given as an indication. The question of the duration of the measurement and permissible maximum standards for impulsive noise forms the subject of future studies.

References

[1] CCITT Recommendation *Characteristics appropriate to international circuits more than 2500 km in length*, Vol. III, Rec. G.153.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

[3] CCITT Recommendation *Specification for an impulsive noise measuring instrument for telephone-type circuits*, Vol. IV, Rec. O.71.

[4] *Ibid.*, § 3.5.2.

Recommendation V.54

LOOP TEST DEVICES FOR MODEMS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984 and at Melbourne, 1988)

1 Introduction

The CCITT,

considering

the increasing use being made of data transmission systems, the volume of the information circulating on data transmission networks, the savings to be made by reducing interruption time on such links, the importance of being able to determine responsibilities in maintenance questions for networks, of necessity involving several parties, and the advantages of standardization in this field,

unanimously declares the following:

The locating of faults can be facilitated in many cases by looping procedures in modems. These loops allow local or remote measurements, analogue or digital, to be carried out optionally by the Administrations and/or users concerned.

2 Scope

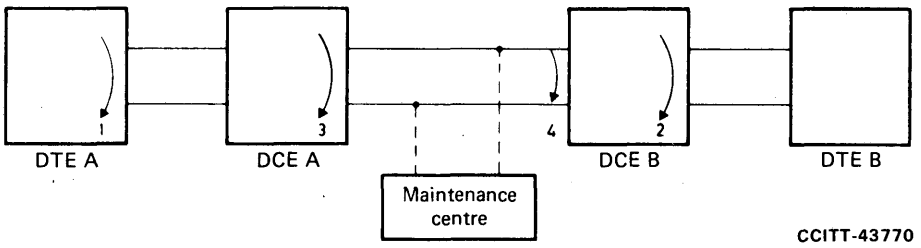
This Recommendation specifies modem loop testing procedures for the following cases:

– for synchronous mode of operation over point-to-point leased circuit, multipoint, tandem and general switched telephone network (GSTN) connections;

– for start-stop mode of operation over point-to-point leased circuit and GSTN connections.

3 Definition of the loops

Four loops are defined (numbered 1 to 4) and their locations as seen from DTE A are shown in Figure 1/V.54. A symmetrical set of four loops could exist as seen from DTE B.



DTE Data terminal equipment
DCE Data circuit-terminating equipment

FIGURE 1/V.54

3.1 *Loop 1*

This loop is used as a basic test on the operation of the DTE, by returning transmitted signals to the DTE for checking. The loop should be set up inside the DTE as close as possible to the interface.

While the DTE is in the loop 1 test condition:

- transmitted data (circuit 103) are connected to received data (circuit 104) within the DTE;
- circuit 108/1 or 108/2 must be in the same condition as it was before the test;
- circuit 105 must be in the OFF condition;
- circuit 125 should continue to be monitored by the DTE so that an incoming call can be given priority over a routine loop test.

Interchange circuit 103 as presented to the DCE must be in the binary 1 condition.

The conditions of the other interchange circuits are not specified but they should if possible permit normal working. The transmitter timing information, in particular if it comes from the DCE, will continue to be sent (see Recommendation V.24, § 4.6.2).

Note – When circuits 108 and 105 are not used by the DTE (for applications on leased lines, for example) the DCE will not be informed of the test condition. This is considered acceptable provided that the remote station is not disturbed.

3.2 *Loop 3*

This is a local loop established in analogue mode as close as possible to the line to check the satisfactory working of the DCE. The loop should include the maximum number of circuits used in normal working (in particular the signal conversion function, if possible) which may in some cases necessitate the inclusion of devices for attenuating signals, for example.

The establishment of the loop presents no difficulty when using a 4-wire line, except in certain cases in which parts of the line equalization system are removed from service.

For certain 2-wire lines the loop may be obtained by simple unbalance of the hybrid transformer.

While the DCE is in the loop 3 test condition:

- the transmission line is suitably terminated, as required by national regulations;
- all interchange circuits are operated normally, except in the case of 2-wire half-duplex operation where the mandatory clamping involving circuits 105 and 109 (as specified in Recommendation V.24, § 4.3.2 a) is disabled;
- circuit 125 should continue to be monitored by the DTE so that an incoming call can be given priority over a routine loop test, after abandoning the loop 3 condition;
- no signal is transmitted to line on the data channel.

Since most interchange circuits operate normally, a diagram of interchange circuit operation sequence is not presented.

Note 1 – In certain switched networks the loop 3 procedure may clear the connection due to national regulations. During the loop 3 condition, however, the DCE must not be switched to the line, if not already connected.

Note 2 – In 4-wire point-to-point connections circuit 105 may be continuously ON. If in such cases synchronous modems are used, no test data should be transmitted until circuits 106, 109 and 142 are in the ON condition.

3.3 *Loop 2*

Loop 2 is designed to permit station A or the network to check the satisfactory working of the line (or part of the line) and of the DCE B. It can only be used with a duplex DCE; the application to the backward channel is left for further study. Pseudo loop 2 may be defined for a half-duplex DCE and will be specified in the Recommendation relating to the DCE concerned.

The establishment of the loop will be effective when the control is applied, regardless of the condition of circuit 108 presented by the DTE associated with the DCE in which the loop is set up.

While the DCE B is in the loop 2 test condition:

- circuit 104 is connected internally in the DCE to circuit 103 (see Note 1);
- circuit 104 to the DTE is maintained in the binary 1 condition;
- circuit 109 is connected internally in the DCE to circuit 105 (see Note 1);
- circuit 109 to the DTE is maintained in the OFF condition;
- circuit 106 to the DTE is maintained in the OFF condition;
- circuit 107 to the DTE is maintained in the OFF condition;
- circuit 115 is connected internally in the DCE to circuit 113 if provided (see Note 1);
- circuit 115 and circuit 114, if provided, to the DTE continue to function.

Note 1 – For the internal DCE connections, the electrical signal characteristics may either be that of the interchange circuits or that of the logic level used inside the DCE.

Note 2 – In certain applications, it may not be desirable to connect circuit 115 to circuit 113. In these cases a flexible buffer between circuits 104 and 103 might be recommended. Alternatively, changes in the transmit clock may be done in a phase-continuous manner.

3.4 *Loop 4*

This loop arrangement is only considered in the case of 4-wire lines. Loop 4 is designed for the maintenance of lines by Administrations using analogue-type measurements. When receiving and transmitting pairs are connected in tandem, such a connection cannot be measured as a data circuit (conformity with a line characteristic curve, for example).

In the loop position the two pairs are disconnected from the DCE and are connected to each other through a symmetrical attenuator designed to prevent any oscillation of the circuit (the loop, therefore, does not include any of the amplifiers and/or distortion correctors used in the DCE). The value of the attenuator will be fixed by each Administration in compliance with Recommendation G.122 [1].

Loop 4 may be established inside the DCE or in a separate unit.

When loop 4 is inside the DCE, and while in the test condition, the DCE presents circuits 107 and 109 to the DTE in the OFF condition and circuit 142 is in the ON condition. When loop 4 is in a separate unit, these conditions are desirable but not mandatory.

4 Loop control

Two (non-exclusive) types of control might be possible on the DCE:

- manual control by a switch on the equipment;
- automatic control through the DCE-DTE interface or upon recognition of a loop initiation signal in the received data.

The test procedures shall be based on either manual or automatic control of loops. Combined use of these control methods shall be avoided. However, manual release of a test loop shall have priority over automatic control in those DCEs where both test methods are implemented.

Note – The response of a DCE to automatic or manual control attempts in the case where the other control method is used, is not specified.

Interchange circuit 142 shall be used to inform the DTE of a loop condition in the local DCE, even in the case of manual control (but see Note 3 to Table 1/V.54). To avoid ambiguity in interpretation of circuit 142 only one loop should be established at any one time in the DCE.

4.1 *Manual control*

See Table 1/V.54.

TABLE 1/V.54

Interface signalling for manual control of loops

Loop	Control switch on	Signal to DTE A		Signal to DTE B		Notes
		Circuit 107	Circuit 142	Circuit 107	Circuit 142	
2	DCE B	*)	*)	OFF	ON	Note 1
3	DCE A	ON	ON	*)	*)	Note 2
4	DCE B	*)	*)	OFF	ON	Note 3

*) Not applicable.

Note 1 – Data station A is in the normal operating condition. The loop is established by a switch on DCE B.

Note 2 – In DCE A, the condition of circuit 107 will be determined by the condition of circuit 108. When circuit 108 is not provided on the interface, circuit 107 is ON. The normal case is considered in the table.

Note 3 – When loop 4 is in a unit separate from the DCE, the signals to DTE B are desirable but not mandatory due to the difficulty of implementation. When the loop is implemented within the DCE, loop establishment shall always be possible by a switch on the DCE.

Note 4 – The conditions represented by ON in the table may also activate a visual indicator on the DCE.

4.2 *Automatic control through the DTE/DCE interface* (see Table 2/V.54)

Automatic control through the interface is achieved by using circuit 140, 141 and 142 as defined in Recommendation V.24. Circuit 140 is used to control loop 2 and circuit 141 is used to control loop 3. The turning ON of circuit 142 indicates the test mode is established. If circuit 107 is ON, the associated terminal is concerned and subsequent data transmitted on circuit 103 will be looped back on circuit 104. If circuit 107 is OFF, the associated terminal is not concerned.

Note 1 – Automatic control of loop 4 is considered of no use either locally or in the remote station and therefore is not provided.

Note 2 – As an alternative to activation of loop 3 via circuit 141, it could be activated via the four-phase procedure defined in § 4.2 here.

TABLE 2/V.54

Interface signalling for automatic control of loops

Loop	Control signals from DTE A		Signals to DTE A		Signals to DTE B		Notes
	Circuit 140	Circuit 141	Circuit 107	Circuit 142	Circuit 107	Circuit 142	
2	ON	OFF	ON	ON	OFF	ON	Notes 1 and 2
3	OFF	ON	ON	ON	*)	*)	Note 2

*) Not applicable.

Note 1 – There is a risk of head-on collision of controls from the two ends.

Note 2 – In DCE A, the condition of circuit 107 will be determined by the condition of circuit 108. When circuit 108 is not provided on the interface, circuit 107 is ON. The normal case is considered in the table.

Normally circuit 103 can only be used to transmit data or the test sequence, so long as the conditions of circuits 106, 140, 141 and 142 are as indicated in Table 3/V.54.

TABLE 3/V.54

Circuit 103	Circuit 106	Circuit 140	Circuit 141	Circuit 142
Data	ON	OFF	OFF	OFF
Loop 2 test sequence	ON	ON	OFF	OFF
Loop 3 test sequence	ON	OFF	ON	ON

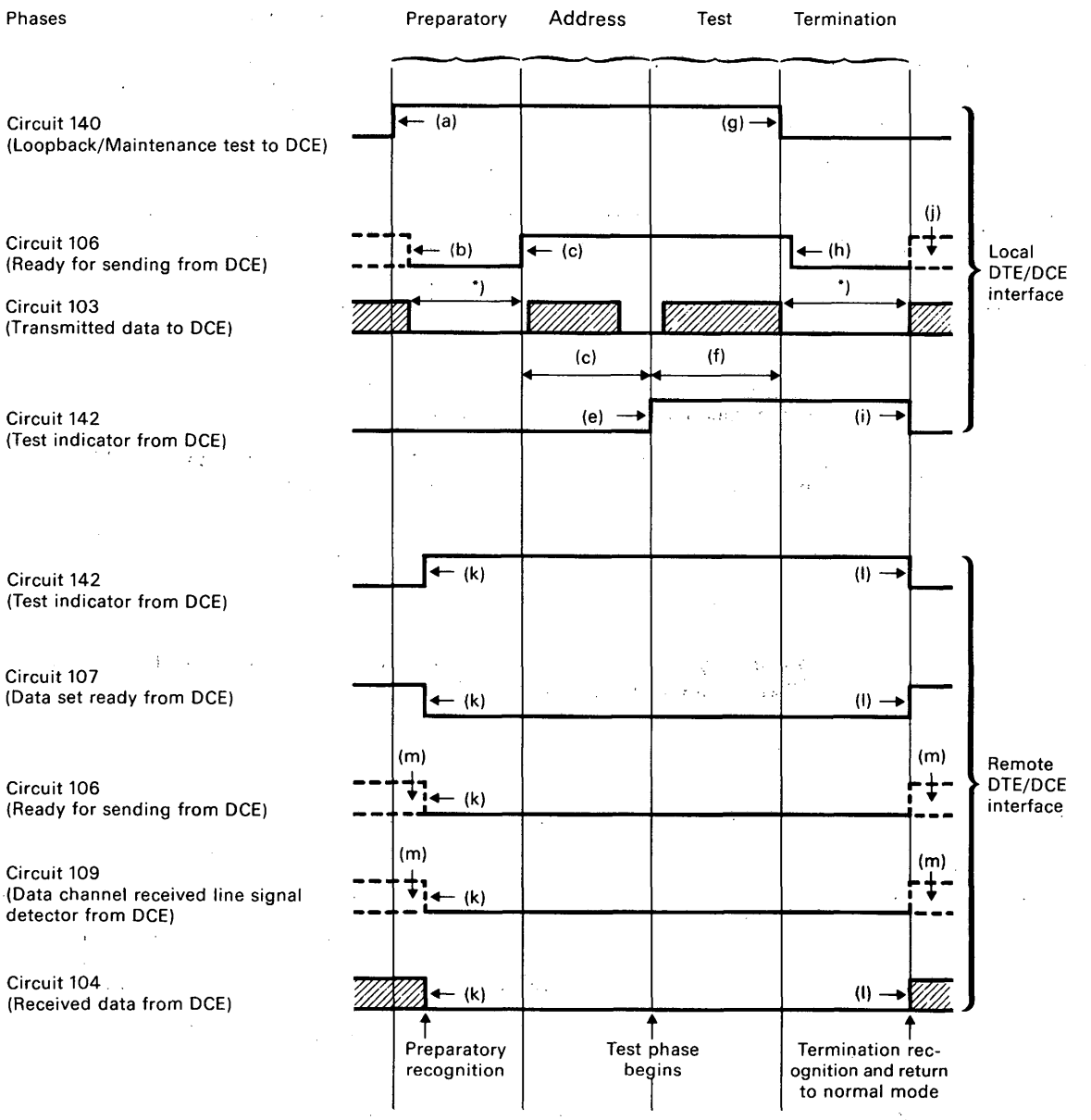
For inter-DCE signalling a four-phase action/reaction sequence should be used. The state of interchange circuits principally involved during this sequence is shown in Figure 2/V.54.

Automatic control with synchronous DCEs is decribed for:

- simple multipoint circuits (see § 5);
- point-to-point duplex circuits (see § 6);
- tadem circuits (see § 7).

Automatic control with asynchronous DCEs is decribed for:

- point-to-point duplex circuits (see § 8).



*) The DCE will ignore circuit 103 during preparatory and terminating phases.

Significant level reference — Binary 0 / Binary 1 — ON / OFF

Note – This sequence may be used for point-to-point duplex circuits. The address phase is not essential for point-to-point applications.

FIGURE 2/V.54

State of interchange circuits during the four-phase action/reaction sequence

Explanation of Figure 2/V.54

Central site

(a) Circuit 140 goes ON (to DCE), requesting a maintenance sequence.

(b) Circuit 106 goes OFF (from DCE), very shortly thereafter, if not already OFF.

(c) Circuit 106 goes ON (from DCE), after a delay, which signifies that the DCE can accept address information.

(d) Circuit 103 is active (to DCE), transmitting the address.

(e) Circuit 142 goes ON (from DCE), after a delay, signifying that the maintenance address has been acted upon and if a loop establishment has been requested, circuit 103 may now be used for the test message.

(f) Circuit 103 is active (to DCE), containing a test message or any other data as required by the maintenance routine being performed.

(g) Circuit 140 goes OFF (to DCE), requesting termination of the maintenance sequence and a return to normal operation.

(h) Circuit 106 goes OFF (from DCE), very shortly thereafter.

(i) Circuit 142 goes OFF (from DCE), after a delay, signifying that the terminating phase is complete and the system is returned to normal operation.

(j) Circuit 106 may be ON or OFF after the maintenance sequence.

During the maintenance the state of circuit 105 would be disregarded.

Remote site

(k) Circuit 142 goes ON (from DCE), indicating test mode to the remote DTE.

Circuit 107 goes OFF. Circuits 106 and 109 go OFF if not already OFF.

Circuit 104 is clamped to binary 1 condition. Before preparatory recognition spurious bits may appear on circuit 104.

(l) Circuit 142 is turned OFF, circuit 107 is turned ON, the clamping of circuit 104 by circuit 142 ON condition is removed, signifying that termination recognition has taken place at the remote DCE, and that it has returned to the normal mode.

(m) Circuits 106 and 109 may be ON or OFF, prior to and after the maintenance sequence.

5 Inter-DCE signalling for simple multipoint circuits with synchronous DCEs

Note 1 – Modems in accordance with Recommendation V.22 are excluded from this procedure.

Note 2 – Considering the fact that there already exist or will exist modems implementing other signalling techniques than the one defined in this Recommendation and that these signalling techniques have been designed according to special conditions formulated by Administrations or users, this Recommendation does not limit the use of such signalling techniques.

A state diagram of the preparatory, address, test and termination phase is shown in Figure A-2/V.54.

5.1 *Preparatory phase*

During the preparatory phase DCE A will transmit a pattern of 2048 ± 100 bits produced by scrambling a binary 0 with the polynominal $1 + x^{-4} + x^{-7}$. No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler. Before transmitting the preparatory pattern, DCE A has to establish a data channel, if not already available.

The criteria for the recognition of this pattern by DCE B are not part of this Recommendation. The criteria that are implemented should offer a very high protection against false recognition due to simulation by user data and some protection against failure to recognize the preparatory pattern due to a high bit error rate. In order to provide protection against false recognition caused by user HDLC frames, the bit sequence consisting of seven consecutive binary 1s, which is at present in the preparatory pattern, must be included in the recognition criteria.

DCE B will start Timer T1 (if implemented) upon recognition of the preparatory phase.

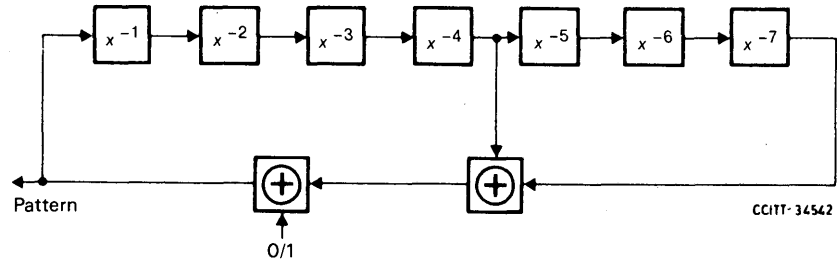


FIGURE 3/V.54

Example of scrambler implementation

5.2 *Address phase*

5.2.1 *Address signalling*

During the address phase the DTE will transmit an address sequence consisting of an address octet that is repeated at least 16 times. The sequence may be preceded and succeeded by other octets as required by the user link level protocol. Synchronous DCEs will transmit these octets in contiguous eight bit groups.

Table 4/V.54 contains a set of possible address octets and the constraints on their use.

When an extension of the address set is required, a similar set consisting of two-octet addresses can be generated.

Note – The set contained in Table 4/V.54 may be regarded as a subset of the extended set, i.e. one consisting of those two-octet addresses whose two octets are identical.

The DCE will recognize its address when it is detected in at least five contiguous octets received. No octet synchronization is required.

When the DCE detects an address sequence (five identical contiguous octets), not containing its address, it will disable the address detection function, thus avoiding false recognition of its own address due to simulation by subsequent test messages.

5.2.2 *Acknowledgement signalling*

DCE B, upon recognition of the address signal containing its address, will transmit a pattern of 1948 ± 100 bits produced by scrambling a binary 1 with the polynomial $1 + x^{-4} + x^{-7}$. No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler.

Before transmitting the acknowledgement pattern, DCE B has to ensure that the data channel to DCE A is available. Since the loop 2 test is in a synchronous DCE, DCE B will use its receiver signal element timing for this data channel.

TABLE 4/V.54

Single-octet address set

Hexadecimal code	Note	Hexadecimal code	Note	Hexadecimal code	Note
01	1	19	1	37	1
03	2	1B	2	3B	1
05	2	1D	2	3D	1
07	1	1F	1, 4	3F	2, 4
09	2	25	1	55	2
0B	3	27	2	57	1
0D	1	2B	2	5B	1
0F	2	2D	2	5F	2, 4
11	2	2F	1	6F	2
13	1	33	2	77	2
15	1	35	2	7F	1, 4
17	2	35	2	7F	1, 4

Note 1 – Odd parity.

Note 2 – Even parity.

Note 3 – Sync (1/6) with odd parity.

Note 4 – Not to be used in ISO 3309 (HDLC) frame structures.

The criteria for the recognition of this pattern by DCE A are not part of this Recommendation. The criteria that are implemented should offer good protection against failure to recognize the acknowledgement signal due to a high bit error rate.

DCE B, after transmission of the acknowledgement pattern, will enter the test phase.

DCE A, upon recognition of the acknowledgement pattern, will time out for a 2148 ± 100 bit period and will then turn ON circuit 142, thus entering the test phase.

DCE A, upon recognition of the acknowledgement pattern, will not take any action if it is in the normal data mode.

5.3 *Test phase*

Signals transmitted during the test phase are not specified in this Recommendation.

5.4 *Termination phase*

During the termination phase, DCE A will transmit a pattern of 8192 ± 100 bits produced by scrambling a binary 1 with the polynomial $1 + x^{-4} + x^{-7}$, followed by 64 binary 1s.

No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler.

DCE B will terminate the test mode in any of the following situations:

- recognition of the termination pattern;
- carrier loss with a duration longer than 1 s;
- expiration of the optional Timer T1.

The criteria for the recognition of this pattern by DCE B are not part of this Recommendation. The criteria that are implemented should offer good protection against false recognition due to simulation by test data and good protection against failure to recognize the termination pattern due to a high bit error rate.

DCE B will normally leave the termination phase during the reception of the binary 1 pattern that concludes the termination pattern.

DCE B upon recognition of the termination pattern will not take any action if it is in the normal data mode.

Note – The length of the time interval of the optional Timer T1 is not specified in this Recommendation.

6 Simplified inter-DCE signalling for use in point-to-point circuits with synchronous DCEs

For point-to-point circuits which require control of one loop 2 only, the four-phase sequence may be simplified by deleting the address signalling. The procedure is then as follows (see Figure A-3/V.54):

- Preparatory phase: in accordance with § 5.1.
- Address phase: acknowledgement signalling only in accordance with § 5.2.2 upon recognition of the preparatory pattern.
- Test phase: signals transmitted during the test phase are not specified in this Recommendation.
- Termination phase: in accordance with § 5.4.

7 Inter-DCE signalling for tandem circuits with synchronous DCEs

For tandem circuits the four-phase sequence may be used to control the loops shown in Figure 4/V.54.

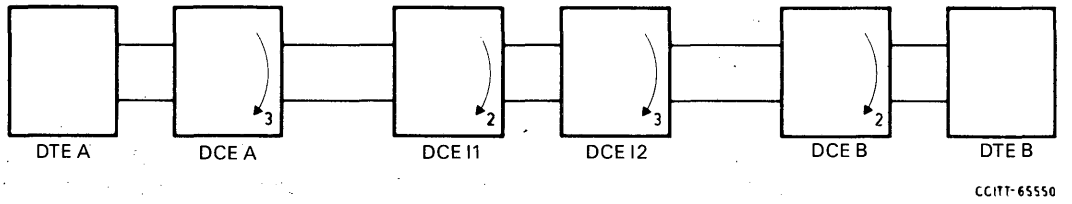
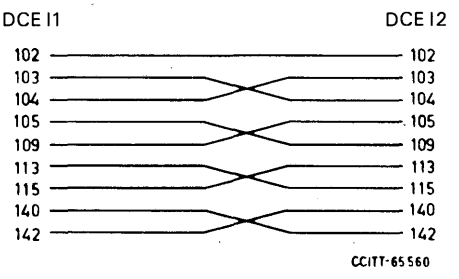


FIGURE 4/V.54

The inter-DCE signalling procedures apply to synchronous modems only, with or without multiplexer features. The interchange circuits of the DCEs at the intermediate site are connected as shown in Figure 5/V.54.



Note 1 - The ON condition on circuit 142 shall not clamp the interchange circuits 107, 109 and 104 in DCE I1.

Note 2 - Signalling the ON condition from circuit 142 to 140 shall not start transmission of the preparatory pattern from DCE I2, but activate the address monitor.

Note 3 - Only those interchange circuits essential for establishing the loops are shown.

FIGURE 5/V.54

A state diagram of the four-phase sequence is shown in Figure A-4/V.54. The procedure is as follows:

- Preparatory phase: in accordance with § 5.1.

  When DCE I1 recognizes the preparatory pattern it will signal this condition via the ON condition on circuit 142 to circuit 140 of DCE I2, which will activate its address monitor.

  The preparatory pattern is transmitted via circuit 103 of DCE I2 to DCE B.
- Address phase: in accordance with § 5.2.
- Test phase: signals transmitted during the test phase are not specified in this Recommendation.
- Termination phase: in accordance with § 5.4.

When a loop has been established in the intermediate site, the part of the link "behind" the loop is in fact inactivated.

When the loop that has been established is a loop 3 in DCE I2, the carrier towards DCE B will be removed from the line. When this condition lasts for more than one second, DCE B will regard the test condition as terminated and return to normal mode (i.e. with data carrier lost). As this situation was preceded by a 142 ON condition, the remote DTE may regard this as a normal situation. When the loop 3 condition in DCE I2 is terminated, which will normally be after the reception of the full termination pattern, the remote DTE will not receive garbled signals after DCE B has recovered the carrier.

When the loop that has been established is a loop 2 in DCE I1 all patterns will pass to DCE B. Thus DCE B will also receive the termination pattern and leave the test mode at the prescribed time. DCE I2 will leave the test mode upon detecting the OFF condition on circuit 140.

Note – When the connection of DCE I1 and DCE I2 is established via a multiplexer without remote signalling capabilities for interchange circuits 109 and 142, DCE I2 may optionally derive the required information from the patterns present on interchange circuit 103.

8 Inter-DCE signalling for point-to-point connections with asynchronous DCEs

For point-to-point duplex circuits with asynchronous DCEs for start-stop operation only, the four-phase sequence may be simplified by deleting the address signalling. Instead of the pseudo-random patterns used for synchronous transmission a simple signalling method shown in Figure 6/V.54 shall be used.

8.1 *Preparatory phase*

During the preparatory phase DCE A will transmit a SPACE-MARK-SPACE pattern. The duration of each interval shall be 320-400 ms.

8.2 *Address phase*

DCE B, upon recognition of the preparatory pattern, will establish loop 2 and transmit the acknowledgement signal consisting of a carrier OFF period of 100-150 ms.

DCE A will turn ON circuit 142 and enter the test phase after it has detected the OFF to ON transition of the carrier signal.

8.3 *Test phase*

Signals transmitted during the test phase are not specified in this Recommendation.

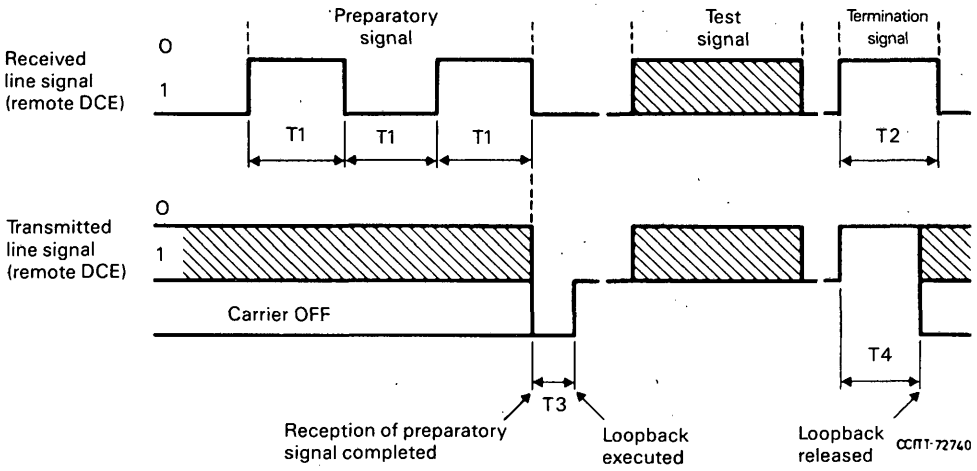
8.4 *Termination phase*

During the termination phase DCE A will transmit a signal consisting of binary 0 (SPACE) for at least 550 ms.

DCE B will terminate the test mode in any of the following situations:

- recognition of the termination signal for 480-550 ms;
- carrier loss with a duration longer than 1s.

DCE B upon recognition of the termination signal will not take any action if it is in the normal data mode.



Time duration
T1 : 320 - 400 ms
T2 : ≥ 550 ms
T3 : 100 - 150 ms
T4 : 480 - 550 ms

Note 1 - Line signals that are transmitted before reception of preparatory signal is completed, and after loopback is released, depend upon the data signals transmitted by the DTE on circuit 103.

Note 2 - Binary 0 (SPACE) and binary 1 (MARK) correspond to the frequencies F_A and F_Z respectively.

FIGURE 6/V.54

Loop 2 signalling method in asynchronous modems

ANNEX A

(to Recommendation V.54)

State diagrams

A.1 *Introduction*

Procedures as outlined in §§ 5, 6 and 7 of Recommendation V.54 are further explained in this Annex by means of state diagrams.

In order to facilitate understanding of these diagrams the following information is provided.

A.2 *Location*

The loop device is considered to be functionally located between the DTE and the remaining part of the DCE.

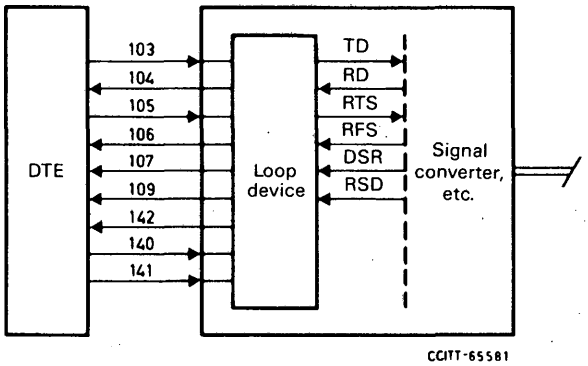


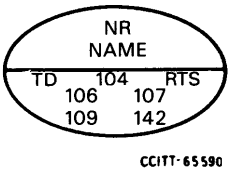
FIGURE A-1/V.54

During the data phase (i.e. no test loops applied), the following relations exist:

TD	(transmitted data)	= 103;
RD	(received data)	= 104;
RTS	(request to send)	= 105;
RFS	(ready for sending)	= 106;
DSR	(data set ready)	= 107;
RSD	(data channel received line signal detector)	= 109.

A.3 *Legend*

A.3.1 *States*



NR	State Number, with:
	LC = Loop Condition
	TL = Timing Loop;
NAME	State name;
TD	Signal on circuit TD to signal converter;
104	Signal on circuit 104 to DTE;
RTS	Signal on circuit RTS to signal converter;
106	Signal on circuit 106 to DTE;
107	Signal on circuit 107 to DTE;
109	Signal on circuit 109 to DTE;
142	Signal on circuit 142 to DTE.

A.3.2 *Signals*

"1"	Steady binary one;
OFF	Continuous OFF (="1");
ON	Continuous ON (="0");
PREP	Preparatory pattern;
ACK	Acknowledgement pattern;
TERM	Termination pattern;
103	Follows circuit 103 from DTE;
RD	Follows circuit RD from signal converter;
105	Follows circuit 105 from DTE;
RFS	Follows circuit RFS from signal converter;
DSR	Follows circuit DSR from signal converter;
RSD	Follows circuit RSD from signal converter.

A.3.3 *Events*

14n ON	OFF to ON transition on circuit 14n;
14n OFF	ON to OFF transition on circuit 14n;
Peripheral	Valid in peripheral DCE;
intermed.	Valid in intermediate DCE;
nnnn	After nnnn bit intervals;
XXX rec.	Recognition of pattern XXX;
Own address	Recognition of unique DCE address sequence;
Other address	Recognition of other address sequence;
RSD OFF 1s	Circuit RSD OFF for 1 second.

A.4 *Examples*

In the lower half of the state symbols, the condition of all interchange circuits that originate in the loop device are given in the order:

- TD (to signal converter);
- 104 (to DTE);
- RTS (to signal converter);
- 106 (to DTE);
- 107 (to DTE);
- 109 (to DTE); and
- 142 (to DTE).

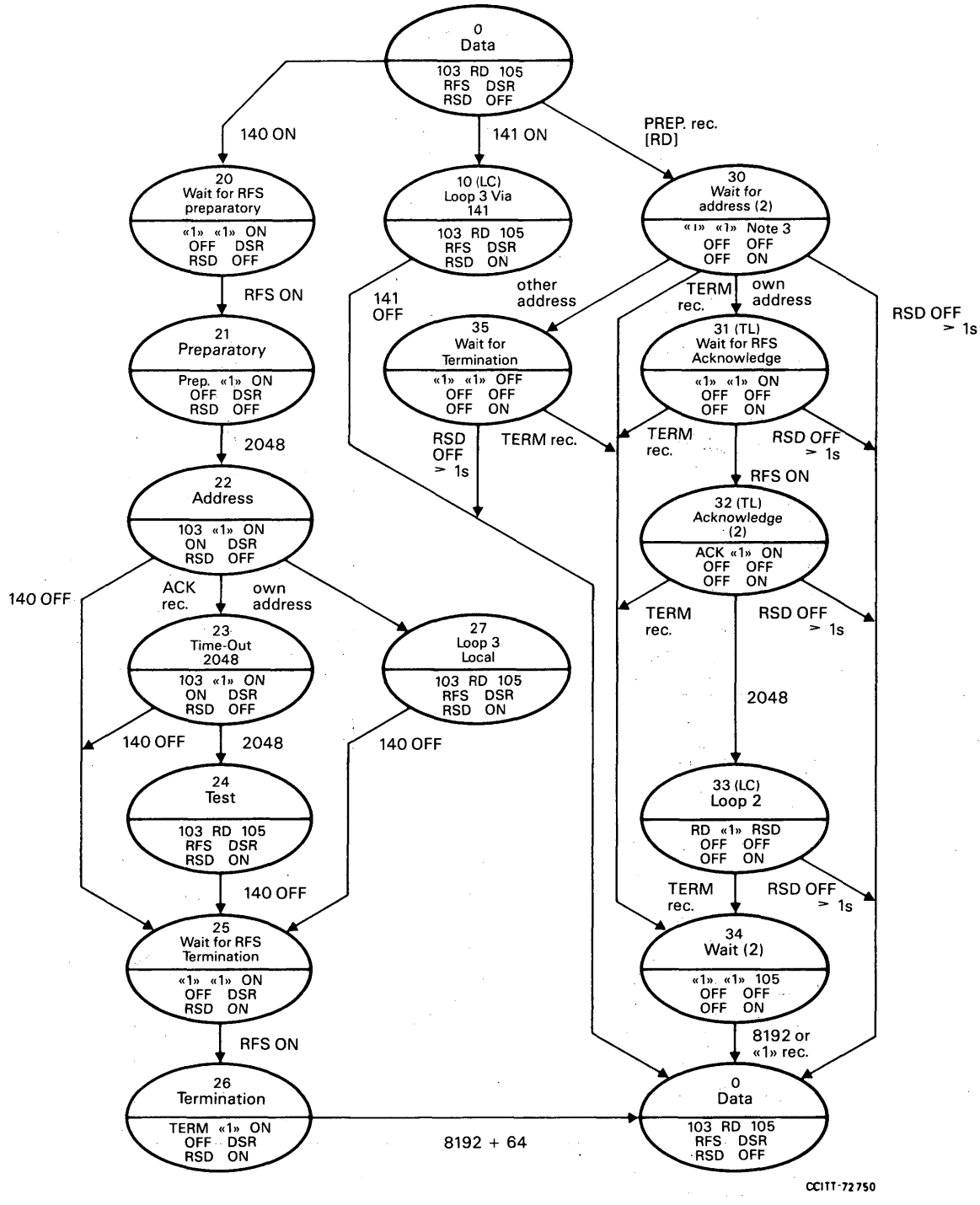
For example:

"RD" in the first position means that circuit TD to the signal converter is connected inside the loop device to RD from the signal converter.

"ACK" in the second position means that the acknowledgement pattern is transmitted on circuit 104.

"OFF" in the third position means that circuit RTS to the signal converter is kept in the OFF condition.

"RFS" in the fourth position means that circuit 106 to the DTE follows circuit RFS from the signal converter.



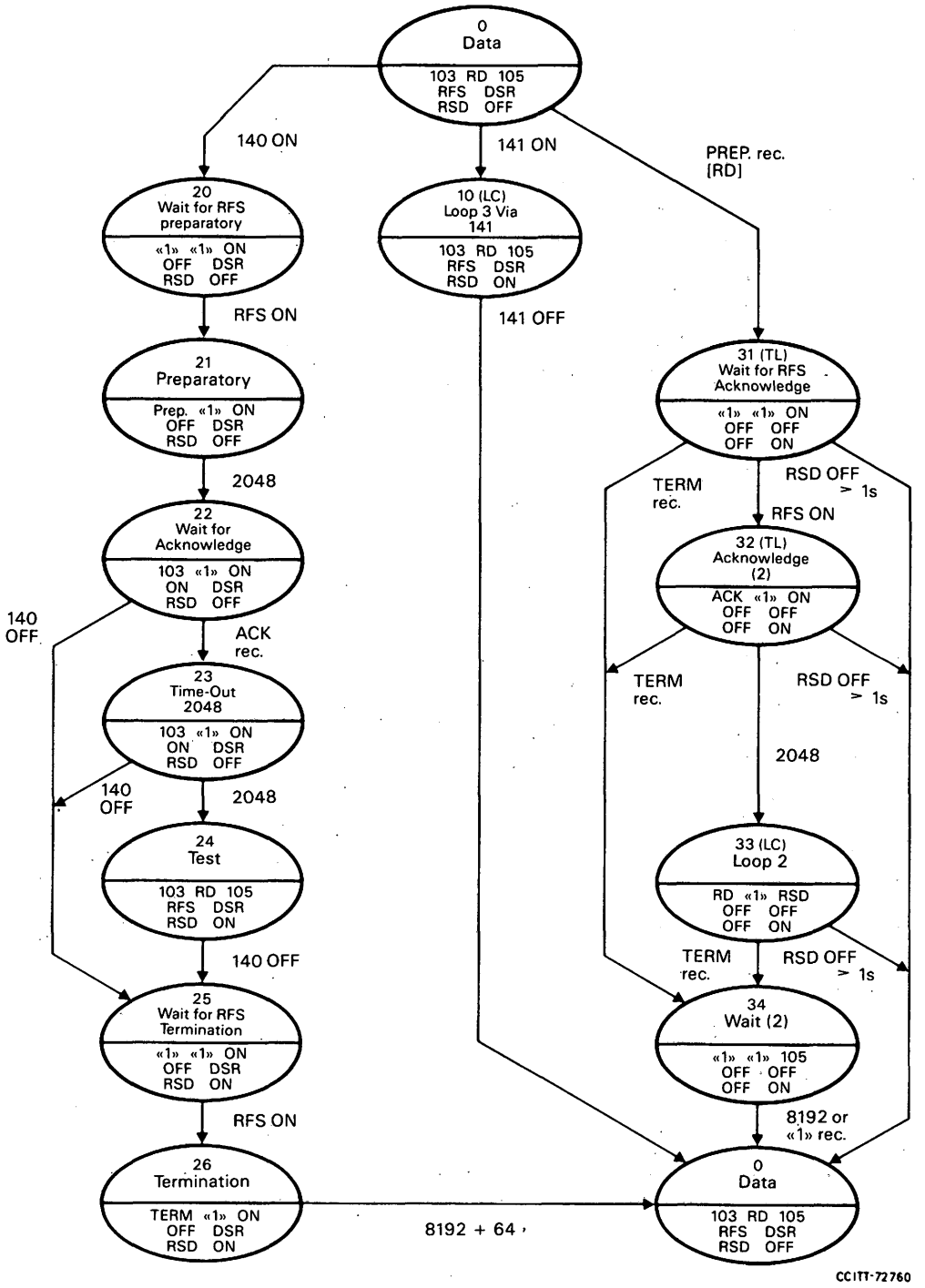
Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 30.

Note 3 - The condition of circuit RTS in state 30 may depend on the actual configuration. Normally circuit RTS will remain unchanged when moving from state 0 to state 30.

FIGURE A-2/V.54

State diagram for simple multipoint circuits

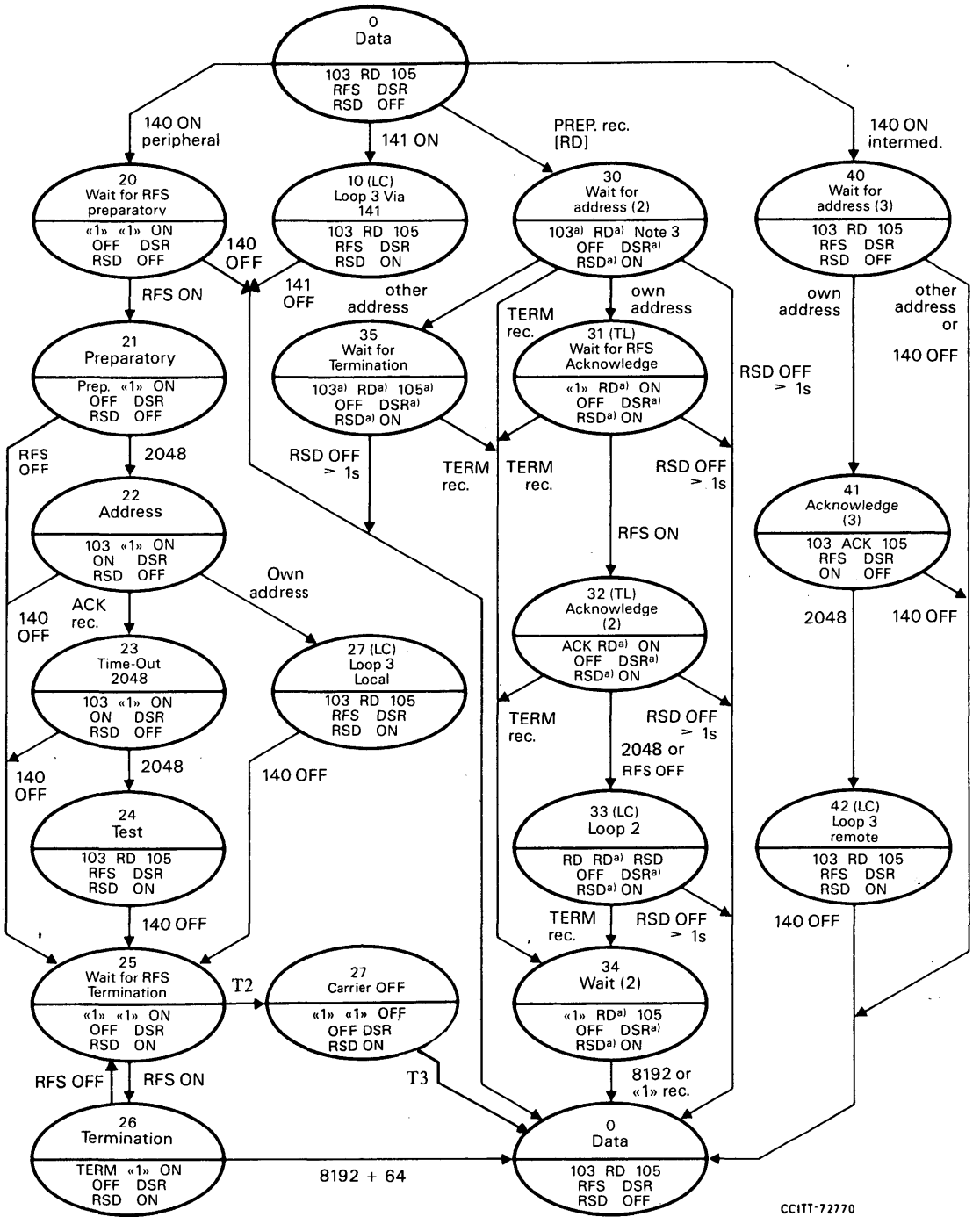


Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 31.

FIGURE A-3/V.54

State diagram for point-to-point circuits



a) Not clamped in intermediate DCE; clamped («1» or OFF) in peripheral DCE.

Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 30.

Note 3 - The condition of circuit RTS in state 30 may depend on the actual configuration. Normally circuit RTS will remain unchanged when moving from state 0 to state 30.

Note 4 - Where interconnection of circuit 109 in DCE I1 to circuit 105 in DCE I2 is possible, during Loop 2 the same condition as in peripheral DCE B is permitted on the interface.

Note 5 – Timer T2 is turned on at first entry of state 25 and turned OFF on exit of state 26.

Note 6 – Timer T3 is turned on at entry of state 27.

FIGURE A-4/V.54

State diagram for tandem circuits

Reference

[1] CCITT Recommendation *Influence of national systems on stability, talker echo and listener echo in international connections*, Vol. III, Rec. G.122.

Recommendation V.55

SPECIFICATION FOR AN IMPULSIVE NOISE MEASURING INSTRUMENT FOR TELEPHONE-TYPE CIRCUITS

(For the text of this Recommendation, see Recommendation O.71, Volume IV, Fascicle IV.4.)

Recommendation V.56

COMPARATIVE TESTS OF MODEMS FOR USE OVER TELEPHONE-TYPE CIRCUITS

(Geneva, 1972; amended at Geneva, 1976 and 1980, Malaga-Torremolinos, 1984 and at Melbourne, 1988)

To facilitate the work of Administrations in making comparative tests of modems for use over telephone-type circuits offered by different manufacturers, it is recommended that the tests should be made in the laboratory under the following operating conditions:

1 List of test parameters (see Table 1/V.56)

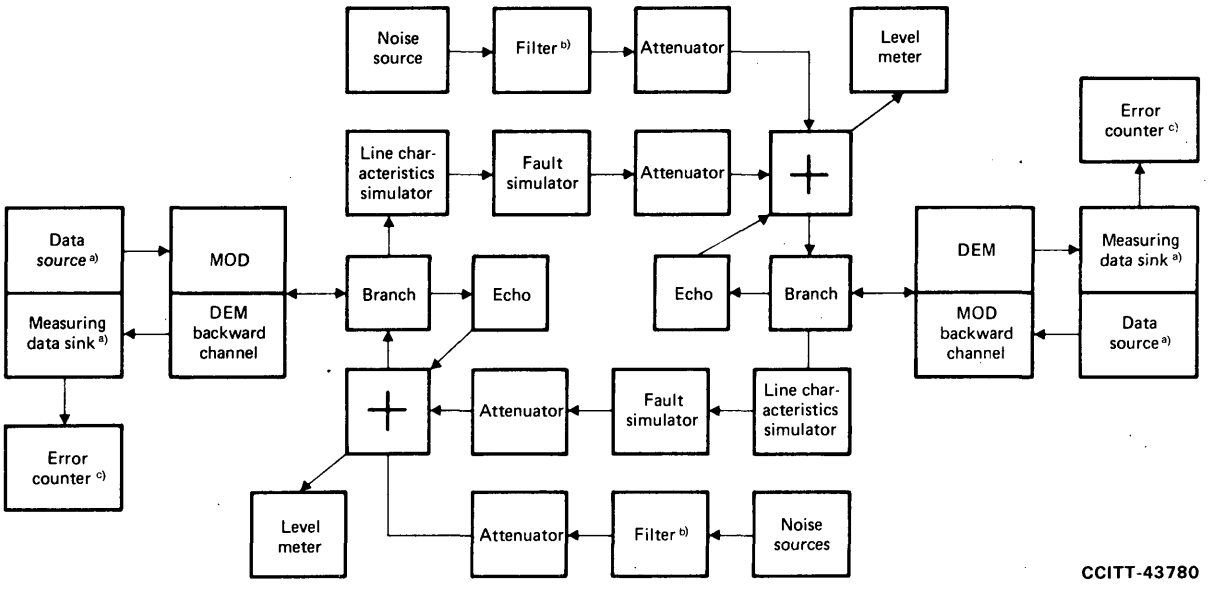
TABLE 1/V.56

Test parameters

Ref. No.	Parameter	Four-wire point-to-point	Two-wire switched network	
			Serial modems	Parallel modems
1	Total attenuation or receiving signal level	X	X	
2	Attenuation distortion	X	X	
3	Envelope or group delay distorsion	X	X	
4	Frequency shift (or offset)	X	X	
5	Sudden changes of attenuation	X	X	
6	Interruptions	X	X	
7	Phase hits	X	X	
8	Phase jitter	X	X	
9	Harmonic distortion	X	X	X
10	Listener echo		X	
11	"White" noise	X	X	
12	Impulsive noise	X	X	
13	Single tone interference		X	

2 Block diagram for standard test measuring set-up

It is proposed that comparative tests be made using either all or parts of the measuring set-up shown in Figure 1/V.56.



a) 511-bit pseudo random text.
b) 300-3400-Hz band pass filter; the filter is left out if impulsive noise in the form of a square wave is used.
c) For bit and block error count, see Recommendation V.52.

FIGURE 1/V.56

Measuring set-up for the standard tests of modems

3 Test parameters

3.1 *Parameters of the line characteristics simulator*

3.1.1 *Symmetric line distortion*

See Tables 2/V.56 and 3/V.56. The tolerances for all values are ± 5%.

3.1.2 *Asymmetric line distortion*

See Tables 4/V.56 and 5/V.56. The tolerances for all values are ± 5%.

3.1.3 *Ripple distortion*

The ripple distortion is within the tolerance scheme of Recommendation M.1020 [1]. See Tables 6/V.56 and 7/V.56. The tolerances for all values are ± 5% ± 0.1 ms.

TABLE 2/V.56

Frequency (Hz)	Attenuation distortion (dB)		
	Mode 1 (see Note 1)	Mode 2 (see Note 2)	Mode 3 (see Note 5)
300	6	12	K_1 [b]
500	3	8	0.35 K_1
800	1	2 [a]	0
≈ 1600	0	0	0
2500	Unspecified	8	0.2 K_1
2800	3	Unspecified	0.3 K_1
3000	6	12	0.4 K_1

[a] To be clarified.

[b] K_1 is a multiplier with values 1, 2, 3, 4, 5, 6 and 7.

TABLE 3/V.56

Frequency (Hz)	Group-delay distortion (ms)		
	Mode 1 (see Note 1)	Mode 2 (see Note 2)	Mode 3 (see Note 5)
500	3	4.5	1.20 K_1 [a]
600	1.5	3	0.90 K_1
1000	0.5	1.5	0.32 K_1
≈ 1800	0	0	0
2600	0.5	1.5	0.12 K_1
2800	3	3	0.23 K_1
2900	Unspecified	4	0.31 K_1
3000	Unspecified	Unspecified	0.40 K_1

[a] K_1 is a multiplier with values 1, 2, 3, 4, 5, 6 and 7.

TABLE 4/V.56

Frequency (Hz)	Attenuation distortion (dB)		
	Mode 1 (see Note 1)	Mode 2 (see Note 2)	Mode 3 (see Note 5)
800	0	0	0
2000	0.75	Unspecified	Unspecified
2500	Unspecified	8	8 K_2[a]
2800	3	Unspecified	Unspecified
3000	6	12	12 K_2

[a] K_2 is a multiplier with values 0.4, 0.8, 1.2 and 1.6.

TABLE 5/V.56

Frequency (Hz)	Group-delay distortion (ms)		
	Mode 1 (see Note 1)	Mode 2 (see Note 2)	Mode 3 (see Note 5)
500	0	0	0
1900	Unspecified	Unspecified	0.075 K_3[a]
2600	0.5	1.5	Unspecified
2800	3	3	0.225 K_3
2900	Unspecified	4	Unspecified
3000	Unspecified	Unspecified	0.30 K_3

[a] K_3 is a multiplier with values 0.5, 1, 2, 4 and 8. All values of Mode 3 are provisional.

TABLE 6/V.56

Frequency (Hz)	Group-delay distorsion (ms)
	Mode 1
500	2.0
600	1.3
1000	0 (see Note 3)
1400	0.5 (see Note 4)
1800	0 (see Note 3)
2200	0.5 (see Note 4)
2600	0.3 (see Note 3)
2800	2.0

TABLE 7/V.56

Frequency (Hz)	Group-delay distorsion (ms)
	Mode 2
500	2.0
600	0,8
800	0.8 (see Note 4)
1000	0 (see Note 3)
1200	0.5 (see Note 4)
1400	0 (see Note 3)
1600	0.5 (see Note 4)
1800	0 (see Note 3)
2000	0.5 (see Note 4)
2200	0 (see Note 3)
2400	0.5 (see Note 4)
2600	0.3 (see Note 3)
2800	2.0

Notes to Tables 2/V.56 to 7/V.56

Note 1 – Mode 1 is in conformity with Recommendation M.1020 [1].

Note 2 – Mode 2 is in conformity with Recommendation M.1025 [2].

Note 3 – Ripple valley values (minima).

Note 4 – Ripple peak values (maxima).

Note 5 – Mode 3 is in conformity with the relevant European specifications.

3.2 *Parameters of the fault simulator*

a) Phase hits: with external control of timing (e.g. 0.25; 1; 100 Hz) adjustable continuously or in steps up to 165 degrees.

b) Frequency shifts e.g. ± 5 Hz, ± 6 Hz or ± 10 Hz by means of channel converters.

c) Peak-to-peak phase jitter from 0.2 degree to 30 degrees continuously from 50 to 300 Hz, sinusoidal waveform.

d) Sudden changes of attenuation: with external control of timing (e.g. 0.1; 0.25; 1; 100 Hz) adjustable continuously or in steps up to total attenuation.

e) Interruptions: with fixed duration of 1 ms and repetition period of 1s and/or with single interruptions with variable duration.

3.3 *Noise sources* (this subject needs further study)

a) White noise.

b) Impulsive noise: with adjustable level and adjustable pulse duration between 100 μs and 1 ms and with repetition period of 1 second.

c) Statistically distributed noise by recording or by simulation which is information to assist in standardizing a "Random noise simulator" which would encourage the utilization of block error counts.

d) Single tone interference: with adjustable level of an additional signal frequency, variable between 300 and 3100 Hz.

e) Harmonic distortion:

i) using a calibrating signal frequency of 700 Hz with the same r.m.s. level as the data signal and with its adjustable harmonic levels: a_{H2}, a_{H3} and a_{H4}, and

ii) using a calibrating signal frequency of 700 Hz with the same peak-to-peak level as the data signal and with its adjustable harmonic levels: a_{H2}, a_{H3} and a_{H4}.

3.4 *Listener echo*

Listener echo: with the variable echo attenuation between 0 and 20 dB and variable echo time delay τ_E between 0 and 20 ms (worst case relevant).

4 Measuring procedure

4.1 *Measurement of the bit error rate* (p_S) *as a function of the signal-to-noise ratio* (S/N) *in the case of white noise*

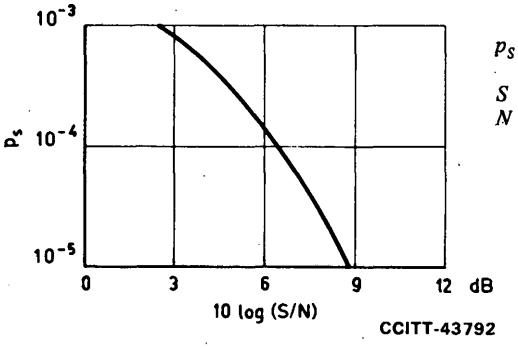
The receiving level at the summation point should be −30 dBm for switched line comparisons and −20 dBm for leased line comparisons.

For a comparison, the value of S/N ratio at defined p_S values can be ascertained (e.g. $3 \cdot 10^{-4}$ or 10^{-5}).

4.2 *Measurement of the number of the bit error per second* (F/t) *as a function of the different faults and noise parameters* (X)

The receiving level at the summation point should be −30 dBm for switched line comparisons and −20 dBm for leased line comparisons.

For a comparison, the value of F/t for different defined fault and noise parameters, or the value of the different parameters at the limit of the error-free region, can be ascertained.

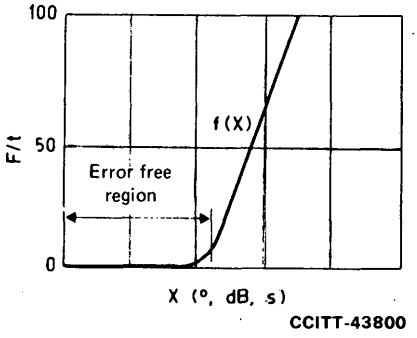


$p_S = f\,(S/N) = \dfrac{\text{error bits}}{\text{transmitted bits}}$

S = signal level
N = noise level

FIGURE 2/V.56

Example of bit error rate as a function of the signal-to-noise ratio



$F/t = f(X)$

$X = \Phi_S, \Phi_j, a_S, t_i, a_p, a_t, a_H$

Φ_S = f(degree of the phase hits)
Φ_j = degree of phase jitter
a_S = relative level of the sudden changes of attenuation
t_i = duration of interruptions
a_p = impulsive noise level (dBm)
a_t = single tone level (dBm)
$a_{H_2}, a_{H_3}, a_{H_4}$ = level of the harmonics below H_1 (dB)

FIGURE 3/V.56

Example of bit error per second as a function of the value of different fault and noise parameters

5 **Comparative tests of modems** (Table 8/V.56)

TABLE 8/V.56

Eighteen selected tests according to §§ 1, 2, 3 and 4

Test	Test parameter according to Table 1/V.56	Test parameters according to §	Measuring procedure according to §
A	11	3.3a)	4.1
B	2, 3, 11	3.1.1 mode 1, 3.3a)	4.1
C	2, 3, 11	3.1.1 mode 2, 3.3a)	4.1
D	2, 3, 11	3.1.2 mode 1, 3.3a)	4.1
E	2, 3, 11	3.1.2 mode 2, 3.3a)	4.1
F	2, 3, 4, 11	3.1.1 mode 1, 3.2b) (± 6 Hz), 3.3.a)	4.1
G	2, 3, 4, 11	3.1.1 mode 2, 3.2b) (± 10 Hz), 3.3.a)	4.1
H	2, 3, 7	3.1.1 mode 1, 3.2a)	4.2
J	2, 3, 7	3.1.1 mode 1, 3.2a)	4.2
K	8	3.2c)	4.2
L	2, 3, 5	3.1.1 mode 1, 3.2d)	4.2
M	2, 3, 5	3.1.1 mode 2, 3.2d)	4.2
N	6	3.2e)	4.2
P	12	3.3b)	4.2
R	13	3.3d)	4.2
S	9	3.3c) ii)	4.1
T	10, 11	3.4, 3.3a)	4.1
U	Statistic noise	3.3c)	4.1 (for block errors)

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with basic bandwidth conditioning*, Vol. IV, Rec. M.1025.

COMPREHENSIVE DATA TEST SET FOR HIGH DATA SIGNALLING RATES

(Geneva, 1972; amended at Geneva, 1980,
Malaga-Torremolinos, 1984)

(Replaced by Recommendation O.153, Melbourne, 1988; see Volume IV.4, Fascicle IV.4 of the Blue Book.)

SECTION 6

INTERWORKING WITH OTHER NETWORKS

Recommendation V.100

INTERCONNECTION BETWEEN PUBLIC DATA NETWORKS (PDNs) AND THE PUBLIC SWITCHED TELEPHONE NETWORKS (PSTN)

(Malaga-Torremolinos, 1984)

The CCITT,

considering that

(a) a data station may have an ingoing or outgoing access to a packet switched public data network (PSPDN) via the national[1] PSTN;

(b) the transmission characteristics of the data station may not be known at the PSPDN access level;

(c) in this case, the transmission characteristics have to be negotiated between modems before establishing the connection;

(d) half-duplex modems as well as full duplex modems may be used;

proposes

that Administrations may optionally introduce the following handshaking procedures including the types of modems to be supported.

1 Procedure description

According to the type of modem (see Table 1/V.100), a half-duplex or a duplex procedure is used.

1.1 *Half-duplex procedure*

See Figure 1/V.100.

1.1.1 *Answer mode modem*

a) Following the transmission of the answer sequence in accordance with Recommendation V.25, the modem shall apply an ON condition to circuit 107, and then transmit a segment S1 in accordance with Table 1/V.100 for 294 ms. Interchange circuits 106 and 109 are in the OFF condition during the procedure.

b) The modem remains silent until it detects S2 (defined in Table 1/V.100) or the synchronizing signals of a V.27 *ter* modem in the fallback mode.

c) Then the modem conditions itself to the selected mode or disconnects.

If no response is detected within 2 seconds following the end of the S1 transmission, the modem resumes transmitting S1.

---

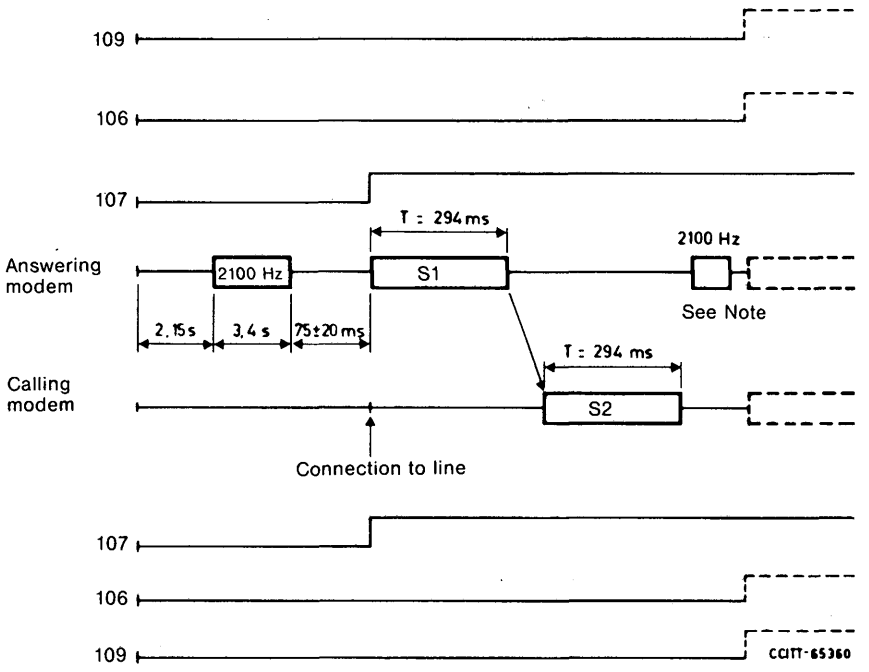
[1] International access to a PSPDN via PSTN is not envisaged.

TABLE 1/V.100

S2 and S1 signals

Categories	Data rate (bit/s)	Recommendation	Procedure	S2 (Calling DCE)	S1 (Answering DCE)
Duplex asynchronous	300	V.21	Duplex	980 Hz	1650 Hz
	1200	V.22	Duplex	1200 Hz	1800 + 2250 Hz
Duplex synchronous (FDM)	1200	V.22	Duplex	1200 Hz	1800 + 2250 Hz
	2400	V.22 *bis*	Duplex	1200 Hz	1800 + 2250 Hz
Duplex synchronous (ECT) [a]	2400	V.26 *ter*	Half-duplex	(See V.26 *ter*)	(See V.26 *ter*)
	4800	V.32	Duplex	(See V.32)	(See V.32)
	9600	V.32	Duplex	(See V.32)	(See V.32)
Half-duplex synchronous	2400	V.27 *ter* (fallback mode)	Half-duplex	None	None
	4800	V.27 *ter*	Half-duplex	1400 Hz	2200 Hz
	9600	(Under study)	Half-duplex	1100 Hz	2300 Hz
Asymmetric asynchronous	75/1200	V.23	Duplex	390 Hz	1300 Hz

[a] ECT = echo cancellation technique.



Note – The 2100 Hz tone is transmitted to disable the echo suppressors in case of duplex transmission (see Recommendation V.26 *ter*). For half-duplex transmission, this tone is not mandatory.

FIGURE 1/V.100

Half-duplex procedure

If S2 indicates a capability not available, the modem shall disconnect from the line.

If S2 indicates a capability available, the modem conditions itself to this mode.

d) After the end of reception of S2, in the case of a duplex modem (see V.26 *ter*), in accordance with Recommendation G.164, the modem transmits a 2100 ± 15 Hz tone for 500 ± 50 ms to disable echo suppressors, then remains silent for 75 ± 20 ms.

Note – In the case of half-duplex modems, the transmission of the 2100 Hz tone is not needed.

1.1.2 *Call mode modem*

a) After connection to line, the modem shall apply an ON condition to circuit 107 (interchange circuits 106 and 109 are in the OFF condition during the procedure). The modem keeps silent during at least 400 ms.

During this period, it detects S1.

The calling modem selects a mode of interworking in accordance with S1 or its nominal one.

b) Then, it transmits S2 in accordance with Table 1/V.100 or the synchronizing signals of a V.27 *ter* modem in the fallback mode at 2400 bit/s.

c) Then, it conditions itself to the selected capability.

1.2 *Duplex procedure*

See Figure 2/V.100.

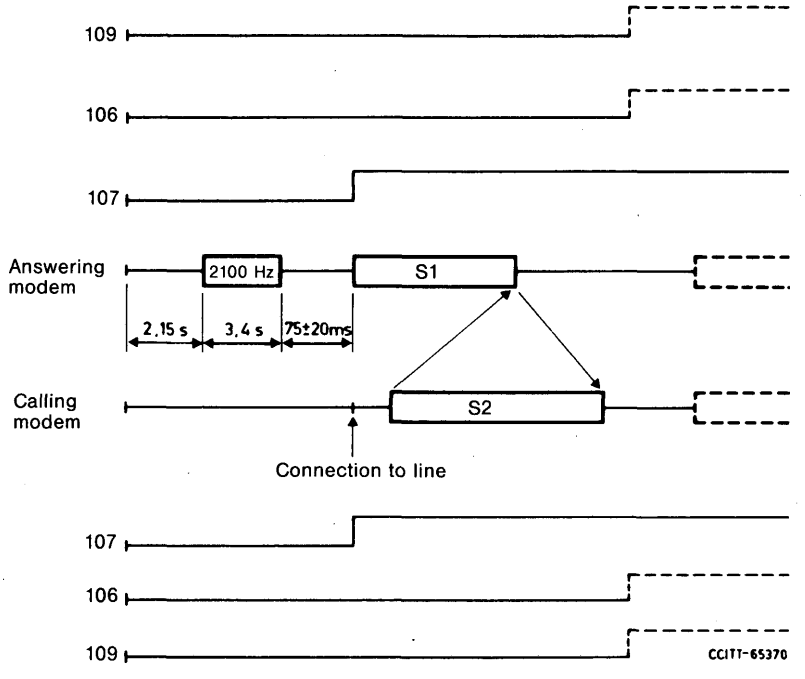


FIGURE 2/V.100
Duplex procedure

1.2.1 *Answer mode modem*

a) Following the transmission of the answer sequence in accordance with Recommendation V.25, the modem shall apply an ON condition to circuit 107 (interchange circuits 106 and 109 are in the OFF condition during the procedure.

b) Then, the modem transmits a segment S1 in accordance with Table 1/V.100 at least 40 ± 10 ms and until it has detected the end of transmission of S2.

Note – During this period, some exchanges may occur between the two modems according to the Series V Recommendation concerned (see Recommendation V.32).

If no response is detected within a time period (under study), the modem shall disconnect from line.

If S2 indicates a capability not available, the modem shall disconnect from the line.

If S2 indicates a capability available, the modem conditions itself to this mode.

1.2.2 *Call mode modem*

a) In accordance with Recommendation V.25, after detection of the 2100 Hz tone and a silent period of 75 ± 20 ms, the modem shall apply an ON condition to circuit 107 (interchange circuits 106 and 109 are in the OFF condition during the procedure).

b) The modem detects S1.

The calling modem selects a mode of interworking in accordance with S1 or its nominal one.

c) Then, it transmits S2 in accordance with Table 1/V.100.

Note – If the modem has only one possibility, it may transmit S2 after being connected to line.

d) Then, it conditions itself to the selected capability.

2 Combined half and duplex procedure

This section describes the interworking between a DCE having the capability of handling the two procedures [referrd to as two procedures (TP)modem] and DCEs having only one procedure.

2.1 *Interworking with half-duplex procedure*

2.1.1 *TP modem in the answering mode*

See Figure 3/V.100.

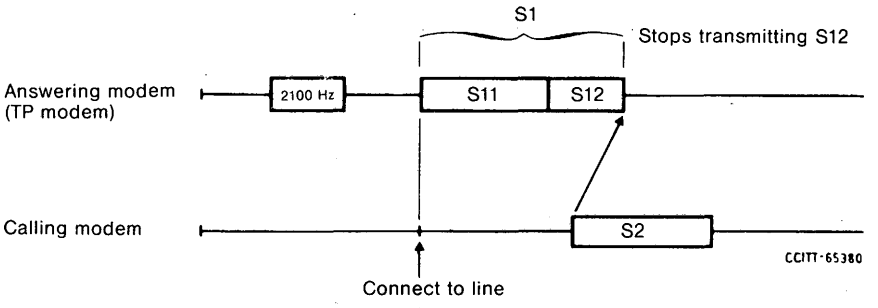


FIGURE 3/V.100
TP modem answer mode

2.1.1.1 *Answer TP modem*

a) After the V.25 sequence, the modem will transmit S1 which is composed of two segments S11 and S12 (as described in Appendix I to Recommendation V.32).

S11 is a modulated signal transmitted during 294 ms in a 600-3000 Hz bandwidth, S12 is a tone out of the 600-3000 Hz band.

b) After the transmission of S12, the modem is waiting for S2. When it detects S2, it stops transmitting S12 and proceeds with the half-duplex procedure.

2.1.1.2 *Calling modem*

The calling modem shall proceed with the half-duplex procedure taking into account that S12 is an out-of-band signal.

2.1.2 *TP modem in the calling mode*

See Figure 4/V.100.

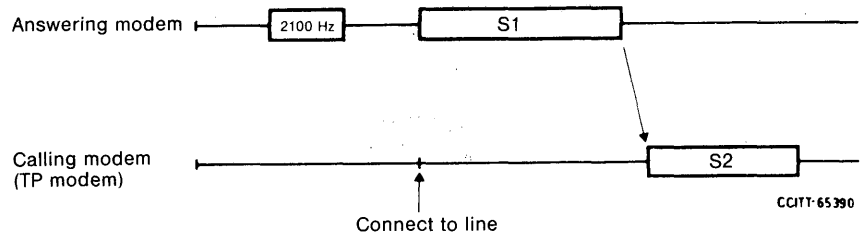


FIGURE 4/V.100

TP modem callmode

2.1.2.1 *Answering modem*

The answering modem shall proceed with the half-duplex procedure.

2.1.2.2 *Calling TP modem*

The calling TP modem after the V.25 sequence and connection to line remains silent. It detects S1 and shall proceed with the half-duplex procedure.

2.2 *Interworking with duplex procedure*

2.2.1 *TP modem in the answering mode*

See Figure 5/V.100.

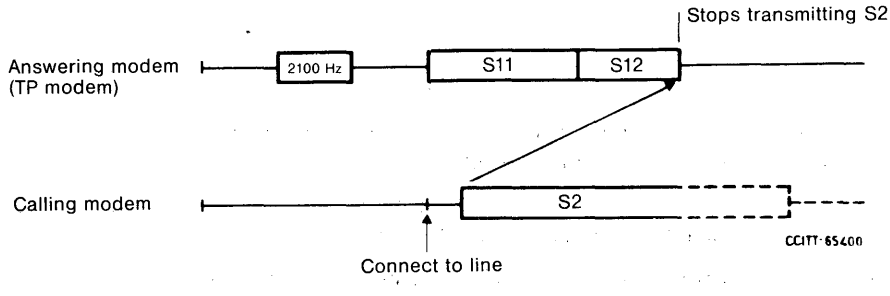


FIGURE 5/V.100

TP modem answer mode

2.2.1.1 *Answering TP modem*

The modem proceeds as in § 2.1.1.1 except that after detection of S2, it shall follow the duplex procedure.

2.2.1.2 *Calling modem*

The calling modem shall proceed with the duplex procedure.

2.2.2 *TP modem in the calling mode*

See Figure 6/V.100.

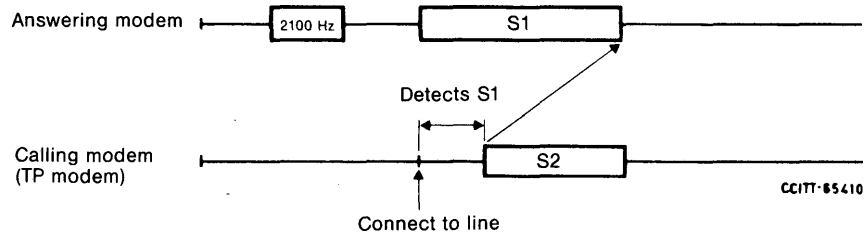


FIGURE 6/V.100
TP modem call mode

2.2.2.1 *Answering modem*

The answering modem shall proceed with the duplex procedure.

2.2.2.2 *Calling TP modem*

The calling TP modem after the V.25 sequence and connection to line remains silent. It detects S1 and shall proceed with the duplex procedure.

Recommendation V.110 [1)]

SUPPORT OF DATA TERMINAL EQUIPMENTS (DTEs) WITH V-SERIES TYPE INTERFACES BY AN INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

The CCITT,

considering

(a) that the ISDN will offer the universal interfaces to connect subscriber terminals according to the reference configuration described in Recommendation I.411;

(b) that during the evolution of ISDN however there will exist for a considerable period DTEs with V-series type interfaces which have to be connected to the ISDN;

(c) that bearer services supported by an ISDN are described in Recommendation I.211;

(d) that the D-channel signalling protocol is described in Recommendations I.430, I.441/Q.921 and I.451/Q.931;

---

1) This Recommendation is also included in the Recommendations of the I-Series under the number I.463.

unanimously declares the view

(1) that the scope of this Recommendation shall cover the connection of terminals with interfaces for modems conforming to current V-Series Recommendations on the ISDN operating in accordance with circuit switched or leased circuit services;

(2) that the following circuit switched service capabilities shall be supported:

- data transmission, (or)
- alternate speech/data transmission, (and/or)
- automatic calling and/or automatic answering;

(3) that the reference configurations of § 1 shall apply;

(4) that the support of interworking of TEs on an ISDN with DTEs on other types of networks, e.g. PSTN, is described in the Recommendation I.500 Series;

(5) that the terminal adaptor (TA) functions necessary to support the connection of DTEs with V-series type interfaces on an ISDN, shall include the following:

- conversion of electrical and mechanical interface characteristics;
- bit rate adaptation;
- end-to-end synchronization of entry to and exit from the data transfer phase;
- call establishment and disestablishment based on either manual or automatic calling and/or automatic answering.

1 Reference configurations

1.1 *Terminal adaptor reference model*

The terminal adaptor functions have been defined in the context of a simple reference model. Annex A describes the reference model in further detail, and defines a basic terminal adaptor TA-A, and an autocalling/autoanswering terminal adaptor TA-B.

1.2 *Connection types*

The terminal adaptor functions described in this Recommendation take into account interworking between TAs of different types, e.g. V-Series TE2 with X.21 TE2, and end-to-end connections of different types. These are described in further detail in Annex A.

2 Line signals at S and T reference points

The TA signals at ISDN reference points S or T shall be in conformance with the characteristics of an ISDN's "Basic user/network interface" as described in Recommendation I.430 (Layer 1 specification), I.441/Q.921 (Layer 2 specification) and I.451/Q.931 (Layer 3 specification).

2.1 *Bit rate adaptation of synchronous data signalling rates up to 19.2 kbit/s*

2.1.1 *General approach*

The bit rate adaptation functions within the TA are shown in Figure 1/V.110. The functions RA1 converts the user data signalling rate to an appropriate intermediate rate expressed by $2^k \times 8$ kbit/s (where $k = 0$, 1 or 2). RA2 performs the second conversion from the intermediate rates to 64 kbit/s. The data signalling rates of 48 and 56 kbit/s are converted directly into the 64 kbit/s B channel rate.

2.1.2 *Adaptation of V-series data signalling rates to the intermediate rates*

The intermediate rate used with each of the V-series data signalling rates are shown in Table 1/V.110.

Note – The specific V-series data signalling rate(s) to be supported by an ISDN are for further study.

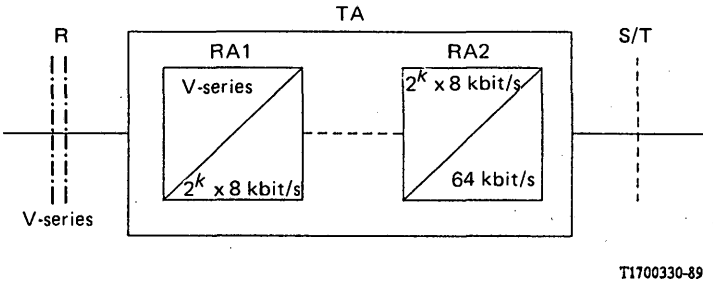


FIGURE 1/V.110

Two step bit rate adaptation

TABLE 1/V.110

First step rate adaptation

Data signalling rate (bit/s)	Intermediate rate		
	8 kbit/s	16 kbit/s	32 kbit/s
600	X		
1 200	X		
2 400	X		
4 800	X		
7 200		X	
9 600		X	
12 000			X
14 400			X
19 200			X

2.1.2.1 *Frame structure*

The frame structure is shown in Table 2/V.110 and is described in the following paragraphs.

As shown in Table 2/V.110, the conversion of the V-series rates to the intermediate rates uses an 80 bit frame. The octet zero contains all binary 0, whilst octet 5 consists of a binary 1 followed by seven E bits (see § 2.1.2.4). Octets 1-4 and 6-9 contain a binary 1 in bit number one, a status bit (S or X bit) in bit number 8 and six data bits (D bits) in bit positions 2-7. The order of bit transmission is from left to right and top to bottom.

TABLE 2/V.110

Frame structure

Octet number	Bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1	D2	D3	D4	D5	D6	S1
2	1	D7	D8	D9	D10	D11	D12	X
3	1	D13	D14	D15	D16	D17	D18	S3
4	1	D19	D20	D21	D22	D23	D24	S4
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D25	D26	D27	D28	D29	D30	S6
7	1	D31	D32	D33	D34	D35	D36	X
8	1	D37	D38	D39	D40	D41	D42	S8
9	1	D43	D44	D45	D46	D47	D48	S9

2.1.2.2 *Frame synchronization*

The 17-bit frame alignment pattern consists of all 8 bits (set to binary 0) of octet zero and bit one (set to binary 1) of the following nine octets (see also § 2.1.3).

2.1.2.3 *Status bits (S1, S3, S4, S6, S8, S9 and X)*

The bits S and X are used to convey channel control information associated with the data bits in the data transfer state, as shown in Table 3/V.110. The S-bits are put into two groups SA and SB, to carry the condition of two interchange circuits. The X-bit is used to carry the condition of circuit 106, and in addition, signals the state of frame synchronization between TAs. The X-bit can also be used optionally to carry flow control information between TAs supporting asynchronous terminal equipment. This usage is specified in § 2.4.2.

The use of S and X bits for synchronization of entry to and exit from the data transfer state is specified in § 4.

The mechanism for proper assignment of the control information from the transmitting signal rate adapter interface via these bits to the receiving signal rate adapter interface is shown in Table 3/V.110 and described in § 4.

For the S and X bits, a ZERO corresponds with the ON condition, a ONE with the OFF condition.

Control information, conveyed by the S bits, and user data, conveyed by the D bits, should not have different transmission delays. The S bits should therefore transmit control information sampled simultaneously with the D bits in the positions specified in Table 4/V.110 and as presented in Figure 2/V.110.

The X bit should be presented upon arrival to control circuit 106. Circuit 106 shall respond as defined in § 3.3 (X = ZERO, 106 = ON).

TABLE 3/V.110

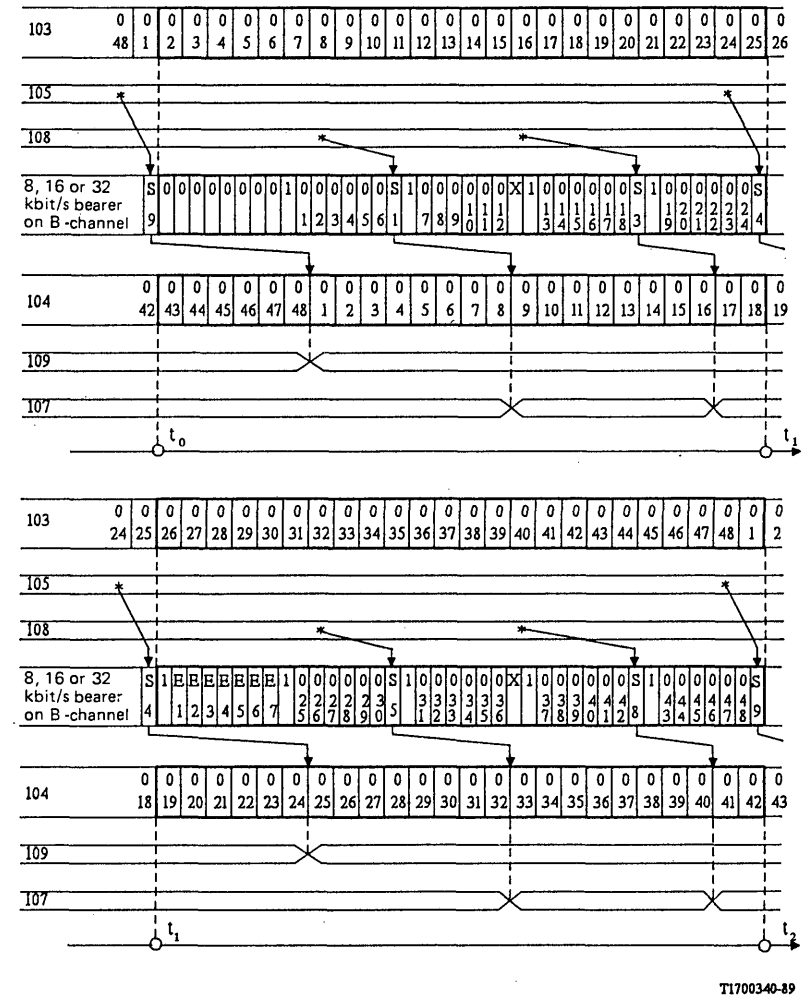
General mapping scheme

108 ----------	S1, S3, S6, S8 = SA	---------- 107
105 ----------	S4, S9 = SB	---------- 109
Frame synch and 106/IWF ----------	X	---------- 106

TABLE 4/V.110

Coordination between S bits and D bits

S bit	D bit	
	Octet No.	Bit No.
S1	2	3 (D8)
S3	3	5 (D16)
S4	4	7 (D24)
S6	7	3 (D32)
S8	8	5 (D40)
S9	9	7 (D48)



Note 1 – In order to maintain conformity with the bit rate adaptation of X.1 user classes of service described in Recommendation X.30 (I.461), the bits S1 and S6, S3 and S8, S4 and S9 are used to convey channel status information associated with the P, Q and R bit groups respectively.

Refer to § 2.1.1.2.3 of Recommendation X.30 (I.461) for detailed information concerning the mapping of the information on circuit C of the X.21 interface to the S bits and to the I bits of the distant interface.

Note 2 – The coordination between S and D bits described in Table 4/V.110 and Figure 2/V.110 is intended to provide for compatibility with Recommendation X.30 (I.461). Whether this coordination is strictly necessary in the context of Recommendation V.110 is for further study.

FIGURE 2/V.110

Coordination between S bits and D bits

2.1.2.4 *E-bit usage*

The E bits are used to carry the following information:

a) Rate repetition information: bits E1, E2 and E3, in conjunction with the intermediate rate (see Table 2/V.110), provide the user data signalling rate (synchronous) identification. The coding of these bits shall be as shown in Table 5/V.110.

b) Network independent clock information: bits E4, E5 and E6 are used as specified in § 5 to carry network independent clock phase information.

c) Multiframe information: bit E7 is used as indicated in Table 5/V.110.

TABLE 5/V.110

E-bit usage
(Note 1)

Intermediate rates kbit/s			E1	E2	E3	E4	E5	E6	E7
8	16	32		(Note 4)			(Note 3)		
bit/s	bit/s	bit/s							
600			1	0	0	C	C	C	1 or 0 (Note 2)
1200			0	1	0	C	C	C	1
2400			1	1	0	C	C	C	1
		12 000	0	0	1	C	C	C	1
	7200	14 400	1	0	1	C	C	C	1
4800	9600	19 200	0	1	1	C	C	C	1

Note 1 – The data signalling rates of 600, 2400, 4800 and 9600 bit/s are also Recommendation X.1 user classes of service (see also Recommendation X.30/I.461).

Note 2 – In order to maintain compatibility with Recommendation X.30 (I.461), the 600 bit/s user rate E7 is coded to enable the 4 × 80 bit multiframe synchronization. To this end, E7 in the fourth 80 bit frame is set to binary 0 (see § 2.1.2.7 and Table 6a/V.110).

Note 3 – C indicates the use of E4, E5 and E6 for the Transport of Network Independent blocking information (see § 5). These bits shall be set to ONE when unused.

Note 4 – Synchronous rate information is carried by bits E1, E2 and E3 as indicated. Asynchronous rate information must be provided with out-of-band signalling (Layer 3 messages in the D channel) or with In Band Parameter Exchange as described in Appendix 1.

2.1.2.5 *Rate negotiation*

Negotiation of the synchronous rate may be appropriate in interworking situations involving interconnections with modems on the PSTN where the remote modem/DTE has the capability of operating at different rates depending upon the conditions. It may also be appropriate in interconnections for asynchronous transmission specified in § 2.3 and accommodate split rate operation. The need for rate negotiation and the method is for further study.

2.1.2.6 *Data bits*

Data are conveyed in D bits, i.e., up to 48 bits per 80-bit frame. In this Recommendation the octet boundaries of the user's data stream are not defined.

2.1.2.7 *Bit assignment*

The adaptation of 600, 1200 and 2400 bit/s rates to the 8 kbit/s intermediate rate are shown in Tables 6a/V.110, 6b/V.110 and 6c/V.110, respectively.

The adaptation of 7200 and 14 400 bit/s rates to the 16 and 32 kbit/s intermediate rate, respectively, use the data bit assignments shown in Table 6d/V.110.

The adaptation of 4800, 9600 and 19 200 bit/s rates to the 8, 16 and 32 kbit/s intermediate rate, respectively, use the data bit assignments shown in Table 6e/V.110.

The adaptation of 12 000 bit/s user rate to 32 kbit/s intermediate rate use the data bit assignments shown in Table 6f/V.110.

TABLE 6a/V.110

Adaptation of 600 bit/s user rate to 8 kbit/s intermediate rate

0	0	0	0	0	0	0	0
1	D1	D1	D1	D1	D1	D1	S1
1	D1	D1	D2	D2	D2	D2	X
1	D2	D2	D2	D2	D3	D3	S3
1	D3	D3	D3	D3	D3	D3	S4
1	1	0	0	E4	E5	E6	E7 [a]
1	D4	D4	D4	D4	D4	D4	S6
1	D4	D4	D5	D5	D5	D5	X
1	D5	D5	D5	D5	D6	D6	S8
1	D6	D6	D6	D6	D6	D6	S9

[a] See Note 2 to Table 5/V.110.

TABLE 6b/V.110

Adaptation of 1200 bit/s user rate to 8 kbit/s intermediate rate

0	0	0	0	0	0	0	0
1	D1	D1	D1	D1	D2	D2	S1
1	D2	D2	D3	D3	D3	D3	X
1	D4	D4	D4	D4	D5	D5	S3
1	D5	D5	D6	D6	D6	D6	S4
1	0	1	0	E4	E5	E6	E7
1	D7	D7	D7	D7	D8	D8	S6
1	D8	D8	D9	D9	D9	D9	X
1	D10	D10	D10	D10	D11	D11	S8
1	D11	D11	D12	D12	D12	D12	S9

TABLE 6c/V.110

Adaptation of 2400 bit/s user rate to 8 kbit/s intermediate rate

0	0	0	0	0	0	0	0
1	D1	D1	D2	D2	D3	D3	S1
1	D4	D4	D5	D5	D6	D6	X
1	D7	D7	D8	D8	D9	D9	S3
1	D10	D10	D11	D11	D12	D12	S4
1	1	1	0	E4	E5	E6	E7
1	D13	D13	D14	D14	D15	D15	S6
1	D16	D16	D17	D17	D18	D18	X
1	D19	D19	D20	D20	D21	D21	S8
1	D22	D22	D23	D23	D24	D24	S9

TABLE 6d/V.110

Adaptation of N [a] × 3600 bit/s user rate to the intermediate rate

0	0	0	0	0	0	0	0
1	D1	D2	D3	D4	D5	D6	S1
1	D7	D8	D9	D10	F	F	X
1	D11	D12	F	F	D13	D14	S3
1	F	F	D15	D16	D17	D18	S4
1	1	0	1	E4	E5	E6	E7
1	D19	D20	D21	D22	D23	D24	S6
1	D25	D26	D27	D28	F	F	X
1	D29	D30	F	F	D31	D32	S8
1	F	F	D33	D34	D35	D36	S9

F = filling bit

[a] N = 2 or 4 only.

TABLE 6e/V.110

Adaptation of N [a] × 4800 bit/s user rate to the intermediate rate

0	0	0	0	0	0	0	0
1	D1	D2	D3	D4	D5	D6	S1
1	D7	D8	D9	D10	D11	D12	X
1	D13	D14	D15	D16	D17	D18	S3
1	D19	D20	D21	D22	D23	D24	S4
1	0	1	1	E4	E5	E6	E7
1	D25	D26	D27	D28	D29	D30	S6
1	D31	D32	D33	D34	D35	D36	X
1	D37	D38	D39	D40	D41	D42	S8
1	D43	D44	D45	D46	D47	D48	S9

[a] N = 1, 2 or 4 only.

TABLE 6f/V.110

Adaptation of 12 000 bit/s user rate to 32 kbit/s intermediate rate

0	0	0	0	0	0	0	0
1	D1	D2	D3	D4	D5	D6	S1
1	D7	D8	D9	D10	F	F	X
1	D11	D12	F	F	D13	D14	S3
1	F	F	D15	F	F	F	S4
1	0	0	1	E4	E5	E6	E7
1	D16	D17	D18	D19	D20	D21	S6
1	D22	D23	D24	D25	F	F	X
1	D26	D27	F	F	D28	D29	S8
1	F	F	D30	F	F	F	S9

F = Filling bit.

2.1.3 *Frame synchronization and additional signalling capacity*

2.1.3.1 *Search for frame synchronization*

The following 17-bit alignment pattern is used to achieve frame synchronization:

00000000 1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX
1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX

It is assumed that the error rate will be sufficiently low to expect frame synchronization following the detection of one 80-bit frame.

2.1.3.2 *Frame synchronization monitoring and recovery*

Monitoring of the frame synchronization shall be a continuous process using the same procedures as for initial detection.

Loss of frame synchronization shall not be assumed unless at least three consecutive frames, each with at least one framing bit error, are detected.

Following loss of frame synchronization, the TA shall enter a recovery state as discussed in § 4.1.5. If recovery is not successful, further maintenance procedures may be used.

2.1.4 *Adaptation of intermediate rates to 64 kbit/s*

Since rate adaptation of a single intermediate rate (e.g., 8, 16, or 32 kbit/s) to the 64 kbit/s B channel rate and the possible multiplexing of several intermediate rate streams[2] to the 64 kbit/s B channel rate must be compatible to enable interworking, a common approach is needed for the second step rate adaptation and, possibly, for intermediate rate multiplexing. This second step rate adaptation method is described in Recommendation I.460.

2.2 *Rate adaptation of 48 and 56 kbit/s user rates to 64 kbit/s*

The 48 and 56 kbit/s user data signalling rates are adapted to the 64 kbit/s B channel rate in one step as indicated in Tables 7a/V.110 and 7b/V.110 or 7c/V.110 respectively.

TABLE 7a/V.110

Adaptation of 48 kbit/s user rate to 64 kbit/s

Octet number	Bit number							
	1	2	3	4	5	6	7	8
1	1	D1	D2	D3	D4	D5	D6	S1
2	0	D7	D8	D9	D10	D11	D12	X
3	1	D13	D14	D15	D16	D17	D18	S3
4	1	D19	D20	D21	D22	D23	D24	S4

Note 1 – 48 kbit/s is also a Recommendation X.1 user class of service (see also Recommendation X.30/I.461, § 2.2.1).

Note 2 – Refer to § 2.1.2.3 for the use of status bits and bit X; however for international operation over restricted 64 kbit/s bearer capabilities, bit X must be set to binary 1.

[2] Multiplexing of several intermediate rate streams is for further study.

TABLE 7b/V.110

Adaptation of 56 kbit/s user rate to 64 kbit/s

Octet number	Bit number							
	1	2	3	4	5	6	7	8
1	D1	D2	D3	D4	D5	D6	D7	1
2	D8	D9	D10	D11	D12	D13	D14	1
3	D15	D16	D17	D18	D19	D20	D21	1
4	D22	D23	D24	D25	D26	D27	D28	1
5	D29	D30	D31	D32	D33	D34	D35	1
6	D36	D37	D38	D39	D40	D41	D42	1
7	D43	D44	D45	D46	D47	D48	D49	1
8	D50	D51	D52	D53	D54	D55	D56	1

TABLE 7c/V.110

Alternative frame structure for the adaptation of 56 kbit/s user rate to 64 bit/s

Octet number	Bit number							
	1	2	3	4	5	6	7	8
1	D1	D2	D3	D4	D5	D6	D7	0
2	D8	D9	D10	D11	D12	D13	D14	X
3	D15	D16	D17	D18	D19	D20	D21	S3
4	D22	D23	D24	D25	D26	D27	D28	S4
5	D29	D30	D31	D32	D33	D34	D35	1
6	D36	D37	D38	D39	D40	D41	D42	1
7	D43	D44	D45	D46	D47	D48	D49	1
8	D50	D51	D52	D53	D54	D55	D56	1

Note 1 – Refer to § 2.1.2.3 for the use status bits and bit X.

Note 2 – Table 7c/V.110 is a permitted option to provide for signalling to enter and to leave the data phase. However, the recommended approach shall be as in Table 7b/V.110 and the responsability shall be on the user of Table 7c/V.110 to insure that interworking can be achieved.

2.3 *Adaptation for asynchronous rates of up to 19 200 bit/s*

2.3.1 *General approach*

The bit rate adaptation functions within the TA are shown in Figure 3/V.110. A three-step method is employed with the functional blocks RA0, RA1, and RA2. The RA0 function is an asynchronous-to-synchronous conversion step, for support of the rates specified in Table 8/V.110, using the same technique as defined in Recommendation V.14. It produces a synchronous bit stream defined by $2^n \times 600$ bits (where $n = 0$ to 5). The functions RA1 and RA2 are the same as specified in § 2.1. Function RA1 adapts the user rate to the next higher rate expressed by $2^k \times 8$ bit/s (where $k = 0$, 1 or 2). RA2 performs the second conversion to 64 kbit/s.

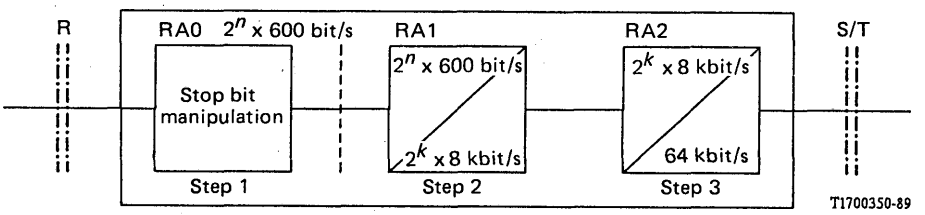


FIGURE 3/V.110

Three step rate adaption bit

2.3.2 *Supported asynchronous user rates*

The asynchronous user rates to be supported, mandatory and optional, are specified in Table 8/V.110.

TABLE 8/V.110

Asynchronous user rates

Data rate (bit/s)	Rate tolerance (%)	No. of data units	No. of stop elements	RA0/RA1 rate (bit/s)	RA1 rate (kbit/s)
50	± 2.5	5	1.5	600	8
75	± 2.5	5.7 or 8	1:1,5:2	600	8
110	± 2.5	7 or 8	1 or 2	600	8
150	± 2.5	7 or 8	1 or 2	600	8
200	± 2.5	7 or 8	1 or 2	600	8
300 *	± 2.5	7 or 8	1 or 2	600	8
600 *	+1 –2.5	7 or 8	1 or 2	600	8
1 200 *	+1 –2.5	7 or 8	1 or 2	1 200	8
2 400 *	+1 –2.5	7 or 8	1 or 2	2 400	8
3 600	+1 –2.5	7 or 8	1 or 2	4 800	8
4 800 *	+1 –2.5	7 or 8	1 or 2	4 800	8
7 200	+1 –2.5	7 or 8	1 or 2	9 600	16
9 600 *	+1 –2.5	7 or 8	1 or 2	9 600	16
12 000	+1 –2.5	7 or 8	1 or 2	19 200	32
14 400	+1 –2.5	7 or 8	1 or 2	19 200	32
19 200	+1 –2.5	7 or 8	1 or 2	19 200	32

Note 1 – * indicates rate whose support is mandatory for universal TA.

Note 2 – Number of data bits includes possible parity bits.

2.3.3 *Asynchronous-to-synchronous conversion (RA0)*

The RA0 function is only used with asynchronous V-series interfaces. Incoming asynchronous data is padded by the addition of stop elements to fit the nearest channel rate defined by $2^n \times 600$ bit/s. Thus, a 7200 bit/s user data signalling rate shall be adapted to a synchronous 9600 bit/s stream and a 110 bit/s user data signalling rate shall be adapted to synchronous 600 bit/s stream. The resultant synchronous stream is fed to RA1. Padding with stop elements is inhibited during the transmission of the break signal as described in § 2.3.5.

2.3.4 *Overspeed/underspeed*

A terminal adaptor shall insert additional stop elements when its associated terminal is transmitting with a lower than nominal character rate. If the terminal is transmitting characters with an overspeed of up to 1% (or 2.5% in the case of nominal speeds lower than 600 bit/s), the asynchronous-to-synchronous converter may delete stop elements as often as is necessary to a maximum of one every eight characters at 1% overspeed. The converter on the receiving side shall detect deleted stop elements and re-insert them in the received data stream (circuit 104).

The nominal length of the start elements and data units shall be the same for all characters. The length of the stop element may be reduced as much as 12.5% by the receiving converter for nominal speeds exceeding 300 bit/s to allow for overspeed in the transmitting terminal. For nominal speeds less than or equal to 300 bit/s, a 25% reduction in stop element is allowed.

2.3.5 *Break signal*

The terminal adaptor shall detect and transmit the break signal as follows:

If the converter detects M to 2M + 3 bits, all of start polarity, where M is the number of bits per character in the selected format including start and stop elements, the converter shall transmit 2M + 3 bits of start polarity.

If the converter detects more than 2M + 3 bits, all of start polarity, the converter shall transmit all these bits as start polarity.

For the cases where the asynchronous rate is lower than the synchronous rate for the converter, the following rules shall apply:

- the converter shall transmit start polarity (to RA1) for a time period equal to 2M + 3 bits at the asynchronous rate if the converter has detected M to 2M + 3 bits of start polarity;
- the converter shall transmit (to RA1) start polarity for a time period as long as the received break condition if the converter has detected more than 2M + 3 bits of start polarity;
- the 2M + 3 or more bits of start polarity received from the transmitting side shall be output to the receiving DTE;
- the DTE must transmit on circuit 103 at least 2M bits of stop polarity after the start polarity break signal before sending further data characters. The converter shall then regain character synchronism from the following stop to start transition.

2.3.6 *Parity bits*

Possible parity bits included in the user data are considered as data bits by the RA0 function.

2.4 *Flow control*

A flow control option, for use with TAs supporting asynchronous DTEs, is described in this section. Flow control allows the connection of asynchronous DTEs operating at different user data rates by reducing the character output of the faster to that of the slower. Support of flow control will require the use of end-to-end (TA-to-TA) protocol defined in § 2.4.2 and an incoming line (from network) buffer in addition to a selected local protocol (see § 2.4.1). Depending upon the local flow control protocol employed, there will also be a requirement for character buffering from the DTE interface. The size of this buffer is not defined in this Recommendation because it is dependent upon implementation.

Local flow control of the DTE interface is required where the DTE operates at a rate higher than the synchronous rate established between TAs. End-to-end flow control is required where the synchronous rate established between TAs is consistent with the operating rate of one DTE (or interworking unit) and higher than the synchronous rate consistent with the operating rate of the other DTE (or interworking unit). Both local and end-to-end flow control could be required in some applications.

2.4.1 *Local flow control: TA to DTE*

Connection may be made between TAs connected to asynchronous DTEs operating at two different speeds. It is the responsibility of the TA connected to the faster DTE to execute a local flow control protocol to reduce the character rate to that of the slower DTE. This operation will require some buffer storage in the TA. A TA may support several different local flow control protocols, although only one will be selected at any one time. There are a number of such protocols in use, some of which are detailed in the following text.

2.4.1.1 *105/106 operation*

This is an out-of-band flow control mechanism, utilizing two of the interchange circuits specified in V.24. If a DTE requires to transmit a character, it turns ON circuit 105 (request to send). The DTE can only begin transmission when it receives in return circuit 106 ON (ready for sending). If, during transmission of a block of characters circuit 106 goes OFF, the DTE must cease transmission (after completing the transmission of any character of which transmission has started) until circuit 106 turns ON again.

2.4.1.2 *XON/XOFF operation*

This is an inband flow control mechanism using two characters of the IA5 set for XON and XOFF operation. If a DTE receives an XOFF character, it must cease transmission. When it receives an XON character, it may resume transmission. The characters typically used for XON and XOFF are DC1 and DC3 (bit combination 1/1 and 1/3 in Recommendation T.50) respectively, although alternative bit-combinations can be used.

2.4.1.3 *Other methods*

Alternative and non-standard methods of asynchronous flow control are in use, and these may be mapped onto the TA flow control protocol.

2.4.2 *End-to-end (TA to TA) flow control*

Matching (by reduction) of the transmitted character rate of the DTE to the rate of the TA is not sufficient in all cases to guarantee correct operation, and end-to-end flow control may be required.

The X bit is used to carry flow control information. A TA will buffer incoming characters. When the number of buffered characters exceeds a threshold TH1, depending upon implementation, the TA will set the X-bit of its outgoing frames to OFF.

Upon receipt of a frame containing an X-bit set to OFF, a TA will execute its selected local flow control procedure indicating that the attached DTE must stop sending characters, and cease the transmission of data after completion of the character in progress by setting the data bits in the outgoing frames to ONE.

When the buffer contents of a TA which has initiated an end-to-end flow control drops below threshold TH2, the TA will reset the outgoing X bit to ON.

When the far-end TA receives a frame with the X bit set to ON, it will recommence data transmission, and, by use of the local flow control procedure, indicate to the attached DTE that it may continue.

Note – There may be a delay between initiation of the end-to-end flow control protocol and termination of the incoming character stream. The characters arriving during this time must be buffered, and the total buffer size will depend upon the character rate, round trip delay and the buffer threshold.

2.4.3 *Use of channel capacity*

Upon accepting a call from a TA supporting flow control and operating at a different user rate and/or intermediate rate, the called TA will adopt the identical intermediate rate and bit repetition factor. This will override the parameters normally selected. In such cases, the TA connected to the faster DTE will execute a local flow control procedure to reduce the character rate to that of the slower DTE.

Thus, if a faster DTE calls a slower DTE, the faster intermediate channel rate and bit repetition factor will be adopted by the TAs on both ends. To reduce the character rate received by the slower DTE, its TA will exercise end-to-end flow control and cause the TA on the calling side to utilize local flow control.

If a slower DTE calls a faster DTE, the slower intermediate channel rate and bit repetition factor will be adopted by the TAs on both ends. To reduce the character rate transmitted by the faster DTE, its TA will exercise local flow control.

If the called TA does not implement the intermediate rate and bit repetition factor used by the calling TA, the call shall be rejected.

2.4.4 *Requirements of a TA supporting flow control*

The following are general requirements for a TA supporting flow control:

i) A TA supporting flow control shall be capable of operating with an intermediate rate and bit repetition factor that is independent of the asynchronous speed used at its DTE interface.

ii) A TA supporting flow control shall, if possible, adapt to the intermediate rate and bit repetition factor required for an incoming call. User rate information will be obtained from signalling.

iii) A TA supporting flow control shall be capable of executing a local flow control protocol to reduce the character rate to that of the far-end DTE.

iv) A TA supporting flow control will support the use of end-to-end (TA to TA) flow control using the X bit, and will contain a character buffer.

3 Interchange circuits

3.1 *Essential and optional interchange circuits*

The essential and optional interchange circuits are listed in Table 9/V.110 below.

3.2 *Timing arrangement*

The TA shall derive ISDN timing from the received bit stream of the ISDN's basic user/network interface (see §§ 5 and 8 of Recommendation I.430). This network timing shall be used by the TA to provide the DTE with transmitter signal element timing on circuit 114 and receiver signal element timing on circuit 115.

3.3 *Circuit 106*

After the start-up and retrain synchronization sequences, the ON state of circuit 106 shall be delayed relative to the ON state of circuit 105 (where implemented) by an interval of at least N bits (a value of N equal to 24 has been proposed, but the value is for further study). ON to OFF state transitions of circuit 106 shall follow ON to OFF state transitions of circuit 105 (when implemented) by less than 2 ms. Where circuit 105 is not implemented, the initial circuit 106 transition to the ON state shall be delayed by an interval greater than or equal to N bits relative to the corresponding transition in the state of circuit 109. Subsequent transitions in the state of circuit 106 should occur solely in accordance with the operating sequences defined in § 4, or when used for the optional flow control in § 2.4.

TABLE 9/V.110

Interchange circuit		Notes
Number	Description	
102	Signal ground or common return	
102a	DTE common return	2
102b	DCE common return	2
103	Transmitted data	
104	Received data	
105	Request for sending	3
106	Ready for sending	
107	Data set ready	
108/1	Connect data set to line	4
108/2	Data terminal ready	4
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	5
112	Data signalling rate selector (DCE source)	5
113	Transmitter signal element timing (DTE source)	6
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source))	
125	Calling indicator	7
140	Loopback/maintenance test	8
141	Local loopback	8
142	Test indicator	8

Note 1 – All essential circuits and any others which are provided shall comply with the functional and operational requirements of Recommandation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommandation for electrical characteristics (see § 3.5).

Note 2 – Interchange circuits 102a and 102b are required where the electrical charactristics defined in Recommandation V.10 are used at data signalling rates above 20 kbit/s.

Note 3 – Not required for DTEs that oprate with DCEs in the continuous carrier mode.

Note 4 – This circuit shall be capable of operating as circuit 108/1 or 108/2, depending on its use (by the associated TE).

Note 5 – The use of this circuit is for further study.

Note 6 – The use of circuit 113 is for further study, since its application is restricted by the synchronous nature of ISDN.

Note 7 – This circuit is used with the automatic answering terminal adaptor function.

Note 8 – The use for loopback testing is for further study.

3.4 *Circuit 109*

OFF to ON and ON to OFF transitions of circuit 109 should occur solely in accordance with the operating sequence defined in § 4.

3.5 *Electrical/mechanical characteristics of interchange circuits*

3.5.1 *Basic ISDN user/network interface*

The electrical and mechanical characteristics of the basic ISDN user/network interface are described in §§ 8 and 10 of Recommendation I.430.

3.5.2 *TE2/TA (DTE/DCE) interface*

3.5.2.1 *Rates less than or equal to 19.2 kbit/s*

Use of electrical characteristics conforming to Recommendation V.28, is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-series application which minimizes the number of interchange circuits (proposed draft Recommendation V.230).

3.5.2.2 *Rates greater than 19.2 kbit/s*

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended together with the use of the connector and pin assignment plan specified by ISO 4902.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

ii) In the case of circuits 105, 106, 107 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1, or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies, with receivers configured as specified by Recommendation V.10 for category 2.

Alternatively, the interface defined in Appendix II to Recommendation V.35 together with connector and pin assignment plan specified by ISO 2593 may be used.

3.6 *Fault condition on interchange circuits*

(See § 7 of Recommendation V.28 for association of the receiver failure detection types).

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Operating sequence

4.1 *TA duplex operation*

When using the TA to provide data transmission service within ISDN, the call is established over a 64 kbit/s connection using the procedures applicable to the particular network and/or terminal configuration.

The internal arrangement of the TA functional parts and the DTE (with a V-series type interface) is not within the scope of this Recommendation. It is assumed that means are provided to control the entry to and the exit from the data transfer mode. For example, it is assumed that the means are provided to control circuits 108/1 (Connect data set to line) or 108/2 (Data terminal ready) internally, that is within the station at the customer premises. However, for the purpose of this Recommendation circuit 108/2, as defined in Recommendation V.24, is assumed.

4.1.1 *Idle (or ready) state*

4.1.1.1 During the idle (or ready) state the TA (DCE) will be receiving the following from the DTE:

Circuit 103 = Continuous binary 1

Circuit 105 = See Note

Circuit 108/1 = OFF; circuit 108/2 = ON

Note – In many duplex DTEs circuit 105 is either permanently in the ON condition or it is not present. If not present, the function must be set in an ON condition in the TA. See § 4.1.2.4 for the case where a duplex DTE can operate circuit 105.

4.1.1.2 During the idle (or ready) state the TA will transmit Continuous binary 1s into the B and D channels (i.e., all bits of Table 2/V.110 = binary 1).

4.1.1.3 During the idle (or ready) state the TA (DCE) will transmit the following toward the DTE:

Circuit 104 = Continuous binary 1

Circuit 107 = OFF

Circuit 106 = OFF

Circuit 109 = OFF

4.1.2 *Connect TA to line state*

4.1.2.1 When the TA is to be switched to the data mode, circuit 108 must be ON. Switching to the data mode causes the TA to transmit the following towards the ISDN (refer to Table 2/V.110):

a) frame synchronization pattern, as follows:
   - octet 0 = all binary 0s
   - bit number one of octets 1-9 = binary 1

b) data bits = binary 1

c) status bits S = OFF and X = OFF (ON = binary 0/OFF = binary 1).

Note 1 – At this time circuit 103 is not connected to the data channel (e.g., the binary 1 condition of the data bits is generated within the TA).

Note 2 – In the following description only the inter-operation between TE2/TA (DTE/DCE) interface and the intermediate rate frames (Tables 6a/V.110 to 6f/V.110) and the 64 kbit/s frame of Tables 7a/V.110 and 7c/V.110 are discussed. The second step of rate adaptation encoding and decoding and the multiplexing and demultiplexing of the ISDN basic user/network interface are discussed in Recommendations I.460 and I.430, respectively.

4.1.2.2 At this time (i.e. switching to data mode) the receiver in the TA will begin to search for the frame synchronization pattern in the received bit stream (see § 2.1.3.1). At the same time, a timer T1 shall be started with a time out value of at least 10 seconds.

4.1.2.3 When the receiver recognizes the frame synchronization pattern, it causes the S and X bits in the transmitted frames to be turned ON (provided that circuit 108 is ON).

4.1.2.4 When the receiver recognizes that the status of bits S and X are in the ON condition, it will perform the following functions:

a) Turn ON circuit 107 toward the DTE and stop timer T1.

   Note – A duplex DTE that implements and is able to operate circuit 105 may be expected to turn this circuit ON at any time. However, if not previously turned ON, it must be turned ON in response to the ON condition on circuit 107.

b) Then, circuit 103 may be connected to the data bits in the frame; however, the DTE must maintain a binary 1 condition until circuit 106 is turned ON in the next portion of the sequence.

c) Turn ON circuit 109 and connect the data bits to circuit 104.

   Note – Binary 1 is being received on circuit 104 at this time.

d) After an N bit interval (see § 3.3), it will turn ON circuit 106.

e) Circuit 106 transitioning from OFF to ON will cause the transmitted data to transition from binary 1 to the data mode.

If circuit 107 has not been turned ON, after expiring of timer T1 the TA shall be disconnected according to the procedures given in § 4.1.4.

4.1.3 *Data transfer state*

4.1.3.1 While in the data transfer state, the following circuit conditions exist:

a) circuits 105 (when implemented), 106, 107, 108/1 or 108/2 and 109 are in the ON condition;

b) data is being transmitted on circuit 103 and received on circuit 104.

4.1.4 *Disconnect mode*

4.1.4.1 At the completion of the data transfer phase, the local DTE will indicate a disconnect request by turning OFF circuit 108. This will cause the following to occur:

a) the status bits S in the frame toward ISDN will turn OFF, status bits X are kept ON;

b) circuit 106 will be turned OFF;

c) the data bits in the frame will be set to binary 0.

4.1.4.2 If circuit 108 is still ON at the remote TA, this TA will recognize the transition of the status bits from ON to OFF and the data bits from data to binary 0 as a disconnected signal and it will turn OFF circuits 107 and 109. This DTE should respond by turning OFF circuit 108 and transferring to disconnected mode. The disconnection will be signaled via the ISDN D channel signalling protocol. At this time, the DTE/DCE interface should be placed in the idle (or ready) state.

4.1.4.3 The TA at the station that originated the disconnect request will recognize reception of S = OFF or the loss of framing signals as a disconnect acknowledgement and turn OFF circuits 107 and 109 and transfer to disconnected mode. The disconnection will be signalled via the ISDN D channel signalling protocol. At this time, the DTE/DCE interface should be placed in the idle (or ready) state.

4.1.5 *Loss of frame synchronization*

In the event of loss of frame synchronization, the TA should attempt to resynchronize as follows:

a) Place circuit 104 in binary 1 condition (passes from the data mode).

b) Turn OFF status bit X in the transmitted frame.

c) The remote TA upon recognition of status bit X OFF will turn OFF circuit 106 which will cause the remote DTE to place circuit 103 in a binary 1 condition.

d) The local TA should attempt to resynchronize on the incoming signal.

e) If after an interval of three seconds the local TA cannot attain synchronization, it should send a disconnect request by turning OFF all of the status bits for several (at least three) frames with data bits set to binary 0 and then disconnect by turning OFF circuit 107 and transferring to the disconnected mode as discussed in § 4.1.4.2 above.

Note – The values of three seconds and three frames are provisional and should be confirmed or amended after further study.

f) If resynchronization is achieved, the TA should turn ON status bit X toward the distant station.

g) If resynchronization is achieved, the TA (which has turned OFF circuit 106) should, after an N bit interval (see § 3.3), turn ON circuit 106. This will cause circuit 103 to change from binary 1 to the data mode.

Note – During a resynchronization attempt, circuits 107 and 109 should remain ON.

4.2 *TA half-duplex operation*

The data call establishment for the interworking of half-duplex DTEs equipped with V-series type interfaces is the same as discussed in § 4.1 above. The only difference between half-duplex operation is in the control of the circuits 105, 106, and 109, as follows.

Note – This is a unique application; therefore, TA arranged for half-duplex operation will not be able to interwork with either a V-series or an X-series duplex DTE (TE2).

4.2.1 In a TA arranged to accommodate half-duplex DTEs, circuit 109 will be under the control of the status bits SB in the incoming frame, as follows:

a) If at the local interface circuit 109 is OFF and circuit 104 is in the binary 1 state, the DTE may "**request to send**" by turning ON circuit 105.

b) The TA will then turn ON status bits SB in the transmitted frame which will turn ON circuit 109 in the remote interface and connect circuit 104 to the data bit stream of the incoming frame.

c) After an *N* bit interval (see § 3.3) the local TA will turn ON circuit 106, which will allow the local DTE to transmit data on circuit 103.

d) Upon completion of the transmission the local DTE will turn OFF circuit 105. This will in turn:

- turn OFF circuit 106 in the local interface and circuit 103 will revert to the binary 1 state,
- turn OFF status bits SB which will in turn at the remote TA turn OFF circuit 109 and place circuit 104 in a binary 1 condition.

e) At this time the remote DTE is able to reverse the sequence by turning ON circuit 105.

4.3 *Automatic calling*

The mapping of V.25 and/or V.25 *bis* automatic calling and/or automatic answering procedures to the ISDN D channel signalling protocols is for further study.

5 Network independent clocks

In cases where synchronous data signals at user rates up to and including 19.2 kbit/s are received from outside the ISDN (e.g., through an interworking unit from a DTE/modem on the PSTN), the data may not be synchronized to the ISDN. The following method shall be used to enable transfer of those data signals and the corresponding bit timing information via the 80-bit frame to the receiving TA. Such a situation would exist where the signals are received through an interworking unit from voice-band data modems on the analogue PSTN where the transmit data from the remote modem is synchronized to the modem clock (normal case for such applications). The frequency tolerance of such modems is 100 ppm.

5.1 *Measurement of phase differences*

The phase difference between the following two frequencies will be measured:

i) R1 = 0.6 × the nominal intermediate rate (except where Fill bits are used; see Note), synchronized with the ISDN;

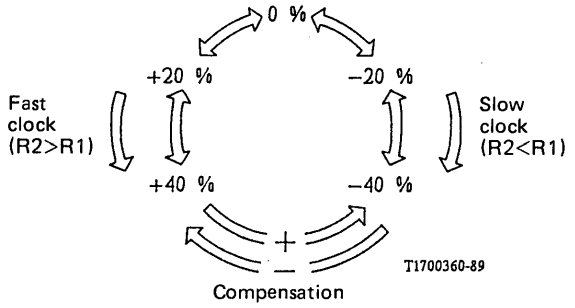
ii) R2 = 0.6 × the nominal intermediate rate (except where Fill bits are used; see Note), derived from and synchronized with the bit timing received from the remote synchronous source, e.g., modem.

Note – Clocks R1 and R2 are nominally either 4800, 9600 or 19 200 Hz at 8 kbit/s, 16 kbit/s and 32 kbit/s intermediate rate, respectively.

Where Fill bits are used, in the cases of 7200 and 14 400 bit/s R1 and R2 will have the same nominal rate as the user bit rate.

Compensation will affect one, one-half, one-quarter or one-eighth of a user data bit, dependent upon the bit repetition factor.

A state diagram for the transmitting TA showing the phase of R2 relative to R1 appears in Figure 4/V.110. Table 10/V.110 shows the related bit coding.



Note 1 – Phase measurements are given relative to R1 by the formula: Phase = phase(R2) – phase(R1).

Note 2 – Receipt of a bit combination requiring an illegal move of more than one state will cause a legal move of one state in the appropriate direction.

Note 3 – The initial state of both the receiving and transmitting sides of the TA will be 0%

FIGURE 4/V.110

Network-independent clocking state diagram

TABLE 10/V.110

Coding of E bits for network-independent clocking

Displacement (in % of nominal R1 clock period at n × 4800 bit/s, n = 1, 2 or 4)	Coding in the 80-bit frame		
	E4	E5	E6
Nominaly 0	1	1	1
+20	0	0	0
+40	0	0	1
−40	0	1	0
−20	0	1	1
Compensation control			
Positive compensation of a one	1	0	1
Positive compensation of a zero	1	0	0
Negative compensation	1	1	0

Comparison of R1 and R2 will give a phase difference relative to R1 which will be encoded as shown in Table 10/V.110. The resultant 3-bit code will be transmitted in bit positions E4, E5 and E6, and used for clock control at the receiving TA.

To avoid continuous jitter between neighbouring displacement positions, hysteresis shall be applied, as follows:

The displacement code shall be changed only when the measured phase difference between R1 and R2 is 15% (of the R1 clock period) more or less than the difference indicated by the existing displacement code.

Example – Bit combination 000 indicates a phase difference of nominally 20%. This bit combination will be changed into 001 when the measured phase difference is 35% or more, and into 111 when the measured phase difference is 5% or less.

5.2 *Positive/negative compensation*

On transition from the +40% state to the −40% state, an extra user D bit has to be transmitted in the 80-bit frame, using bit E6 (positive compensation). At the receiving TA, this extra bit will be inserted between D24 and D25 as shown in Table 2/V.110, immediately following the E bits.

On transition from the −40% state to the +40% state, a bit combination is transmitted in the 80-bit frame (E4, E5 and E6 = 1, 1, 0, respectively), indicating to the receiving TA that bit D25 of the 80-bit frame, being set to ONE, does not contain user data and should be removed (negative compensation).

5.3 *Encoding*

The encoding of the measured phase difference for clock control and the positive/negative compensation control overrides and replaces the clock control coding.

6 Inband parameter exchange state

The capabilities provided and operation in an optional inband parameter exchange state are described in Appendix I to this Recommendation.

7 Testing facilities

The provision of maintenance test loops is for further study, taking in consideration I.603 and V.54.

ANNEX A

(to Recommendation V.110)

Reference configurations

A.1 *Introduction*

Figures A-1/V.110 and A-2/V.110 show the two basic reference models used in the development of V.110, and provide valuable examples of the way in which the terminal adaptor may be used. These are provided simply as an aid to the interpretation of V.110 and should not be seen as restrictive in any way.

A.2 *Terminal adaptor reference model for V.110*

Figure A-1/V.110 shows the basic reference model for a V.110 terminal adaptor.

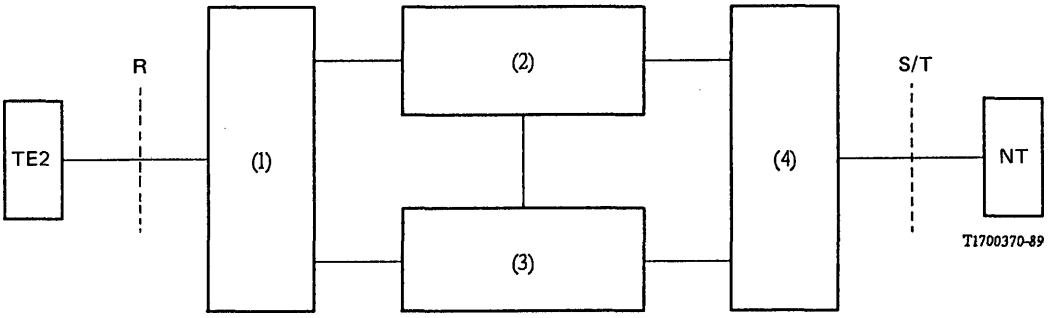
The elements (1), (2), (3) and (4) shown in Figure A-1/V.110 represent the functionality required of a terminal adaptor. The elements are not intended to correspond to separate physical units. However, a terminal adaptor need not necessarily constitute a single physical unit. The functions of these elements are:

1) Provision of Layer 1, in accordance with Recommendations V.24 and V.28 or other applicable Recommendations and ISO 2110 or other applicable standards, of the interface at reference point R.

2) Specific TA functions, including the adaption of the TE2 data (rate and format) for transmission over an ISDN B Channel and provision of R interface lead control information. This Recommendation covers primarily these functions.

3) Network control signalling functions, including the mapping of call control signals (in accordance with Recommendation V.25 *bis* or other applicable standard) at the R interface into signals (according to Recommendation Q.931) for transmission on the D Channel across the S/T interface.

4) Provision of Layer 1, in accordance with Recommendation I.430 of the interface at reference points S or T.



NT Network termination

TE2 Data terminal equipment (DTE) with an interface complying to Recommendation V.24

(1) R interface functions (according to Recommendations V.24, V.28, etc.)

(2) Specific TA functions (e.g., data rate adaption)

(3) Control access signalling function (e.g., signalling in accordance with Recommendations Q.921 and Q.931, auto calling in accordance with Recommendation V.25*bis*)

(4) S/T interface Layer 1 functions (according to Recommendation I.430)

FIGURE A-1/V.110

Terminal adaptor reference model

A.3 *Terminal adaption type*

A.3.1 *Terminal adaptor – type A*

The TA-A provides manual call control functions and the functions necessary for data transfer. The following data transfer functions are included:

a) Conversion of electrical, mechanical, functional and procedural characteristics of the V-Series type interface(s) to those required by an ISDN at reference points S and/or T, as discussed in § 3.5.

b) Bit rate adaption of the V-Series data signalling rates to the 64 kbit/s B Channel rate as described in §§ 2.1, 2.2 and 2.3.

c) End-to-end synchronization of entry to and exit from the data transfer phase, as described in § 4.

Terminal adaptor TA-A may be implemented using a physically separate TE1 for providing the network control signalling function, unit (3) in Figure A-1/V.110, or the function may be part of an integrated implementation. The function provides for data connection establishment when using the circuit-mode 64 kbit/s unrestricted bearer service. The function includes provisions for speech and data connection establishment when using for speech, either circuit-mode 64 kbit/s bearer service usable for 3.1 kHz audio information transfer, and, for data, the circuit-mode 64 kbit/s unrestricted bearer service concurrently on two B Channels.

A.3.2 *Terminal adaptor – type B*

The TA-B includes, in addition to those functions provided by a TA-A, the mapping functions necessary to convert the automatic calling and/or automatic answering procedures of Recommendations V.25 and V.25 *bis* to the ISDN D Channel signalling protocol. This additional functionality is in functional unit (3) in Figure A-1/V.110. Terminal adaptor type B is to be used with the 64 kbit/s unrestricted bearer service.

The need for provisions covering functional unit (3) in Figure A-1/V.110 for the implementation of a type B terminal adaptor is for further study.

Note – Reference to the use of the term "unrestricted bearer". During an interim period, some networks may only support restricted 64 kbit/s signal digital information transfer capability; i.e., information transfer capability solely restricted by the requirement that the all-zero octet is not allowed. Such networks may offer bearer services with restricted transport capabilities.

A.4 *Types of end-to-end connection*

The terminal adaptor functions described in this Recommendation take into account the end-to-end connection types shown in Figure A-2/V.110. The Figure shows the interoperational cases considered in this Recommendation, as follows:

V-Series TE2 with V-Series TE2

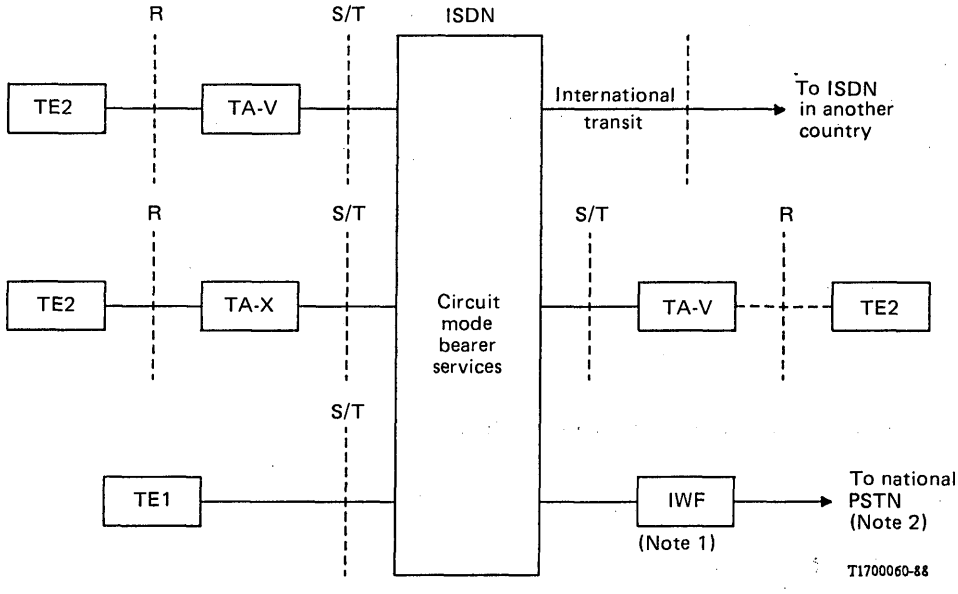
V-Series TE2 with X.21 TE2

V-Series TE2 with TE1

V-Series TE2 with V-Series DTE on the PSTN through an interworking function (IWF)

Note – The adaption of terminals by the connection of modem-equipped TE2s to the analogue side of a CODEC to provide for the use of 3.1 kHz bearer capabilities is not addressed in this Recommendation.

Interworking with PSTNs may be provided on the basis of a trunk interconnection using interworking functions (IWFs) (Note 1 of Figure A-2/V.110). The reference connections illustrated in Figure A-2/V.110 do not envisage a direct connection between an ISDN in one country and a public switched telephone network (PSTN) in another country via a network-provided Interworking Function in the first country. However, access to non-ISDN countries could be through the normal PSTN international connections.



IWF Interworking function
TA-V Terminal adaptor function – (DTEs with V-Series interfaces)
TA-X Terminal adaptor function – (DTEs with X.21 or X.21*bis* interfaces)
See Recommendations X.30/I.461

Note 1 – The location of this interworking function is discussed in Recommendation I.510 and general requirements are given in Recommendations I.515 and I.530. The need for a Recommendation covering detailed requirements for such an IWF is for further study.

Note 2 – For access to national non-ISDN terminals or international access to PSTNs of non-ISDN countries.

FIGURE A-2/V.110

Network reference connections

APPENDIX I

(to Recommendation V.110)

In-band parameter exchange

I.1 *Introduction*

During the evolution of ISDN there will exist for a considerable period:

- DTEs with V-Series type interfaces which are to be connected to an ISDN by terminal adaptors, and
- requirements for interoperation between DTEs/TAs connected to ISDNs, that are interconnected with facilities which do not provide for the full ISDN out-of-band signalling capability necessary to support parameter exchange between terminal adaptors.

Considering that Recommendation I.530 defines interworking between an ISDN and a PSTN in general, that Recommendation I.515 describes the parameter exchange for interworking between ISDNs and existing networks, the specific procedure to be used for inband parameter exchange (IPE) within the context of terminal adaptors following Recommendation V.110 is as described here. This procedure is consistent with Recommendations I.530 and I.515.

It enhances the capability of V.110 in order to support:

- the transfer of the end-to-end information required for the comptability checking of data calls,
- an exchange of terminal adaptor parameter information, and
- an exchange of information related to maintenance operations.

I.2 *Definitions*

For the IPE, which is described here, the following definitions apply. These definitions are ordered logically to minimize forward referencing.

I.2.1 **TA**

A terminal adaptor.

I.2.2 **calling TA**

The TA requesting the connection to be established.

I.2.3 **called TA**

The TA accepting the connection.

I.2.4 **originating TA**

The TA which is responsible for initiating the next exchange of parameter information. Initially, the calling TA takes on the role of the originating TA.

I.2.5 **answering TA**

The TA which is not responsible for initiating the next exchange of parameter information. Initially, the called TA takes on the role of the answering TA.

I.2.6 **parameter information**

Terminal adaptation protocol information, TA parameters, and (optionally) maintenance information.

I.2.7 **parameter block**

The complete set of parameter information structured into message groups, which are transferred by each TA towards the other during each parameter exchange.

I.2.8 **message group**

The arrangement of octets based on a repeated sequence of command octets followed by a series of three LOW-HIGH data octet pairs. Each message group transfers one octet of the parameter information.

I.2.9 **sequence of command octets**

The repeated transmission of at least 32 command octets transmitted without interval for 64 kbit/s unrestricted and restricted channels. In the case of asynchronous IPE the sequence may be interrupted, within the limits of the procedures.

I.2.10 **series of LOW-HIGH data octet pairs**

The transmission of six octets grouped into three pairs of LOW-HIGH data octets, the LOW data octet being transmitted in each pair before the HIGH data octet. The six octets are transmitted without interval for 64 kbit/s unrestricted and restricted channels. In the case of asynchronous IPE, the transmission of the six octets may be interrupted, within the limits of the procedures.

I.2.11 **verification**

Establishment of the validity of a piece of data according to the specified error handling procedures.

I.3 *Overview*

The in-band parameter exchange (IPE) described here is based on the transfer of parameter information within the user data stream of an established connection. Specific IPE rates have been selected to cover the application of IPE to connections based on 64 kbit/s unrestricted channels, 64 kbit/s restricted channels and intermediate rate channels. For IPE at rates other than 64 kbit/s, rate adaption according to Recommendation V.110 is applied to the user data stream containing the parameter information.

In the case of IPE within intermediate rate channels, it is first necessary to achieve frame synchronization according to Recommendation V.110 before the exchange can commence. The parameter information is transferred in a parameter block during one or more exchanges between the two TAs. The block structure is based on message groups, containing a sequence of command octets which identify the information carried in the message group, and a series of general purpose LOW-HIGH data octet pairs which carry the information. The command octets are always transmitted in a repeated sequence of at least 32 octets to allow persistency error handling techniques to be employed. The LOW-HIGH data octet pairs are always transmitted in a series of three to enable majority voting error recovery techniques to be used.

After the first exchange of parameters, the called TA determines whether the parameter exchange has been successful. If it is, both TAs proceed to the data transfer state directly unless the agreed data transfer rate first requires re-synchronization to a new intermediate rate according to Recommendation V.110. After the first exchange, and each subsequent exchange, the responsibility for determining the success of the exchange is transferred, to allow the negotiation of parameters to progress evenly. Status information is also transferred during the IPE to enable both TAs to monitor the progression of the exchange. If at any time either TA concludes that a successful exchange of parameters cannot be achieved, the TA should clear the connection.

Interworking with TAs not supporting IPE is specified.

I.4 *Reference configuration*

Figure I-1/V.110 gives an example of a scenario for an IPE procedure. It illustrates the connection of ISDNs using the connectivity of existing networks. As the evolution towards a ubiquitous international ISDN capability proceeds, the connection of ISDN islands will often use existing network capabilities. Two alternatives are indicated in Figure I-1/V.110. Either arrangement indicated may exist though the use of "digital connectivity" based on the existing IDN has many advantages including the avoidance of the need for layer 1 interworking functions. The IDN, however, does not have the ISDN signalling capability and this leads to the need for an IPE procedure. The IPE capability is required to enable communicating TAs to exchange parameters as well as to perform other operations such as maintenance functions. Even where the ISDN signalling capability is available, the IPE capability may be used to provide enhanced parameter exchange.

I.5 *Procedures*

I.5.1 *General*

Described in § I.5 are the procedures which permit a TA to exchange parameter and maintenance information in-band by using messages within the user data stream.

Once the call has been established, the IPE is initiated at one of four user data rates as per Table I-1/V.110. It is recommended that, where possible, the IPE is performed using the unrestricted/restricted 64 kbit/s rate. If the TA is not capable of starting at this rate, then the appropriate default intermediate rate is used. Default intermediate-rate channels are selected according to the Recommendation for single stream operation described in Recommendation I.460. Subrate multiplexing cannot be supported until the IPE is complete.

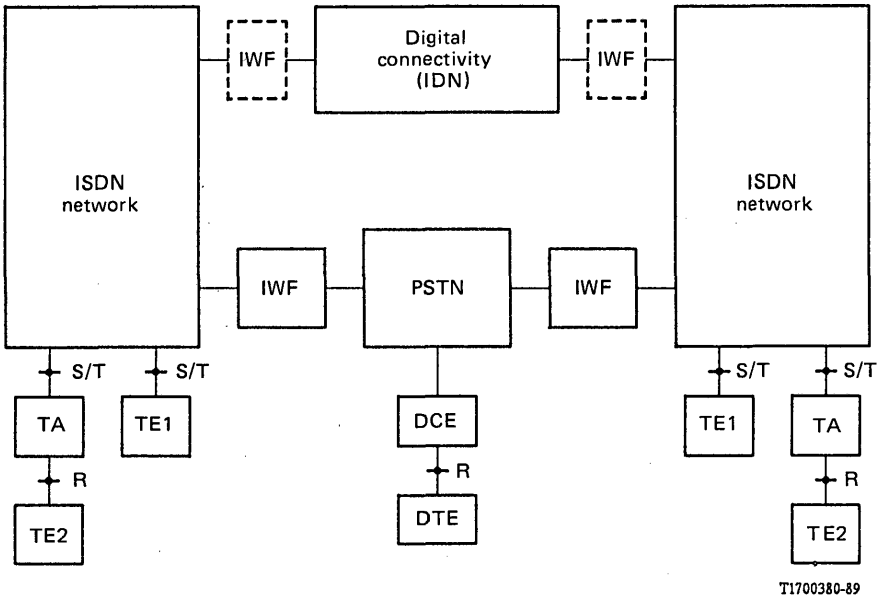


FIGURE I-1/V.110

Reference configuration

The final rate of data transfer is not restricted by the choice of IPE user rate. It is therefore possible for an IPE at 4.8 kbit/s async, for example, to agree on the use of 64 kbit/s unrestricted during the data transfer state. For IPE at rates other than 64 kbit/s, rate adaption according to Recommendation V.110 is applied to the user data stream containing the IPE information. In order to prevent unintended disconnection when rate adaption according to Recommendation V.110 is used, it is necessary to avoid the condition S = OFF, X = ON and all the data bits set to ZERO. This is achieved by the use of asynchronous characters with one Stop bit and the permanent setting of bit 8 in all octets to ONE.

Paragraph I.5.2 describes how IPE is initiated, with the procedures for IPE itself described in § I.5.3. If the parameter exchange results in the selection of a data rate based on a different intermediate rate to that used for IPE, re-synchronization is required. The procedures for re-synchronization and data transfer are given in §§ I.5.4 and I.5.5 respectively. In § I.5.6, the procedures for interworking with a TA not supporting IPE are given. In § I.5.7 the procedures associated with maintenance are described. § I.5.8 defines re-entry to IPE from the data transfer state, and § I.5.9 provides the procedures for error protection and handling. Message codings are given in § I.6, timer values in § I.7 and state transition diagrams in § I.8.

TABLE I-1/V.110

Selection of IPE user rate

IPE intermediate rate	IPE data rate
Unrestricted/restricted (64 kbit/s)	56 kbit/s
32 kbit/s intermediate-rate channel	19.2 kbit/s async
16 kbits/s intermediate-rate channel	9.6 kbit/s async
8 kbits/s intermediate-rate channel	4.8 kbit/s async

I.5.2 *Initiating the exchange*

An IPE TA requires a local memory flag (the re-entry flag) to control the re-entry into IPE from the data transfer state.

During the inactive state, the TA shall transmit continuous ONEs into the B channel (see § I.8). Once a connection has been established, both TAs will initiate the parameter exchange at the selected user rate and set the re-entry flag to ZERO. Before beginning the parameter exchange, both TAs start Timer T2 and may send repeated IDLE status octets (see § I.6.5).

In the case where the TAs operate on a different IPE user rate, the following procedure shall be applied:

- during the first half of period T2, the called TA only tries to adapt to the IPE rate of the calling TA before transmitting its initial exchange of information;
- during the second half of period T2, the calling TA only tries to adapt to the called TA, and retransmits the initial exchange of information at the called TA user rate.

If Timer T2 expires before a complete parameter block has been received, both TAs shall begin data transfer using their default parameters.

In the case of user rates of 4.8, 9.6 or 19.2 kbit/s, the TA first completes the frame synchronization procedure described in Recommendation V.110, with the changes detailed below:

a) The transmitter sends frames towards its peer with status information S = OFF and X = OFF and enters the awaiting synchronization-parameter exchange state (State 6).

b) When the TA recognizes the frame synchronization pattern in the awaiting synchronization-parameter exchange state (State 6), it verifies the status information received and then enters the appropriate state, in a coordinated manner, as follows:
   - data transfer (State 4), upon receipt of S = ON and X = ON (see § I.5.6),
   - IPE default exchange (State 5), upon receipt of S = OFF and X = OFF,
   - parameter exchange (State 7), upon receipt of S = OFF and X = ON (see § I.5.3).

c) When the TA is in the IPE default exchange state (State 5), it shall transmit frames with status information S = OFF and X = ON and verify the status information received and then enter the appropriate state, in a coordinated manner, as follows:
   - data transfer (State 4), upon receipt of S = ON and X = ON (see § I.5.6),
   - parameter exchange (State 7), upon receipt of S = OFF and X = ON (see § I.5.3).

In the case of user rates of 56 or 64 kbit/s there is no frame synchronization requirement.

I.5.3 *Parameter exchange*

I.5.3.1 *Octer alignment*

In the case of user rates of 4.8, 9.6 or 19.2 kbit/s, each octet of the parameter exchange message is carried as a single start-stop character (see § I.6.1). In the case of user rates of 56 or 64 kbit/s, network-provided octet alignment shall be used.

I.5.3.2 *Transfer of parameters*

The correct interpretation of this section requires careful adherence to the definitions made in § I.2, particularly for the meaning of a "sequence of command octets" (§ I.2.9) and a "series of LOW-HIGH data octet pairs" (§ I.2.10). Further detailed information is given in § I.5.9 and § I.6.

After the connection has been established, the calling TA takes on the role of the originating TA and the called TA the role of the answering TA.

The originating TA begins by starting Timer T1 and transmitting a sequence of XSTART command octets (see § I.6.3). After verifying the receipt of the XSTART command octets, the answering TA starts Timer T1 and begins parameter transfer as described below. Once the originating TA has verified the receipt of the RA VERSION command octet (at the start of the parameter transfer) from the answering TA, the originating TA also begins parameter transfer in the same manner. Figure I-2/V.110 portrays the normal sequence of events during the parameter exchange.

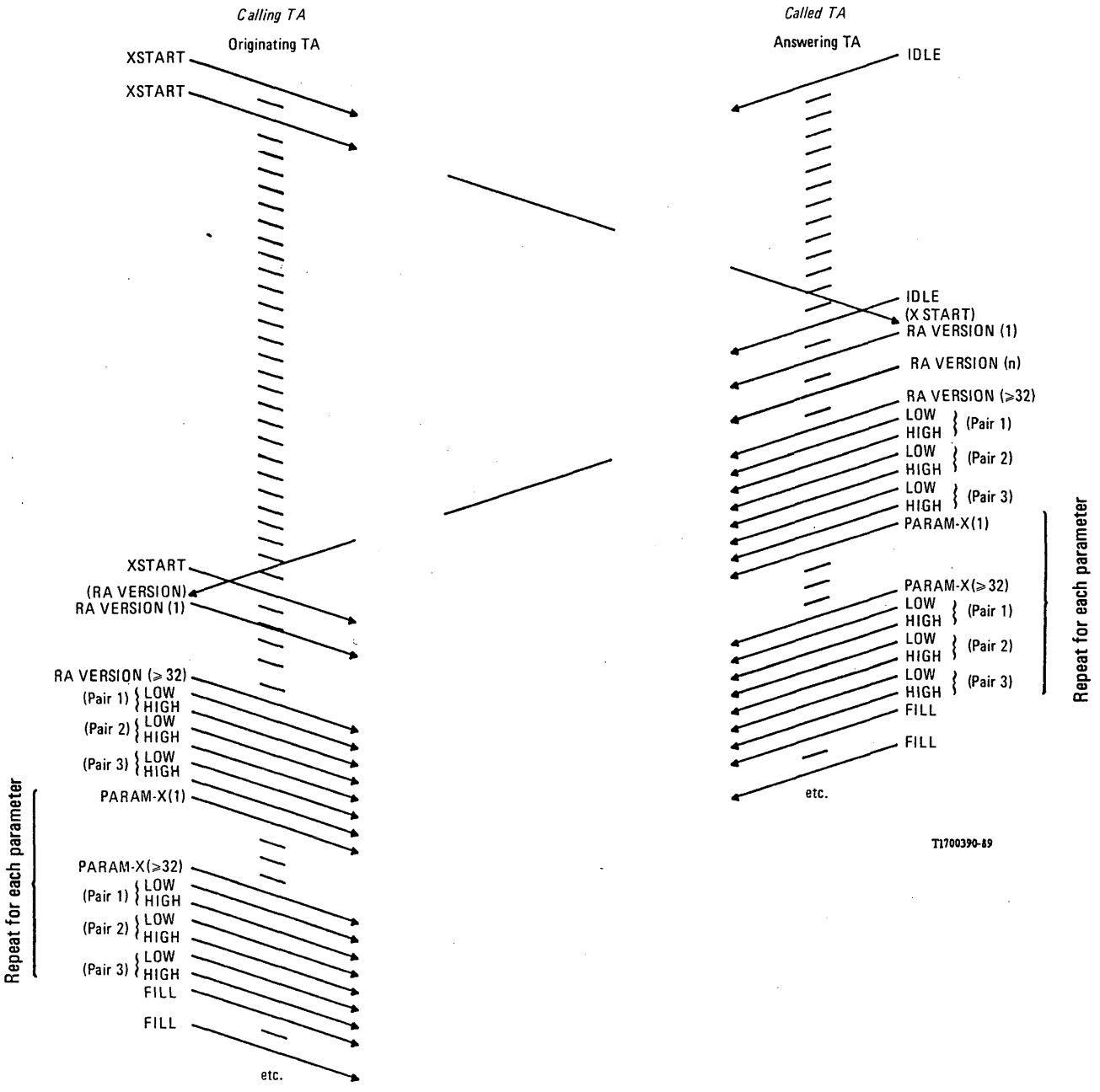


FIGURE I-2/V.110

Initial sequence of events during a parameter exchange

The parameter transfer commences with the transmission of a sequence of RA VERSION command octets followed by a series of LOW-HIGH data octet pairs containing the rate adaption identifier (see § I.6.2). Directly following the transmission of the rate adaption identifier, the transfer continues with the parameters themselves in five groups: PARAM-0 to PARAM-4 (see § I.6.4), transmitted in ascending order. Each group begins with the transmission of a sequence of the appropriate PARAM command octet followed by a series of LOW-HIGH data octet pairs which carry the parameters. At the completion of the parameter information transfer, both TAs send repeated FILL status octets until the next stage of the parameter exchange. Transmission of the complete parameter block shall be made within the period T2.

After receiving and processing the rate adaption and parameter information, the answering TA determines whether the parameters exchanged in both directions are compatible, or whether it can adapt to the parameters of the originating TA. In either case, the exchange has been successful and the procedures described in § I.5.3.3 are followed. If the parameters were not compatible and the answering TA decides to continue, it now takes on the role of the originating TA and recommences the parameter exchange with the transmission of a sequence of XSTART command octets. The parameter transfer procedures therefore continue as described above, but with the roles of originating and answering carried out by the opposing TAs. In the first exchange, the called TA should attempt to adapt to the parameters of the calling TA. When continuing the exchange the new originating TA should attempt, as far as possible, to move the values of its next transmitted parameters towards the values of those previously received. If either TA determines that there is no point in continuing the parameter exchange, the procedures described in § I.5.3.4 are followed.

Parameter information continues to be exchanged in this manner, with alternate reversal of the roles of originating and answering TA until the outcome is successful, unsuccessful, or Timer T1 expires.

In order that the service offered is not degraded from that provided without IPE, a TA should connect using its default parameters upon expiry of Timer T1. This does not prohibit either TA initiating disconnection at any time.

I.5.3.3 *Successful exchange*

A parameter exchange is considered successful when the last set of TA parameters transferred in both directions are compatible, or when the answering TA can adapt to the parameters of the originating TA. The answering TA shall notify the originating TA of a successful exchange before proceeding; this notification is provided by the transmission of a sequence of READY status octets. Both TAs shall set the re-entry flag to ONE. In any case, both TAs will proceed into the data transfer state (see § I.5.5.1) unless re-synchronization to a new intermediate rate is required (see § I.5.4).

I.5.3.4 *Unsuccessful exchange*

If at any time during the exchange either TA concludes that a successful exchange of parameters cannot be achieved or that the rate adaption protocols are not compatible, the TA should clear the connection.

I.5.4 *Re-synchronization to a new intermediate rate*

If the outcome of the IPE is the selection of a user data rate requiring a new intermediate rate, re-synchronization will be necessary, and the TA enters the Awaiting Re-synchronization state (State 8). Whilst in this state the transmitter of the TA will send frames with S = OFF and X = OFF towards the peer TA in the new intermediate rate channel agreed. The default intermediate-rate channel positions correspond to those recommended for single stream operation in Recommendation I.460.

At the same time, the receiver of the TA will commence searching for the frame synchronization pattern in the selected sub-rate channel. When the TA recognizes the frame synchronization pattern, it shall verify the status information received and enter the appropriate state, in a coordinated manner, as follows:

- Data Transfer (State 4), upon receipt of S = ON and X = ON (see § I.5.6.),
- No Exchange (State 9), upon receipt of S = OFF and X = OFF.

When the TA is in the No Exchange state (State 9), it shall transmit frames with status information S = ON and X = ON and enter the data transfer state (State 4) upon receipt of S = ON and X = ON.

I.5.5 *Data transfer*

I.5.5.1 *Transition into the data transfer state*

Entry into the Data Transfer state should be carried out in a coordinated manner, as described by Recommendation V.110 by both TAs after sufficient time has been given to enable the processing of the parameter information.

I.5.5.2 *The data transfer state*

The procedures on entering the Data Transfer state (State 4) and the values of S and X status information in the case of data rates less than 56 kbit/s are described in Recommendation V.110.

I.5.6 *Interworking with a TA not supporting IPE*

A TA may choose to by-pass IPE; for example, when it is used in a pre-configured arrangement, or when the parameter exchange can be effected by out-of-band signalling. In this situation a TA supporting IPE may receive S = ON and X = ON verified status information, causing the TA to directly enter the Data Transfer state. See § I.8.

A TA not supporting IPE can receive frames containing the status information S = OFF and X = ON from its peer. In this situation the non-IPE TA may either continue to transmit the status information S = OFF and X = OFF, or change to the Data Transfer state and transmit the status information S = ON and X = ON. Both cases will lead to entry into the Data Transfer state without IPE. See § I.8.

In the case of IPE at 64 kbit/s unrestricted or restricted, or in the case of a TA continuing to transmit the status information S = OFF and X = OFF, Timer T2 ensures that service is not degraded from that provided without IPE. See § I.8.

I.5.7 *Maintenance*

A TA maintenance (MNT) call is made by indicating in PARAM-0 that the calling TA requires MNT support and by directly following the parameter transfer with a MAINTENANCE message group identifying the function required (see § I.6.6). A TA which supports MNT shall indicate in PARAM-0 that MNT support is available. When an MNT function is requested by a calling TA, the called TA capable of supporting MNT shall acknowledge the request by initiating a subsequent parameter exchange including at the end the identical MAINTENANCE message group, before continuing directly to invoke the required MNT function.

A successful MNT call with no timer required is terminated by either TA clearing the call. A successful MNT call with timer required returns the called TA to the inactive state upon expiry of Timer T3, or to the Null state upon disconnection.

A TA which does not support MNT shall indicate in PARAM-0 of the initial exchange that no MNT support is provided, and should clear the connection after the initial parameter exchange when an MNT call is received.

I.5.8 *Re-entering IPE from the data transfer state*

Test loopbacks in this Recommendation refer to the I.600-Series. The major application of this facility is to provide a mechanism to allow a remote loopback to be established for maintenance purposes without disconnecting the equipment in the established path. This mechanism may also be used generally to re-enter IPE.

This mechanism is not applicable to unrestricted 64 kbit/s or restricted 64 kbit/s connection types, or when the rate during data transfer is 64 kbit/s, 56 kbit/s or 48 kbit/s.

If re-entry to IPE is required and the Re-entry flag has the value ONE then the initiating TA enters the Awaiting Re-entry to IPE state (State 10) and transmits S = OFF, X = ON and D = IDLE. Re-entry to IPE in order to set a test Loop 4 shall only be initiated by a calling TA.

Receipt of S = OFF, X = ON and D = IDLE shall cause a TA in State 4 to re-enter the Parameter Exchange state (State 7) at the IPE user rate defined in § I.5.1 which is of the same intermediate rate as that used for data transfer.

Receipt of S = OFF, X = ON and D = IDLE shall cause the initiating TA to re-enter the Parameter Exchange state (State 7) at the IPE user rate defined in § I.5.1 which is of the same intermediate rate as that used for data transfer.

I.5.9 *Error protection and handling*

Error protection and handling is required to overcome the possibility of data corruption. In addition, error recovery procedures are required, for example in the case of loss of frame synchronization.

To protect against data corruption, IPE commands shall be sent in a repeated sequence of at least 32 octets. Verification of the correct receipt of a command octet can then be carried out based on persistence checking techniques. Once a verified command octet has been received, it can be identified by the codings given in § I.6. Any command octet not recognized shall be ignored. To protect against data corruption, LOW-HIGH data message pairs shall be sent in groups of three pairs. This enables majority voting techniques to be employed by the receiving TA.

Upon the detection of irrecoverable data corruption during the parameter exchange, loss of frame synchronization or other situations requiring the exchange to be restarted, the TA shall complete the current message flow and initiate error recovery by transmitting a sequence of XSTART command octets and assuming the role of the originating TA. Upon receipt of a sequence of XSTART commands octets, a TA will recommence the parameter exchange as described in § I.5.3.2. In this case of a collision of XSTART octets, the original originating and answering roles are assumed by the TAs.

I.6 *Coding*

I.6.1 *General*

Information transfer during IPE is based on a group of messages. These messages are used to carry out a variety of tasks. The messages associated with rate adaption identification are described in § I.6.2, whilst those associated with the actual parameter transfer are given in § I.6.4. The messages associated with the control of the IPE are described in § I.6.3, and § I.6.5 covers those used to indicate status. Finally, § I.6.6 covers the coding of the maintenance message.

The messages are all based on octets structured as shown in Figure I-4/V.110.

In the case of a user rate of 64 kbit/s, the octets are transmitted to line in bit sequence from bit 1 to bit 8. Network-provided octet alignment shall be used.

In the case of a user rate of 56 kbit/s, the data is transmitted to line in bit sequence from bit 1 to bit 7 followed by an 8th bit set to ONE – according to the Recommendation V.110, rate adaptation (in total this is the equivalent data stream to 64 kbit/s). Network-provided octet alignment shall be used.

In the case of user rates of 4.8, 9.6 or 19.2 kbit/s, the octets are packaged as single start-stop characters, using the following format:

- 1 start bit,
- 8 data bits (in order of transmission shown in Figure I-3/V.110),
- No parity, and
- 1 stop bit.

Figure I-5/V.110 provides a complete set of octet codings for use in IPE.

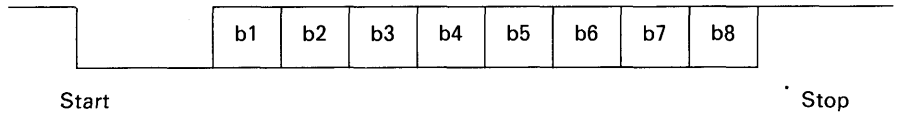
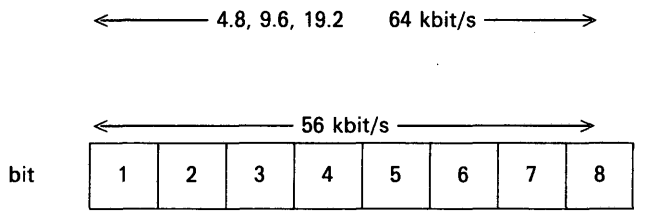


FIGURE I-3/V.110

Asynchronous character format



bit 8: Set to ONE (and ignored on receipt)

Note – Equivalent data stream to that for 64 kbit/s is created with 56 kbit/s when rate adaptation according to Rec. V.110 is used.

bit 7: Set to ZERO for IPE data
Set to ONE for IPE signal

For IPE data

bit 6: Set to ONE
(Set to ZERO: message reserved for private use and ignored if not implemented)

bit 5: Set to ZERO when carrying data bits d0-d3
Set to ONE when carrying data bits d4-d7

bits 1-4: Carrying data bits (d0-d3) or (d4-d7)

For IPE signal

bit 6: Set to ONE
(Set to ZERO: message reserved for private use and ignored if not implemented)

bit 5: Set to ZERO for command messages
Set to One for status messages

bits 1-4: The signal code

FIGURE I-4/V.110

Octet structure of the IPE coding

		Message	←4.8, 9.6, 19.2 & 64 kbit/s→							
			←56 kbit/s→							
			b1	b2	b3	b4	b5	b6	b7	b8
IPE Signals	Command	PARAM-0	0	0	0	0	0	1	1	1
		PARAM-1	0	0	0	1	0	1	1	1
		PARAM-2	0	0	1	0	0	1	1	1
		PARAM-3	0	0	1	1	0	1	1	1
		PARAM-4	0	1	0	0	0	1	1	1
		RA VERSION	0	1	0	1	0	1	1	1
		XSTART	0	1	1	0	0	1	1	1
		MAINTENANCE	0	1	1	1	0	1	1	1
	Status									
		READY	0	1	0	1	1	1	1	1
		IDLE	0	1	1	1	1	1	1	1
		FILL	1	1	0	1	1	1	1	1
		INACTIVE	1	1	1	1	1	1	1	1
IPE data										
		LOW	d0	d1	d2	d3	0	1	0	1
		HIGH	d4	d5	d6	d7	1	1	0	1

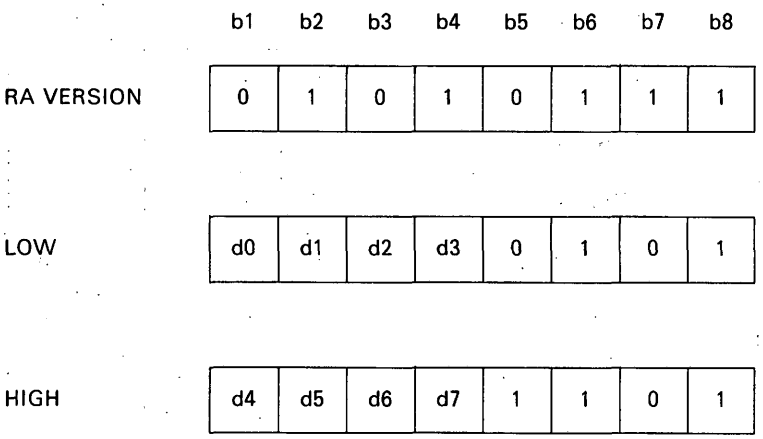
Note – All spare codings are reserved (unless indicated for private use). Any octet received, and verified, which is not recognized shall be ignored.

FIGURE I-5/V.110

IPE octet codings

I.6.2 *Rate adaption version identification*

Transfer of the rate adaption identifier is achieved by a message group based on three octets and transferred according to the procedures described in §§ I.5.3.2 and I.5.9. The message consists of a sequence of RA VERSION command octets followed by a series of LOW-HIGH data octet pairs, the LOW data octet being transmitted in the pair before the HIGH data octet. Figure I-6/V.110 shows the message codings for rate adaption identification.



Rate adaptation version identifier encoding

	HIGH				LOW			
	d7	d6	d5	d4	d3	d2	d1	d0
	I3	I2	I1	I0	x	x	x	x
13-10:	I3	I2	I1	I0				
Identifier V.110	0	0	0	1				

x: Reserved (if not used set ZERO and ignored on receipt)

Note – All other codings are reserved.

FIGURE I-6/V.110

Rate adaption version identifier

I.6.3 *Control*

Before each transfer of TA parameter information can begin, a sequence of XSTART command octets is transmitted by the originating TA towards the answering TA as described in §§ I.5.3.2 and I.5.9. Figure I-7/V.110 shows the coding for the XSTART command octet.

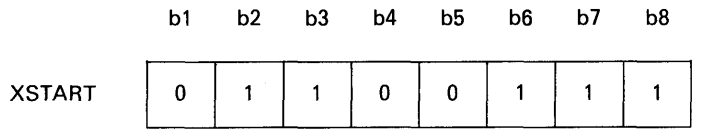


FIGURE I-7/V.110

XSTART coding

I.6.4 *Parameters*

Transfer of the TA parameters is achieved in a series of five message groups each based on three octets and transferred according to the procedures described in §§ I.5.3.2 and I.5.9. Each message group consists of a sequence of PARAM-X command octets (PARAM-0 to PARAM-4) followed by a series of LOW-HIGH data octet pairs, the LOW data octet being transmitted in the pair before the HIGH data octet. Figure I-8/V.110 shows the command octet codings and Figures I-9/V.110 to I-13/V.110 show the data octet codings for parameter transfer.

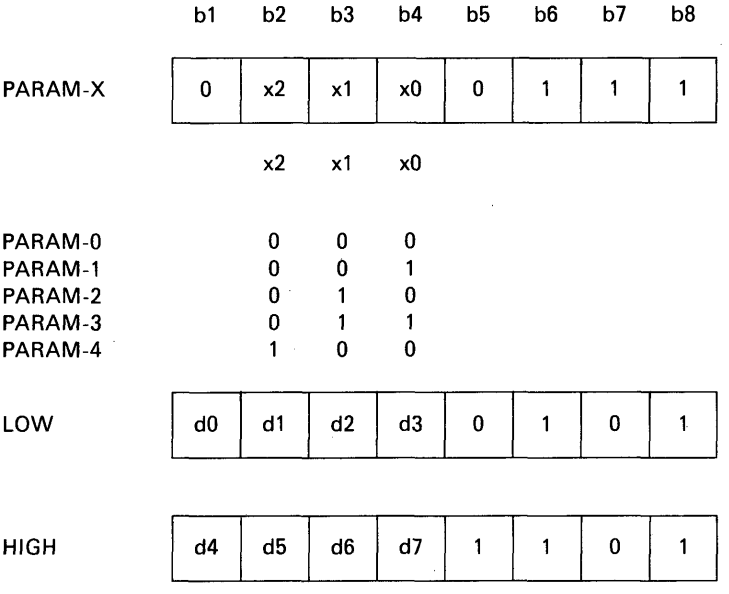


FIGURE I-8/V.110

Format of parameter message group

HIGH				LOW			
d7	d6	d5	d4	d3	d2	d1	d0
Sp	Sp	Ms	Mr	x	x	x	Ex

Sp (Spare): Set to ZERO on transmission, ignored on reception.

Ms (Maintenance supported):
Maintenance not supported 0
Maintenance supported 1

Mr (Maintenance required):
Maintenance not required 0
Maintenance required 1

Ex (Extension):
If TA does not require octet alignment according to Rec. X.30. 0
If TA does require octet alignment according to Rec.X.30. 1

x: Reserved
(if not used set to ZERO and ignored on receipt)

FIGURE I-9/V.110

Parameter 0 encoding

HIGH				LOW			
d7	d6	d5	d4	d3	d2	d1	d0
P2	P1	P0	Mo	x	x	x	Ch

P2-P0: Parity

	P2	P1	P0
Odd	0	0	0
Even	0	1	0
None	0	1	1
Forced to ZERO	1	0	0
Forced to ONE	1	0	1

Mo (Mode):
Asynchronous 0
Synchronous 1

Ch (Check):
DTE Parity check made when required 0
No DTE parity check made when required 1

x: Reserved
(if not used set to ZERO and ignored on receipt)

FIGURE I-10/V.110

Parameter 1 encoding

HIGH				LOW			
d7	d6	d5	d4	d3	d2	d1	d0
S1	S0	C1	C0	x	x	x	Cx

S1-S0: Stop bits

	S1	S0
Not used	0	0
1	0	1
1,5	1	0
2	1	1

C1-C0: Character length

	C1	C0
Not used	0	0
5	0	1
7	1	0
8	1	1

Note – Character length includes parity.

Cx (Character length extension):

Standard C1-C0 codings used	0
9-bits character length used	1

x: Reserved
(if not used set to ZERO
and ignored on receipt)

FIGURE I-11/V.110

Parameter 2 coding

HIGH				LOW			
d7	d6	d5	d4	d3	d2	d1	d0
Sp	R6	R5	R4	R3	R2	R1	R0

Sp(d7): Set to ZERO on transmission, ignored on reception.

R6-R0: Rates	R6	R5	R4	R3	R2	R1	R0
Reserved	0	0	0	0	0	0	0
600	0	0	0	0	0	0	1
1200	0	0	0	0	0	1	0
2400	0	0	0	0	0	1	1
3600	0	0	0	0	1	0	0
4800	0	0	0	0	1	0	1
7200	0	0	0	0	1	1	0
Reserved	0	0	0	0	1	1	1
9600	0	0	0	1	0	0	0
14 400	0	0	0	1	0	0	1
Reserved	0	0	0	1	0	1	0
19 200	0	0	0	1	0	1	1
Reserved	0	0	0	1	1	0	0
Reserved	0	0	0	1	1	0	1
48 000	0	0	0	1	1	1	0
56 000	0	0	0	1	1	1	1
Reserved	0	0	1	0	0	0	0
50	0	0	1	0	0	0	1
75	0	0	1	0	0	1	0
110	0	0	1	0	0	1	1
150	0	0	1	0	1	0	0
200	0	0	1	0	1	0	1
300	0	0	1	0	1	1	0
12 000	0	0	1	0	1	1	1
Reserved	0	0	1	1	0	0	0
				to			
Reserved	1	1	1	1	1	1	0
64 000	1	1	1	1	1	1	1

FIGURE I-12/V.110

Parameter 3 encoding

HIGH				LOW			
d7	d6	d5	d4	d3	d2	d1	d0
Sp	Fc	TNIC	RNIC	x	x	x	Mm

NIC Network Independent Clock (see § 5)

Sp (Spare): Set to ZERO on transmission, ignored on reception.

Fc (Flow control):
No end-to-end flow control supported 0
End-to-end flow control supported 1

TNIC: if TA need not use NIC 0
if TA needs to use NIC 1

RNIC: if TA cannot accept NIC 0
if TA can accept NIC 1

Mm (Modem):
TA not connected to a modem 0
TA connected to a modem 1

x: Reserved
(if not used set to ZERO and ignored on receipt)

FIGURE I-13/V.110

Parameter 4 encoding

I.6.5 *Status*

To inform the peer TA that a parameter exchange has been successful, a sequence of READY status octets shall be transmitted towards the peer according to the procedures in § I.5. Figure I-14/V.110 shows the coding for the READY status octet.

To inform the peer TA that it is in an idle condition prior to parameter exchange, a sequence of IDLE status octets are transmitted towards the peer according to the procedures in § I.5. Figure I-15/V.110 shows the message coding for the IDLE status octet.

The FILL status octet is used as a fill between parameter transfers, according to the procedures in § I.5. Figure I-16/V.110 shows the coding for the FILL status octet.

To inform the peer TA that the channel is currently inactive, a sequence of INACTIVE status octets are transmitted towards the peer according to the procedures in § I.5. Figure I-17/V.110 shows the coding for the INACTIVE status octet.

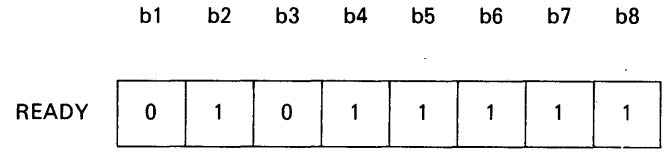


FIGURE I-14/V.110

READY octet coding

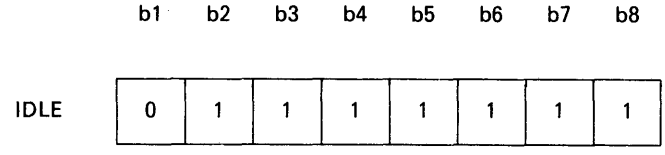


FIGURE I-15/V.110

IDLE octet coding

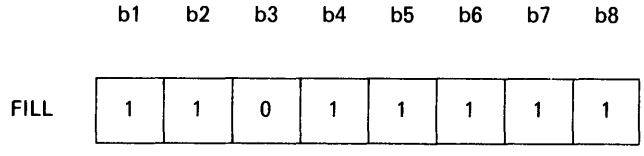


FIGURE I-16/V.110

FILL octet coding

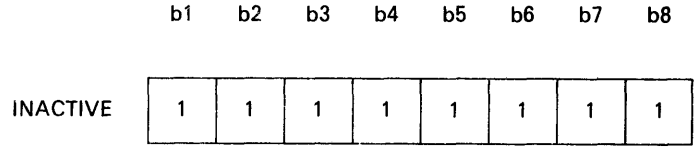


FIGURE I-17/V.110

INACTIVE octet coding

I.6.6 *Maintenance*

This message group based on three octets is used to carry information in association with maintenance operations. The message group consists of a sequence of MAINTENANCE command octets followed by a series of LOW-HIGH data octet pairs, the LOW data octet being transmitted in the pair before the HIGH data octet. Figure I-18/V.110 shows the message codings.

	b1	b2	b3	b4	b5	b6	b7	b8
MAINTENANCE	0	1	1	1	0	1	1	1
LOW	d0	d1	d2	d3	0	1	0	1
HIGH	d4	d5	d6	d7	1	1	0	1

Maintenance encoding

HIGH				LOW			
d7	d6	d5	d4	d3	d2	d1	d0
Sp	Rt	L1	L0	x	x	x	R1

Sp(d7): SET to ZERO on transmission, ignored on reception

Rt (Request for timer T3 – § I.5.7):
- No timer required: 0
- Timer required: 1

L1-L0 (Loop required):

	L1	L0
No loopback	0	0
Test loop 4 (I.600-Series)	0	1
Reserved	1	0
Reserved	1	1

R1 (d0 Test loop 5) (I.600-Series):
- Test loop 5 not required: R1 = 0
- Test loop 5 required: R1 = 1

x: Reserved (if not used set to ZERO and ignored on receipt)

Note 1 – Test loop 5 is applied as near to the interface at the R reference point as practicable, and is outside the scope of this Recommandation.

Note 2 – Loop definitions 4 and 5 are defined in the I.600-Series.

Note 3 – Definitions are for the direction of calling TA to called TA. In the reverse direction they represent confirmation of the maintenance function.

FIGURE I-18/V.110

Coding of MAINTENANCE message group

I.7 *Timer values*

I.7.1 *Timer values for parameter exchange*

Timer T1 shall be at least 8 seconds but less than Timer T1 in § 4.1.2.2.

Timer T2 shall be 3 seconds.

I.7.2 *Timer values for maintenance*

Timer T3 shall be 60 seconds.

I.8 *State transition diagrams*

I.8.1 *General*

In this section, state transition diagrams are provided to show the states of a terminal adaptor in the following situations:

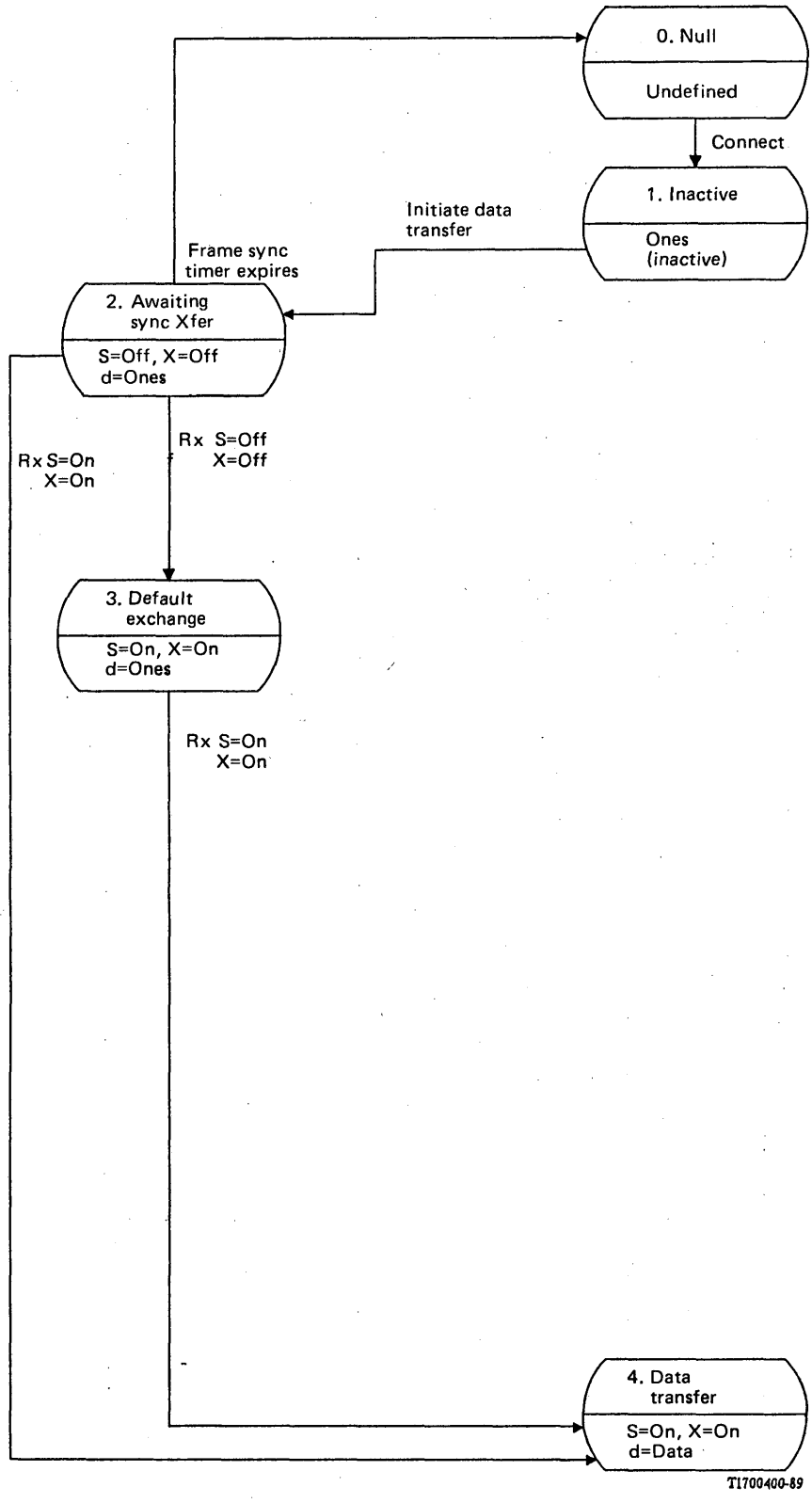
- a terminal adaptor not supporting the exchange of parameter information (Figure I-19/V.110);
- a terminal adaptor interworking with a terminal adaptor not supporting the exchange of parameter information (Figure I-20/V.110);
- a terminal adaptor capable of supporting the exchange of parameter information (Figure I-21/V.110);
- a terminal adaptor capable of supporting a maintenance test loop 4 (Figure I-22/V.110).

Following is a summary of the basic states involved:

State 0 Null
State 1 Inactive
State 2 Awaiting synchronization – data transfer
State 3 Default exchange
State 4 Data transfer
State 5 IPE default exchange
State 6 Awaiting synchronization – parameter exchange
State 7 Parameter exchange
State 8 Awaiting re-synchronization
State 9 No exchange
State 10 Awaiting re-entry to IPE
State 11 Maintenance loop 4 loopback

I.8.2 *List of acronyms*

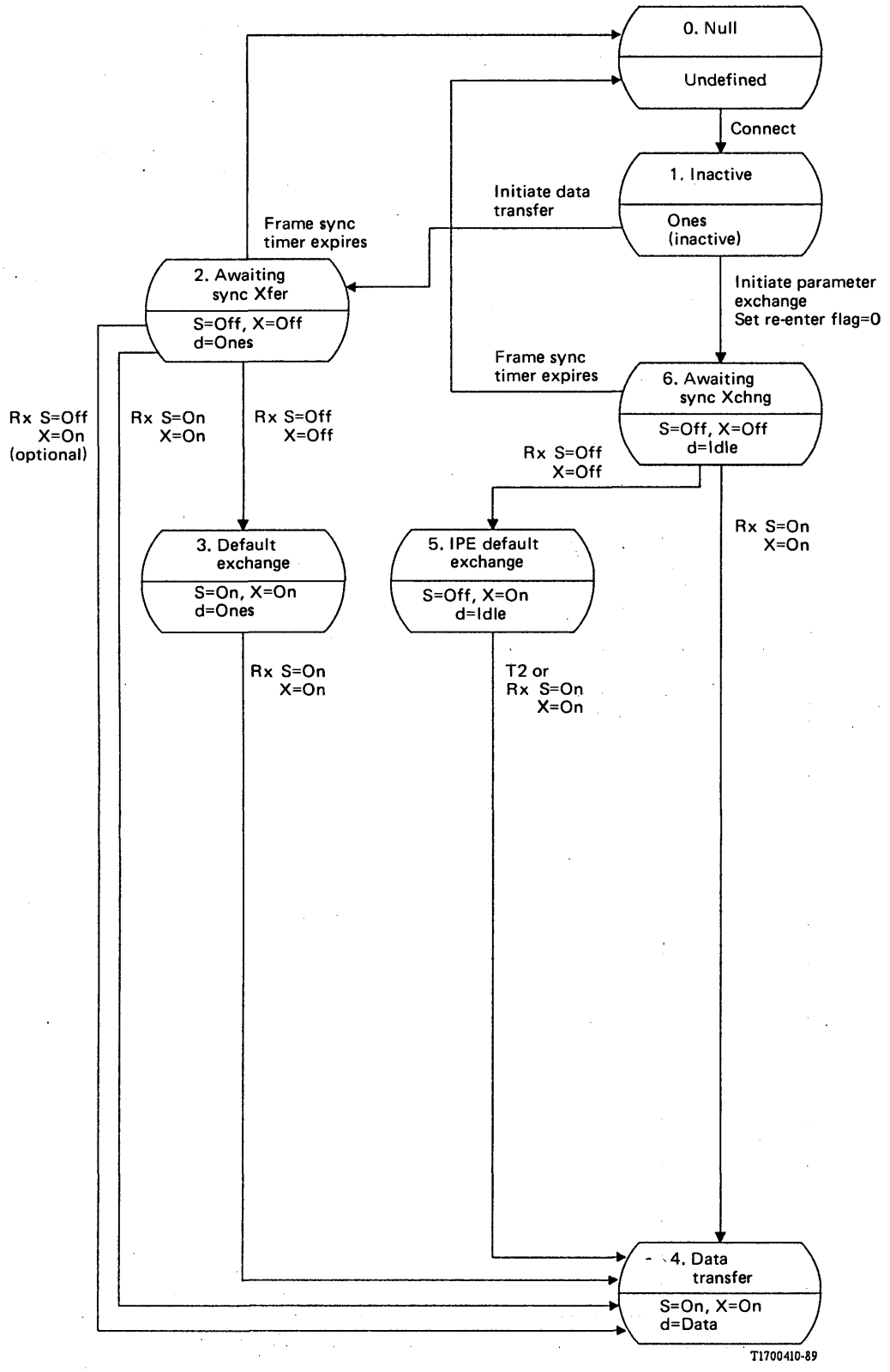
DTE	Data Terminal Equipment
ISDN	Integrated Services Digital Network
IPE	In-band Parameter Exchange
IWF	Inter-Working Function
MNT	Maintenance
Mm	Modem
NIC	Network Independent Clock
PARAM-X	Parameter X (X = 0,1,2,3,4)
PSTN	Public Switched Telephone Network
RA	Rate Adaption
TA	Terminal Adaptor
TE1	Terminal Equipment Type 1
TE2	Terminal Equipment Type 2
Tn	Timer Tn (n = 1,2,3)



Note – Release sequences not shown.

FIGURE I-19/V.110

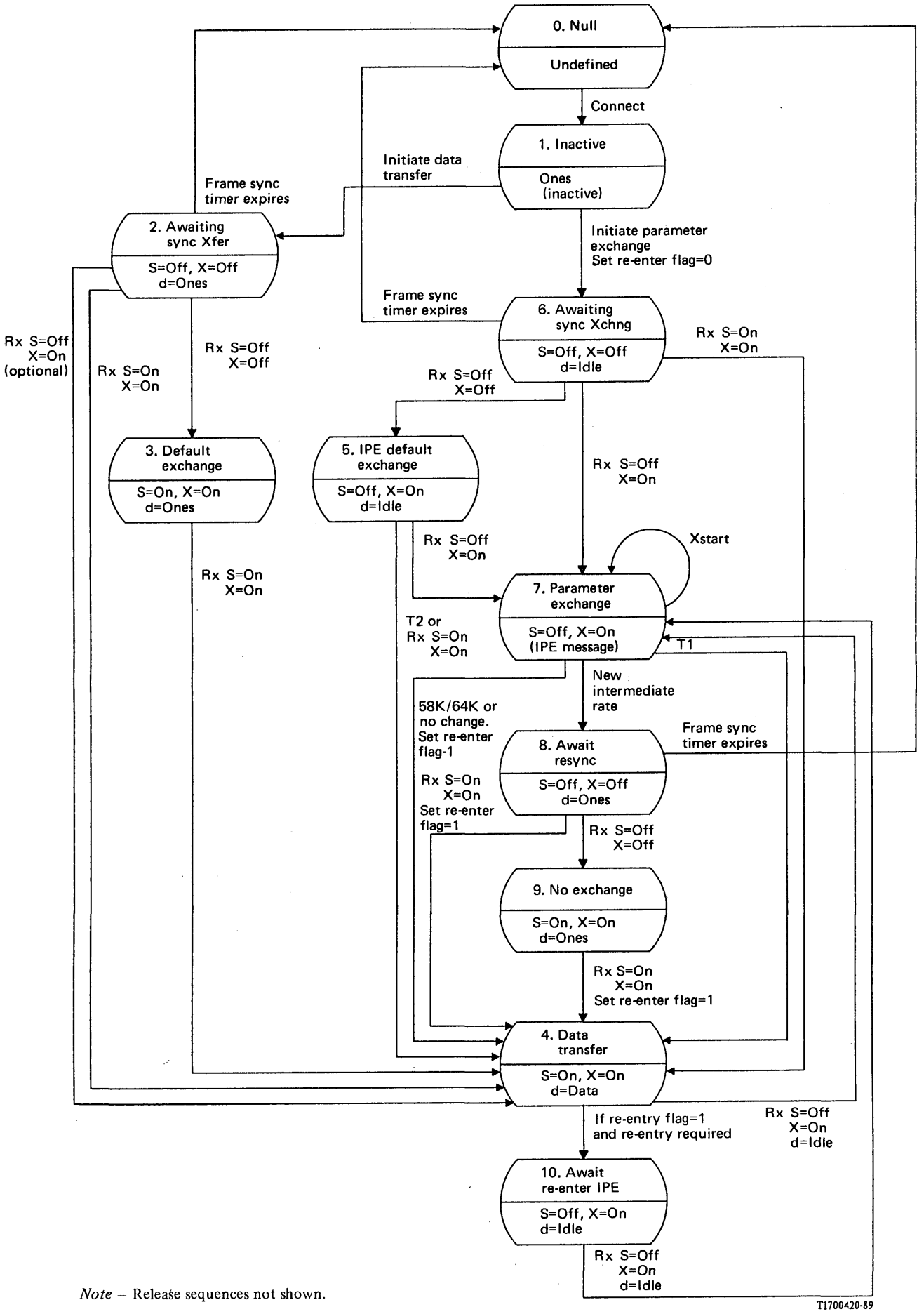
State diagram: TA' not supporting IPE



Note – Release sequences not shown.

FIGURE I-20/V.110

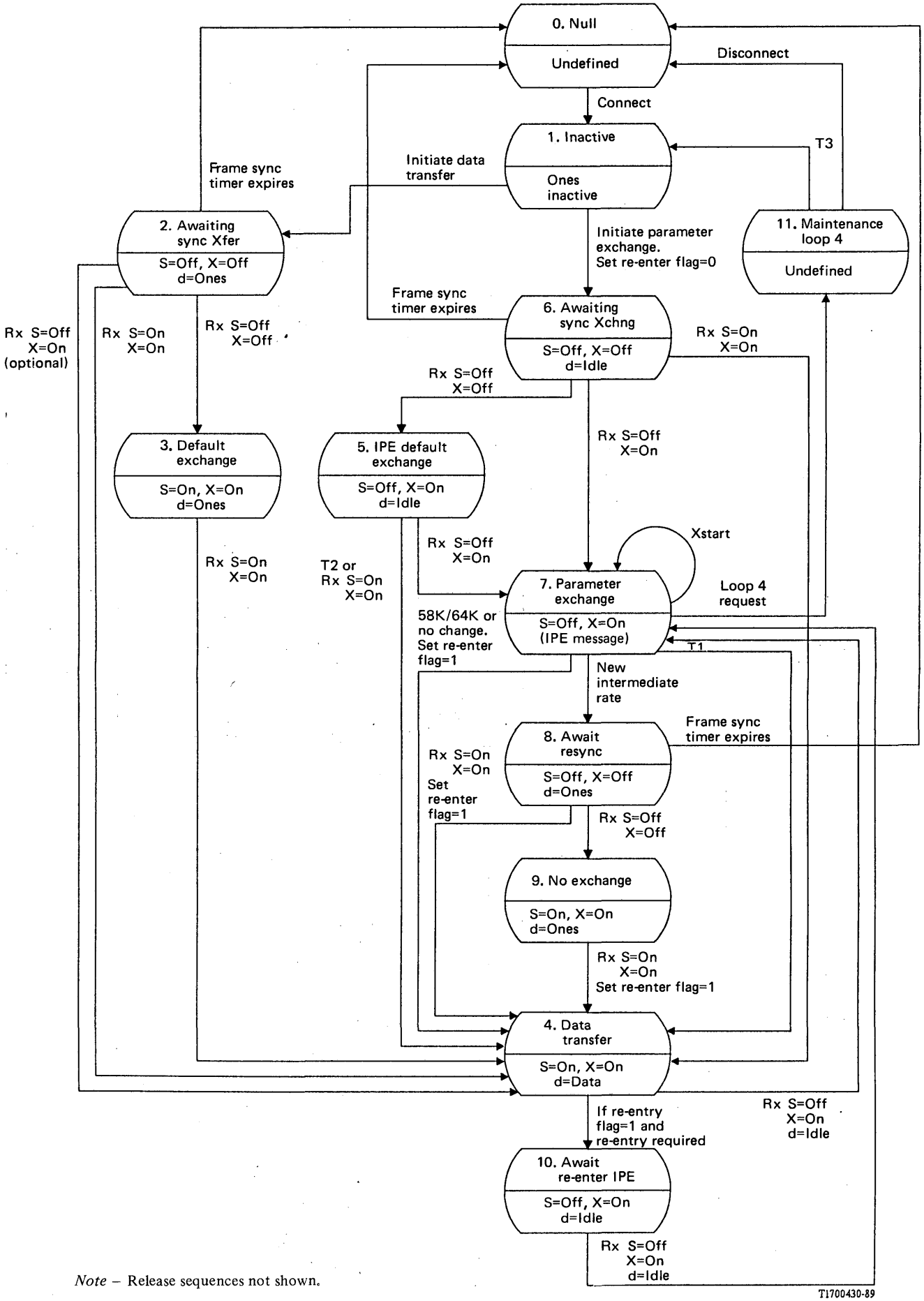
State diagram: Interworking with a TA' not supporting IPE



Note – Release sequences not shown.

FIGURE I-21/V.110

State diagram: TA' supporting IPE



Note – Release sequences not shown.

FIGURE I-22/V.110

State diagram: Maintenance Loop 4

Recommendation V.120

SUPPORT BY AN ISDN OF DATA TERMINAL EQUIPMENT WITH V-SERIES TYPE INTERFACES WITH PROVISION FOR STATISTICAL MULTIPLEXING

(Melbourne, 1988)

The CCITT,

considering

(a) that the ISDN will offer the universal interfaces to connect subscriber terminals in accordance with the reference configuration described in Recommendation I.411;

(b) that during the evolution of ISDN there will exist for a considerable period DTEs with V-Series interfaces which need to connect to ISDN;

(c) that it would be desirable that terminals with V-Series interfaces interwork easily with ISDN TE1s;

(d) that statistical multiplexing provides improved utilization of bandwidth in some applications;

(e) that the D channel signalling protocol is described in Recommendations I.430, I.431, Q.921 and Q.931;

(f) that there exists CCITT Recommendation V.110 for adapting DTEs with a V-Series interface onto B Channels;

unanimously declares

(1) that the scope of this Recommendation shall cover the connection to the ISDN of terminals with interfaces for modems conforming to current V-Series Recommendations, operating in accordance with circuit or leased circuit bearer services on bearer channels (B, H0, H11 or H12) (see Note);

(2) that the following circuit-switched services may be supported:

- multiplexing of several data links on a single bearer channel; (and/or)
- automatic establishment and disestablishment of additional data links;

(3) that the reference configurations of § 1 shall apply;

(4) that the terminal adaptor (TA) functions necessary to support the connection of DTEs with V-Series type interfaces on an ISDN shall include the following:

- conversion of the electrical and mechanical interface characteristics;
- bit rate adaption;
- end-to-end synchronization;
- call establishment and disestablishment based on either manual or automatic calling and/or answering;
- maintenance functions.

Note – The compatibility of V.120 with protocols developed in other Study Groups for Additional Packet Mode Bearer Service (APMBS) as defined in Recommendation I.122 is for further study and the provisions of this Recommendation, V.120, shall not prejudice this study.

Significant further study related both to aspects of the protocol and the alignment with other ISDN protocols is needed on this Recommendation.

1 Reference configurations

1.1 *Customer access configurations*

There are two basic classes of devices capable of data transmission in the ISDN environment:

- devices directly attached to the ISDN, i.e. TE1s; and
- devices attached to the ISDN through a terminal adaptor, i.e. V-Series TE2s.

1.2 *Connectivity*

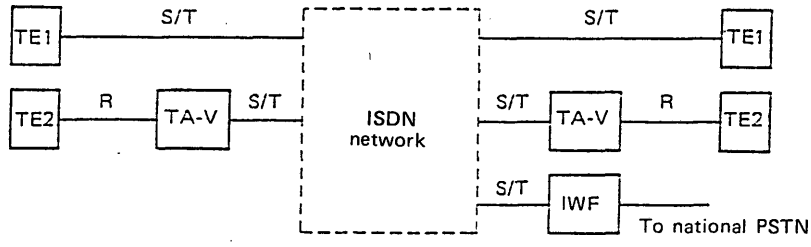
ISDN connectivity requirements include support for TE1-to-TE1, TE2-to-TE2 (TA-to-TA) and TE1-to-TE2 (TE1-to-TA) connections as discussed and illustrated in Figure 1/V.120. This document specifies a terminal adaption protocol based on a modification of LAPD that supports these connections. LAPD is specified in CCITT Recommendation Q.921. The modifications are specified in § 2.4 of this Recommendation.

This protocol provides a consistent protocol for carrying different types of data streams (see §§ 3.3 to 3.5). This approach using a HDLC based protocol provides the capability for multiplexing multiple logical circuits on a channel. This also allows for different higher layer protocols to be running concurrently on a single channel (see § 2.2).

In come cases the speed of the communicating TE2s is the same. It is possible in certain cases to connect devices with different speeds using the frame encapsulation procedures described later in § 2, and in more detail in § 3. The key factors that make this concept viable are TA buffering, TA flow control, HDLC encapsulation and HDLC flow control.

The application of this protocol to TE1-to-TA applications is discussed in Appendix I.

Within I.515, parameter exchange procedureds are *generally described* to allow interworking between incompatible terminal adaptors (TAs) that may not require interworking functions within the network. Interworking between different types of TAs can be accomplished with Multifunctional Terminal Adaptors (MTAs) that are capable of supporting more than one protocol. However, Figure 1/I.515 also depicts other interworking scenarios that will require IWFs when TAs are not capable of supporting more than one protocol.



TA-V V.120 terminal adaptor supporting V-Series TE2s
IWF Interworking function

Note – Other configurations are shown in Recommendation I.515.

FIGURE 1/V.120

ISDN connection scenarios for V.120 terminal adaptors

2 Data transport protocol specification

This protocol relies on procedures similar to those in CCITT 1986 Recommendation Q.921/I.441. It provides the capability for use with compatible TE1 or TA equipments.

The use in TE1s of the protocols specified in this document is described in Appendix I. The remainder of this document is concerned with their use in TAs.

2.1 *Functions provided by protocol*

2.1.1 *Categories of functions*

There are two categories of functions provided by this specified protocol. There is a set of base functions and a set of additional functions. The additional functions depend upon the type of data flow (character coded or message).

2.1.2 *Base functions*

The base functions of the protocol include the following:

- transparent transport of data;
- generation and interpretation of messages for peer communication (i.e. post call connection handshake);
- administration of timers and counters used in communication;
- error detection.

2.1.3 *Additional functions*

The additional functions of the protocol include the following:

- transport and interpretation of interface status change at the R reference point;
- segmenting and reassembly of messages;
- transport of detected interface errors at the R reference point;
- support for operation with a network independent clock;
- multiplexing of synchronous and asynchronous protocols;
- interworking of two TEs operating at different data rates;
- flow control;
- retransmission on error detection.

2.2 *General terminal adaption*

The terminal adaption mechanisms are divided into two general categories:

- protocol sensitive operation for character or message encapsulation; and
- bit transparent operation where no alignment (above the bit level) of information from the interface at the R reference point is made within the frame transport in the bearer channel.

The interface bit rate at the R reference point must be less than the bearer channel capability. The terminal adaptor may support single or multiple interfaces at the R reference point. In the later case the protocol applies separately to the data streams associated with each interface. The use of logical link identifiers to distinguish between data streams will be described.

2.2.1 *Protocol sensitive operation with start/stop mode TE2s (asynchronous mode)*

The start and stop bits are removed and parity may be checked (see § 3.3.1). The resultant character(s) is placed in a frame for transport on the bearer channel to a peer entity. The peer entity may be in a peer TA where the reverse process takes place to another interface at an R reference point, or the peer entity may be in a TE1 where the character(s) is passed to a higher layer within the TE1, or in an interworking function. Errors detected on the interface at the R reference point are relayed to the peer entity which will:

1) notify the higher layer of the detected error; or
2) replicate the error (see §§ 3.3.1 and 3.3.2) at the outbound interface at the R reference point.

The terminal adaptor will recognize and remove any erroneous NULL characters (created by the initiation of BREAK) before transmission.

2.2.2 *Protocol sensitive operation with synchronous HDLC TE2s (synchronous mode)*

The flags and zero bit insertion are removed and the FCS is checked and removed but the address, control, and information fields flow transparently through the TA. The resultant octet-aligned message is placed in one or more frames for transport to a peer entity over the data link connection on the bearer channel. The original message from the interface at the R reference point may be segmented within the TA and forwarded in parts to the peer entity. This segmenting and forwarding process may occur as the message is received. This avoids the delays associated with accumulating a full message. The peer entity performs the reverse process at the peer interface R reference point.

If an FCS error is detected at the interface at the R reference point, this is relayed to the peer entity which will either:

1) discard the entire message; or
2) cause an abort to be sent on the interface at the R reference point in the message which is in progress; or
3) generate an incorrect FCS in the message which is in progress.

Note – Support of non-octet aligned messages is for further study.

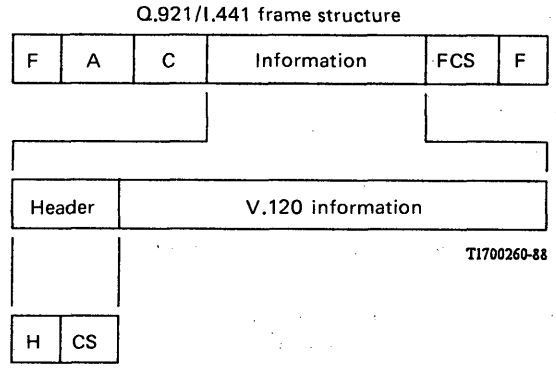
2.2.3 *Transport operation (bit transparent mode)*

In bit transparent operation the TA will encapsulate the bits from the interface at the R reference point into frames as they are received. These frames are forwarded to a peer entity. The peer TA removes the bits from the frames and sends them on the interface at the R reference point. No processing or modification of the bits is performed and there is no checking fot bit stream errors on the interface at the R reference point. This mode is used for all modes not covered by the asynchronous or synchronous modes defined above.

Note – In many cases UI frames will be used to convey frames in this mode.

2.3 *General messages and formats*

The frame structure used is that specified in Recommendation Q.921/I.441. There is an optional one or two octet header. The header octet(s), when present, directly follows the control field of the V.120 frame as shown in Figure 2/V.120.



F HDLC flag
A Address (default is 2 octets)
C Control (HDLC formats)
FCS Frame check sequence
H Terminal adaption header (optional for bit transparent mode)
CS Optional header extension for control state information

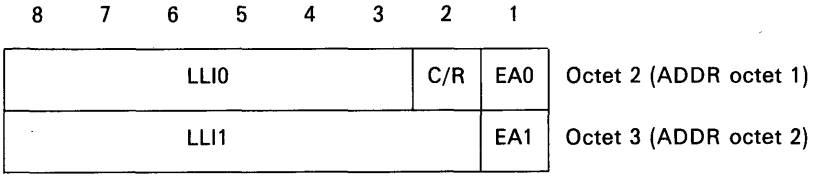
Note – The A, C, H, CS and information fields are transmitted an octet at a time, low order bit first (bit 1). The FCS is transmitted high order bit first.

FIGURE 2/V.120

Frame format

2.3.1 *Address field*

The format of the V.120 address field in Figure 2/V.120 is similar to that specified in Recommendation Q.921/I.441. The LLI0 and LLI1 fields may be viewed as a single 13 bit logical link identifier (LLI) field or alternatively as two separate fields. This is shown in Figure 3/V.120.



LLI0 High order 6 bits of LLI
LLI1 Low order 7 bits of LLI
C/R Command/response bit
EA0 Octet 2 address extension bit – set to 0
EA1 Octet 3 address extension bit – set to 1 (for two octet address field)

FIGURE 3/V.120

Address field format

The LLI is considered to be the concatenation of the LLI0 field with the LLI1 field. The LLI can take on values in the range 0-8191. Table 1/V.120 indicates values that are reserved.

TABLE 1/V.120

Reserved LLI values

LLI	Function
0	In-channel signalling
1-255	Reserved for future standardization
256	Default LLI
257-2047	For LLI assignment
2048-8190	Reserved for future standardization
8191	In-channel layer management

2.3.2 *Address extension bit (EA)*

The address field range is extended by using bit 1, the first transmitted bit, of the address field octets to indicate the final octet of the address field. The presence of a "1" in bit 1 of an address field octet signals that it is the final octet of the address field.

2.3.3 *C/R bit*

The C/R bit identifies a V.120 frame as either a command or a response (see § 2.4). The C/R bit is employed symmetrically for the two directions of transmission and is coded as shown in Table 2/V.120.

TABLE 2/V.120

Coding of C/R bit

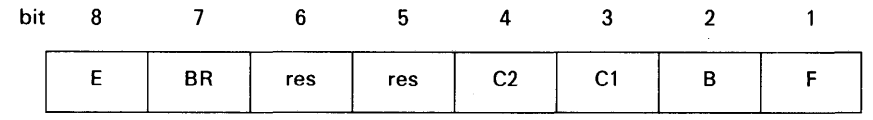
C/R	Meaning
0	Command
1	Response

2.3.4 *Control field*

The use of the V.120 control field is described in § 2.4.

2.3.5 *Header octet*

The format of the header octet is shown in Figure 4/V.120 (see §§ 3.3 to 3.5 for details on the use of these fields). The header octet is mandatory for protocol sensitive modes and is optional for bit transparent mode.



E Extension bit
BR Break/HDLC idle bit
C1, C2 Error control bits
B, F Segmentation bits
res Reserved for future standardization

FIGURE 4/V.120

Header octet format

2.3.5.1 *E-extension bit (bit 8)*

The E bit is the header extension bit. It allows for extension of the header to provide additional control state information. A "0" bit indicates that a control state information octet follows (see § 2.3.6).

2.3.5.2 *BR-break/HDLC idle bit (bit 7)*

In asynchronous applications, the break bit indicates the invocation of the BREAK function by the TE2. A "1" in this bit position indicates BREAK (see § 3.3).

In protocol sensitive operation for synchronous HDLC applications, the BR bit is used to indicate an HDLC idle condition on the interface at the R reference point. A "1" in this bit position indicates that the interface at the R reference point is receiving HDLC idle condition (see § 3.4).

2.3.5.3 *Bits 5 and 6*

Bit 5 and bit 6 of the header octet are reserved and set to "0".

2.3.5.4 *C1, C2-error control (bits 3 and 4)*

Bit 3 and bit 4 of the header octet are defined as Control 1 and Control 2 respectively and are used for TA error detection and transmission.

The meanings of the C1 and C2 bits are encoded as shown in Table 3/V.120.

TABLE 3/V.120

Coding of C1 and C2 bits

C1	C2	Meaning		
		Synchronous	Asynchronous mode	Bit transparent mode
0	0	No error detected	No error detected	No error detected
0	1	FCS error (interface at R)	Stop-bit error	Not applicable
1	0	Abort	Parity error on the last character in frame	Not applicable
1	1	TA overrun (from interface at the R reference point)	Both stop-bit and parity error	Not applicable

2.3.5.5 *B, F-segmentation bits (bit 2 and bit 1)*

The B and F bits are used for segmenting and reassembly of messages in synchronous mode applications. Setting the B bit to "1" indicates that the frame contains an information portion beginning a message. Setting the F bit to "1" indicates the frame contains the final portion of the message. If the entire message is contained within a single frame then both B and F bits will be set to "1". A frame which is neither first nor last is termed a middle frame. For the asynchronous mode and the bit transparent mode these bits are set to "1".

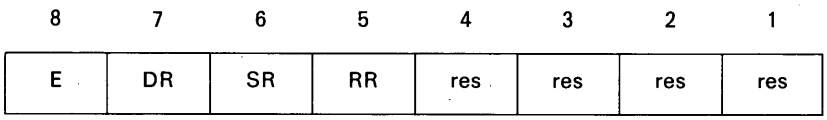
TABLE 4/V.120

Coding of B and F bits

B	F	Synchronous	Asynchronous	Bit transparent
1	0	Begin frame	Not applicable	Not applicable
0	0	Middle frame	Not applicable	Not applicable
0	1	Final frame	Not applicable	Not applicable
1	1	Single frame	Required	Required

2.3.6 *Control state information*

The control state information is contained in the second octet of the header when present. In general, for TAs, this field serves as a physical status/interface control field for the interface at the R reference point. Control state information may be sent whenever one of the mapped control leads changes, although the TA should be able to accept the CS octet anytime the H field is present. Figure 5/V.120 shows the format of the control state information octet. For an example of the mapping of the V.24 leads, see Annex A. See § 2.6 for the procedures and see § 3.2.1 for the use of the RR bit for flow control.



E Extension bit
DR Data ready
SR Send ready
RR Receive ready
res Reserved for future standardization

FIGURE 5/V.120

Control state information octet

2.3.6.1 *E-extension bit (bit 8)*

The extension bit allows for further extension of the header octets. The E bit set to "1" to indicate no further extension of the header.

2.3.6.2 *DR – data ready (bit 7)*

This bit set to "1" indicates that the interface at the R reference point is activated. For TE1 it implies the terminal interface is activated.

2.3.6.3 *SR – send ready (bit 6)*

This bit set to "1" indicates that the TE is ready to send data.

2.3.6.4 *RR – receive ready (bit 5)*

This bit set to "1" indicates that the TE is ready to receive data.

2.3.6.5 *Bits 4, 3, 2, 1*

Bits 4, 3, 2 and 1 of the control state information octet are reserved and set to "0".

2.3.7 *Interframe time fill*

Interframe time fill should normally be HDLC flags. For special applications it may be all ones.

2.4 *Elements of procedure and procedures*

Two types of logical connections are available using the procedures described in this specification, namely:

1) support of unacknowledged information transfer only (see § 5.2 of Recommendation Q.921);
2) support of both multiple frame acknowledged information transfer and unacknowledged information transfer (see § 5.5 of Recommendation Q.921).

For either type, the elements of procedure and procedures are as specified in §§ 3 and 5 of Recommendation Q.921, with the following differences:

- C/R bit symmetry;
- receipt of I frame response;
- transmission of FRMR response;
- no TE1 management procedures;
- management of address field LLI.

These differences are detailed below.

2.4.1 *C/R bit symmetry*

The use of the C/R bit is symmetric as described in § 2.3.3.

2.4.2 *Receipt of I frame response*

During multiple frame acknowledged information transfer operation, I frames sent as either commands or responses shall be received. I frame responses are optional to send.

Q.921 variable description

N(S) Send sequence number
N(R) Receive sequence number
V(R) Next expected received N(S)

When a data link layer entity receives a valid I frame command whose N(S) is equal to the current V(R) and whose N(R) is in the proper range, it shall follow the procedures stated in §§ 5.6.2 and 5.6.6 of Recommendation Q.921.

When a data link layer entity that is not in a timer recovery state receives a valid I frame response with F bit set to "0" with its N(S) equal to the current V(R) and whose N(R) is in the proper range, it shall treat the frame as a valid I frame command with P bit set to "0" and follow the procedures stated in §§ 5.6.2 and 5.6.6 of Recommendation Q.921. If the received I frame response has its F bit set to "1", the data link layer entity shall indicate an error to the connection management entity.

When a data link layer entity is in a timer recovery condition and receives a valid I frame response with F bit set to "0" with its N(S) equal to the current V(R) and whose N(R) is in the proper range, it shall treat the frame as a valid I frame command with P bit set to "0" and follow the procedures stated in §§ 5.6.2 and 5.6.6 of Recommendation Q.921.

When a data link layer entity is in a timer recovery condition and receives a valid I frame response with F bit set to "0" with its N(R) in the proper range, it shall clear the timer recovery condition and reset timer T200 as if it had received a supervisory frame response with F bit set to "1", as described in § 5.6.7 of Recommendation Q.921. If the I frame has N(S) equal to the current V(R), it is then processed as if it were an I frame command with P bit set to "0", following the procedures stated in §§ 5.6.2 and 5.6.6 of Recommendation Q.921. If the I frame has N(S) not equal to the current V(R), the data link layer entity shall transmit a REJ command prior to resumption of transmission or retransmission of I frames and enter the REJ exception condition as described in § 5.8.1 of Recommendation Q.921.

2.4.3 *Transmission of FRMR response*

A frame rejection condition results from one of the following:

1) the receipt of a supervisory or unnumbered frame with incorrect length;
2) the receipt of an invalid N(R);
3) the receipt of an I frame with an information field which exceeds the maximum allowed length; or
4) the receipt of a command or response control field that is undefined or not implemented.

Upon occurrence of a frame rejection condition, the data link layer entity shall:

- transmit a FRMR response with F bit set to the value of the P bit in the rejected frame;
- indicate an error to the connection management entity; and
- enter the "multiframe not established" state. The "multiframe not established" state is essentially equivalent to the "TE1 assigned" state described in Recommendation Q.921. It is the state initially entered by the data link layer entity when the logical connection establishment procedure is completed successfully.

The format and coding of the FRMR response is as shown in Table 5/Q.921 and Figure 6/Q.921.

2.4.4 *No TE1 management procedures*

The TE1 has no counterpart and the associated Recommendation Q.921 procedures for TE1 management do not apply.

2.4.5 *Management of address field LLI*

The address field is managed using the procedures of § 4.3.

2.5 *Data field length*

The maximum number of octets in a data field (N2xx) is a system parameter. Its value must be less than or equal to N201 (see Recommendation Q.921) minus the length of the header.

2.6 *Control state information processing*

This section describes the use of the control state variables and the processing of the control state information field, when present, defined in § 2.3.6. Use of the control state information field is optional (see octet 5b, bit 7 of low layer compatibility, § 4.4.5).

The terminal adaption entity maintains six control state variables that indicate the current state of the DR, SR and RR indicators as follows:

- send variables DR(S), SR(S) and RR(S) – equal to the current local states of DR, SR and RR, respectively, as transmitted to the far end peer entity;
- receive variables DR(R), SR(R) and RR(R) – equal to the current states of DR, SR and RR, respectively, in the peer entity as received from it.

2.6.1 *Control state information initialization*

Whenever the protocol is initialized to start communications, the protocol entity will set the receive variables (DR(R), SR(R) and RR(R)) to "0" and the send state variables to reflect the status of the interface at the R reference point.

2.6.2 *Sending a control state information field*

A control state information field will be sent whenever a send control state variable changes. A send control state variable will change with a change to the interface at the R reference point or a change to a receive control state variable. The control state information held will be sent following any queued data for interface at the S/T reference point. The control state information field is sent in the last frame containing data received across the interface at the R reference point prior to the control state variable change, or in a separate frame.

The contents of the control state information octet is set to the state of the corresponding send control state variables. DR is set to DR(S), SR is set to SR(S) and RR to RR(S).

2.6.3 *Receiving a control state information field*

Upon receipt of a control state information field, the control field is checked with the receive control state variables: DR to DR(R), SR to SR(R) and RR to RR(R). The receive control state variables are set to their received values.

If SR(R) was "0" and the SR bit in the received control state information field is "1", then the interface at the R reference point and the RR(S) state are changed.

If SR(R) was "1" and the SR bit in the received control state information field is "0", then the interface at the R reference point and the RR(S) state are changed, consistent with one of the following:

- if received data (from peer entity) does not remain to be forwarded (no message in progress), then the control actions can occur immediately;
- if received data (from peer entity) is incomplete (e.g. in protocol sensitive mode the final frame was not received), then the incomplete message is forwarded (continued) until completion on the interface at the R reference point, at which time the control actions can occur;
- if received data (for peer entity) is complete, then the received data is forwarded until completion on the interface at the R reference point, at which time the control actions can occur.

If RR(R) and the RR bit in the received control state information field are not the same, then the interface at the R reference point is changed.

If DR(R) was "0" and the DR bit in the received control state information field is "1", then the interface at the R reference point is changed.

If DR(R) was "1" and the DR bit in the received control state information field is "0", then the interface at the R reference point is changed consistent with the following:

- if the received message from the peer entity is incomplete, it is discarded;
- if the received message from the peer entity is a complete, message, then it should be forwarded to the interface at the R reference point until completetion prior to the control actions taking place.

2.7 *Parameter negotiation*

Parameter negotiation during the bearer channel establishment is in accordance with the procedures described in CCITT Recommendation Q.931. During logical link negotiation, a specific value for a parameter may be requested by including the low layer compatibility information element containing the desired parameters in the SETUP message. The receiving TA may accept the requested parameter values by responding with a CONNect message. If the receiving TA does not accept the parameter values included in the SETUP message, it may negotiate by including the desired values in a low layer compatibility information element in the CONNect message. The originating TA may refuse the parameters receiving in the connect message by initiating clearing with the cause number 21 "Call Rejected".

3 Terminal adaptor (TA) functions

3.1 *Clock synchronization*

The specific mechanisms for providing clock synchronization is implementation dependent. See Appendix II for a discussion.

3.2 *Data flow control and buffering*

Once a frame is assembled (from the interface at the R reference point), it is sent on the interface at the S/T reference point at the nearest opportunity. V.120 procedures may control the flow of frames to the interface at the S/T reference point. The handling of overflow conditions will be described below in the appropriate sections on each mode of operation.

3.2.1 *Asynchronous mode*

In the asynchronous mode, upon the TA receiving a frame from the interface at the S/T reference point, the characters will be sent to the interface at the R reference point at the earliest opportunity. In the asynchronous mode under-run is not a problem, only the over-run condition is of concern. When all buffers are full, the TA flow controls the sender by not acknowledging until a buffer becomes available, when operating in multiple frame acknowledged mode, or using the RR bit in the control state information octet, if available, when operating in unacknowledged mode.

Flow control is indicated when a control state information field with the R bit set to "0" is received. The flow control condition is removed when a flow controlled TA receives a control state information field with the RR bit set to "1". A TA may indicate a change in the state of the RR control state variable by sending UI frames with zero length V.110 information fields containing the control state information field even when it is flow controlled by the other TA.

Note – Some asynchronous terminals may use local flow control.

3.2.2 *Synchronous mode*

In the synchronous mode, a possible under-run condition exists as well as the over-run. Adequate buffering should be provided to normally prevent under-running the interface at the R reference point.

If under-run towards the interface at the R reference point occurs, the current message will be treated by sending an abort or forcing an FCS error.

If an over-run occurs on buffers toward the interface at the S/T reference point a frame will be sent across the interface at the S/T reference point indicating "final" and having the C1 and C2 bits set to "1" following any messages completely received from the interface at the R reference point. Additional data received from the interface at the R reference point will be discarded until the start of a new message is detected.

3.2.3 *Bit transparent mode*

In the bit transparent mode, either under-run or over-run may occur. In this mode the TE2s must operate at the same data rate. Adequate buffering should be provided to minimize under-running the interface at the R reference point.

When the buffers are empty, the interface at the R reference point will be set to the mark hold condition.

If the buffer to the interface at the S/T reference point over-flows, the buffer pool will be set to empty state and accumulation of data restarted.

3.3 *Asynchronous mode operation*

3.3.1 *Character processing – TE2 to S/T direction*

The following processing will be performed on start/stop data received from the TE2:

1) the start and stop bits will be removed from each character;
2) the remaining bit in the character may be checked for correct parity;
3) the parity bit will be removed if the code being used is an 8-bit code; otherwise passed as part of the octet;
4) codes using less than 8 bits (including parity) are padded in the high order bits.

The resulting data is placed in frames, with the segment bits indicating single segment and set to "1".

Frames may be sent based on a timer, after a certain frame size, after a carriage return, etc. However, the forwarding mechanism used is an implementation issue and may vary.

If a BREAK is detected by the TA on the interface at the R reference point, a frame with the BR bit set in the Header will be transmitted in the same frame or after all queued characters have been sent. The C1 and C2 bits should be set to "0".

If a parity error is detected on a character of data being received from the TE2, the C1 bit is set to "1" and the frame sent following any frames already queued for transmission. Thus, setting of the C1 bit to "1" indicates that the last character in the frame in which the C1 bit is set to "1" was received by the TA with a parity error. If a stop bit error is detected on a character of data being received from the TE2, the C2 bit is set to "1" and the frame sent following any frames already queued for transmission. Thus, setting of the C2 bit to "1" indicates that a stop bit error was detected by the TA immediately following the last character contained in the frame in which the C2 bit is set to "1".

3.3.2 *Character processing – S/T to TE2 direction*

The TA will perform the following processing on the data received from the interface at the S/T reference point:

1) if the asynchronous character is less than 8 data bits, the characters will be sent to the TE2 as is;
2) if the asynchronous character contains 8 data bits, each character will be sent to the TE2 with the appropriate parity bit appended;
3) if the C2 bit is set to "1" indicating a stop bit error, the TA action is not defined;
4) if the C1 bit is set to "1" and the asynchronous character contains 8 data bits, indicating a parity error, then the TA may force a parity error on the last character sent to the TE2;
5) if the BREAK bit is set to "1", then the TA will send BREAK to the TE2 following all characters received prior to the break;
6) start and stop bits will be appended to the characters as required.

3.4 *Synchronous mode operation*

3.4.1 *Message processing – TE2 to S/T direction*

The following processing will be performed on the HDLC frame received from the TE2:

1) the beginning flag(s) will be removed;
2) all inserted zeros will be removed;
3) FCS will be accumulated until a flag is detected. The polynomial G(X) = X**16 + X**12 + X** 5 + 1 will be used for the FCS accumulation. The accumulated FCS will be compared with the FCS received from the TE2;
4) the FCS character received from the TE2 will be removed in all cases except for when UI frames are used to carry HDLC frames, in which case the FCS of the original HDLC frame is also carried as data;
5) the ending flag will be removed.

The resulting data will be segmented, if necessary, with each segment preceded by the header. Segmentation shall be such that no frame transmitted on the interface at the S/T reference point is longer than N201 octets.

If only one segment is required, the header will indicate both beginning segment and final segment in the "B" bit and the "F" bit. If more than one segment is required, the header of the first segment will indicate "begin" segment and the last segment of the message will indicate "final" segment. All intermediate segments will have both "begin" and "final" segment indicators set to "0".

The C1 and C2 bits will be set as follows in the final or only segment to indicate detected error conditions:

- if an FCS error is detected as a result of the FCS accumulation process described in step 3 above, then the C2 bit will be set to "1" with the C1 bit set to "0";
- if an abort sequence is detected on the interface at the R reference point, then the C1 bit will be set to "1" with the C2 bit set to "0";
- if an over-run occurs on buffers toward the interface at the S/T reference point, as described above in § 3.2.2, then both the C1 and C2 bits will be set to "1".

When the TA first detects an HDLC idle condition on the interface at the R reference point, it will transmit a frame with the BR bit in the header set to "1" following any queued data frames.

3.4.2 *Message processing – S/T to TE2 direction*

The TA will perform the following processing on the data received:

1) The header will be checked as follows:
   a) if the "begin" segment bit is "1" and the previous segment did not have the "final" segment bit set to "1", then the previous message will be terminated with an ABORT sequence;
   b) if the "begin" segment bit is "0" and there is no message currently in process, the segment will be discarded;
   c) if the C1 and C2 error bit is "1" with the "final" bit a "1", an ABORT sequence will be sent to the TE2 instead of the FCS characters.
2) The FCS is recalculated for TA reconstructed messages when transmitted at the interface at the R reference point except in the case where UI frames are used to carry HDLC frames. In this case the FCS of the original HDLC frame is used in the reconstructed frame. The TA has the option of examining the original FCS, which has been passed to it in the data stream and taking appropriate action.

If an under-run occurs toward the interface at the R reference point, then the frame being sent to the TE2 shall be treated as described in § 3.2.2.

If the BR bit is "1", then the TA will set an HDLC idle condition on the interface at the R reference point following data queued for transmission. The HDLC idle condition will be maintained until a frame is received with its BR bit set to "0".

3.5 *Bit transparent mode operation*

The TA breaks synchronous data stream into fixed size frames and sends it over the channel as it is received from the TE2. The TA takes data from frames received and sends it to the TE2.

The terminal adaption header must be used in bit transparent mode if it is necessary to transmit the control state information. When the terminal adaption header is used in this mode C1 and C2 bits must both be set to "0" (no error). B and F bits must both be set to "1" and reserve bits must be set to "0".

If an under-run occurs toward the interference at the R reference point, then the frame being sent to the TE2 shall be treated as described in § 3.2.3.

For unique applications, the contents of a frame with an FCS error may be delivered across the interface at the R reference point.

4 Connection control procedures

This section describes the procedures for establishing connections for V.120 terminal adaption. Procedures are described for:

- establishment of an ISDN circuit-switched connection; and
- optional procedures for the negotiation of logical link identifiers.

The protocol described in the following sections describing procedures for negotiating logical links is based on Recommendation Q.931 messages, information elements and procedures, but is tailored for this particular application. It is differentiated from the full Recommendation Q.931 procedures by the use of a unique protocol identifier ("00001001"). In addition to the information elements of Recommendation Q.931, an additional information element is required to convey the logical link identifier for this application and is defined in the following sections.

The selection of V.120 as a terminal adaption protocol at the establishment of the bearer channel is specified by information in the bearer capability information and/or low layer compatibility information elements of the bearer channel SETUP procedure.

Logical link negotiation procedures may be carried out by means of user information messages in a Recommendation Q.931 Call associated temporary signalling connection on the ISDN D Channel, or by means of logical link zero within the bearer channel using Recommendation Q.921 elements of procedure (i.e. either UI or I frames). The choice of methods is a terminal equipment option and is partially determined by the availability of end-to-end ISDN signalling capability. The optional establishment of logical links between equipments that support different options may not be possible.

4.1 *Establishment of circuit-switched connection*

The bearer channel between the TAs is controlled using the D channel signalling procedure for call establishment is described in Recommendation Q.931.

On the basis of call setup information, the network provides a bearer channel to the requested end-point. The transfer mode and transfer capability in the bearer capability (BC) information element of the setup message is coded as circuit, unrestricted or restricted.

4.2 *Establishment of logical links*

This procedure requires that all TAs either be "default assignees" or "assignor only". The TAs that must always assign the LLI (e.g., TAs with pre-assigned LLIs) are assignor only, all other TAs are default assignee. An assignor/assignee field is provided in the low layer compatibility (LLC) and bearer capability (BC) information elements for V.120. This field must be coded as "0" when the TA is a default assignee, and as "1" when the TA is an assignor only. The "default assignee" may assume the role of "assignor only" during negotiation.

4.2.1 *During the bearer channel setup phase*

The first logical link is established between the two TAs using the default LLI = 256 using the information provided in the LLC information element.

4.2.2 *During the bearer channel active phase*

4.2.2.1 *Resolving when both sides are default assignees*

The first TA initiating a request for a logical link other than the default will assume the assignee role. The TA that receives that request will assume the assignor role.

If both TAs simultaneously send SETUP messages, the SETUP message containing the larger "call reference" (see Recommendation Q.931 for definition of call reference) is accepted and treated in accordance with the above procedure. The response to the SETUP message with the lower "call reference" is a RELease COMPlete message. If both SETUP messages contain the same "call reference", they are both cleared with RELease COMPlete messages, and the TAs select different "call references" and try again.

4.2.2.2 *LLI assignee*

If a TA is determined to be LLI assignee, it must set the assignor/assignee field contained in any additional SETUP messages to zero.

The LLI assignee TAs request additional logical links by sending a SETUP message without the LLI information element. The TA receiving this SETUP message assigns an LLI by including the LLI information element in the CONNect message.

4.2.2.3 *LLI assignor*

If a TA is determined to be LLI assignor, it must set the assignor/assignee field contained in any additional SETUP message to one.

The LLI assignor TAs set up additional logical links by sending SETUP messages that include the LLI information element. The receiving TA responds with a CONNect message and sets up a logical link using the information provided in the SETUP message.

4.3 *Messages used for logical connection control*

The following messages are used for establishing logical links within a bearer channel.

Call establishment	SETUP
	CONNect
Call clearing	RELease
	RELease COMPlete

4.3.1 *Setup*

See Table 5/V.120.

This message is sent by either TA to indicate that it desires to initiate a new logical link. It must contain protocol discriminator, call reference, and message type. Low layer compatibility information element can optionally be included in the SETUP message. Logical link identifier information element must be included in the SETUP message if the TA is assigning the LLI, and not included if requesting an LLI from the other TA.

TABLE 5/V.120

SETUP message content

Information element	Ref. V.120	Type	Length
Protocol discriminator	4.4.1	M	1
Call Reference	4.4.3	M	2
Message type	4.4.2	M	1
Low layer compatibility	4.4.5	O (Note 1)	2-13
Logical link identifier	4.4.6	O (Note 2)	4

M Mandatory
O Optional

Note 1 – Included when the calling user wants to pass low layer compatibility information to the called user.

Note 2 – Included if the calling user has the responsibility for assigning LLI for that physical link.

4.3.2 *CONNect*

See Table 6/V.120.

This message is sent by the TA that has received a SETUP message to indicate that the request for establishment of an additional logical link has been accepted. It must include protocol discriminator, call reference, and message type information elements. The low layer compatibility information element can optionally be included in the CONNect message. The logical link identifier information element must be included if not included in the SETUP message, and is not included otherwise.

TABLE 6/V.120

CONNect message content

Information element	Ref. V.120	Type	Length
Protocol discriminator	4.4.1	M	1
Call reference	4.4.3	M	2
Message type	4.4.2	M	1
Low layer compatibility	4.4.5	O (Note 1)	2-13
Logical link identifier	4.4.6	O (Note 2)	4

Note 1 – Included to allow the called user to negotiate low layer compatibility information with the calling user.

Note 2 – Included if the called user has the responsibility for assigning LLI.

4.3.3 *RELease*

See Table 7/V.120.

The RELease message is used to indicate that the TA intends to release the call reference and the logical link, and that the TA receiving this message must release the logical link and prepare to release the call reference after sending a RELease COMPlete. This message must contain protocol discriminator, call reference message type, and optionally cause information elements.

TABLE 7/V.120

RELease message content

Information element	Ref. V.120	Type	Length
Protocol discriminator	4.4.1	M	1
Call reference	4.4.3	M	2
Message type	4.4.2	M	1
Cause	4.4.4	O	2-4

4.3.4 *RELease COMPlete*

See Table 8/V.120.

The RELease COMPlete message is sent to acknowledge that the TA sending the message has released the logical link and call reference. This message must contain protocol discriminator, call reference, and message type and optionally cause information elements.

TABLE 8/V.120

RELease COMPlete message content

Information element	Ref. V.120	Type	Length
Protocol discriminator	4.4.1	M	1
Call reference	4.4.3	M	2
Message type	4.4.2	M	1
Cause	4.4.4	O	2-4

4.4 *Information elements*

4.4.1 *Protocol discriminator*

The protocol discriminator is "00001001".

4.4.2 *Message type*

Message types are identical to message types in Recommendation Q.931.

4.4.3 *Call reference*

The call reference field should be two octets in length.

4.4.4 *Cause information element*

See Figure 6/V.120.

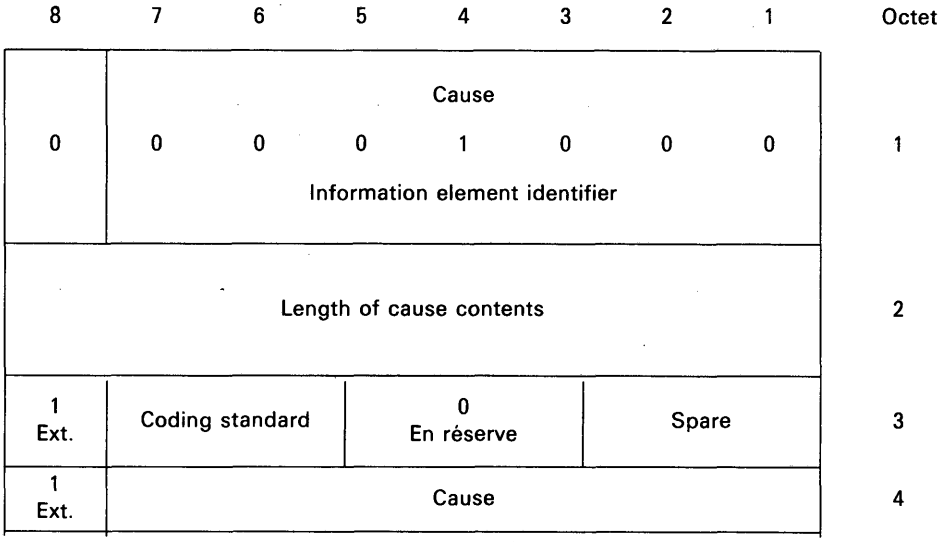


FIGURE 6/V.120

4.4.5 *Low layer compatibility information element*

See Figure 7/V.120.

4.4.6 *Logical link identifier information element*

The purpose of the logical link identifier information element is to identify a logical link within the bearer channel. The default length of this element is four octets. The logical link identifier information element is coded as shown in Figure 8/V.120.

4.5 *Logical connection control procedures*

This optional procedure defines the method for negotiation logical links other than the default (LLI = 256). For setup and clearing of the bearer channel, the procedure described in Recommendation Q.931 must be followed.

8	7	6	5	4	3	2	1	Octet
0	Low layer compatibility 1 1 1 1 1 0 0 Information element identifier							1
Length of the low layer compatibility contents								2
1 Ext.	Coding standard		Information transfer capability					3
0/1 Ext.	Transfert mode		Information transfer rate					4
0/1 Ext.	Structure			Configuration		Establishment		4a* (Note 1)
1 Ext.	Symmetry		Information transfer rate (destination → origination)					4b* (Note 1)
0/1 Ext.	0 1 layer 1 ident.		User information layer 1 protocol					5* (Note 3)
0/1 Ext.	Synch./ asynch.	Negot.	User rate					5a* (Note 2)
0/1 Ext.	Hdr/no Hdr	Multi frame	Mode	LLI negot.	Assign/ assgnee	In- Band/out Band	0 Spare	5b* (Notes 2, 3)
0/1 Ext.	Number of stop bits		Number of data bits		Parity			5c* (Note 2)
1 Ext.	Duplex mode	Modem type						5d* (Note 2)
1 Ext.	1 0 Layer 2 ident.		User information layer 2 protocol					6*
1 Ext.	1 1 Layer 3 ident.		User information layer 3 protocol					7*

Note 1 – If default values are used for all fields of octet 4a and 4b, then these octets shall not be included. If default values are used for all fields of octet 4b, but not for one or more fields of octet 4a, then only octet 4a shall be included. Otherwise, both octets 4a and 4b shall be included.

Note 2 – This octet is present only if octet 5 indicates rate adaption.

Note 3 – Description of bits used in octet 5:

User information layer 1 protocol (octet 5)

Bits 5 4 3 2 1	
0 1 0 0 0	CCITT standardized terminal adaption V.120 (based on LAPD). This implies the presence of octets 5a, 5b as defined below, and optionally octets 5c and 5d.

Rate adaptation header/no header (octet 5b, bit 7)

Bit 7	
0	optional portions of terminal adaption header not included
1	optional portions of terminal adaption header included.

Multiple frame establishment support in data link (octet 5b, bit 6)

Bit 6	
0	multiple frame establishment not supported. Only UI frames are allowed
1	multiple frame establishment supported

Mode of operation (octet 5b, bit 5)

Bit 5	
0	bit transparent mode of operation
1	protocol sensitive mode of operation

LLI negotiation (octet 5b, bit 4)

Bit 4	
0	default LLI = 256 only
1	full LLI negotiation

Assignor/assignee (octet 5b, bit 3)

Bit 3	
0	message originator is «default assignee»
1	message originator is «assignor only»

In-band/out-of-band negotiation (octet 5b, bit 2)

Bit 2	
0	negotiation is done with user information messages on a call associated temporary signalling connection
1	negotiation is done in-band using logical link zero

FIGURE 7/V.120

Logical link identifier information element

8	7	6	5	4	3	2	1	Octets
0	Logical link identifier 0 1 1 0 1 0 0 Information element identifier							1
Length of logical link identifier contents 0 0 0 0 0 0 1 0								2
0	0 Spare	Logical link identifier (high order 6 bits)						3
1 Ext.	Logical link identifier (low order 7 bits)							4

FIGURE 8/V.120

4.5.1 *Logical link establishment*

A logical link may be established by either TA by sending a SETUP message.

If the TA sending the SETUP message assigns the LLI, the SETUP message must also include the assigned LLI value for the logical link.

If the TA does not assign the LLI, it must not include the LLI information element in the SETUP message. In this case the LLI is assigned by the receiving TA by including an LLI information element in the CONNect message.

A TA may request a logical link by sending a SETUP message, setting timer T303, and entering "call initiated" state.

If no response to the SETUP message is received before the first expiry of timer T303, the SETUP message must be transmitted and timer T303 restarted. After the second expiry of timer T303, the "Null" state is entered.

A TA receiving the SETUP message must send a CONNect message and enter the "Active" state if able; otherwise, it must send a RELease COMPlete message and enter the "Null' state.

When the initiating TA receives the CONNect message, it must stop timer T303, and enter the "Active" state.

4.5.2 *Logical link clearing*

Either TA may request to clear a logical link by sending a RELease message, setting timer T308, and entering "Release Request" state.

When a TA receives a RELease message, it must release the logical link, send a RELease COMPlete message, release the call reference, and enter the "Null" state.

When the TA initiating a RELease receives RELease COMPlete message, it must stop timer T308, release the logical link, release the call reference, and enter the "Null" state.

If the TA initiating the RELease does not receive a RELease COMPlete message before the first expiry of timer T308, the RELease message must be retransmitted and timer T308 restarted. If RELease COMPlete message is not received before timer T308 expires for the second time, the TA must release the call reference and enter the logical link into the "Null" state.

If both TAs simultaneously request to clear the same logical link by sending RELease messages, both must stop timer T308, release the logical link, release the call reference, and enter the "Null" state.

ANNEX A

(to Recommendation V.120)

Mappings of V.24 circuits to DR, SR, and RR

This Annex describes mapping of V.24 circuits intended to provide proper operation with most DTEs.

A.1 *DR-data ready (bit 7)*

The DR bit maps according to DTE attachment as follows:

- for sending DR-DR(S) state variable:
  - indicates DTR-data terminal ready (Recommendation V.24 circuit 108/2) from DTE;
- for receiving DR-DR(R) state variable: no mapping is required.

Note – Dropping DTR may be used by the TE2 to indicate to the TA to clear the logical link or call.

A.2 *SR-send ready (bit 6)*

The SR bit maps according to DTE attachment as follows:

- for sending SR-SR(S) state variable;
  - indicates request to send (RTS – Recommendation V.24 circuit 105) status from DTE;
- for receiving SR-SR(R) state variable;
  - drives receive line signal detect (RLSD – Recommendation V.24 circuit 109) to DTE;
  - the received ST bit is also mapped to the send RR bit (i.e. SR(R) → RR(S)).

A.3 *RR-receive ready (bit 5)*

The RR bit maps according to DTE attachment as follows:

- for sending RR-RR(S) state variable: no mapping is required;
- for receiving RR-RR(R) state variable:
  - drives ready for send (RFS – Recommendation V.24 circuit 106) to DTE.

APPENDIX I

(to Recommendation V.120)

TE1 application

The protocols and procefures defined in Recommendation V.120 may be used for data transport by compatible TE1s as well as terminal adapters (TAs). In the TE1 case, the interface at the R reference point is effectively replaced by a virtual interface within the TE1 to a higher layer entity. This appendix describes the application of Recommendation V.120 in TE1s.

I.1 *Asynchronous mode operation*

I.1.1 *Transmission onto the ISDN channel*

The B, F bits are set to "1", and the C1 and C2 bits in the header are set to "0". The data to be transmitted is segmented as required, and each segment is appended to the header before transmission.

If a BREAK is received from the next higher layer, a frame with the BR bit set to "1" in the header will be transmitted at the earliest opportunity following data queued for transmission.

I.1.2 *Reception from the ISDN channel*

Processing of received data is as follows, based on the values of the C1 and C2 bits in the header:

- if the C1 and C2 bits are both set to "0", the received characters are forwarded to the next higher layer without error indication;
- if the C1 bit is set to "1", then a parity error indication is forwarded to the next higher layer with the characters received; the parity error applies to the last character in the frame;
- if the C2 bit is set to "1", then a stop-bit error is forwarded to the next higher layer with the characters received; the error occurred immediately following the last character in the frame.

If the BR bit is set to "1" in the header of the received frame, then a BREAK indication is forwarded to the next higher layer after all data queued has been forwarded.

I.2 *Synchronous mode operation*

The messages passed to and received from the higher layer include the HDLC address and control fields, but do not include HDLC flags, FCS or inserted "0"s.

I.2.1 *Transmission onto the ISDN channel*

The message length is compared with N2xx. The message is processed depending on its length as follows:

- if the message length is less than or equal to N2xx, then the entire message is appended behind the header and both in the B and F bits set to "1". The resulting message is then transmitted;
- if the message length is greater than N2xx, the first N2xx octets are appended to the header, with the B bit set to "1" and the F bit set to "0". The resulting message is then transmitted;
  - if the remaining portion of the message is greater in length than N2xx, the next N2xx octets are appended to the header, with both the B and F bits set to "0". The resulting message is then transmitted;
  - if the length of the remaining portion of the message is less than or equal to N2xx, then the remaining portion of the message is appended to the header with the F bit set to "1" and the B bit set to "0". The resulting message is then transmitted.

The C1 and C2 bits are normally set to "0".

I.2.2 *Reception from the ISDN channel*

Any messages that were segmented at the transmit end are reassembled as indicated by the B and F header bits.

The header of a received frame will be checked for error conditions as follows:

- if the "begin" segment bit is "1" and the previous segment did not have the "final" segment bit set to "1", then the previous message will be aborted;
- if the "begin" segment bit is set to "0" and there is no message currently in process, the segment will be discarded;
- if the C1 or C2 error bit is "1" with the "final" bit a "1", the message will be discarded.

If a frame is received with the BR bit set to "1" in the header, then the TE1 management entity will be notified of an HDLC idle condition sent from the far end. The HDLC idle condition is maintained until a frame is received with the BR bit in its header set to "0".

When a message has been reassembled it is passed to the next higher layer.

I.3 *Bit transparent mode operation*

I.3.1 *Transmission onto the ISDN channel*

The transmitting entity accepts data from the process using its services, segments the data into segments of length at most N2xx, and transmits that data within frame to its peer entity. The length of the data segments and the length of the transmitted interframe time fill are adjusted so that the average data transmission rate matches the rate selected during call establishment.

I.3.2 *Reception from the ISDN channel*

The receiving entity upon receiving a frame from its peer entity, checks the FCS and if the FCS is valid it passes any data contained in the frame to the process using its services. If the FCS is not valid the entity may, on an application specific basis, discard the data contained in the errored frame or pass that data, with or without error indication, to the process using the services of the entity.

I.4 *TE1 control state variable processing*

In TE1 applications, the six control state variable DR(S), SR(S), RR(S), DR(R), SR(R), and RR(R) are maintained as described in § 2.3.6, with the following meanings:

- for sending DR – DS(S) state variable:
  - indicates that the sending TE1 is powered up and connected for communication;
- for receiving DR – DR(R) state variable:
  - indicates that the sending TE1 (far end) is powered up and connected for communication;
- for sending SR – SR(S) state variable:
  - indicates that the sending TE1 is ready to send frames;
- for receiving SR – SR(R) state variable:
  - indicates that the sending TE1 (far end) is ready to send frames;
- for sending RR – RR(S) state variable:
  - indicates that the sending TE1 is ready to receive frames;
- for receiving RR – RR(R) state variable:
  - indicates that the sending TE1 (far end) is ready to receive frames.

The following sections describe the procedures for control state variable processing in a TE1 using V.120. Note that the control states in a TE1 as described above are essentially analogous to those in a TA as described in § 2.3.6. Thus, the TE1 control state variable processing described below is completely compatible with that described in § 2.6 for the TA.

I.4.1 *Control state variable initialization*

Whenever the protocol is initialized to start communications, the protocol entity will set the receive state variables (DR(R), SR(R), and RR(R)) to "0" and the send state variables to reflect the status of the TE1 as described above.

I.4.2 *Sending a control state information octet*

A control state information octet will be sent whenever a send control state variable changes. A send control state variable will change with a change to the state of the TE1 as described above. A frame containing the control state information octet will be sent following any queued data for the interface at the S/T reference point.

The control state information field is sent in the last frame assembled when the control state change occurs, or in a separate frame.

The contents of the control state information octet is set to the state of the corresponding send control state variables. DR is set to DR(S), SR is set to SR(S), and RR to RR(S).

I.4.3 *Receiving a control state information octet*

Upon receipt of a control state information octet, the control field is checked with the receive control state variables: DR to DR(R), SR to SR(R), and RR to RR(R). The receive control state variables are set to their received values.

If SR(R) was "0" and the SR bit in the received control state information octet is "1", notification is made to the TE1 management entity.

If SR(R) was "1" and the SR bit in the received control state information octet is "0", notification is made to the TE1 management entity consistent with one of the following:

- if received data (from the peer entity) does not remain to be forwarded (no message in progress), then the control actions can occur immediately;
- if received data (from the peer entity) is incomplete (e.g. in protocol sensitive mode the final frame is not received), then the incomplete message is forwarded with indication of incomplete message and the notification made to the TE1 management entity;
- if received data (from the peer entity) is complete, the message is forwarded and the notification of the TE1 management entity occurs.

If RR(R) and the RR bit in the received control field differ, notification is made to the TE1 management entity.

If DR(R) was "0" and the RR bit in the received control field is "1", notification is made to the TE1 management entity.

If DR(R) was "1" and the DR bit in the received control field is "0", then notification is made to the TE1 management entity consistent with the following:

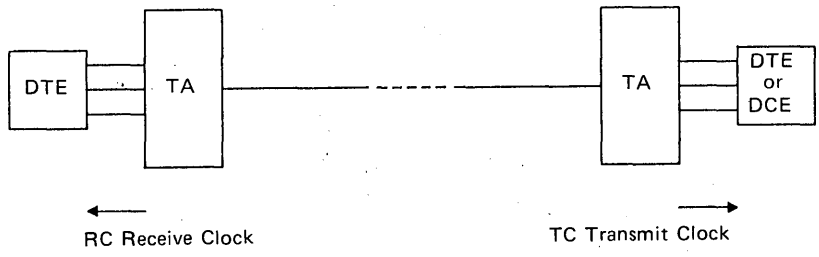
- if received data from peer entity is incomplete, it is discarded;
- if received data from peer entity is a complete message, then it should be forwarded until completion prior to the control actions taking place.

APPENDIX II

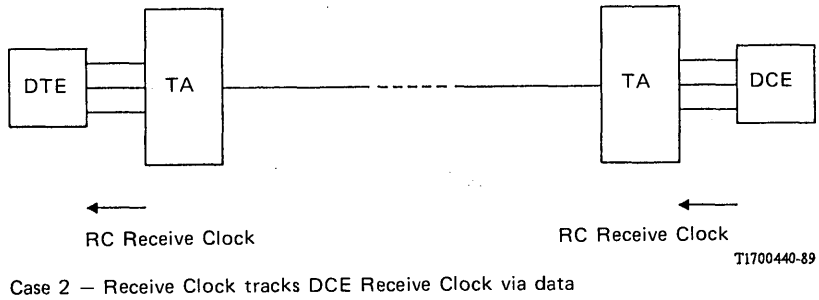
(to Recommendation V.120)

Clock synchronization

Figure II-1/V.120 shows two DTE/DCE configurations and their respective clock synchronization.



Case 1 – Receive Clock tracks Transmit Clock via data or system synchronization.



Case 2 – Receive Clock tracks DCE Receive Clock via data

FIGURE II-1/V.120

Clock tracking

In the first case in Figure II-1/V.120, the TA is providing the clocks to the DTE or DCE. In the second case in Figure II-1/V.120, the DCE provides the Receive Clock to the TA for data to the DTE, and the TA at the DTE end provides the Receive Clock to the DTE for this same data.

There are three strategies which could be used for clock tracking. The first is to use the data buffers as clock variance buffers by having these buffers absorb the accumulated clock variance. In this case, no clock tracking is performed. If the buffer is completely depleted, and under-run occurs causing an error on the synchronous interface at the R reference point. Buffer space over-run can also happen, causing an error. However, the buffer accumulation or depletion to the point of over-run or under-run due to clock error is a slow process and is predictable in the worst case within the CCITT clock tolerance of 100 parts per million. The second

strategy is for the clocks at both ends to be synchronized to the network. This strategy solves the problem but is not applicable to case 2 in Figure II-1/V.120. The third strategy is to monitor the buffer state as data is being received from the interface at the S/T reference point in the TA that is providing the Receive Clock to the DTE. This strategy monitors the rate of data at this interface by checking the buffer state when a new frame is received, and adjusts the clock speed accordingly.

For asynchronous applications, the first strategy (no clock correction) should be sufficient. For these applications a clock tolerance of $+1/-2.5\%$ is permissible, see Recommendation V.14. Under-run is not possible and buffering in the TA should be sufficient to avoid over-run.

For synchronous mode applications, appropriate buffer setup and management using no clock correction should be sufficient.

For bit transparent mode applications, continuous data does not allow for buffer resynchronization. For case 2 the frames are read into a buffer at the receiving TA and are clocked out to the TE2 by a time source derived in the TA. If the data is clocked out at the rate transmitted, each frame will fill the receive buffer to precisely the same level. If the rate is low the fill level will increase and provide an indication that the clock rate must be increased and vice versa.

In some implementations, the clock adjustments might be in the form of repeated small adjustments in the phase of the clock, which would be derived from the ISDN network clock. Where the TE2 is tolerant of large phase steps the process may be simple.

APPENDIX III

(to Recommendation V.120)

Bearer channel initialization procedures for circuit switched applications

To reduce the possibility of transmitting a frame to a TA that is not yet connected:

- a TA that receives a CONNect message from the network should always transmit a frame to initiate the connection, and
- a TA that receives a CONNect ACKnowledge message from the network should wait for T200 or until it receives a frame (whichever is earlier) before transmitting a frame.

Recommendation V.230

GENERAL DATA COMMUNICATIONS INTERFACE LAYER 1 SPECIFICATION

(Melbourne, 1988)

1 General

This Recommendation defines the layer 1 characteristics of a General Data Communications Interface (GDCI) between Data Circuit-Terminating Equipment (DCE) and/or Data Terminal Equipment (DTE). Applications include DTE-DCE interfaces, DCE-DCE interfaces, and possible DTE-DTE interfaces (see Figure 1/V.230). The interface specification is based on the ISDN basic user-network interface defined in Recommendation I.430. The differences between the GDCI and the ISDN basic user-network interface provide for the different wiring configurations expected for these interfaces, and they provide a means by which equipment conforming to V.230 can identify whether it has been connected to an interface operating according to V.230 or to an interface operating according to I.430. The characteristics of the GDCI have been chosen so that it is possible to design terminals which are compatible with both I.430 and V.230, and so that inadvertent connection of I.430 equipment to a V.230 passive bus or of GDCI equipment to an I.430 passive bus will not result in passive bus malfunction.

Note – DTE-DTE interfaces are not defined by CCITT.

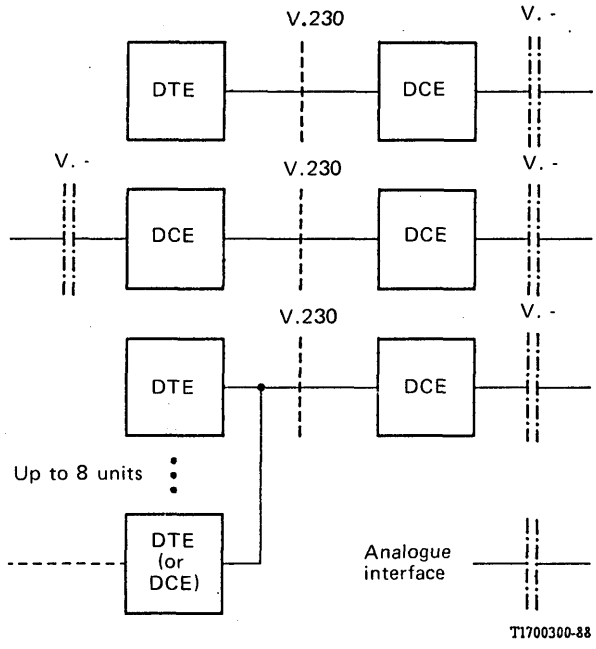


FIGURE 1/V.230

GDCI applications

2 Service characteristics

2.1 *Services required from the physical medium*

Layer 1 of this interface requires a balanced metallic transmission medium, for each direction of transmission, capable of supporting 192 kbit/s.

2.2 *Services provided to layer 2*

Layer 1 provides the following services to layer 2 and the management entity.

2.2.1 *Transmission capability*

Layer 1 provides the transmission capability, by means of appropriately encoded bit streams, for the BV and DV channels and the related timing and synchronization functions.

Note – The BV and DV channels correspond to the B and D channels, respectively, as defined in the I-Series Recommendations. Use of the BV and DV channels is defined in Recommendations V.yy and V.zz (V.yy and V.zz: still under study).

2.2.2 *Activation/deactivation*

Layer 1 provides the signalling capability and the necessary procedures to enable equipment to be deactivated when required and reactivated when required. The activation and deactivation procedures are defined in § 6.2.

2.2.3 *D-channel access*

Layer 1 provides the signalling capability and the necessary procedures to enable equipment to gain access to the common resource of the DV channel in an orderly fashion while meeting the performance requirements of the DV-channel signalling system. These DV-channel access control procedures are defined in § 6.1

2.2.4 *Maintenance*

Layer 1 provides the signalling capability, procedures and necessary functions at layer 1 to enable the maintenance functions to be performed.

2.2.5 *Status indication*

Layer 1 provides an indication to the higher layers of the status of layer 1.

2.3 *Primitives between layer 1 and other entities*

Primitives represent, in an abstract way, the logical exchange of information and control between layer 1 and other entities. They neither specify nor constrain the implementation of entities or interfaces.

The primitives to be passed across the layer 1/2 boundary or to the management entity and parameter values associated with these primitives are defined and summarized in Table 1/V.230. For a description of the syntax and use of the primitives, refer to Recommendation X.211 and relevant detailed description in § 6.

TABLE 1/V.230

Primitives associated with layer 1

Generic name	Specific name		Parameter		Message unit contents
	Request	Indication	Priority indicator	Message unit	
L1 < – – > L2					
PH-DATA	X (Note 1)	X	X (Note 2)	X	Layer 2 peer-to-peer message
PH-ACTIVATE	X	X	–	–	
PH-DEACTIVATE	X	X	–	–	
M < – – > L1					
MPH-ERROR	–	X*	–	X	*Type of error or recovery from a previously reported error
MPH-ACTIVATE	X	X	–	–	
MPH-DEACTIVATE	X	X	–	–	
MPH-INFORMATION	–	X	–	X	Connected Attached V-DCE Attached V-DTE Attached NT Attached TE Disconnected

Note 1 – PH-Data Request implies underlying negotiation between layer 1 and layer 2 for the acceptance of the data.

Note 2 – Priority indication applies only to the request type.

3 Modes of operation

Both point-to-point and point-to-multipoint modes of operation, as described below, are intended to be accommodated by the layer 1 characteristics of the GDCI. In this Recommendation, the modes of operation apply only to the layer 1 procedural characteristics of the interface and do not imply any constraints on modes of operation at higher layers.

3.1 *Point-to-point operation*

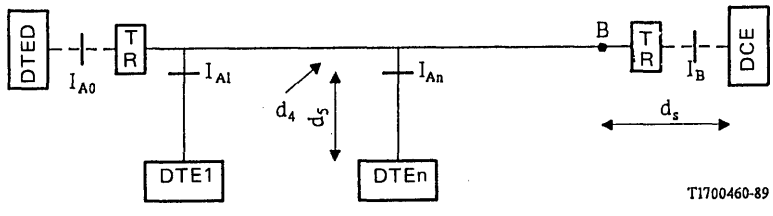
Point-to-point operation at layer 1 implies that only one source (transmitter) and one sink (receiver) are active at any one time in each direction of transmission at an S or T reference point. (Such operation is independent of the number of interfaces which may be provided on a particular wiring configuration – see § 4.)

3.2 *Point-to-multipoint operation*

Point-to-multipoint operation at layer 1 allows more than one equipment (source and sink pair) to be simultaneously active at a GDCI. (The multipoint mode of operation may be accommodated, as discussed in § 4, with point-to-point or point-to-multipoint wiring configurations.)

4 Types of wiring configuration

The electrical characteristics of the GDCI are determined on the basis of certain assumptions about the various wiring configurations which may exist in the user premises. These assumptions are identified in two major configuration descriptions, §§ 4.1 and 4.2, together with additional material contained in Annex A to this Recommendation. Figure 2/V.230 shows a general reference configuration for wiring in the user premises.



TR Terminating resistor
I Electrical interface
B Location of I_B when the terminating resistor (TR) is inclued in the DCE

FIGURE 2/V.230

Reference configuration for wiring in the user premises location

4.1 *Point-to-point configuration*

A point-to-point wiring configuration implies that only one source (transmitter) and one sink (receiver) are interconnected on an interchange circuit.

4.2 *Point-to-multipoint configuration*

A point-to-multipoint wiring configuration allows more than one source to be connected to the same sink or more than one sink to be connected to the same source on an interchange circuit. Such distribution systems are characterized by the fact that they contain no active logic elements performing functions (other than possibly amplification or regeneration of the signal).

The equipment connected to interface point I_B must operate in the "master timing mode" discussed in § 6.6. This equipment is normally a V-DCE. The equipment connected to interface points I_{A0} through I_{An} must operate in the "slave timing mode". These are normally V-DTEs, although a V-DCE may be connected to this point to achieve a DCE-to-DCE connection on the GDCI. Use of a V-DTE as the master timing mode equipment is for further study.

4.3 *Wiring polarity integrity*

For a point-to-point wiring configuration, the two wires of the interchange circuit pair may be reversed. However, for a point-to-multipoint wiring configuration, the wiring polarity integrity of the interchange circuit (slave-to-master direction) must be maintained between slave mode equipment.

In addition, the wires of the optional pairs, which may be provided for powering, may not be reversed in either configuration.

4.4 *Location of the interfaces*

The wiring in the user premises is considered to be one continuous cable run with jacks for the equipment attached directly to the cable or using stubs less than 1 meter in length. The jacks are located at interface points I_A and I_B (see Figure 2/V.230). One interface point, I_A, is adjacent to the master mode equipment. The other interface point, I_B, is adjacent to the master mode equipment. However, in some applications, the equipment may be connected to the wiring without the use of a jack or with a jack which accommodates multiple interfaces. The required electrical characteristics (described in § 8) for I_A and I_B are different in some aspects.

4.5 *Wiring associated with the equipment*

The wiring connecting the V-DCE or V-DTE to associated jacks or to other equipment affects the interface electrical characteristics. Equipment that is not permanently connected to the interface wiring may be equipped with one of the following means of connection to the interface point:

- a hard wired connecting cord (of not more than 10 m in the case of a V-DTE and not more than 3 m in the case of a V-DCE) equipped with a suitable plug, or
- a jack with a connecting cord (of not more than 10 m in the case of a V-DTE and not more than 3 m in the case of a V-DCE) equipped with a suitable plug at each end, or
- two jacks with suitable connecting cords or cables which may be used to form a "daisy-chain" connection from one equipment unit to the next, provided that the connecting cords and cables meet the distance limitations set in Annex A. In this case, the electrical interface exists inside the equipment, where the two jacks are wired together with each pin on one jack connected to the like-numbered pin on the other jack and to the internal circuitry of the equipment.

The requirements of V.230 apply to the interface point (I_A or I_B), and the cord forms part of the associated equipment. Note that the equipment may attach directly to the interface wiring without a detachable cord.

Although an equipment may be provided with a cord of less than 5 m in length, it shall meet the requirements of this Recommendation with a cord having a minimum length of 5 m. As specified above, the equipment cord may be detachable. Such a cord may be provided as part of the equipment, or the equipment may be designed to conform to the electrical characteristics specified in § 8 with a "standard ISDN basic access TE cord" conforming to the requirements specified in § 8.9 of Recommendation I.430, and having the maximum permitted capacitance.

The use of an extension cord, of up to 25 m in length, with an equipment in point-to-point operation, is permitted. (The total attenuation of the wiring and of the cord in this case should not exceed 6 dB.)

5 Functional characteristics

The following paragraphs show the functions for the interface.

5.1 *Interface functions*

5.1.1 *BV channel*

This function provides, for each direction of transmission, two independent 64 kbit/s channels for use as BV channels.

5.1.2 *Bit timing*

This function provides bit (signal element) timing at 192 kbit/s to enable the equipment to recover information from the aggregate bit stream.

5.1.3 *Octet timing*

This function provides 8 kHz timing for the equipment.

5.1.4 *Frame alignment*

This function provides information to enable equipment to recover the time division multiplexed channels.

5.1.5 *DV channel*

This function provides, for each direction of transmission, one DV channel at a bit rate of 16 kbit/s.

5.1.6 *DV channel access procedure*

This function is specified to enable slave mode equipment to gain access to the common resource of the DV channel in an orderly controlled fashion. The functions necessary for these procedures include an echoed DV channel at a bit rate of 16 kbit/s in the direction master to slave equipment. For the definition of the procedures relating to DV channel access, see § 6.1.

5.1.7 *Power feeding*

This function provides for the capability to transfer power across the interface. The direction of power transfer depends on the application. In a typical application, it may be desirable to provide for power transfer from the V-DCE towards V-DTEs in order to, for example, power an adaptor for a unit which does not conform to V.230. (In some applications, unidirectional power feeding or no power feeding at all, across the interface, may apply.) Other Recommendations concerning power feeding capability are contained in § 9.

5.1.8 *Activation and deactivation*

Activation is necessary to initialize an equipment when power is applied, or when it is connected to the GDCI. Deactivation and activation may also be used to control entry to and exit from a low power consumption mode. The procedures and precise conditions under which these actions take place are specified in § 6.2. For many applications, it will be appropriate for the equipment to remain in the active state at all times after initial activation.

5.2 *Interchange circuits*

Two interchange circuits, one for each direction of transmission, shall be used to transfer digital signals across the interface. All of the functions described in § 5.1, except for power feeding, shall be carried by means of a digitally multiplexed signal structured as defined in § 5.4.

5.3 *Connected/disconnected indication*

The criterion used by equipment to determine whether it is connected or disconnected at the interface is reception of valid incoming frames.

The layer 1 entity within the equipment shall inform the management entity of the connection status using the MPH-INFORMATION INDICATION primitive. The method for determining the message unit contents is discussed in § 6.2.

5.4 *Frame structure*

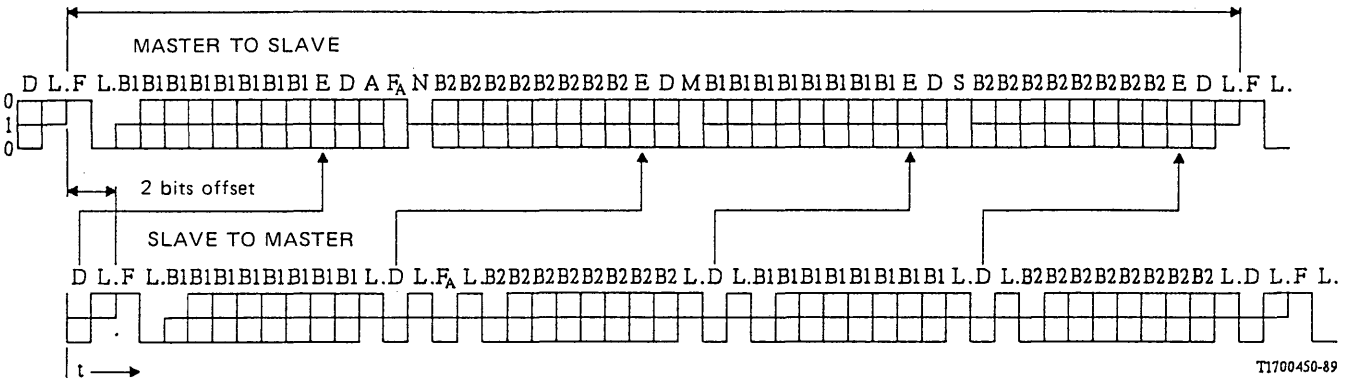
In both directions of transmission, the bits shall be grouped into frames of 48 bits each. The frame structure shall be identical for all configurations (point-to-point and point-to-multipoint).

5.4.1 *Bit rate*

The nominal transmitted bit rate at the interfaces shall be 192 kbit/s in both directions of transmission.

5.4.2 *Binary organization of the frame*

The frame structures are different for each direction of transmission. Both structures are illustrated diagramatically in Figure 3/V.230.



F framing bit
L DC balancing bit
D DV-channel bit
E DV-echo-channel bit
F_A Auxiliary framing bit (see § 6.3)

N bit set to a binary value N = $\overline{F}_A$ (master to slave) (see § 6.3)
B1 bit within BV channel 1
B2 bit withing BV channel 2
A bit used for activation
S S-channel multiframe bit (see § 6.3.4)
M multiframing bit

Note 1 – Dots demarcate those parts of the frame that are independently DC-balanced.

Note 2 – The F_A bit in the direction slave to master is used as a Q bit in every fifth frame if the Q channel capability is applied (see § 6.3.3).

Note 3 – The nominal 2-bit offset is as seen from the slave mode equipment (I_A in Figure 1/V.230). The corresponding offset at the master mode equipment may be greater due to delay in the interface cable and varies by configuration.

FIGURE 3/V.230

Frame structure at the GDCI

5.4.2.1 *Slave to master*

Each frame consists of the following groups of bits; each individual group is DC-balanced by its last bit (L bit):

Bit position	*Group*
1 and 2	framing signal with balance bit
3-11	BV1 channel (first octet) with balance bit
12 and 13	DV-channel bit with balance bit
14 and 15	F_A auxiliary framing bit or Q bit with balance bit
16-24	BV2 channel (first octet) with balance bit
25 and 26	DV-channel bit with balance bit
27-35	BV1 channel (second octet) with balance bit
36 and 37	DV-channel bit with balance bit
38-46	BV2 channel (second octet) with balance bit
47 and 48	DV channel bit with balance bit

5.4.2.2 *Master to slave*

Frames transmitted by the master contain an echo channel (E bits) used to retransmit the DV bits received from the slaves. The DV-echo channel is used for DV-channel access control. The last bit of the frame (L bit) is used for balancing each complete frame.

The bits are grouped as follows:

Bit position	*Group*
1 and 2	framing signal with balance bit
3-10	BV1 channel (first octet)
11	E, DV-echo-channel bit
12	DV-channel bit
13	bit A used for activation
14	F_A auxiliary framing bit
15	N bit (coded as defined in § 6.3)
16-23	BV2 channel (first octet)
24	E, DV-echo-channel bit
25	DV-channel bit
26	M, multiframing bit
27-34	BV1 channel (second octet)
35	E, DV-echo-channel bit
36	DV-channel bit
37	S, layer 1 multiframe channel bit
38-45	BV2 channel (second octet)
46	E, DV-echo-channel bit
47	DV-channel bit
48	frame balance bit

5.4.2.3 *Relative bit positions*

At the slave mode equipment, timing in the direction to the master mode equipment shall be derived from the frames received from the master mode equipment.

The first bit of each frame transmitted from a slave equipment towards the master equipment shall be delayed, nominally, by two bit periods with respect to the first bit of the frame received from the master equipment. Figure 3/V.230 illustrates the relative bit positions for both transmitted and received frames.

5.5 *Line code*

For both directions of transmission, pseudo-ternary coding is used with 100% pulse width as shown in Figure 4/V.230. Coding is performed in such a way that a binary ONE is represented by no line signal; whereas, a binary ZERO is represented by a positive or negative pulse. The first binary ZERO following the framing balance bit is of the same polarity as the framing balance bit. Subsequent binary ZEROs must alternate in polarity. A balance bit is a binary ZERO if the number of binary ZEROs following the previous balance bit is odd. A balance bit is a binary ONE if the number of binary ZEROs following the previous balance bit is even.

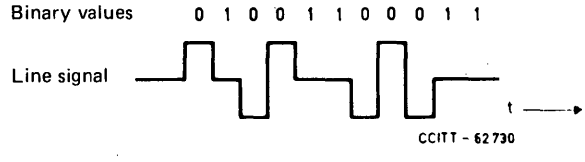


FIGURE 4/V.230

Pseudo-ternary code – example of application

5.6 *Timing considerations*

Equipment may employ one of two timing sources, if available, for transmission of frames across the interface:

- timing derived from an internal source or from an external source conveyed to the equipment by other means (e.g. timing derived from the receive line timing by a V-DCE). This is referred to as "master timing mode". Exactly one equipment on a GDCI bus must operate in this mode.
- timing derived from the receive side of the interface ("loopback timing"). This is referred to as "slave timing mode".

6 Interface procedures

6.1 *DV-channel access procedure*

The following procedure allows for a number of slave mode equipments connected in a multipoint configuration to gain access to the DV channel in an orderly fashion. The procedure always ensures that, even in cases where two or more equipments attempt to access the DV channel simultaneously, one, but only one, of the equipments will be successful in completing transmission of its information. This procedure relies upon the use of layer 2 frames delimited by flags consisting of the binary pattern "01111110" and the use of zero bit insertion to prevent flag imitation (see Recommendation I.441).

The procedure also permits equipment to operate in a point-to-point manner.

6.1.1 *Interframe (layer 2) time fill*

When a slave mode equipment has no layer 2 frames to transmit, it shall send binary ONEs on the DV channel, i.e., the interframe time fill in the slave-to-master direction shall be all binary ONEs.

When a master timing mode equipment has no layer 2 frames to transmit, it shall send binary ONEs or HDLC flags on the DV channel, i.e., the interframe time fill in the master-to-slave direction shall be either all binary ONEs or repetitions of the octet "01111110". When the interframe time fill is HDLC flags, the flag which defines the end of a frame may define the start of the next frame.

6.1.2 *D-echo channel*

The master timing mode equipment, on receipt of a DV-channel bit, shall reflect the binary value, in the next available DV-echo-channel bit position towards the slave mode equipment.

6.1.3 *DV-channel monitoring*

Slave mode equipment, while in the active condition, shall monitor the DV-echo channel, counting the number of consecutive binary ONEs. If a ZERO bit is detected, the equipment shall restart counting the number of consecutive ONE bits. The current value of the count is called C.

Note – C need not be incremented after the value eleven has been reached.

6.1.4 *Priority mechanism*

Layer 2 frames are transmitted using one of two priority classes. Priority class 1 frames are given priority over priority class 2 frames. Furthermore, to ensure that within each priority class all competing equipments are given a fair access to the DV channel, once an equipment has successfully completed the transmission of a frame, it is given a lower level of priority within that class. The equipment is given back its normal level within a priority class when all equipments have had an opportunity to transmit information at the normal level within that priority class.

The priority class of a particular layer 2 frame may be a characteristic of the equipment which is preset at manufacture or at installation, or it may be passed down from layer 2 as a parameter of the PH-DATA REQUEST primitive. A dual mode (GDCI/ISDN) terminal may thus use the PH-DATA REQUEST primitive to establish the proper priorities for its operation.

The priority mechanism is based on the requirement that slave mode equipment may start layer 2 frame transmission only when C (see § 6.1.3) is equal to, or exceeds, the value X_1 for priority class 1 or is equal to, or exceeds, the value X_2 for priority class 2. The value of X_1 shall be eight for the normal level and nine for the lower level of priority. The value of X_2 shall be ten for the normal level and eleven for the lower level of priority.

In a priority class, the value of the normal level of priority is changed into the value of the lower level of priority (i.e., higher value) when the equipment has successfully transmitted a layer 2 frame of that priority class.

The value of the lower level of priority is changed back to the value of the normal level of priority when C (see § 6.1.3) equals the value of the lower level of priority (i.e., higher value).

6.1.5 *Collision detection*

While transmitting information in the DV channel, slave mode equipment shall monitor the received DV-echo channel and compare the last transmitted bit with the next available DV-echo bit. If the transmitted bit is the same as the received echo, the equipment shall continue its transmission. If, however, the received echo is different from the transmitted bit, the equipment shall cease transmission immediately and return to the DV-channel monitoring state.

6.1.6 *Priority system*

Annex B describes an example of how the priority system may be implemented.

6.2 *Activation/deactivation*

6.2.1 *Definitions*

6.2.1.1 *Slave mode equipment states (normally DTE)*

6.2.1.1.1 State F1 (inactive): In this inactive state, the equipment is not transmitting. This state is entered upon loss of power.

6.2.1.1.2 State F2 (sensing): This state is entered after the equipment has been powered on, but has not determined the type of signal (if any) being received.

6.2.1.1.3 State F3 (deactivated): This is the deactivated state of the physical protocol. Neither the master nor the slave equipment is transmitting.

6.2.1.1.4 State F4 (awaiting signal): When the equipment is requested to initiate activation by means of an ACTIVATE REQUEST primitive, it transmits a signal (INFO 1) and waits for a response.

6.2.1.1.5 State F5 (identifying input): At the first receipt of any signal from the master mode equipment, the slave mode equipment ceases to transmit INFO 1 and awaits identification of signal INFO 2 or INFO 4.

6.2.1.1.6 State F6 (synchronized): When the equipment receives an activation signal (INFO 2) from the master, it responds with a signal (INFO 3) and waits for normal frames (INFO 4).

6.2.1.1.7 State F7 (identifying interface): This is a transition state during entry to normal activation. When this state is entered, a timer (T4) is started, and the appropriate (DTE or DCE) identification character is transmitted on the multiframe Q channel. This state continues until either a V-series identification character is received on the multiframe S channel or T4 times out.

6.2.1.1.8 State F8 (lost framing): This is the condition where the equipment has lost frame synchronization and is awaiting re-synchronization by receipt of INFO 2 or INFO 4 or deactivation by receipt of INFO 0.

6.2.1.1.9 State F9 (activated): This is the normal active state with the protocol activated in both directions. Both the master and slave mode equipments are transmitting normal frames.

6.2.1.2 *Master mode equipment states (normally DCE)*

6.2.1.2.1 State G1 (deactive): In this deactivated state, the equipment is not transmitting.

6.2.1.2.2 State G2 (pending activation): In this partially active state, the master mode equipment sends INFO 2 while waiting for INFO 3. This state will be entered after receiving an ACTIVATE REQUEST primitive, or on the receipt of INFO 0 or lost framing while in state G3 or G5. Then the choice to eventually deactivate is up to higher layers within the equipment.

6.2.1.2.3 State G3 (identifying interface): This is a transition state during entry to normal activation. When this state is entered, a timer (T4) is started, and the appropriate (DTE or DCE) identification character is transmitted on the multiframe S channel. This state continues until either a V-series identification (DTE or DCE) is received on the multiframe Q channel or T4 times out.

6.2.1.2.4 State G4 (pending deactivation): When the equipment wishes to deactivate, it may wait for a timer to expire before returning to the deactivated state.

6.2.1.2.5 State G5 (active): This is the normal active state where the master and slave mode equipment are transmitting INFO 4 and INFO 3 respectively. A deactivation may be initiated by a DEACTIVATE REQUEST primitive, or the equipment may remain in the active state all the time, under non-fault conditions.

6.2.1.3 *Activate primitives*

The following primitives should be used between layers 1 and 2 and between layer 1 and the management entity in the activation procedures. For use in state diagrams, etc., abbreviations of the primitive names are also given.

PH-ACTIVATE REQUEST (PH-AR)

PH-ACTIVATE INDICATION (PH-AI)

MPH-ACTIVATE REQUEST (MPH-AR)

MPH-ACTIVATE INDICATION (MPH-AI)

6.2.1.4 *Deactivate primitives*

The following primitives should be used between layers 1 and 2 and between layer 1 and the management entity in the deactivation procedures. For use in state diagrams, etc., abbreviations of the primitive names are also given.

MPH-DEACTIVATE REQUEST (MPH-DR)

MPH-DEACTIVATE INDICATION (MPH-DI)

PH-DEACTIVATE REQUEST (PH-DR)

PH-DEACTIVATE INDICATION (PH-DI)

6.2.1.5 *Management primitives*

The following primitives should be used between layer 1 and the management entity. For use in state diagrams, etc., abbreviations of the primitive names are also given.

MPH-ERROR INDICATION (MPH-EI)
Message unit contains type of error or recovery from a previously reported error.

MPH-INFORMATION INDICATION (MPH-II)
Message unit contains information regarding the physical layer conditions. The provisionally defined parameters are: connected, disconnected, attached DTE, attached DCE, attached TE, and attached NT.

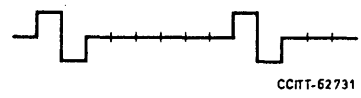
Note – Implementation of primitives in equipment is not for recommendation.

6.2.2 *Signals*

The identifications of specific signals across the GDCI are given in Table 2/V.230. Also included is the coding for these signals.

TABLE 2/V.230

Definition of INFO signals (Note 1)

Signals from MASTER TO SLAVE		Signals from SLAVE TO MASTER	
INFO 0	No signal	INFO 0	No signal
		INFO 1 (Note 2)	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs  CCITT-62731 Nominal bit rate = 192 kbit/s
INFO 2 (Note 3)	Frame with all bits of BV, DV and DV-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.		
		INFO 3	Synchronized frames with operational data on BV and DV channels.
INFO 4 (Note 3)	Frames with operational data on BV, DV and DV-echo channels. Bit A set to binary ONE.		

Note 1 – For configurations where the wiring polarity may be reversed (see § 4.3) signals may be received with the polarity of the binary ZEROs inverted. All receivers should be designed to tolerate wiring polarity reversals.

Note 2 – Slave mode equipment which does not need the capability to initiate activation of a deactivated V.230 interface need not have the capability to send INFO 1. In all other respects, this equipment shall be in accordance with § 6.2. It should be noted that in the point-to-multipoint configuration more that one slave mode equipment transmitting simultaneously will produce a bit pattern, as received by the master mode equipment, different from that described above, e.g., two or more overlapping (asynchronous) intances of INFO 1.

Note 3 – During the transmission of INFO 2 or INFO 4, the F bits and the M/bits from the master mode equipment provide the Q-bit pattern designation as described in § 6.3.3.

6.2.3 *Activation/deactivation procedure for slave mode equipment*

6.2.3.1 *General procedures*

All slave mode equipment conforms to the following procedures (these statements are an aid to understanding; the complete procedures are specified in § 6.2.3.2):

a) Equipment, when first connected, when power is applied, or upon the loss of frame alignment (see § 6.3.1.1) shall transmit INFO 0. However, an equipment that is disconnected but powered could be transmitting INFO 1 when connected.

b) Equipment transmits INFO 3 when frame alignment is established (see § 6.3.1.2). However, the satisfactory transmission of operational data cannot be assured prior to the receipt of INFO 4.

c) Equipment shall, when power is removed, initiate the transmission of INFO 0 before frame alignment is lost.

6.2.3.2 *Specification of the procedure*

The procedure for equipment to follow during activitation/deactivation is shown in the form of a finite state matrix Table 3/V.230. The use of the primitives at the layer 1/2 boundary and at the layer 1/management entity boundary are also included. Those primitives serve to identify the connection status, and to identify whether other equipment connected to the passive bus is operating according to V.230 or I.430.

TABLE 3/V.230

Activation/deactivation layer 1 finite state matrix for GDCI slave (DTE)

Event \ State name	Inactive	Seizing	Deactivated	Awaiting signal	Identifying input	Synchronized	Identifying interface	Lost framing	Activated
State number	F1	F2	F3	F4	F5	F6	F7	F8	F9
INFO sent	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0	INFO 3
Loss of power	/	F1	MPH-II(d); F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1
App. of power	F2	/	/	/	/	/	/	/	/
MPH-Act. Req. or PH-Act. Req.	/	|	ST.T3 F4	|	|	–	|	–	|
Expiry T3	/	/	–	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	–	–	–
Rec. INFO 0	/	MPH-II(c); F3	–	–	–	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	MPH-DI, PH-DI, MPH-EI2; F3	MPH-DI, PH-DI; F3
Rec. any signal (Note 1)	/	–	–	F6	–	/	/	–	/
Rec. INFO 2	/	MPH-II(c); F6	F6	/	F6	–	MPH-EI1; F6	MPH-EI2; F6	MPH-EI1; F6

TABLE 3/V.230 *(cont.)*

Event \ State name	Inactive	Seizing	Deactivated	Awaiting signal	Identifying input	Synchronized	Identifying interface	Lost framing	Activated
State number	F1	F2	F3	F4	F5	F6	F7	F8	F9
INFO sent	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0	INFO 3
Rec. INFO 4 (Note 2)	/	MPH-II(c), MF-Q, ST.T4; F7	Send MF-Q ST.T4; F7	/	Send MF-Q ST.T4; F7	MPH-EI2, Send MF-Q, ST.T4; F7	–	MPH-EI2, Send MF-Q, ST.T4; F7	–
Rec. MF-S (DTE)	/	/	/	/	/	/	PH-AI, MPH-AI, MPH-II (a-DTE); F9	/	Send MF-Q; –
Rec. MF-S(DCE)	/	/	/	/	/	/	PH-AI, MPH-AI, MPH-II (a-DCE); F9	/	Send MF-Q; –
Expiry T4	–	–	–	–	–	–	PH-AI, MPH-AI, MPH-II (a-NT); F9	–	–
Lost framing	/	/	/	/	/	MPH-EI1; F8	MPH-EI1; F8	–	MPH-EI1; F8

–	No change, no action
|	Impossible by the definition of the layer 1 service
/	Impossible situation
a, b; Fn	Issue primitives or take actions "a" and "b" and then go to state "Fn"
PH-AI	Primitive PH - ACTIVATE INDICATION
PH-DI	Primitive PH - DEACTIVATE INFORMATION
MPH-AI	Primitive MPH - ACTIVATE INDICATION
MPH-DI	Primitive MPH - DEACTIVATE INDICATION
MPH-EI1	Primitive MPH - ERROR INDICATION REPORTING ERROR
MPH-EI2	Primitive MPH - ERROR INDICATION REPORTING RECOVERY
MPH-II(c)	Primitive MPH - INFORMATION INDICATION (connected)
MPH-II(d)	Primitive MPH - INFORMATION INDICATION (disconnected)
MPH-II(a-DCE)	Primitive MPH - INFORMATION INDICATION (attached, V-series DCE)
MPH-II(a-DTE)	Primitive MPH - INFORMATION INDICATION (attached, V-series DTE)
MPH-II(a-NT)	Primitive MPH - INFORMATION INDICATION (attached, I-series NT)
MF-Q	Multiframe V-series equipment ID on Q-channel (either DTE or DCE ID)
MF-S	Multiframe V-series equipment ID on Q-channel
ST.T3	Start timer T3
ST.T4	Start timer T4

Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals which are available all the time. The multiframe signals must be sent for a fixed number of multiframe periods, provisionally 6 periods.

Note 1 – This event reflects the case where a signal is received and the equipment has not (yet) determined whether it is INFO 2 or INFO 4.

Note 2 – Timer 4 (T4) is a supervisory timer which provides for the master timing mode equipment(s) to recognize the multiframe identification signal and reply. If no reply is received before T4 times out, connection to an I-series NT is assumed. The value of T4 is provisionally 500 ms.

6.2.4 *Activation/deactivation for master mode equipment*

6.2.4.1 *Activating/deactivating equipment*

The procedure is shown in the form of a finite state matrix Table 4/V.230. The primitives at the layer 1/2 boundary and layer 1/management entity boundary are also shown. Those primitives serve to identify the connection status, and to identify whether other equipment connected to the passive bus is operating according to V.230 or I.430.

6.2.4.2 *Non-activating/non-deactivating equipment*

The behaviour of such equipment is the same as that of an activating/deactivating equipment never receiving DEACTIVATE REQUEST primitive. States G1 (deactive), G4 (pending deactivation) and timers 1 and 2 may not exist for such equipment.

6.2.5 *Timer values*

Timers are defined in the finite state matrix tables for both the master and slave mode GDCI equipment. The following values are defined for timers:

- Timer 1 in master mode equipment: values from 2 s (for GDCI only application) to 30 s (for dual mode GDCI or ISDN application) are acceptable.
- Timer 2 in master mode equipment: values from 25 to 100 ms are acceptable. The value may be zero if the equipment does not provide for deactivation.
- Timer 3 in slave mode equipment: value must be selected longer than the worst case time to activate the equipment. The value should be at least one second longer than the value of T1 in the master equipment connected to the GDCI.
- Timer 4: This is the time allowed for other equipment in the GDCI to recognize a V-series equipment ID on the multiframe (S or Q) channel and to respond. This should normally take less than 30 ms, so the value of T4 is provisionally set to 50 ms.

6.2.6 *Activation and deactivation times*

Slave mode equipment in the deactivated state (F3) shall, upon receipt of INFO 2, establish frame synchronization and begin transmission of INFO 3 within 100 ms. It shall recognize receipt of INFO 4 within two frames (in the absence of errors).

Slave mode equipment in the "waiting for signal" state (F4) shall, upon the receipt of INFO 2, cease the transmission of INFO 1 and initiate the transmission of INFO 0 within 5 ms and then respond to INFO 2, within 100 ms, as above. (Note that in Table 3/V.230, the transition from F4 to F5 is indicated as the result of the receipt of "any signal" which is in recognition of the fact that the equipment may not know that the signal being received is INFO 2 until after it has recognized the presence of a signal.)

Master mode equipment use of the "deactivated" and "pending activation" states remains a topic for future study. If these states and transitions are implemented, the timing recommendations of I.430 § 6.2.6.2 should be followed.

6.2.7 *Multiframe identification codes*

Two characters must be selected from the unassigned values on the multiframe Q channel to identify a V-series DTE and a V-series DCE operating in the slave timing mode. Similarly, one character must be selected from the unassigned values on the multiframe S channel (SC1) to identify a V-series DCE operating in the master timing mode.

Since there are only 16 characters available on each of these multiframe channels, the selection must be done carefully. The following character codes have provisionally been selected for the purpose of identifying V-series equipment using a GDCI:

Value ($S_{11}S_{12}S_{13}S_{14}$ or $Q_1Q_2Q_3Q_4$)	Meaning
1101 on Q channel	V-DTE, slave mode
1100 on Q channel	V-DCE, slave mode
0110 on S channel	V-DCE, master mode

Note – These codes are unassigned in the current US Draft Specification.

TABLE 4/V.230

Activation/deactivation layer 1 finite state matrix for CDCI master (DCE)

Event \ State name	Deactive	Pending activation	Identifying interface	Pending deactivation	Active
State number	G1	G2	G3	G4	G5
INFO sent	INFO 0	INFO 2	INFO 4	INFO 0	INFO 4
MPH-Act. Req. or PH-Act. Req.	Start T1; G2	|	|	Start T1; G2	|
MPH-Deact. Req. or PH-Deact. Req.	|	Start T2; PH-DI; G4	Start T2; PH-DI; G4	|	Start T2; PH-DI; G4
Expiry T1 (Note 1)	–	Start T2; PH-DI; G4	/	–	/
Expiry T2 (Note 2)	–	–	–	G1	–
Rec. INFO 0	–	–	MPH-DI, MPH-EI; G2	G1	MPH-DI, MPH-EI; G2
Rec. INFO 1	Start T1; G2	–	/	–	/
Rec. INFO 3	/	Stop T1, Start T4, Send MF-S; G3 (Note 3)	–	–	–
Rec. MF-Q (DTE)	/	/	PH-AI, MPH-AI, MPH-II(a-DTE); G5	–	Send MF-S; –
Rec. MF-Q (DCE)	/	/	PH-AI, MPH-AI, MPH-II(a-DCE); G5	–	Send MF-S; –
Expiry T4	–	–	PH-AI, MPH-AI, MPH-II(a-TE); G5	–	–
Lost framing	/	/	MPH-DI, MPH-EI; G2	–	MPH-DI, MPH-EI; G2

–	No change, no action
|	Impossible by the definition of the layer 1 service
/	Impossible situation
a, b; Gn	Issue primitives or take actions "a" and "b" then go to state "Gn"
PH-AI	Primitive PH - ACTIVATE INDICATION
PH-DI	Primitive PH - DEACTIVATE INDICATION
MPH-AI	Primitive MPH - ACTIVATE INDICATION
MPH-DI	Primitive MPH - DEACTIVATE INDICATION
MPH-EI	Primitive MPH - ERROR INDICATION REPORTING ERROR
MPH-II(a-DCE)	Primitive MPH - INFORMATION INDICATION (attached, V-series DCE)
MPH-II(a-DTE)	Primitive MPH - INFORMATION INDICATION (attached, V-series DTE)
MPH-II(a-TE)	Primitive MPH - INFORMATION INDICATION (attached, I-series TE)
MF-S	Multiframe V-series equipment ID on S-channel (currently only a DCE ID is defined)
MF-Q	Multiframe V-series equipment ID on Q-channel (DCE or DTE)

Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals which are available all the time. The multiframe signals must be sent for a fixed number of multiframe periods, provisionally 6 periods.

Note 1 – Timer 1 (T1) is a supervisory timer which has to take into account the overall time to activate.

Note 2 – Timer 2 (T2) prevents unintentional reactivation. Its value is normally between 25 ms and 100 ms. This implies that a slave timing mode equipment must recognize INFO 0 and react on it within 25 ms. If the master timing mode equipment is able to unambiguously recognize INFO 1, or if the master timing mode equipment does not use the MPH-DEACTIVATE REQUEST primitive, then the value of T2 may be 0.

Note 3 – Timer 4 (T4) is a supervisory timer which provides time for the slave timing mode equipment(s) to recognize the multiframe identification signal and reply. If no reply is received before T4 times out, connection to an I-series TE is assumed. The value of T4 is provisionally 50 ms.

6.3 *Frame alignment procedures*

The first bit of each frame is the framing bit, *f*; it is a binary ZERO.

The frame alignment procedure makes use of the fact that the framing bit is represented by a pulse having the same polarity as the preceding pulse (line code violation). This allows rapid reframing.

According to the coding rule, both the framing bit and the first binary ZERO bit following the framing balance bit (in the same frame) produce a line code violation. To guarantee secure framing, the auxiliary framing bit pair F_A and N in the direction master-to-slave or the auxiliary framing bit F_A with the associated balancing bit L in the direction slave-to-master are introduced. This ensures that there is a line code violation at 14 bits or less from the framing bit F, due to F_A or N being a binary ZERO bit (master-to-slave) or to F_A being a binary ZERO bit (slave-to-master) if the F_A bit position is not used as a Q bit. The framing procedures do not depend on the polarity of the framing bit F, and thus are not sensitive to wiring polarity.

The coding rule for the auxiliary framing bit pair F_A and N, in the direction master-to-slave, is such that N is the binary opposite of F_A ($N = \overline{F_A}$). The F_A and L bits in the direction slave-to-master are always coded such that the binary values of F_A and L are equal.

6.3.1 *Frame alignment procedure in the direction master-to-slave to slave timing mode equipment*

Frame alignment, on initial activation of the slave mode equipment, shall comply with the procedures defined is § 6.2.

6.3.1.1 *Loss of frame alignment*

Loss of frame alignment may be assumed when a time period equivalent to two 48-bit frames has elapsed without having detected valid pairs of line code violations obeying the $\leqslant$ 14 bit criterion as described above. The slave timing mode equipment shall cease transmission immediately.

6.3.1.2 *Frame alignments*

Frame alignment may be assumed to occur when three consecutive pairs of line code violations obeying the $\leqslant$ 14 bit criterion have been detected.

6.3.2 *Frame alignment in the direction slave-to-master timing mode equipment*

The criterion of a line code violation at 13 bits or less from the framing bit (F) shall apply except if the Q channel (see § 6.3.3) is provided, in which case the 13-bit criterion applies in four out of five frames.

6.3.2.1 *Loss of frame alignment*

The master mode equipment may assume loss of frame alignment if a time equivalent to at least two 48-bit frames has elapsed since detecting consecutive violations according to the 13-bit criterion, if all F_A bits have been set to binary ZERO. Otherwise, a time period equivalent to at least three 48-bit frames shall be allowed before assuming loss of frame alignment. On detection of loss of frame alignment, the master equipment shall continue transmitting towards the slave equipment.

6.3.2.2 *Frame alignment*

The master timing mode equipment may assume that frame alignment has been regained when three consecutive pairs of line code violations obeying the 13-bit criterion has been detected.

6.3.3 *Multi-framing*

A multi-frame described in the following paragraphs is intended to provide extra layer 1 capacity in the slave-to-master direction through the use of an extra channel between the slave and master equipment (Q channel).

The use of the Q bits shall be the same in point-to-point as in point-to-multipoint configurations. Future standardization for the use of Q bits is for further study. (There is no inherent collision detection mechanism provided, and any collision detection mechanism that is required for any application of the Q bits will be outside the scope of this Recommendation.)

6.3.3.1 *General mechanism*

a) Q bit identication: The Q bits (slave mode to master mode equipment) are defined to be the bits in the F_A bit position of every fifth frame. The Q bit positions in the slave-to-master direction are identified by binary inversions of the F_A/N bit pair (F_A = binary ONE, N = binary ZERO) in the master-to-slave direction. The provison for identification of the Q-bit positions in the master-to-slave direction permits all slave mode equipment to synchronize transmission in Q-bit positions, thereby avoiding interference of F_A bits from one equipment with the Q bits of a second equipment in passive bus configurations.

b) Multi-frame identification: A multi-frame, which provides for structuring the Q bits in groups of four (Q1-Q4), is established by setting the M bit, in position 26 of the master-to-slave frame, to binary ONE in every twentieth frame. This structure provides for 4-bit characters in a single channel, slave-to-master.

6.3.3.2 *Q-bit position identification algorithm*

The Q-bit position identification algorithm is illustrated in Table 5/V.230. Two examples of how such an identification algorithm can be realized are as follows. The slave mode equipment Q-bit identification algorithm may be simply the transmission of a Q-bit in each frame in which a binary ONE is received in the F_A-bit position of the master-to-slave frame (i.e., echoing of the received F_A bits). Alternatively, to minimize the Q-bit transmission errors that could result from errors in the F_A bits of master-to-slave frames, a slave mode equipment may

synchronize a frame counter to the Q-bit rate and transmit Q bits in every fifth frame, i.e., in frames in which F_A should be present. Q bits would be transmitted only after counter synchronization to the binary ONEs in the F_A bit positions of the master-to-slave frames is achieved (and only if such bits are received). When the counter is not synchronized (not achieved or lost), a slave mode equipment which uses such an algorithm shall transmit binary ZEROs in Q-bit positions. The algorithm used by a slave mode equipment to determine when synchronization is defined to be achieved or the algorithm used to determine when it is defined to be lost is not described in this Recommendation.

No special Q-bit identification is required in the master mode equipment because the maximum round trip delay of the master-to-slave-to-master is a small fraction of a frame, and therefore, Q-bit identification is inherent in the master timing mode equipment.

TABLE 5/V.230

Q-bit position identification and multiframe structure

Frame number	MASTER TO SLAVE F_A bit position	SLAVE TO MASTER F_A bit position (1, 2)	MASTER TO SLAVE M bit
1	ONE	Q1	ONE
2	ZERO	ZERO	ZERO
3	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO
6	ONE	Q2	ZERO
7	ZERO	ZERO	ZERO
8	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO
11	ONE	Q3	ZERO
12	ZERO	ZERO	ZERO
13	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO
16	ONE	Q4	ZERO
17	ZERO	ZERO	ZERO
18	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO
1	ONE	Q1	ONE
2	ZERO	ZERO	ZERO
etc.			

Note 1 – If the Q bits are not used by a slave mode equipment, the Q bits shall be set to binary ONE.

Note 2 – Where multiframe identification is not provided with a binary ONE in an appropriate M bit, but where Q-bit positions are identified, Q bits 1 through 4 are not distinguished.

6.3.3.3 *Slave timing mode equipment multiframe identification*

The first frame of the multiframe is identified by the M bit equal to a binary ONE. Slave mode equipment shall use the M bit equal to a binary ONE to identify the start of the multiframe.

The algorithm used by a slave mode equipment to determine when synchronization or loss of synchronization of the multiframe is achieved is not described in this Recommendation.

6.3.4 *S channel structuring algorithm*

The algorithm for structuring the S bits (master-to-slave frame bit position 37) into an S channel uses the same combination of the F_A bit inversions and the M bit that is used to structure the Q channel as described in § 6.3.3. The S channel structure, shown in Table 6/V.230, provides for five subchannels, SC1 through SC5. Each subchannel SCn is comprised of the bits SCn1 through SCn4 which provides for the transfer of one 4-bit character per multiframe (5 ms). This Recommendation discusses the use of subchannel SC1 only. Subchannels SC2 through SC5 are reserved for future use, and shall be coded with all binary ZEROs. The coding and use of the 4-bit character of SC1 are discussed in § 6.2.7.

TABLE 6/V.230

S-channel structure

Frame number	F_A bit	M bit	S bit
1	ONE	Q1	SC11
2	ZERO	ZERO	SC21
3	ZERO	ZERO	SC31
4	ZERO	ZERO	SC41
5	ZERO	ZERO	SC51
6	ONE	ZERO	SC12
7	ZERO	ZERO	SC22
8	ZERO	ZERO	SC32
9	ZERO	ZERO	SC42
10	ZERO	ZERO	SC52
11	ONE	ZERO	SC13
12	ZERO	ZERO	SC23
13	ZERO	ZERO	SC33
14	ZERO	ZERO	SC43
15	ZERO	ZERO	SC53
16	ONE	ZERO	SC14
17	ZERO	ZERO	SC24
18	ZERO	ZERO	SC34
19	ZERO	ZERO	SC44
20	ZERO	ZERO	SC54
1	ONE	ONE	SC11
2	ZERO	ZERO	SC21
etc.			

Note – Subchannels SC2 through SC5 are reserved for future standardization, and are set to all binary ZEROs.

6.4 *Idle channel code on the BV channels*

A slave mode equipment shall send binary ONEs in any BV channel which is not assigned to it.

7 Layer 1 maintenance

Test loopbacks, similar to those defined in Recommendation I.430, are for further study.

8 Electrical characteristics

8.1 *Bit rate*

8.1.1 *Nominal rate*

The nominal bit rate is 192 kbit/s.

8.1.2 *Tolerance*

The tolerance (free running mode) is ± 100 ppm.

8.2 *Jitter and bit-phase relationship between slave mode equipment input and output*

8.2.1 *Test configurations*

The jitter and phase deviation measurements are carried out with four different waveforms at the slave mode equipment input, in accordance with the following configurations:

i) point-to-point configuration with 6 dB attenuation measured between the two terminating resistors at 96 kHz (high capacitance cable);

ii) short passive bus with 8 units (including the unit under test) clustered at the far end from the signal source (high capacitance cable);

iii) a) and b) short passive bus with the unit under test adjacent to the signal source and the other seven units clustered at the far-end from the signal source (high and low capacitance cable);

iv) ideal test signal condition, with one source connected directly to the receiver of the unit under test (i.e., without artificial line).

Examples of waveforms that correspond to the configurations i), ii), iiia) and iiib) are given in Figures 5/V.230 to 8/V.230. Test configurations which can generate these signals are given in Annex C.

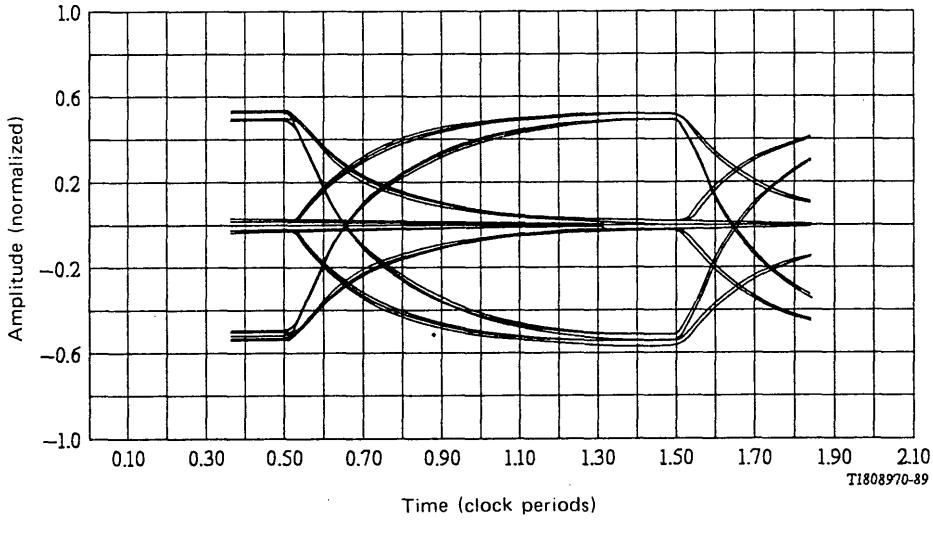


FIGURE 5/V.230

Waveform for test configuration i) – point-to-point (6 dB) (C = 120 nF/km)

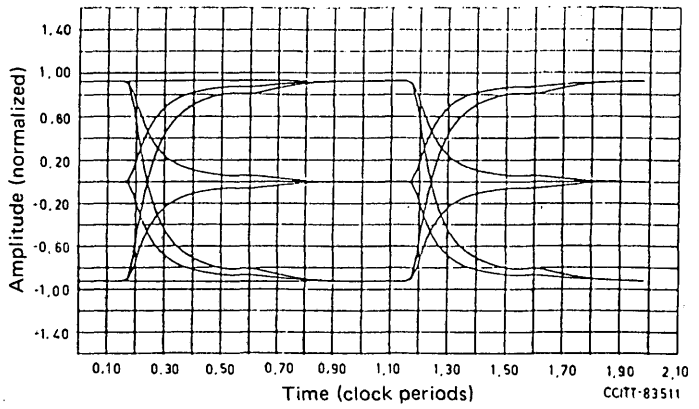


FIGURE 6/V.230

Waveform for test configuration ii) – short passive bus with 8 clustered slave mode equipments at the far end (C = 120 nF/km)

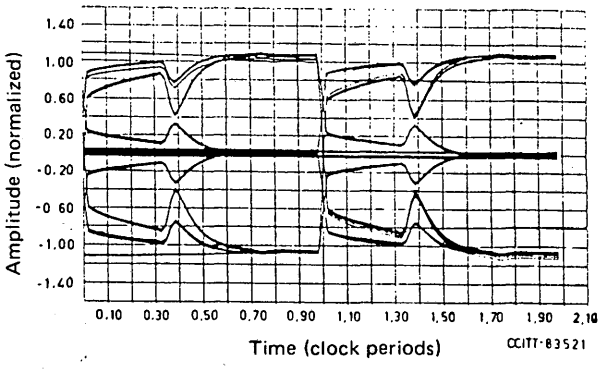


FIGURE 7/V.230

Waveform for test configuration iii a) – short passive bus with 1 slave mode equipment near to the master mode equipment and 7 slave mode equipments at the far end (C = 120 nF/km)

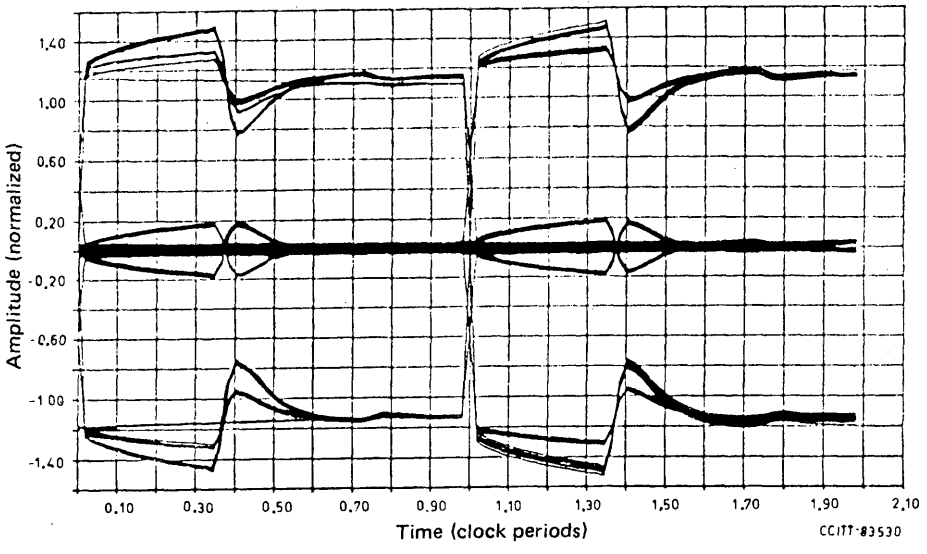


FIGURE 8/V.230

Waveform for test configuration iii b) – short passive bus with 1 slave mode equipment near to the master mode equipment and 7 slave mode equipments at the far end (C = 30 nF/km)

8.2.2 *Timing extraction jitter*

Timing extraction jitter, as observed at the slave mode equipment output, shall be within −7% to +7% of a bit period, when the jitter is measured using a high pass filter with a cut-off frequency (3 dB point) of 30 Hz under the test conditions described in § 8.2.1. The limitation applies with an output data sequence having binary ZEROs in both BV channels and with input data sequences described in a) to c) following. The limitation applies to the phase of all zero-volt crossings of all adjacent binary ZEROs in the output data sequence.

a) A sequence consisting of continuous frames with all binary ONEs in DV, DV-echo and both BV channels.

b) A sequence, repeated continuously for at least 10 seconds, consisting of:

   – 40 frames with continuous octets of "10101010" (the first bit to be transmitted is binary ONE) in both BV channels and continuous binary ONEs in DV and DV-echo channels followed by:

   – 40 frames with continuos binary ZEROs in DV, DV-echo and both BV channels.

c) A sequence consisting of a pseudo-random pattern with a length of $2^{19} - 1$ in DV, DV-echo and both BV channels. (This pattern may be generated with a shift register with 19 stages with the outputs of the first, the second, the fifth and the nineteenth stages added together (modulo 2) and fed back to the input.)

8.2.3 *Total phase deviation, input to output*

The total phase deviation (including effects of timing extraction in the slave mode equipment), between the transitions of signal elements at the output of the slave mode equipment and the transitions of signal elements associated with the signal applied to the input, should not exceed the range of −7% to +15% of a bit period. This limitation applies to the output signal transitions of each frame with the phase reference defined as the average phase of the crossing of zero volts which occurs between the framing pulse and its associated balance pulse at the start of the frame and the corresponding crossings at the start of the three preceding frames of the input signal. For the purposes of demonstrating compliance of an equipment, it is sufficient to use (as the input signal phase

reference) only the crossing of zero volts between the framing pulse and its associated balance pulse of the individual frame. This latter method, requiring a simpler test set, may create additional jitter at frequencies higher than about 1 kHz and is therefore more restrictive. The limitation applies to the phase of the zero-volt crossings of all adjacent binary ZEROs in the output data sequence, which shall be as defined in § 8.2.2. The limitation applies under all test conditions described in § 8.2.1, with the additional input signal conditions specified in a) to d) following, and with superimposed jitter as specified in Figure 9/V.230 over the range of frequencies from 5 Hz to 2 kHz. The limitation applies for input bit rates of 192 kbit/s ± 100 ppm.

a) A sequence consisting of continuous frames with all binary ONEs in the DV, DV-echo and both BV channels.

b) A sequence consisting of continuous frames with the octet "10101010" (the first bit to be transmitted is binary ONE) in both BV channels and binary ONEs in DV and DV-echo channels.

c) A sequence of continuous frames with binary ZEROs in DV, DV-echo and both BV channels.

d) A sequence of continuous frames with a pseudo-random pattern, as described in § 8.2.2 c), in DV, and both BV channels.

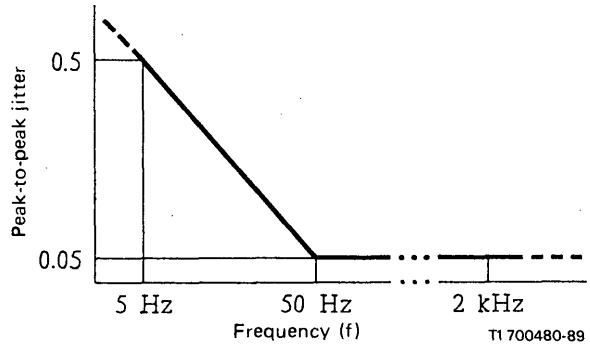


FIGURE 9/V.230

Lower limit of maximum tolerable jitter at slave mode equipment input (log-log scale)

8.3 *Master mode equipment jittter characteristics*

The maximum jitter (peak-to-peak) in the output sequence of a master mode equipment shall be 5% of a bit period when measured using a high pass filter having a cut-off frequency (3 dB point) of 50 Hz and an asymptotic roll off 20 dB per decade. The limitation applies for all data sequences, but for the purpose of demonstrating the compliance of an equipment, it is sufficient to measure jitter with output data sequence consisting of binary ONEs in DV and BV channels and with additional sequence as described in § 8.2.2. c) in DV and BV channels. The limitation applies to the phase of all-zero volt crossings of all adjacent binary ZEROs in the output data sequence.

8.4 *Termination of the line*

The interchange circuit pair termination (resistive) should be 100 ohms ± 5% (see Figure 2/V.230).

8.5 *Transmitter output characteristics*

8.5.1 *Transmitter output impedance*

The following requirements apply at interface point I_A (see Figure 2/V.230 for slave mode equipment) and at interface point I_B for master mode equipment (see §§ 4.5 and 8.9 regarding cordage capacitance).

8.5.1.1 *Master mode equipment transmitter output impedance*

a) When inactive or transmitting a binary ONE, the output impedance, in the frequency range of 2 kHz to 1 MHz, shall exceed the impedance indicated by the template in Figure 10/V.230. The requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value).

Note – In some applications, the terminating resistor can be combined with the master mode equipment (see point B of Figure 2/V.230). The resulting impedance is the impedance needed to exceed the combination of the template and the 100-ohm termination.

b) When terminating a binary ZERO, the output impedance shall be $\geqslant$ 20 ohms.

Note – The output impedance limit shall apply for two nominal load impedance (resistive) conditions: 50 ohms and 400 ohms. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10%. The peak amplitude shall be defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

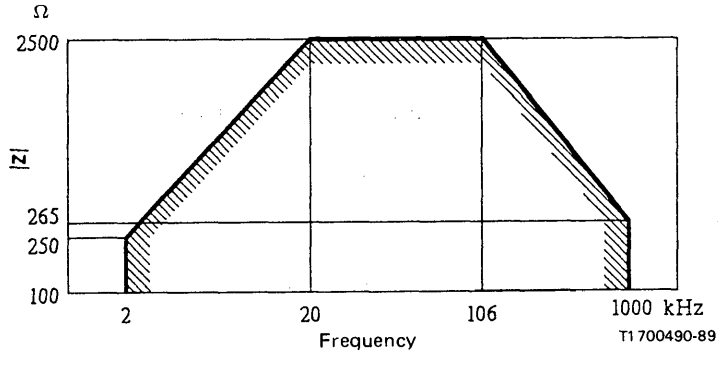


FIGURE 10/V.230

Master mode equipment impedance template (log-log scale)

8.5.1.2 *Slave mode equipment transmitter output impedance*

a) In the inactive and powered down states or when transmitting a binary ONE, the following requirements apply:

i) the output impedance, in the frequency range of 2 kHz to 1 MHz, should exceed the impedance indicated by the template in Figure 11/V.230. This requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value);

ii) at a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1.2 V (peak value) should not exceed 0.6 mA (peak value).

b) When transmitting a binary ZERO, the output impedance shall be $\geqslant$ 20 ohms.

Note – The output impedance limit shall apply for two nominal load impedance (resistive) conditions: 50 ohms and 400 ohms. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10%. The peak amplitude shall be defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

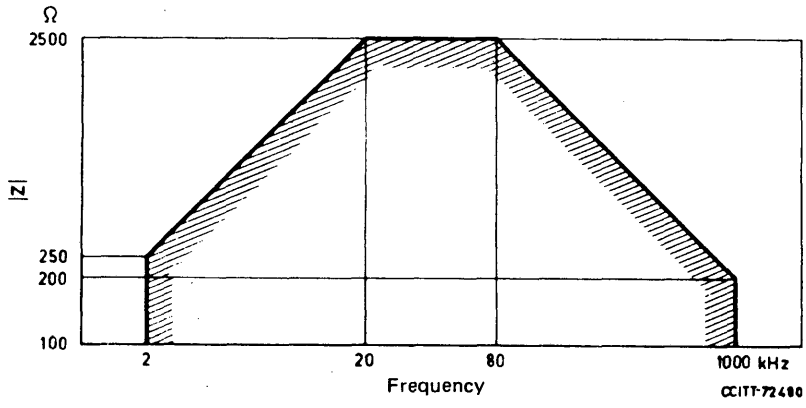


FIGURE 11/V.230

Slave mode equipment impedance template (log-log scale)

8.5.2 *Test load impedance*

The test load impedance shall be 50 ohms (unless otherwise indicated).

8.5.3 *Pulse shape and amplitude (binary ZERO)*

8.5.3.1 *Pulse shape*

Except for overshoot, limited as follows, pulses shall be within the mask of Figure 12/V.230. Overshoot, at the leading edge of pulses, of up to 5% of the pulse amplitude at the middle of a signal element, is permitted, provided that such overshoot has, at 1/2 of its amplitude, a duration of less than 0.25 μs.

8.5.3.2 *Nominal pulse amplitude*

The nominal pulse amplitude shall be 750 mV, zero to peak.

A positive pulse (in particular, a framing pulse) at the output port of master mode and slave mode equipment is defined as a positive polarity of the voltage measured between access leads e to f and d to c respectively (see Figure 20/I.430). (See Table 7/V.230 for the relationship to connector pins.)

8.5.4 *Pulse unbalance*

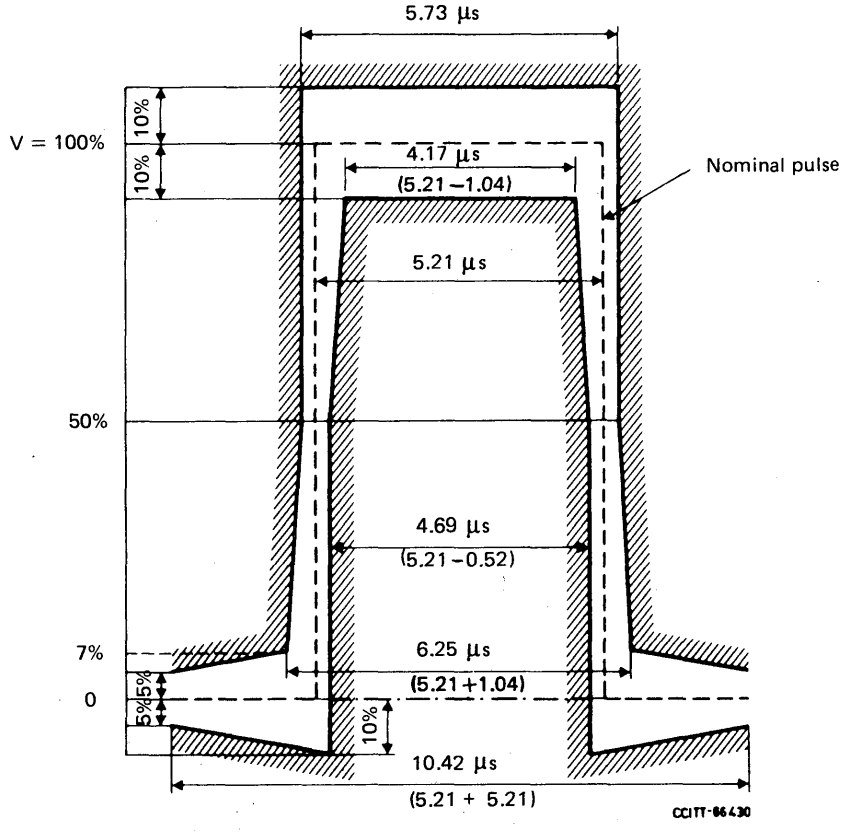
The "pulse unbalance", i.e., the relative difference in $\int U(t)\,dt$ for positive pulses and $\int U(t)\,dt$ for negative pulses shall be $\leqslant$ 5%.

8.5.5 *Voltage on other test loads (slave mode equipment)*

The following requirements are intended to assure compatibility with the condition where multiple slave mode equipments are simultaneously transmitting pulses on to a passive bus.

8.5.5.1 *400-ohm load*

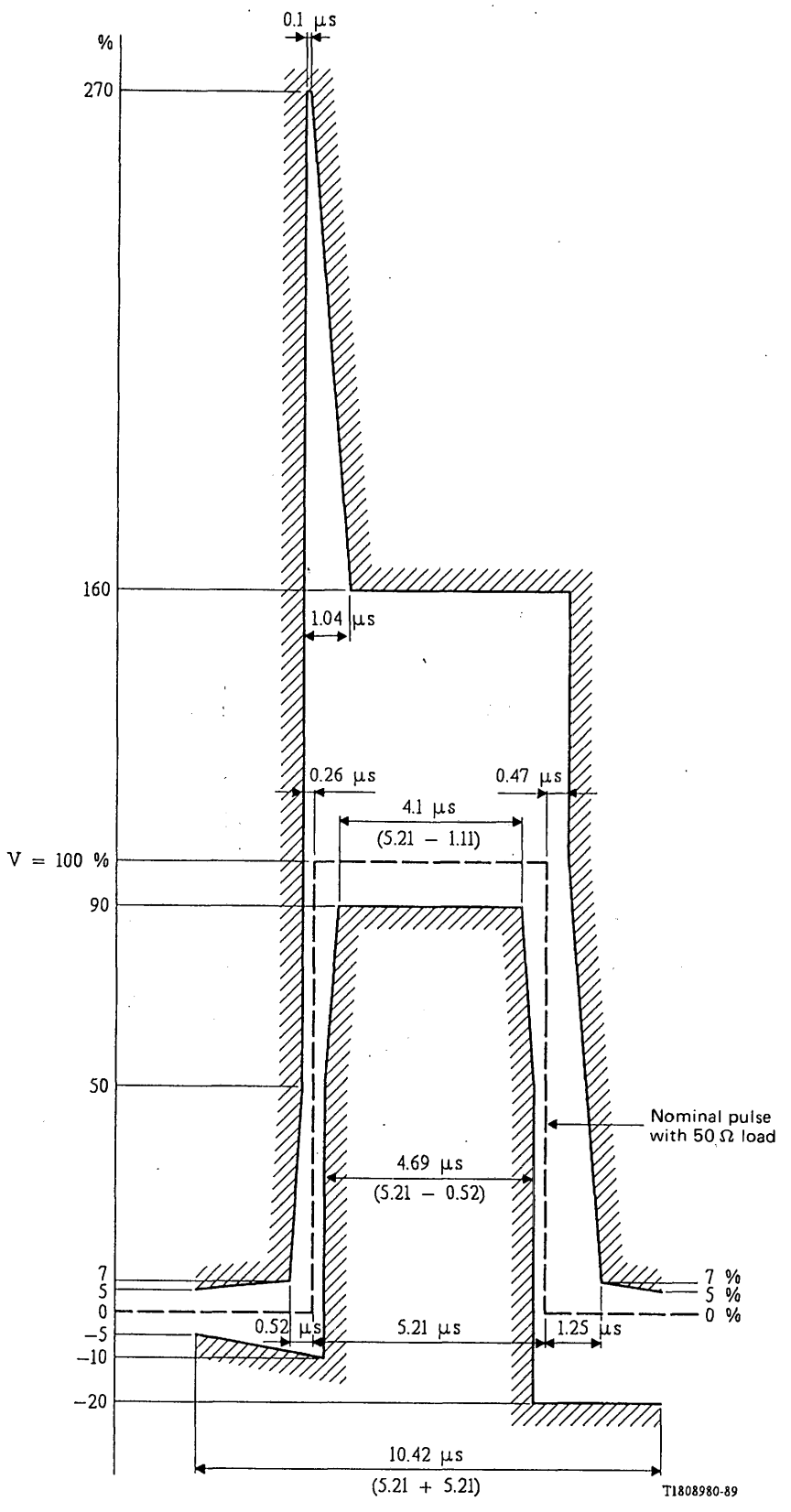
A pulse (binary ZERO) shall conform to the limits of the mask shown in Figure 13/V.230 when the transmitter is terminated in a 400-ohm load.



Note – For clarity of presentation, the above values are based on a pulse width of 5.21 µs. See § 8.1 for a precise specification of the bit rate.

FIGURE 12/V.230

Transmitter output pulse mask



Note – For clarity of presentation, the above values are based on a pulse width of 5.21 µs. See § 8.1 for a precise specification of the bit rate.

FIGURE 13/V.230

Voltage for an isolated pulse with a test load of 400 ohms

8.5.5.2 *5.6-ohm load*

To limit the current flow with two drivers having opposite polarities, the pulse amplitude (peak) with a 5.6-ohm load shall be $\leqslant$ 20% of the nominal pulse amplitude.

8.5.6 *Unbalance about earth*

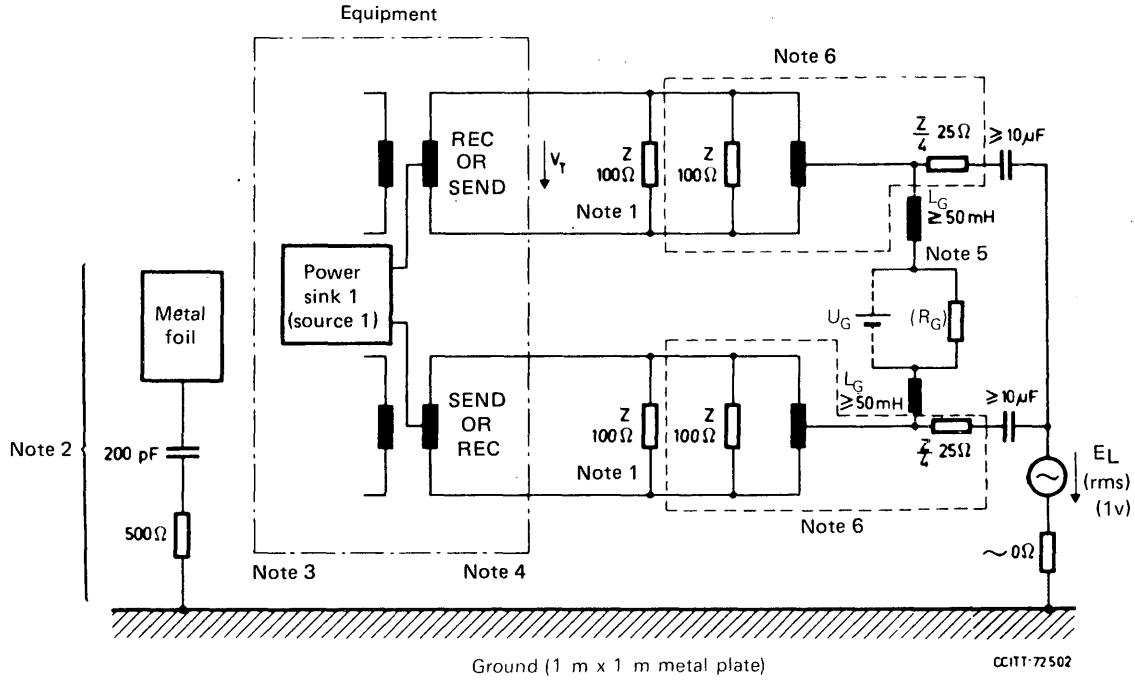
The following requirements apply under all possible power feeding conditions, under all possible connections of the equipment to ground, and with two 100-ohm terminations across the transmit and receive ports.

8.5.6.1 *Longitudinal conversion loss*

Longitudinal conversion loss (LCL), which is measured in accordance with Recommendation G.117, § 4.1.3 (see Figure 14/V.230), shall meet the following requirements:

a) 10 kHz $< f \leqslant$ 300 kHz: $\geqslant$ 54 dB

b) 300 kHz $< f \leqslant$ 1 MHz: minimum value decreasing from 54 dB at 20 dB/decade.



The longitudinal conversion loss: $LCL = 20 \log_{10} \left| \frac{E_L}{V_T} \right|$ dB

The voltages V_T and E_L should be measured within the frequency range from 10 kHz up to 1 MHz using selective test measuring equipment.

The measurement should be carried out in the states:

- deactivated (receive, send),
- power off (receive, send),
- activated (receive).

The interconnecting cord shall lie on the metal plate.

Note 1 – This resistor must be omitted if the termination is already built into the equipment.

Note 2 – Hand imitation is a thin metal foil with approximately the size of a hand.

Note 3 – Equipment with metallic housing shall have a galvanic connection to the metal plate. Other equipment with non-metallic housing shall be placed on the metal plate.

Note 4 – The power cord for mains-powered equipment shall lie on the metal plate and the earth protective wire of the mains shall be connected to the metal plate.

Note 5 – If there is no power source 1 in the master mode equipment, R_G and L_G are not required.

Note 6 – This circuit provides a transverse termination of 100 ohms and a balanced longitudinal termination of 25 ohms. Any equivalent circuit is acceptable. However, for equivalent circuits given in Recommendations G.117 and O.121, powering cannot be provided.

FIGURE 14/V.230

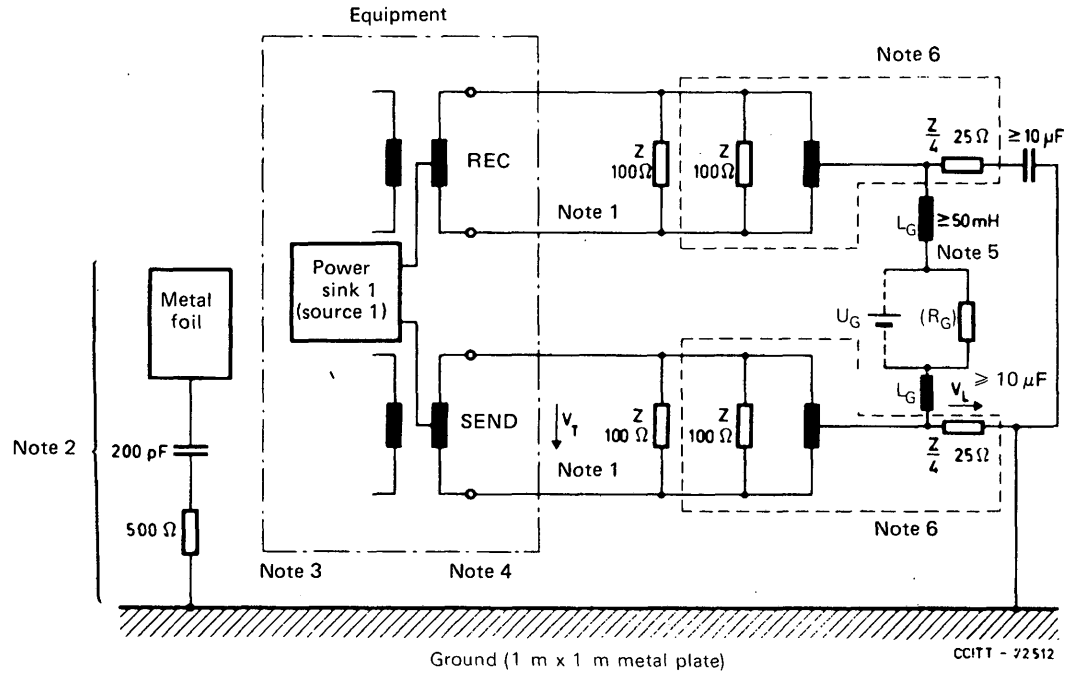
Receiver input or transmitter output unbalance about earth

8.5.6.2 *Output signal balance*

Output signal balance which is measured in accordance with Recommendation G.117, § 4.3.1 (see Figure 15/V.230), shall meet the following requirements:

a) f – 96 kHz: $\geqslant$ 54 dB

b) 96 kHz $< f \leqslant$ 1 MHz: minimum value decreasing from 54 dB at 20 dB/decade.



Output signal balance = $20 \log_{10} \left| \frac{V_T}{V_L} \right|$ dB

The voltage V_T and V_L should be measured within the frequency range from 10 kHz up to 1 MHz using selective test measuring equipment. The measurement should be carried out in the active state. The pulse patterns should contain all binary ZEROs. However, for the purpose of demonstrating the compliance of an equipment, it is sufficient to measure the output signal unbalance about earth with a pulse pattern of continuous frames with at least the B1 and B2 Channels containing all binary ZEROs.

The interconnecting cord shall lie on the metal plate.

Note – See notes to this figure in Figure 14/V.230.

FIGURE 15/V.230

Transmitter output unbalance about earth

8.6 *Receiver input characteristics*

8.6.1 *Receiver input imbalance*

8.6.1.1 *Slave mode equipment receiver input impedance*

Slave mode equipment shall meet the same input impedance requirements as specified in § 8.5.1.2 a) for the output impedance.

8.6.1.2 *Master mode equipment receiver input impedance*

In the inactive and powered-down states, the following requirements apply:

i) The input impedance in the frequency range of 2 kHz to 1 MHz, should exceed the impedance indicated by the template in Figure 11/V.230. This requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value).

ii) At a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1.2 V (peak value) should not exceed 0.5 mA (peak value).

Note – In some applications, the 100-ohm terminating resistor can be combined with the master mode equipment (see point B of Figure 2/V.230). The resulting impedance is the impedance needed to exceed the combination of the template and the 100-ohm termination.

8.6.2 *Receiver sensitivity – noise and distortion immunity*

Requirements applicable to the equipments for three different interface wiring configurations are given in the following sub-paragraphs. Equipment shall receive, without errors (for a period of at least one minute), an input with a pseudo-random sequence (word length $\geqslant$ 511 bits) in all information channels (combination of BV channel, DV channel and, if applicable, the DV-echo channel).

The receiver shall operate, with any input sequence, over the full range indicated by the waveform mask.

8.6.2.1 *Slave mode equipment*

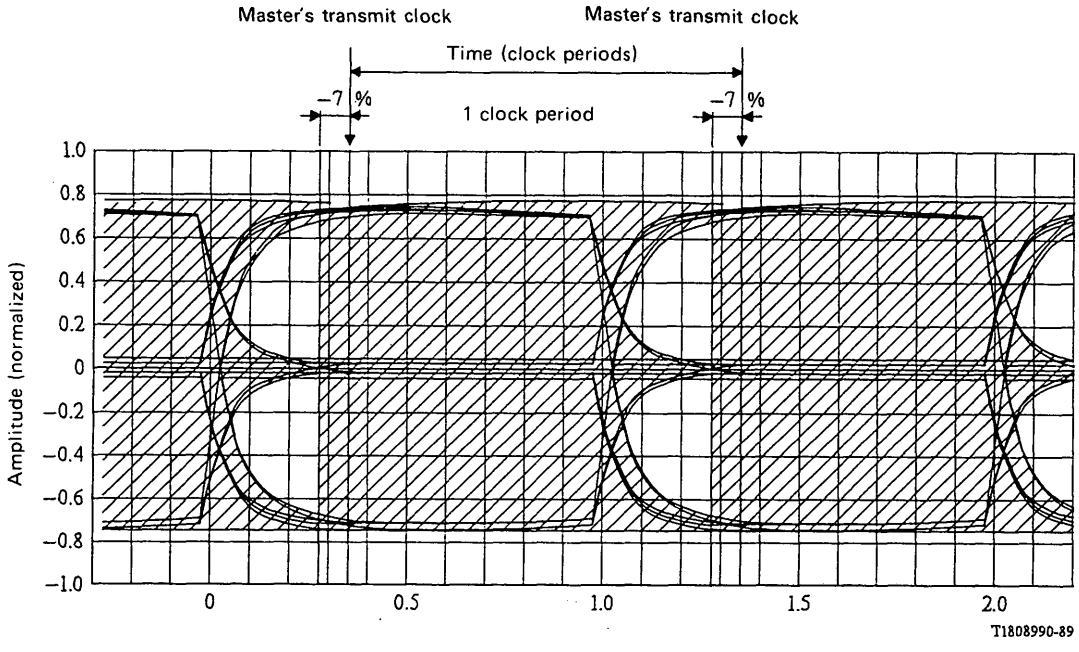
Slave mode equipment shall operate with the input signals conforming to the waveforms specified in § 8.2.1. For the waveforms in Figures 6/V.230 to 8/V.230, slave mode equipment shall operate with the input signals having any amplitude in the range of +1.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. For signals conforming to the waveform in Figure 5/V.230, operation shall be accomplished for signals having any amplitude in the range of +1.5 to −7.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. Additionally, the slave mode equipment shall operate with sinusoidal signals having an amplitude of 100 mV (peak-to-peak value) at frequencies of 200 kHz and 2 MHz superimposed individually on the input signals having the waveform shown in Figure 5/V.230.

8.6.2.2 *Master mode equipment for short passive bus (fixed timing)*

Master mode equipment designed to operate with only short passive bus wiring configurations shall operate when receiving input signals indicated by the waveform shown in Figure 16/V.230. Master mode equipment shall operate, with the input signals having any amplitude in the range of +1.5 dB to −3.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2.

8.6.2.3 *Master mode equipment for both point-to-point and short passive bus configurations (adaptive timing)*

Master mode equipment designed to operate with either point-to-point or short passive bus wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in Figure 17/V.230. These master mode equipments shall operate with the input signals having any amplitude in the range of +1.5 dB to −3.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. These master mode equipments shall also operate when receiving signals conforming to the waveform in Figure 5/V.230. For signals conforming to this waveform, operation shall be accomplished for signals having any amplitude in the range of +1.5 to −7.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. Additionally, these master mode equipments shall operate with the sinusoidal signals, as specified in § 8.6.2.1, superimposed on the input signals having the waveform in Figure 5/V.230.

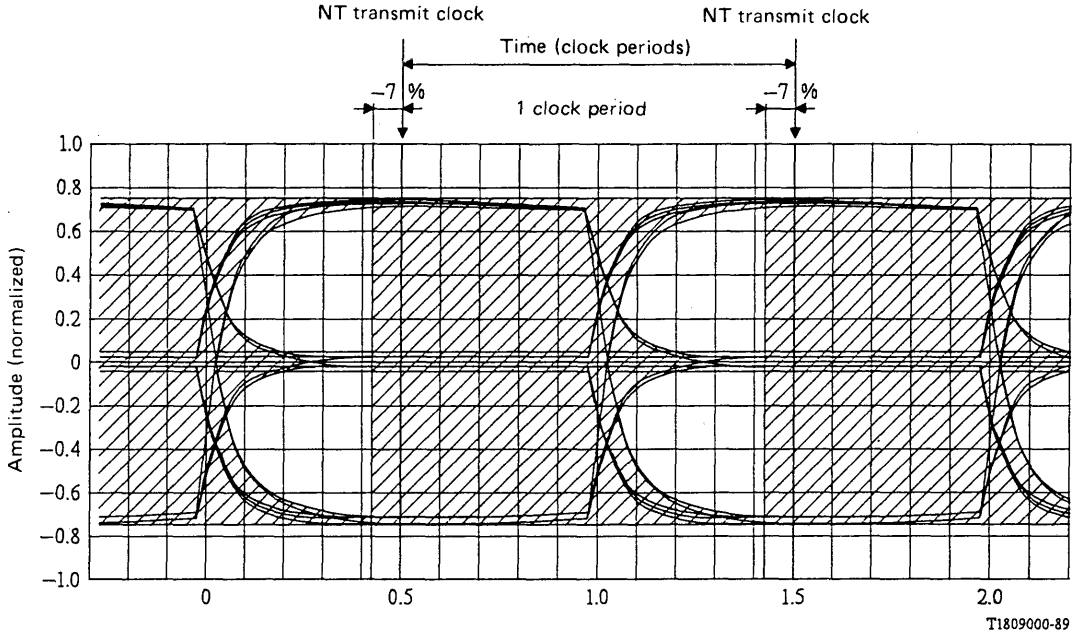


Note 1 – Shaded area is the region in which pulse transitions may occur.

Note 2 – The waveform mask is based on the "worst case" configuration shown in Annex C, Figure C-1/V.230 and waveforms ii) and iii) in § 8.2.1. The shaded area of −7% of one clock period accounts for the situation of a single slave mode equipment connected directly to the master mode equipment with a zero length passive bus. However, the waveform mask does not show the higher possible amplitude of framing and DV-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 16/V.230

Short passive bus receive pulse waveform mask



Note 1 – Shaded area is the region in which pulse transitions may occur.

Note 2 – The waveform mask is based on the same "worst case" passive bus configuration as the waveform mask in Figure 16/V.230 except that the permitted round trip delay of the cable is reduced. The shaded area of −7% of one clock period accounts for the situation of a single slave mode equipment connected directly to the master mode equipment with a zero length passive bus. However, the waveform mask does not show the higher possible amplitude of framing and DV-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 17/V.230

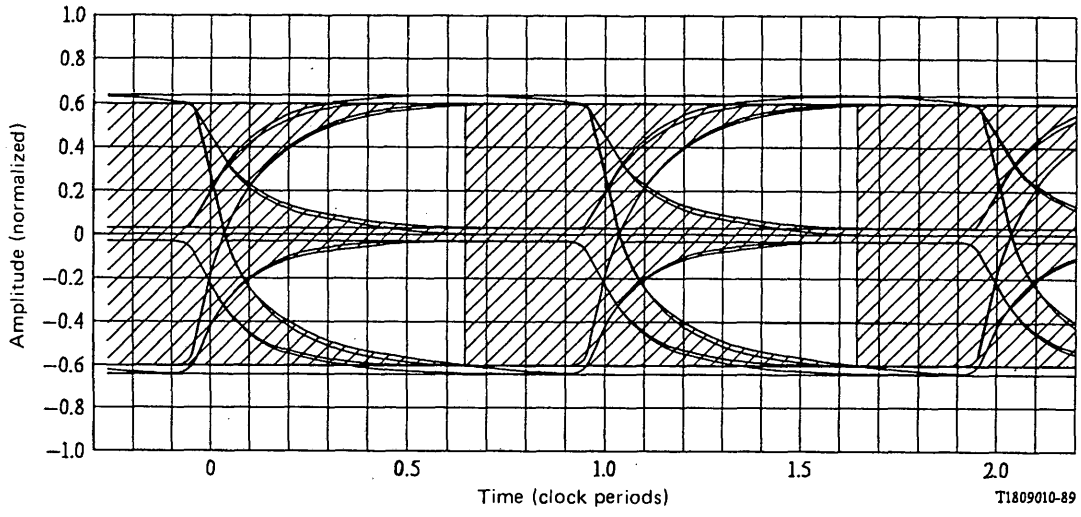
Passive bus receive pulse waveform mask
(Master mode equipment designed to operate with either point-to-point or short passive bus wiring configurations)

8.6.2.4 *Master mode equipment for extended passive bus wiring configurations*

Master mode equipment designed to operate with extended passive bus wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in Figure 18/V.230. These master mode equipments shall operate with the input signals having any amplitude in the range of +1.5 dB to −5.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. Additionally, these master mode equipments shall operate with the sinusoidal signals, as specified in § 8.6.2.1, superimposed on the input signals having the waveform shown in Figure 18/V.230. (The above values assume a maximum cable loss of 3.8 dB. Master mode equipment may be implemented to accommodate higher cable loss.)

8.6.2.5 *Master mode equipment for point-to-point configurations only*

Master mode equipment designed to operate with only point-to-point wiring configurations shall operate when receiving input signals having the waveform shown in Figure 5/V.230. These master mode equipments shall operate with the input signals having any amplitude in the range of +1.5 to −7.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. Additionally, these master mode equipments shall operate with the sinusoidal signals, as specified in § 8.6.2.1, superimposed on the input signals having the waveform shown in Figure 5/V.230.



Note 1 – Shaded area is the region in which pulse transitions may occur.

Note 2 – The waveform mask is based on the worst case extended passive bus wiring configuration. It consists of a cable having a characteristic impedance of 75 ohms, a capacitance of 120 nF/km, a loss of 3.8 dB at 96 kHz, four slave mode equipments connected such that the differential delay is at the maximum permitted by § 8.6.3.3. The waveform mask does not show the higher possible amplitude of framing and DV-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 18/V.230

Extended passive bus receive pulse waveform mask

8.6.3 *Master mode equipment receiver input delay characteristics*

Note – Round trip delay is always measured between the zero-volt crossings of the framing pulse and its associated balance bit pulse at the transmit and receive sides of the master mode equipment (see also Annex A).

8.6.3.1 *Master mode equipment for short passive bus*

Master mode equipment shall accommodate round trip delays of the complete installation, including slave mode equipment, in the range 10 to 14 μs.

8.6.3.2 *Master mode equipment for both point-to-point and passive bus*

Master mode equipment shall accommodate round trip delays (for passive bus configurations) in the range 10 to 13 μs.

Master mode equipment shall accommodate round trip delays (for point-to-point configurations) in the range 10 to 42 μs.

8.6.3.3 *Master mode equipment for extended passive bus*

Master mode equipment shall accommodate round trip delays in the range 10 to 42 μs, provided that the differential delay of signals from different slave mode equipments is in the range 0 to 2 μs.

8.6.3.4 *Master mode equipment for point-to-point only*

Master mode equipment shall accommodate round trip delays specified in § 8.6.3.2 for point-to-point configurations.

8.6.4 *Unbalance about earth*

Longitudinal conversion loss (LCL) of receiver inputs, measured in accordance with Recommendation G.117, § 4.1.3, by considering the power feeding and two 100-ohm terminations at each port, shall meet the following requirements (see Figure 14/V.230):

a) 10 kHz $\leqslant f \leqslant$ 300 kHz: $\geqslant$ 54 dB

b) 300 kHz $< f \leqslant$ 1 MHz: minimum value decreasing from 54 dB with 20 dB/decade.

8.7 *Isolation from external voltages*

The electrical environment of interface cable pairs is not specified in this Recommendation.

IEC Publication 479-1, Second Issue 1984, specifies current limitations dealing with human safety. According to that publication, the value of a touchable leakage alternating current measured through a resistor of 2 kOhms is to be limited to 9 mA. The application of this requirement to the user-network interface is not a subject of this Recommendation.

It may be necessary to apportion this value between the number of mains powered equipments connected to the passive bus. A possible maximum value of (touchable) leakage alternating current for each mains powered equipment could be 1 mA. However, it should be noted that leakage current of a fraction of this magnitude may interfere with the satisfactory operation of the equipments.

8.8 *Interconnecting media characteristics*

Longitudinal conversion loss of pairs at 96 kHz shall be $\geqslant$ 43 dB.

8.9 *Standard GDCI access cord*

A connecting cord designed to connect equipment to a jack on a passive bus cable must meet the requirements specified in Recommendation I.430 for the "standard ISDN basic access TE cord".

9 Power feeding

Power feeding across the General Data Communication Interface is not required by this Recommendation. All equipment should be capable of operating if power is present in accordance with Recommendation I.430, § 9. In the case of a GDCI application which uses power feed across the interface, power source 2 defined in Recommendation I.430 should be the first choice, followed by either power source 1 or power source 3. Any considerations for operation under restricted power conditions are at the discretion of the application.

10 Interface connector and contact assignments

The interface connector and contact assignments are the subject of an ISO standard. Table 7/V.230 is reproduced from the Draft International Standard, DIS 8877, dated November 1985. For the transmit and receive leads, pole numbers 3 through 6, the polarity indicated is for the polarity of the framing pulses. For the power leads, pole numbers 1, 2, 7 and 8, the polarity indicated is for the polarity of the d.c. voltages. See Figure 20/I.430 for the polarity of power provided in the phantom mode. In that figure, the leads that are lettered a, b, c, d, e, f, g and h correspond with pole numbers 1, 2, 3, 6, 5, 4, 7 and 8, respectively.

TABLE 7/V.230

Pole (contact) assignment for 8-pole connections (plugs and jacks)

Pole number	Function		Polarity
	Slave mode equipment	Master mode equipment	
1	Power source 3	Power sink 3	+
2	Power source 3	Power sink 3	–
3	Transmit	Receive	+
4	Receive	Transmit	+
5	Receive	Transmit	–
6	Transmit	Receive	–
7	Power sink 2	Power source 2	–
8	Power sink 2	Power source 2	+

Note – This reference is only provisional.

ANNEX A

(to Recommendation V.230)

Wiring configurations and round trip delay considerations used as a basis for electrical characteristics

A.1 *Introduction*

A.1.1 In § 4 of this Recommendation, two major wiring arrangements are identified. These are point-to-point configuration and a point-to-multipoint configuration using a passive bus.

While these configurations may be considered to be the limiting cases for the definition of the interfaces and the design of the associated equipments, other significant arrangements should be considered.

A.1.2 The values of overall length, in terms of cable loss and delay assumed for each of the possible arrangements, are indicated below.

A.1.3 Figure 2/V.230 is a composite of the individual configurations. These individual configurations are shown in this Annex.

A.2 *Wiring configurations*

A.2.1 *Point-to-multipoint*

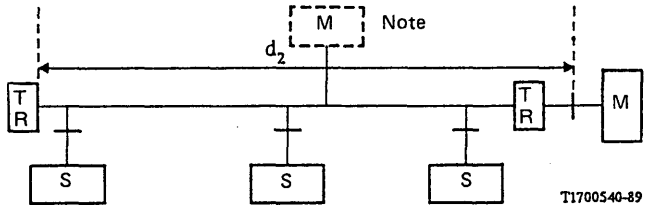
A.2.1.1 The point-to-multipoint wiring configuration identified in § 4.2 of this Recommendation may be provided by the "short passive bus" or other configurations such as "extended passive bus".

A.2.1.2 *Short passive bus* (Figure A-1/V.230)

An essential configuration to be considered is a passive bus in which the slave mode devices may be connected at random points along the full length of the cable. This means that the master mode equipment receiver must cater for pulses arriving with different delays from various terminals. For this reason, the length limit for this configuration is a function of the maximum round trip delay and not of the attenuation.

A master mode equipment receiver with fixed timing can be used if the round trip delay is between 10 to 14 μs. This relates to a maximum operational distance from the master mode equipment in the order of 100-200 m (d_2 in Figure A-1/V.230) [200 m in the case of a high impedance cable (Z_c = 150 ohms) and 100 m in the case of a low impedance cable (Z_c = 75 ohms)]. It should be noted that the slave master equipment connections acts as stubs on the cable, thus reducing the master mode equipment receiver margin over that of a point-to-point configuration. A maximum number of 8 slave mode equipments with connections of 10 m in length are to be accommodated.

The range of 10 to 14 μs for the round trip delay is composed as follows. The lower value of 10 μs is composed of two bits offset delay (see Figure 3/V.230) and the negative phase deviation of −7% (see § 8.2.3). In this case the slave mode equipment is located directly at the master mode equipment. The higher value of 14 μs is calculated assuming the slave mode equipment is located at the far end of a passive bus. This value is composed of the offset delay between frames of two bits (10.4 μs), the round trip delay of the unloaded bus installation (2 μs), the additional delay due to load of the slave mode equipment (i.e., 0.7 μs) and the maximum delay of the slave mode equipment transmitter according to § 8.2.3 (15% = 0.8 μs).



TR Terminating resistor
M Master
S Slave

Note – In principle, the master mode equipment may be located at any point along the passive bus. The electrical characteristics in this Recommendation, however, are based on the master mode equipment located at one end. The conditions related to other locations require confirmation.

FIGURE A-1/V.230

Short passive bus

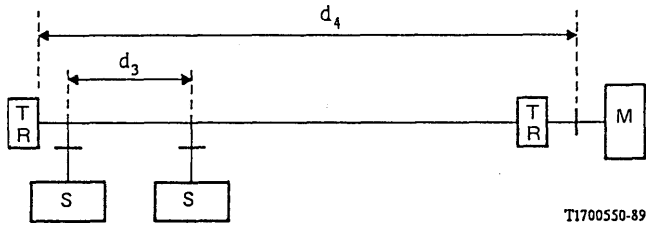
A.2.1.3 *Extended passive bus* (Figure A-2/V.230)

A configuration which may be used at an intermediate distance in the order of 100 m and 1000 m is known as an extended passive bus. This configuration takes advantage of the fact that terminal connection points are restricted to a grouping at the far end of the cable from the master mode equipment. This places a restriction on the differential distance between slave mode equipments. The differential round trip delay is defined as that between zero-volt crossings of signals from different slave mode equipments and is restricted to 2 μs.

This differential round trip delay is composed of a slave mode equipment differential delay of 22% or 1.15 μs according to § 8.2.3, the round trip delay of the unloaded bus installation of 0.5 μs (line length: 25 to 50 m) and an additional delay due to the load of 4 slave mode equipments (0.35 μs).

d_3 depends on the characteristics of the cable to be used.

The objective for this extended passive bus configuration is a total length of at least 500 m (d_4 in Figure A-2/V.230) and a differential distance between slave mode equipment connection points of 25 to 50 m (d_3 in Figure A-2/V.230). However, an appropriate combination of the total length, the differential distance between slave mode equipment connection points, and the number of slave mode equipments connected to the cable, may be determined by individual Administrations.



TR Terminating resistor
M Master
S Slave

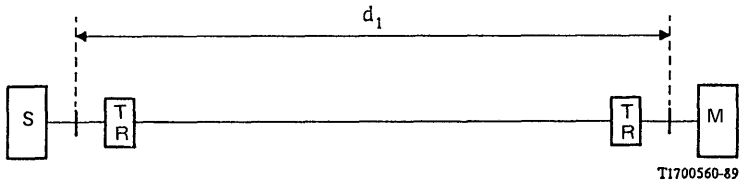
FIGURE A-2/V.230

Extended passive bus

A.2.2 *Point-to-point* (Figure A-3/V.230)

This configuration provides for one transmitter/receiver only at each end of the cable (see Figure A-3/V.230). It is, therefore, necessary to determine the maximum permissible attenuation between the ends of the cable to establish the transmitter output level and the range of receiver input levels. In addition, it is necessary to establish the maximum round trip delay for any signal which must be returned from one end to the other within a specified time period (limited by DV-echo bits).

A general objective for the operational distance between equipment units is 1.0 km (d_1 in Figure A-3/V.230). It is agreed to satisfy this general objective with a maximum cable attenuation of 6 dB at 96 kHz. The round trip delay is between 10 to 42 μs.



TR Terminating resistor
M Master
S Slave

FIGURE A-3/V.320

Point-to-point

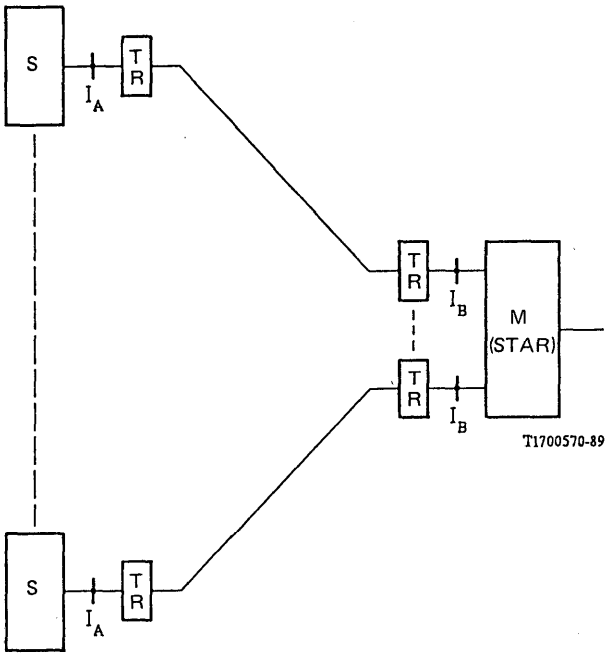
The lower value of 10 μs is derived in the same way as for the passive bus configuration. The upper value is composed of the following elements:

- 2 bits due to frame offset (2 × 5.2 μs = 10.4 μs, see § 5.4.2.3);
- maximum 6 bits delay permitted due to the distance between master and slave devices and the required processing time (6 × 5.2 μs = 31.2 μs);
- the fraction (+15%) of a bit period due to phase deviation between slave mode equipment input and output (see § 8.2.3, 0.15 × 5.2 μs = 0.8 μs).

It should be noted that an adaptive timing device at the receiver is required at the master mode equipment to meet these limits.

For the master mode equipment used for point-to-point and passive bus configurations (see § 8.6.3.2), the tolerable round trip delay in passive bus wiring configurations is reduced to 13 μs due to the extra tolerance required for the adaptive timing. Using this type of wiring configuration, it is also possible to provide point-to-multipoint mode of operation at layer 1.

Note – Point-to-multipoint operation can be accommodated using only point-to-point wiring. One suitable arrangement is STAR illustrated in Figure A-4/V.230. In such an implementation, bit streams from slave mode equipments must be buffered to provide for operation of the DV-echo channel(s) to provide for contention resolution, but only layer 1 functionality is required. It is also possible to support passive bus wiring configurations on the ports of STARs.



TR Terminating resistor
M Master
S Slave

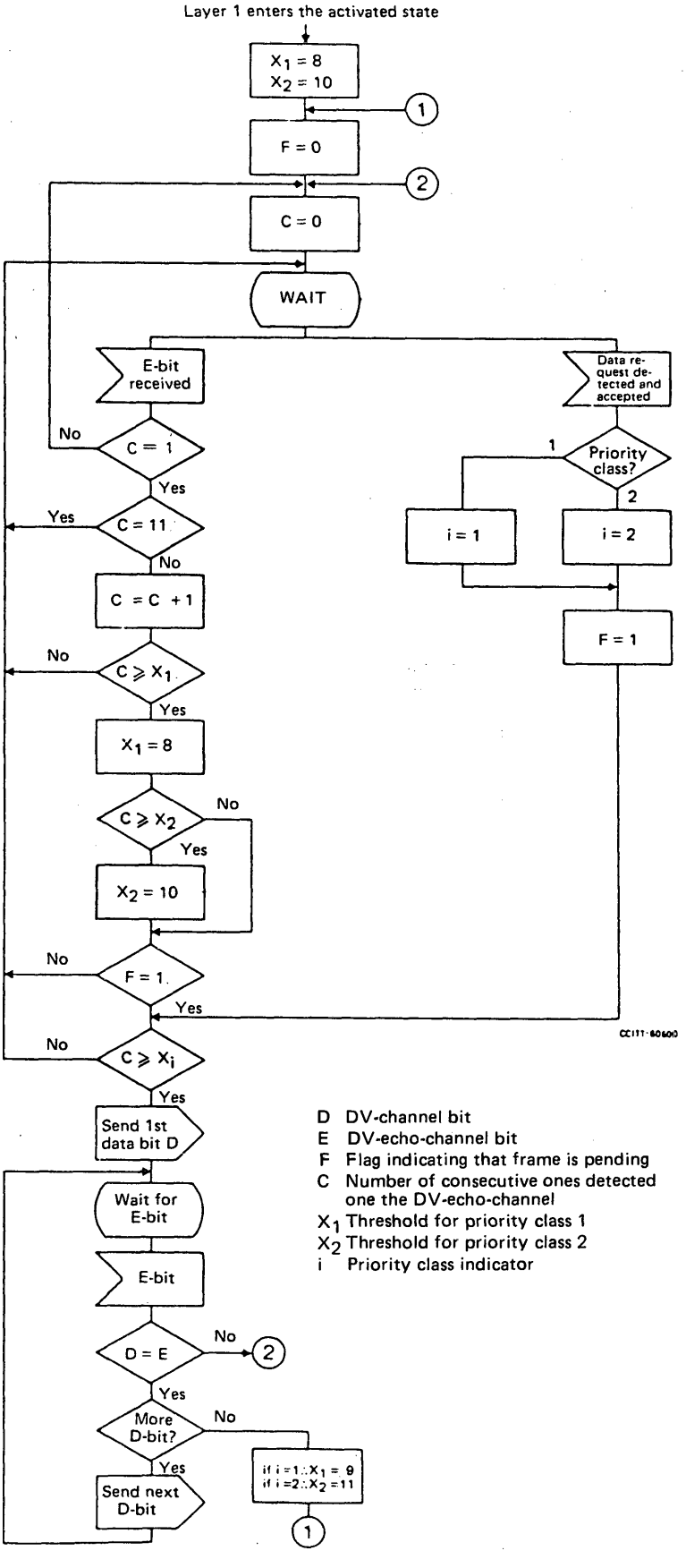
FIGURE A-4/V.230

Star

ANNEX B

(to Recommendation V.230)

SDL representation of a possible implementation of the DV-channel access



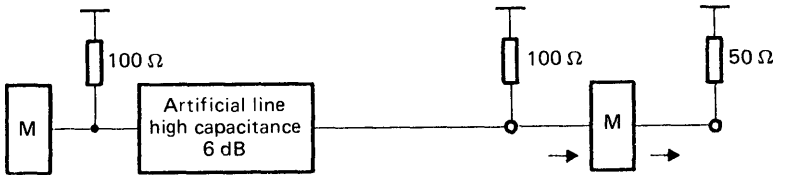
ANNEX C

(to Recommendation V.230)

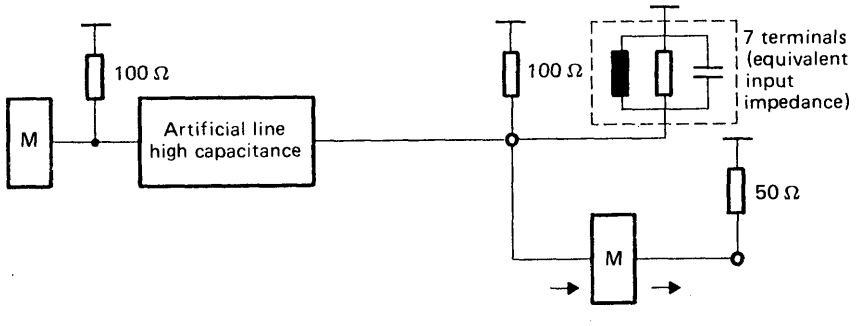
Test configurations

In § 8 of this Recommendation, waveforms are shown for testing master and slave mode equipment. This Annex describes configurations, for testing slave mode equipment, which can be used to generate these waveforms (see Figure C-1/V.230). Similar configurations can be used to test master mode equipment.

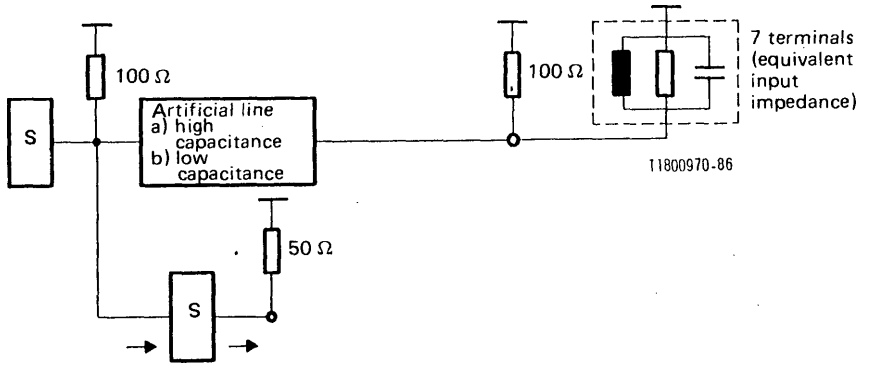
Table C-1/V.230 gives the parameters for the artificial lines reproduced in Figure C-1/V.230. The artificial lines are used to derive the waveforms. For test configurations ii) and iii), the cable length used corresponds to a signal delay of 1 µs.



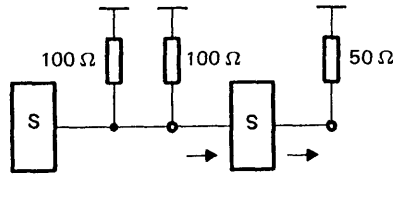
Configuration i) Point-to-point



Configuration ii) Short passive bus



Configuration iiia), iiib) Short passive bus



Configuration iv) Ideal test signal

M. Master
S Slave

FIGURE C-1/V.230

Test configurations

TABLE C-1/V.230

Parameters for the artificial lines

Parameters	High capacitance cable	Low capacitance cable
R (96 kHz)	160 ohms/km	160 ohms/km
C (1 kHz)	120 nF/km	30 nF/km
Zo (96 kHz)	75 ohms	150 ohms
Wire diameter	0.6 mm	0.6 mm

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