INTERNATIONAL TELECOMMUNICATION UNION

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THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

BLUE BOOK

VOLUME III – FASCICLE III.4

GENERAL ASPECTS OF DIGITAL TRANSMISSION SYSTEMS; TERMINAL EQUIPMENTS

RECOMMENDATIONS G.700-G.795

IXTH PLENARY ASSEMBLY
MELBOURNE, 14-25 NOVEMBER 1988

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CONTENTS OF THE CCITT BOOK
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BLUE BOOK

FASCICLE III.6 – Line transmission of non-telephone signals. Transmission of sound-programme and television signals. Series H and J Recommendations (Study Group XV).

FASCICLE III.7 – Integrated Services Digital Network (ISDN) – General structure and service capabilities. Recommendations I.110-I.257 (Study Group XVIII).

FASCICLE III.8 – Integrated Services Digital Network (ISDN) – Overall network aspects and functions, ISDN user-network interfaces. Recommendations I.310-I.470 (Study Group XVIII).

FASCICLE III.9 – Integrated Services Digital Network (ISDN) – Internetwork interfaces and maintenance principles. Recommendations I.500-I.605 (Study Group XVIII).

Volume IV

FASCICLE IV.1 – General maintenance principles: maintenance of international transmission systems and telephone circuits. Recommendations M.10-M.782 (Study Group IV).

FASCICLE IV.2 – Maintenance of international telegraph, phototelegraph and leased circuits. Maintenance of the international public telephone network. Maintenance of maritime satellite and data transmission systems. Recommendations M.800-M.1375 (Study Group IV).

FASCICLE IV.3 – Maintenance of international sound-programme and television transmission circuits. Series N Recommendations (Study Group IV).

FASCICLE IV.4 – Specifications for measuring equipment. Series O Recommendations (Study Group IV).

Volume V – Telephone transmission quality. Series P Recommendations (Study Group XII).

Volume VI

FASCICLE VI.1 – General Recommendations on telephone switching and signalling. Functions and information flows for services in the ISDN. Supplements. Recommendations Q.1-Q.118 *bis* (Study Group XI).

FASCICLE VI.2 – Specifications of Signalling Systems Nos. 4 and 5. Recommendations Q.120-Q.180 (Study Group XI).

FASCICLE VI.3 – Specifications of Signalling System No. 6. Recommendations Q.251-Q.300 (Study Group XI).

FASCICLE VI.4 – Specifications of Signalling Systems R1 and R2. Recommendations Q.310-Q.490 (Study Group XI).

FASCICLE VI.5 – Digital local, transit, combined and international exchanges in integrated digital networks and mixed analogue-digital networks. Supplements. Recommendations Q.500-Q.554 (Study Group XI).

FASCICLE VI.6 – Interworking of signalling systems. Recommendations Q.601-Q.699 (Study Group XI).

FASCICLE VI.7 – Specifications of Signalling System No. 7. Recommendations Q.700-Q.716 (Study Group XI).

FASCICLE VI.8 – Specifications of Signalling System No. 7. Recommendations Q.721-Q.766 (Study Group XI).

FASCICLE VI.9 – Specifications of Signalling System No. 7. Recommendations Q.771-Q.795 (Study Group XI).

FASCICLE VI.10 – Digital subscriber signalling system No. 1 (DSS 1), data link layer. Recommendations Q.920-Q.921 (Study Group XI).

FASCICLE VI.11 – Digital subscriber signalling system No. 1 (DSS 1), network layer, user-network management. Recommendations Q.930-Q.940 (Study Group XI).

FASCICLE VI.12 – Public land mobile network. Interworking with ISDN and PSTN. Recommendations Q.1000-Q.1032 (Study Group XI).

FASCICLE VI.13 – Public land mobile network. Mobile application part and interfaces. Recommendations Q.1051-Q.1063 (Study Group XI).

FASCICLE VI.14 – Interworking with satellite mobile systems. Recommendations Q.1100-Q.1152 (Study Group XI).

Volume VII

FASCICLE VII.1 – Telegraph transmission. Series R Recommendations. Telegraph services terminal equipment. Series S Recommendations (Study Group IX).

FASCICLE VII.2 – Telegraph switching. Series U Recommendations (Study Group IX).

FASCICLE VII.3 – Terminal equipment and protocols for telematic services. Recommendations T.0-T.63 (Study Group VIII).

FASCICLE VII.4 – Conformance testing procedures for the Teletex Recommendations. Recommendation T.64 (Study Group VIII).

FASCICLE VII.5 – Terminal equipment and protocols for telematic services. Recommendations T.65-T.101, T.150-T.390 (Study Group VIII).

FASCICLE VII.6 – Terminal equipment and protocols for telematic services. Recommendations T.400-T.418 (Study Group VIII).

FASCICLE VII.7 – Terminal equipment and protocols for telematic services. Recommendations T.431-T.564 (Study Group VIII).

Volume VIII

FASCICLE VIII.1 – Data communication over the telephone network. Series V Recommendations (Study Group XVII).

FASCICLE VIII.2 – Data communication networks: services and facilities, interfaces. Recommendations X.1-X.32 (Study Group VII).

FASCICLE VIII.3 – Data communication networks: transmission, signalling and switching, network aspects, maintenance and administrative arrangements. Recommendations X.40-X.181 (Study Group VII).

FASCICLE VIII.4 – Data communication networks: Open Systems Interconnection (OSI) – Model and notation, service definition. Recommendations X.200-X.219 (Study Group VII).

FASCICLE VIII.5 – Data communication networks: Open Systems Interconnection (OSI) – Protocol specifications, conformance testing. Recommendations X.220-X.290 (Study Group VII).

FASCICLE VIII.6 – Data communication networks: interworking between networks, mobile data transmission systems, internetwork management. Recommendations X.300-X.370 (Study Group VII).

FASCICLE VIII.7 – Data communication networks: message handling systems. Recommendations X.400-X.420 (Study Group VII).

FASCICLE VIII.8 – Data communication networks: directory. Recommendations X.500-X.521 (Study Group VII).

Volume IX – Protection against interference. Series K Recommendations (Study Group V). Construction, installation and protection of cable and other elements of outside plant. Series L Recommendations (Study Group VI).

Volume X

FASCICLE X.1	–	Functional Specification and Description Language (SDL). Criteria for using Formal Description Techniques (FDTs). Recommendation Z.100 and Annexes A, B, C and E, Recommendation Z.110 (Study Group X).
FASCICLE X.2	–	Annex D to Recommendation Z.100: SDL user guidelines (Study Group X).
FASCICLE X.3	–	Annex F.1 to Recommendation Z.100: SDL formal definition. Introduction (Study Group X).
FASCICLE X.4	–	Annex F.2 to Recommendation Z.100: SDL formal definition. Static semantics (Study Group X).
FASCICLE X.5	–	Annex F.3 to Recommendation Z.100: SDL formal definition. Dynamic semantics (Study Group X).
FASCICLE X.6	–	CCITT High Level Language (CHILL). Recommendation Z.200 (Study Group X).
FASCICLE X.7	–	Man-Machine Language (MML). Recommendations Z.301-Z.341 (Study Group X).

CONTENTS OF FASCICLE III.4 OF THE BLUE BOOK

Recommendations G.700 to G.795

General aspects of digital transmission systems; terminal equipments

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PRELIMINARY NOTES

In this fascicle, the expression "Administration" is used for shortness to indicate both a telecommunication Administration and a recognized private operating agency.

FASCICLE III.4

Recommendations G.700 to G.795

GENERAL ASPECTS OF DIGITAL TRANSMISSION SYSTEMS; TERMINAL EQUIPMENTS

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SECTION 7

GENERAL ASPECTS OF DIGITAL TRANSMISSION SYSTEMS; TERMINAL EQUIPMENTS

7.0 General

Recommendation G.700

FRAMEWORK OF THE SERIES G.700, G.800 AND G.900 RECOMMENDATIONS

(former Recommendation G.701 of Volume III of the Yellow Book)

SECTION 7 – *General aspects of digital transmission systems; terminal equipments*

7.0	**General**
G.700	Framework of the series G.700, G.800 and G.900 Recommendations
G.701	Vocabulary of digital transmission and multiplexing, and pulse code modulation (PCM) terms
G.702	Digital hierarchy bit rates
G.703	Physical/electrical characteristics of hierarchical digital interfaces
G.704	Functional characteristics of interfaces associated with network nodes
G.705	Characteristics required to terminate digital links on a digital exchange
G.706	Frame alignement and cyclic redundancy check (CRC) procedures relating to basic frame structures defined in Recommendation G.704
G.707	Synchronous digital hierarcy bit rates
G.708	Network node interface for the synchronous digital hierarchy
G.709	Synchronous multiplexing structure
7.1	**Coding of analogue signals by pulse code modulation**
G.711	Pulse code modulation (PCM) of voice frequencies
G.712	Performance characteristics of PCM channels between 4-wire interfaces at voice frequencies
G.713	Performance characteristics of PCM channels between 2-wire interfaces at voice frequencies

G.714 Separate performance characteristics for the encoding and decoding sides of PCM channels applicable to 4-wire voice-frequency interfaces

G.715 Separate performance characteristics for the encoding and decoding side of PCM channels applicable to 2-wire interfaces

7.2 Coding of analogue signals by methods other than PCM

G.721 32 kbit/s adaptive differential pulse code modulation (ADPCM)

G.722 7 kHz audio-coding within 64 kbit/s

G.723 Extensions of Recommendation G.721 ADPCM to 24 and 40 kbit/s for DCME application

G.724 Characteristics of a 48-channel low bit rate encoding primary multiplex operating at 1544 kbit/s

G.725 System aspects for the use of the 7 kHz audio codec within 64 kbit/s

7.3 Principal characteristics of primary multiplex equipment

G.731 Primary PCM multiplex equipment for voice frequencies

G.732 Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s

G.733 Characteristics of primary PCM multiplex equipment operating at 1544 kbit/s

G.734 Characteristics of synchronous digital multiplex equipment operating at 1544 kbit/s

G.735 Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s and offering synchronous digital access at 384 kbit/s and/or 64 kbit/s

G.736 Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s

G.737 Characteristics of an external access equipment operating at 2048 kbit/s offering synchronous digital access at 384 kbit/s and/or 64 kbit/s

G.738 Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s and offering synchronous digital access at 320 kbit/s and/or 64 kbit/s

G.739 Characteristics of an external access equipment operating at 2048 kbit/s offering synchronous digital access at 320 kbit/s and/or 64 kbit/s

7.4 Principal characteristics of second order multiplex equipments

G.741 General considerations on second order multiplex equipments

G.742 Second order digital multiplex equipment operating at 8448 kbit/s and using positive justification

G.743 Second order digital multiplex equipment operating at 6312 kbit/s and using positive justification

G.744 Second order PCM multiplex equipment operating at 8448 kbit/s

G.745 Second order digital multiplex equipment operating at 8448 kbit/s and using positive/zero/negative justification

G.746 Characteristics of second order PCM multiplex equipment operating at 6312 kbit/s

G.747 Second order digital multiplex equipment operating at 6312 kbit/s and multiplexing three tributaries at 2048 kbit/s

7.5 Principal characteristics of higher order multiplex equipments

G.751 Digital multiplex equipments operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification

G.752 Characteristics of digital multiplex equipments based on a second order bit rate of 6312 kbit/s and using positive justification

G.753 Third order digital multiplex equipment operating at 34 368 kbit/s and using positive/zero/negative justification

G.754 Fourth order digital multiplex equipment operating at 139 264 kbit/s and using positive/zero/negative justification

G.755 Digital multiplex equipment operating at 139 264 kbit/s and multiplexing three tributaries at 44736 kbit/s

7.6 Principal characteristics of transcoder and digital circuit multiplication equipments

G.761 General characteristics of a 60-channel transcoder equipment

G.762 General characteristics of a 48-channel transcoder equipment

G.763 Digital circuit multiplication equipment using 32 kbit/s ADPCM and digital speech interpolation

7.7 Operations administration and maintenance features of transmission equipments

G.771 Q-interfaces and associated protocols for transmission equipment in the telecommunications management network (TMN)

G.772 Digital protocol monitoring points

7.9 Other terminal equipments

G.791 General considerations on transmultiplexing equipments

G.792 Characteristics common to all transmultiplexing equipments

G.793 Characteristics of 60-channel transmultiplexing equipments

G.794 Characteristics of 24-channel transmultiplexing equipments

G.795 Characteristics of codecs for FDM assemblies

SECTION 8 – *Digital networks*

8.0 General aspects of digital networks

G.801 Digital transmission models

G.802 Interconnection between networks based on different digital hierarchies and speech encoding laws

8.1 Design objectives for digital networks

G.810 Considerations on timing and synchronization issues

G.811 Timing requirements at the outputs of primary reference clocks suitable for plesiochronous operation of international digital links

G.812 Timing requirements at the outputs of slave clocks suitable for plesiochronous operation of international digital links

VOCABULARY OF DIGITAL TRANSMISSION AND MULTIPLEXING, AND PULSE CODE MODULATION (PCM) TERMS

1 Introduction

This Recommendation provides a vocabulary of terms and definitions that are appropriate to digital and pulse code modulation multiplexing and transmission systems.

A small number of the terms in the Recommendation are duplicated in Recommendation I.112. References to these definitions are given in parenthesis as an aid to ensuring consistency between the two Recommendations in the event of future amendments.

According to the conventions applied in this Recommendation any term in common usage, but whose use is deprecated in the sense defined, is shown after the recommended term as in the following example: "2026 controlled slip [slip]".

Where a truncated term is widely used in an understood context the complete term is quoted following the colloquial form, for example: "1007 circuit, telecommunication circuit".

Furthermore, any term which is in general use in addition to the principal term is shown after the principal term as in the following example: "6002 timing recovery (timing extraction)".

In the interest of standardization in the drafting of documents the following abbreviations are recommended:

kbit/s,

Mbit/s,

Gbit/s.

To avoid misinterpretation of the use of the point (.) and the comma (,) in different languages to separate the whole and decimal parts, it is recommended that the use of decimals should be avoided wherever possible. For example, "2048 kbit/s" is preferred to "2.048 Mbit/s" or "2,048 Mbit/s.

Annex A to this Recommendation contains an alphabetical list of all of the terms defined in this Recommendation.

2 Vocabulary of digital transmission and multiplexing and pulse code modulation terms (PCM)

CONTENTS

2.1 *General*

1001 **signal** [102]

F: signal

S: señal

A physical phenomenon one or more of whose characteristics may vary to represent information.

1002 **analogue signal** [103]

F: signal analogique

S: señal analógica

A signal one of whose characteristic quantities follows continuously the variations of another physical quantity representing information.

1003 **discretely-timed signal** [104]

F: signal (temporel) discret

S: señal discretamente temporizada

A signal composed of successive elements in time, each element having one or more characteristics which can convey information, for example, its duration, its waveform and its amplitude.

1004 **transmission** [106]

F: transmission

S: transmisión

The action of conveying signals from one point to one or more other points.

Note 1 – Transmission can be effected directly or indirectly, with or without intermediate storage.

Note 2 – The use of the English word "transmission" in the sense of "emission" is deprecated.

1005 **channel, transmission channel** [108]

F: voie, voie de transmission

S: canal, canal de transmisión

A means of unidirectional transmission of signals between two points.

Note 1 – Several channels may share a common path; for example each channel may be allocated a particular frequency band or a particular time slot.

Note 2 – The term may be qualified by the nature of the transmitted signals, by the bandwidth, by the digit rate, or by an arbitrary designation.

Note 3 – See also Recommendation I.112, Term 414, access channel.

1006 **telecommunication** [110]

F: télécommunication

S: telecomunicación

Any transmission and/or emission and reception of signals representing signs, writing, images and sounds or intelligence of any nature by wire, radio, optical or other electromagnetic systems.

1007 **circuit, telecommunication circuit** [111]

F: circuit, circuit de télécommunications

S: circuito, circuito de telecomunicación

A combination of two transmission channels permitting bidirectional transmission of signals between two points, to support a single communication.

Note 1 – If the telecommunication is by nature unidirectional (for example: long distance television transmission), the term "circuit" is sometimes used to designate the single channel providing the facility.

Note 2 – In a telecommunication network, the use of the term "circuit" is generally limited to a telecommunication circuit directly connecting two switching devices or exchanges, together with associated terminating equipment.

Note 3 – A telecommunication circuit may permit transmission in both directions simultaneously (duplex), or not simultaneously (simplex).

Note 4 – A telecommunication circuit that is used for transmission in one direction only is sometimes referred to as a unidirectional telecommunication circuit. A telecommunication circuit that is used for transmission in both directions (whether simultaneously or not) is sometimes referred to as a bidirectional telecommunication circuit.

1008 **interface** [408]

F: jonction (interface)

S: interfaz

The common boundary between two associated systems.

2.2 *Digital signals*

2001 **digit**

F: élément numérique

S: dígito

A member selected from a finite set.

Note 1 – In digital transmission, a digit may be represented by a signal element, being characterized by the dynamic nature, discrete condition and discrete timing of the element, for example it may be represented as a pulse of specified amplitude and duration.

Note 2 – In equipment used in digital transmission, a digit may be represented by a stored condition being characterized by a specified physical condition, for example it may be represented as a binary magnetic condition of a ferrite core.

Note 3 – The context of the use of the term should be such as to indicate the radix of notation. (The meaning of "digit" in Notes 1, 2 and 3 translates into French as "élément numérique".)

Note 4 – In telephone subscriber numbering, a digit is any of the numbers 1, 2, 3 . . . 9 or 0 forming the elements of a telephone number (Recommendation Q.10 [1]). (This meaning of "digit" translates into French as "chiffre".)

2002 **binary figure**

F: chiffre binaire

S: cifra binaria

One of the two figures (that is, 0 or 1) used in the representation of numbers in binary notation.

2003 **binary digit** (bit)

F: élément binaire

S: dígito binario (bit)

A member selected from a binary set.

Note 1 – Bit is an abbreviation for binary digit.

Note 2 – In the interest of clarity, it is recommended that the term "bit" should not be used in two-condition start-stop modulation instead of "unit element".

2004 **octet**

F: octet

S: octeto

A group of eight binary digits or eight signal elements representing binary digits operated upon as an entity.

2005 **code word [character signal]**

F: mot de code [signal de caractère]

S: palabra de código [señal de carácter]

A set of signal elements representing the quantized value of a sample in PCM.

Note – In PCM, the term "PCM word" may be used in this sense.

2006 **digital signal** [105]

F: signal numérique

S: señal digital

A discretely timed signal in which information is represented by a number of well-defined discrete values that one of its characteristic quantities may take in time.

Note – The term may be qualified to indicate the digit rate, for example: "140 Mbit/s digital signal".

2007 **signal element**

F: élément de signal

S: elemento de señal

A part of a digital signal, characterized by its discrete timing and its discrete value, and used to represent a digit.

2008 **digit position**

F: position d'un élément de signal; position d'un élément numérique

S: posición de dígito

The position in time or space into which a representation of a digit may be placed.

2009 **n-ary digital signal**

F: signal numérique n-aire

S: señal digital n-aria

A digital signal in which each signal element has one of n permitted discrete values.

2010 **redundant digital signal**

F: signal numérique redondant

S: señal digital redundante

The signal that is produced by encoding a given signal in accordance with a redundant line code.

2011 **redundant n-ary signal**

F: signal n-aire redondant

S: señal n-aria redundante

A digital signal whose elements can assume n discrete states where the average equivalent binary content per signal element is less than $\log_2 n$.

Note – The relative redundancy R, of an n-ary digital signal, is given by:

$$R = 1 - \frac{r_e}{r_d \cdot \log_2 n} = \left[1 - \frac{r_e}{r_d \cdot \log_2 n}\right] \cdot 100\%$$

where r_d is the symbol rate of the n-ary signal and r_e is the equivalent bit rate.

This may also be expressed in terms of the number of binary digits which can be transmitted by an element of a particular line code. Examples are:

AMI (37% redundant), 1 binary digit per element;
4B3T (16% redundant), 1.33 binary digit per element.

2012 **pseudo n-ary signal**

F: signal pseudo n-aire

S: señal seudo n-aria

A redundant *n*-ary digital signal that is derived from a *m*-ary digital signal without change of the line digit rate.

Note – An alternate mark inversion signal is an example of a pseudo-ternary signal, i.e. $n = 3$, $m = 2$.

2013 **digit rate**

F: débit numérique

S: velocidad digital

The number of digits per unit time.

Note 1 – An appropriate adjective may precede the word "digit", for example, binary digit rate.

Note 2 – In the interests of clarity it is recommended that this term should not be used to express the symbol rate on the line.

2014 **line digit rate [symbol rate]**

F: débit numérique en ligne [débit de symboles]

S: velocidad digital de linea [velocidad de símbolos]

The number of signal elements of the line signal transmitted per unit time.

Note 1 – The baud is usually used to quantify this, one baud being equal to one single element per second.

Note 2 – Modulation rate is the term used in telegraphy and data communication; it is the reciprocal of the duration of the unit interval.

2015 **equivalent binary content**

F: contenu binaire équivalent

S: contenido binario equivalente

The number of binary digits strictly necessary to convey the same information as a defined number of signal elements in a given digital signal.

2016 **equivalent bit rate**

F: débit binaire équivalent

S: velocidad binaria equivalente

The value of the bit rate strictly necessary to convey the same information in the same time as a given digital signal at a given digit rate.

2017 **significant instant, significant instant of a digital signal**

F: instant significatif, instant significatif d'un signal numérique

S: instante significativo, instante significativo de una señal digital

The instant at which a signal element commences in a discretely-timed signal.

2018 **unit interval**

F: intervalle unitaire

S: intervalo unitario (o intervalo unidad)

The nominal difference in time between consecutive significant instants of an isochronous signal.

2019 **decision instant, decision instant of a digital signal**

F: instant de décision, instant de décision d'un signal numérique

S: instante de decisión instante de decisión de una señal digital

The instant at which a decision is taken as to the probable value of signal element of a received digital signal.

2020 **decision circuit**

F: circuit de décision

S: circuito de decisión

A circuit that decides the probable value of a signal element of a received digital signal.

2021 **regeneration**

F: régénération

S: regeneración

The process of receiving and reconstructing a digital signal so that the amplitudes, waveforms and timing of its signal elements are constrained within specified limits.

2022 **regenerator**

F: régénérateur

S: regenerador

A device that performs regeneration.

2023 **regenerative repeater**

F: répéteur régénérateur

S: repetidor regenerativo

A repeater that regenerates digital signals.

Note 1 – A regenerative repeater may operate in one or both directions of transmission, and the term may be qualified by "unidirectional" or "bidirectional" as appropriate.

Note 2 – Repeater is defined in Recommendation G.601.

2024 **jitter**

F: gigue

S: fluctuación de fase

Short-term non-cumulative variations of the significant instants of a digital signal from their ideal positions in time.

2025 **wander**

F: dérapage

S: fluctuación lenta de fase

Long term non-cumulative variations of the significant instants of a digital signal from their ideal positions in time.

2026 **controlled slip [slip]**

F: glissement commandé [saut]

S: deslizamiento controlado [deslizamiento]

The irretrievable loss or gain of a set of consecutive digit positions in a digital signal, in which both the magnitude and instant of that loss or gain are controlled, to enable the signal to accord with a rate different from its own.

Note – Where appropriate the term may be qualified, for example: controlled octet slip, controlled frame slip.

2027 **uncontrolled slip**

F: glissement non commandé

S: deslizamiento incontrolado

The loss or gain of a digit position or a set of consecutive digit positions in a digital signal resulting from an aberration of the timing processes associated with transmission or switching of a digital signal, and in which either the magnitude or the instant of that loss or gain is not controlled.

2028 **scrambler**

F: embrouilleur

S: aleatorizador

A device that converts a digital signal into a pseudo-random digital signal having the same meaning and the same digit rate.

2029 **descrambler**

F: désembrouilleur

S: desaleatorizador

A device that performs the complementary operation to that of a scrambler.

2030 **error, digital error**

F: erreur, erreur numérique

S: error, error digital

An inconsistency between a digit in a transmitted digital signal and the corresponding digit in the received digital signal.

2031 **error ratio [error rate]**

F: taux d'erreur [rapport d'erreur]

S: tasa de errores [proporción de errores]

The ratio of the number of digital errors received in a specified period to the total number of digits received in the same period.

Note 1 – Numerical values of error ratio should be expressed in the form

$$n \cdot 10^{-p}$$

where p is a positive integer.

Note 2 – Error ratio may be qualified, for example by the term "bit" or "block".

2032 **error multiplication**

F: multiplication d'erreurs

S: multiplicación de errores

The property of an apparatus whereby a single digital error in the input signal presented to it results in more than one digital error in the output signal.

Note – Line code converters and descramblers are examples of apparatus that may cause error multiplication.

2033 **error multiplication factor**

F: facteur de multiplication d'erreurs

S: factor de multiplicación de errores

The ratio of the number of digital errors in the output signal to the number of digital errors in the input signal.

Note – The error multiplication factor may be expressed as either an average or maximum value.

2034 **error spread**

F: étalement d'erreurs [répartition des erreurs]

S: dispersión de errores

The number of consecutive digits of the output signal over which digital errors are distributed when a single digital error in the input signal causes error multiplication.

2.3 *Digital transmission*

3001 **digital transmission** [107]

F: transmission numérique

S: transmisión digital

The transmission of digital signals by means of a channel or channels that may assume in time any one of a defined set of discrete states.

3002 **digital channel, digital transmission channel** [109]

F: voie numérique, voie de transmission numérique

S: canal digital, canal de transmisión digital

The means of unidirectional digital transmission of digital signals between two points.

3003 **digital circuit, digital telecommunication circuit** [112]

F: circuit numérique, circuit numérique de télécommunications

S: circuitó digital, circuito de telecomunicación digital

A combination of two digital transmission channels permitting bidirectional digital transmission in both directions between two points, to support a single communication.

Note 1 – If the telecommunication is by nature unidirectional (for example, long-distance television transmission), the term "digital circuit" is sometimes used to designate the single digital channel providing the facility.

Note 2 – In a telecommunication network, use of the term "digital circuit" is generally limited to a digital telecommunication circuit directly connecting two switching devices or exchanges, together with associated terminating equipment.

Note 3 – A digital telecommunication circuit may permit transmission in both directions simultaneously (duplex), or not simultaneously (simplex).

Note 4 – A digital telecommunication circuit that is used for transmission in one direction only is sometimes referred to as a unidirectional digital telecommunication circuit. A digital telecommunication circuit that is used for transmission in both directions (whether simultaneously or not) is sometimes referred to as a bidirectional digital telecommunication circuit.

3004 **digital connection** [310]

F: connexion numérique

S: conexión digital

A concatenation of digital transmission channels or digital telecommunication circuits, switching and other functional units set up to provide for the transfer of digital signals between two or more points in a telecommunication network, to support a single communication.

3005 **digital link, digital transmission link [digital path]** [302]

F: liaison numérique, liaison de transmission numérique [conduit numérique]

S: enlace digital, enlace de transmisión digital [trayecto digital]

The whole of the means of digital transmission of a digital signal of specified rate between two digital distribution frames (or equivalent).

Note 1 – A digital link comprises one or more digital sections and may include multiplexing and/or demultiplexing, but not switching.

Note 2 – The term may be qualified to indicate the transmission medium used, for example, "digital satellite link".

Note 3 – The term always applies to the combination of "go" and "return" directions of transmission, unless stated otherwise.

Note 4 – The term "digital path" is sometimes used to describe one or more digital links connected in tandem, especially between equipments at which the signals of the specified rate originate and terminate.

3006 **digital distribution frame**

F: répartiteur numérique

S: repartidor digital

A structure that provides flexibility of semipermanent interconnection of digital channels or digital circuits.

Note – Digital sections and digital links normally terminate at digital distribution frames.

3007 **digital section** [1)]

F: section numérique

S: sección digital

The whole of the means of digital transmission of a digital signal of specified rate between two consecutive digital distribution frames or equivalent.

Note 1 – A digital section forms either a part or the whole of a digital link, and includes terminating equipments at both ends, but excludes multiplexers.

Note 2 – Where appropriate, the digital rate or multiplex order should qualify the title.

Note 3 – The definition applies to the combination of "go" and "return" directions of transmission, unless stated otherwise.

3008 **section termination**

F: extrémité de section

S: extremo de sección

A connectional interface selected to be the boundary between a physical transmission medium and its associated equipment.

Note – This point will usually be the connectors at the input and output of an equipment.

3009 **elementary cable section [repeater section]**

F: section élémentaire de câble [section (élémentaire) d'amplification]

S: sección elemental de cable [sección con amplificación]

The whole of the physical transmission medium between the section termination at the output of one equipment and the section termination at the input of the following equipment.

Note 1 – An elementary cable section usually consists of several factory lengths of cable connected together and any associated accessories (such as flexible cables) necessary to connect it to the section terminals.

Note 2 – Examples of the physical transmission media are a coaxial or symmetric pair, and optical fibre.

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1) Figure 1/G.701 gives examples of digital sections, digital links, digital line sections, etc.

3010 **elementary repeater section**

F: section élémentaire amplifiée

S: sección elemental de repetición

In a given direction of transmission, an elementary cable section together with the immediately following analogue repeater.

3011 **elementary regenerator section [regenerator section]**

F: section élémentaire régénérée [section de régénération]

S: sección elemental de regeneración [sección de regeneración]

In a given direction of transmission, an elementary cable section together with the immediately following regenerative repeater.

3012 **digital line section**[2)]

F: section de ligne numérique

S: sección de línea digital

A digital section implemented on a single type of manufactured transmission medium, such as symmetric pair, coaxial pair, or optical fibre.

Note – A digital line section includes line terminating equipments at both ends, and regenerative repeaters if needed, but excludes multiplexers.

3013 **digital line link [digital line path]**[2)]

F: liaison de ligne numérique [conduit de ligne numérique]

S: enlace de línea digital [trayecto de línea digital]

A digital link that comprises a digital line section or a number of tandem-connected digital line sections.

3014 **digital transmission system**

F: système de transmission numérique

S: sistema de transmisión digital

A specific means of providing a digital section.

3015 **digital line system**

F: système de ligne numérique

S: sistema de línea digital

A digital transmission system that provides a digital line section.

3016 **digital radio section**[2)]

F: section radioélectrique numérique

S: sección radiodigital

A digital section implemented on a radio-relay system.

3017 **digital radio link [digital radio path]**[2)]

F: liaison radioélectrique numérique [conduit radioélectrique numérique]

S: enlace radiodigital, [trayecto radiodigital]

A digital link that comprises a digital radio section or a number of tandem-connected digital radio sections.

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2) Figure 1/G.701 gives examples of digital sections, digital links, digital line sections, etc.

3018 **digital radio system**

F: système radioélectrique numérique

S: sistema radiodigital

A digital transmission system that provides a digital radio section.

3019 **bit sequence independence**

F: indépendance de la séquence des bits

S: independencia de la secuencia de bits

The property of a binary transmission channel, telecommunication circuit or connection, that permits all sequences of binary signal elements to be conveyed over it at its specified bit rate, without change to the value of any signal elements.

Note – Practical transmission systems that are not completely bit sequence independent may be described as quasi bit sequence independent. In such cases the limitations should be clearly stated.

3020 **digit sequence integrity**

F: intégrité de la suite des éléments numériques

S: integridad de la secuencia de dígitos

The property of a digital transmission channel, telecommunication circuit or connection, that permits a digital signal to be conveyed over it without change to the order of any signal elements.

3021 **octet sequence integrity**

F: intégrité de la suite des octets

S: integridad de la secuencia de octetos

The property of a digital transmission channel, telecommunication circuit or connection that permits a digital signal to be conveyed over it without change to the order of any octets.

3022 **transparency, digital transparency**

F: transparence, transparence numérique

S: transparencia, transparencia digital

The property of a digital transmission channel, telecommunication circuit or connection, that permits any digital signal to be conveyed over it without change to the value or order of any signal elements.

Note – The digital transmission channel, telecommunication circuit or connection concerned may introduce delay, and may contain reversible code conversion functions.

3023 **alarm indication signal (AIS)**

F: signal d'indication d'alarme (SIA)

S: señal de indicación de alarma (SIA)

A signal that replaces the normal traffic signal when a maintenance alarm indication has been activated.

3024 **upstream failure indication**

F: indication de défaillance en amont

S: indicación de fallo atrás

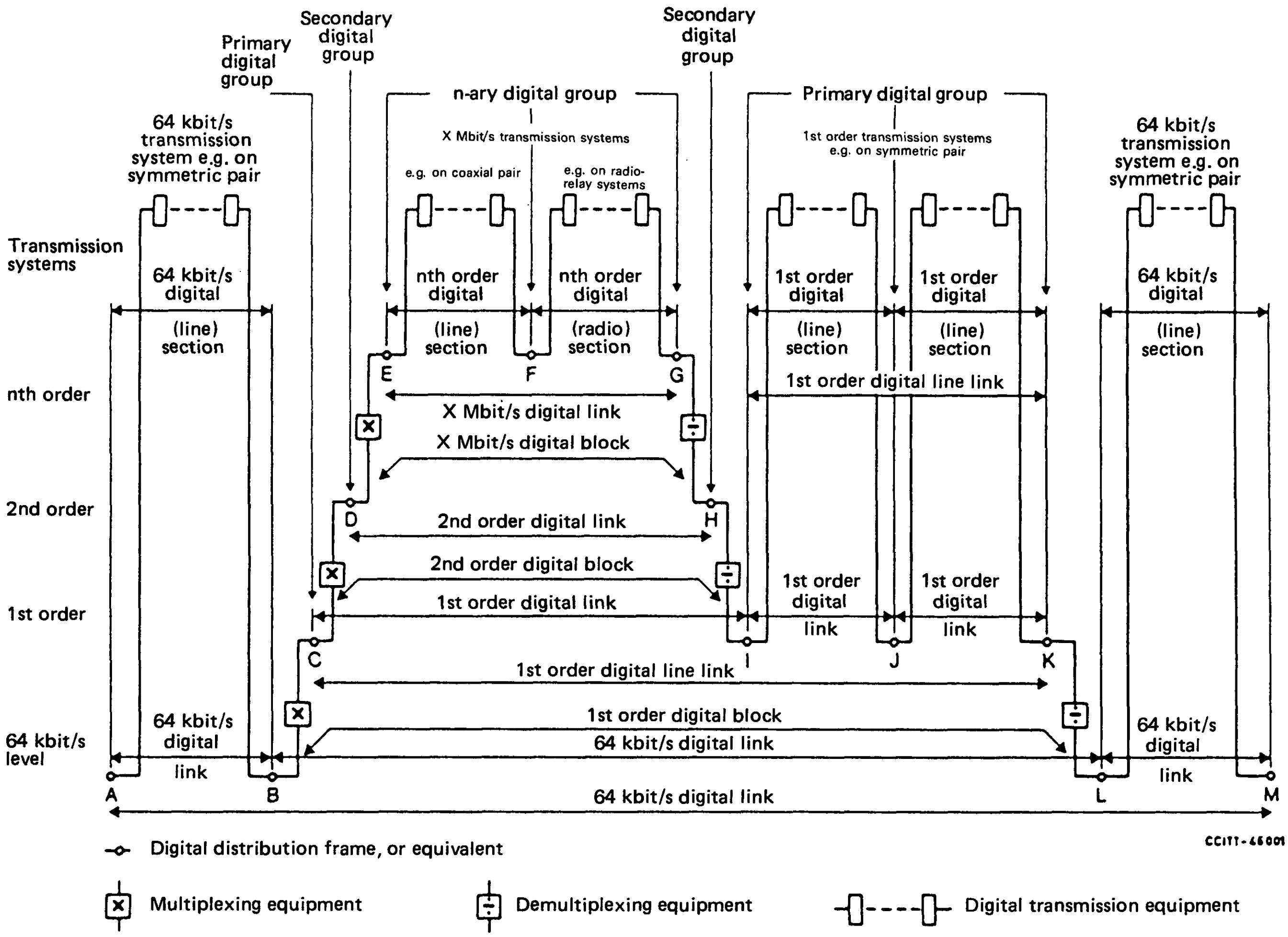
An indication provided by a digital multiplexer, line section or a radio section, that a signal applied at its input port is outside its prescribed maintenance limit.

3025 service digits [housekeeping digits]

F: éléments numériques de service

S: dígitos de servicio

Digits that are added, to a digital signal at the sending end of a digital link, normally at regular intervals and removed at the receiving end of that link and used to provide ancillary facilities.



Note 1 — Digital line and radio sections may be at digit rates which are either hierarchical or non-hierarchical.

Note 2 — A-B is a 64 kbit/s digital link consisting of a single 64 kbit/s digital section.

Note 3 — A-M is a 64 kbit/s digital link which contains six 64 kbit/s digital sections, A-B, E-F, F-G, I-J, J-K and L-M.

Note 4 — F-G is an X Mbit/s digital radio section which forms part of an X Mbit/s digital link E-G.

Note 5 — G-I is a 1st order digital link which contains a 2nd order digital link D-H.

Note 6 — I-K is an example of a digital line link.

FIGURE 1/G.701

Examples of digital link, digital section, digital line section, etc.

2.4 *Digital multiplexing*

4001 **highway (American: bus)**

F: bus (jonction multiplex interne) [canal]

S: arteria (bus)

A common path within an apparatus or station over which pass signals from a number of channels identified by time division.

4002 **channel gate**

F: porte de canal

S: puerta de canal

A device for connecting a channel to a highway, or a highway to a channel, at specified times.

4003 **digital multiplex hierarchy**

F: hiérarchie de multiplexage numérique

S: jerarquía de los múlitplex digitales

A series of digital multiplexers graded according to capability so that multiplexing at one level combines a defined number of digital signals, each having the digit rate prescribed for a lower order, into a digital signal having a prescribed digit rate which is then available for further combination with other digital signals of the same rate in a digital multiplexer of the next higher order.

4004 **primary digital group**

F: groupe numérique primaire

S: grupo digital primario

An assembly, by digital multiplexing, of digital signals occupying a specified number of channel time-slots to form a composite signal having a digit rate of 2048 kbit/s or 1544 kbit/s.

Note – Normally each channel time-slot has eight digit time-slots and an effective digit rate of 64 kbit/s.

4005 **primary PCM group [primary block] (American: digroup)**

F: groupe primaire MIC [bloc primaire]

S: grupo primario MIC [bloque primario]

An assembly, by digital multiplexing, of PCM signals occupying a specified number of channel time-slots to form a composite signal having a digit rate of 1544 kbit/s or 2048 kbit/s, in both directions of transmission.

Note – The following conventions could be useful:

Primary group μ – a basic group of PCM signals derived from 1544-kbit/s PCM multiplex equipment.

Primary group A – a basic group of PCM signals derived from 2048-kbit/s PCM multiplex equipment.

4006 **n-ary digital group**

F: groupe numérique n-aire

S: grupo digital n-ario

A number of primary digital or pcm groups assembled by digital multiplexing to form a composite signal of specified digit rate, in both directions of transmission.

Note 1 – A secondary digital group may comprise four primary digital or pcm groups to form a composite signal having a digit rate of 8448 or 6312 kbit/s.

Note 2 – A tertiary digital group may comprise four 8448 kbit/s secondary digital groups or five or seven 6312 kbit/s secondary digital groups to form a composite signal having a digit rate of 34368, 32064 or 44736 kbit/s.

Note 3 – A quaternary digital group may comprise four 34368 kbit/s tertiary digital groups to form a composite signal having a digit rate of 139264 kbit/s.

4007 **frame**

F: trame

S: trama

A cyclic set of consecutive time slots in which the relative position of each time slot can be identified.

4008 **multiframe**

F: multitrame

S: multitrama

A cyclic set of consecutive frames in which the relative position of each frame can be identified.

4009 **subframe**

F: sous-trame, secteur de trame

S: subtrama

A sequence of noncontiguous time-slots within a frame, each occurring at n times the frame repetition rate where n is an integer >1.

4010 **parallel to serial converter (American: serializer) [dynamicizer]**

F: convertisseur parallèle/série

S: convertidor paralelo/serie

A device that converts a group of signal elements, all of which are presented simultaneously, into a corresponding sequence of consecutive signal elements.

4011 **serial to parallel converter (American: deserializer) [staticizer]**

F: convertisseur série/parallèle

S: convertidor serie/paralelo

A device that converts a sequence of consecutive signal elements into a corresponding group of signal elements all of which are presented simultaneously.

4012 **time-division multiplexing**

F: multiplexage temporel [multiplexage par répartition dans le temps]

S: multiplexación por división en el tiempo

Multiplexing in which several signals are interleaved in time for transmission over a common channel.

4013 **digital multiplexing**

F: multiplexage numérique

S: multiplexación digital

A form of time division multiplexing applied to digital channels which convey digital signals.

4014 **digital multiplexer**

F: multiplexeur numérique

S: multiplexor digital

Equipment that combines by time-division multiplexing several digital signals into a single composite digital signal.

4015 **digital demultiplexing**

F: démultiplexage numérique

S: demultiplexación digital

The separation of a composite digital signal into its component digital signals.

4016 **digital demultiplexer**

F: démultiplexeur numérique

S: demultiplexor digital

Equipment that separates a composite digital signal into its component digital signals.

4017 **digital multiplex equipment**

F: équipement de multiplexage numérique

S: equipo múltiplex digital

The combination of a digital multiplexer and a digital demultiplexer at the same location, operating in opposite directions of transmission.

4018 **PCM multiplex equipment**

F: équipement de multiplexage MIC

S: equipo múltiplex MIC

Equipment that derives a single digital signal at a defined digit rate from several voice frequency channels by a combination of pulse code modulation and time division multiplexing, and that also carries out the complementary functions in the opposite direction of transmission.

4019 **digital block**

F: bloc numérique

S: bloque digital

The combination of a digital link and associated digital multiplex equipments.

Note – The bit rate of the digital link should form part of the title.

4020 **transmultiplexer**

F: transmultiplexeur

S: transmultiplexor

An equipment that transforms a frequency-division multiplexed signal (such as group or supergroup) into a corresponding time-division multiplexed signal that has the same structure as if it had been derived from PCM multiplex equipment, and that also carries out the complementary function in the opposite direction of transmission.

4021 **digital filling [digital padding]**

F: remplissage numérique

S: relleno digital [complementación digital]

The addition of signal elements at regular intervals to a digital signal to change the digit rate from its original value to a predetermined higher value.

Note – The added digits are not normally used to transmit information.

4022 **justification [stuffing, pulse stuffing]**

F: justification

S: justificación [relleno de impulsos]

The process of changing the digit rate of a digital signal in a controlled manner so that it can accord with a digit rate different from its own inherent rate, usually without loss of information.

4023 **positive justification [positive stuffing, positive pulse stuffing]**

F: justification positive

S: justificación positiva [relleno positivo de impulsos]

A method of justification in which the digit time-slots used to convey a digital signal have a digit rate that is always higher than the digit rate of that original signal.

Note 1 – Positive justification is usually achieved by the provision of a fixed number of digit time-slots (justifiable digit time-slots) per frame in the resultant signal which may be used to transmit either information from the original signal, or no information, according to the relative digit rates of the resultant signal and the original signal.

Note 2 – Information which indicates whether the justifiable digit time-slots contain information digits or justifying digits is conveyed by means of the justification service digits.

4024 **negative justification [negative stuffing, negative pulse stuffing]**

F: justification négative

S: justificación negativa [relleno negativo, relleno negativo de impulsos]

A method of justification in which the digit time-slots used to convey a digital signal have a digit rate that is always lower than the digit rate of that original signal.

Note 1 – The deleted digits are conveyed by separate means.

Note 2 – Information which facilitates the recovery of the deleted digits is conveyed by means of the justification service digits.

4025 **positive/zero/negative justification [positive/zero/negative stuffing, positive/zero/negative pulse stuffing]**

F: justification positive/nulle/négative

S: justificatión positiva/nula/negativa [relleno positivo/nulo/negativo de impulsos]

A method of justification in which the digit time-slots used to convey a digital signal have a digit rate that may be higher than, the same as, or lower than the digit rate of the original signal.

Note 1 – Justifiable digit time-slots are provided in accordance with Note 1 of 4023 above.

Note 2 – Separate means of transmitting deleted digits are provided in accordance with Note 2 of 4024 above.

Note 3 – Information which facilitates the recovery of the original digits, which are conveyed by means of the justification service digits.

Note 4 – Usually the digit time-slots used to convey a digital signal have the same nominal digit rate as the original signal.

4026 **justifiable digit time-slot [stuffable digit time-slot]**

F: créneau temporel élémentaire justifiable

S: intervalo de tiempo de dígito justificable [intervalo de tiempo de dígito rellenable]

A digit time-slot that is provided for the purpose of justification and which may contain either an information digit or a justifying digit.

4027 **justifying digit [stuffing digit]**

F: élément numérique de justification

S: dígito de justificación [dígito de relleno]

A digit inserted in a justifiable digit time-slot when that time slot is not required for an information digit.

4028 **justification service digit [stuffing service digit]**

F: élément numérique de service de justification

S: dígito de servicio de justificación [dígito de servicio de relleno]

A digit that transmits information concerning the status of a justifiable digit time-slot.

4029 **justification rate [stuffing rate]**

F: débit de justification

S: velocidad de justificación [velocidad de relleno]

The rate at which justifying digits are inserted, or at which information digits are transmitted by other means.

4030 **nominal justification rate [nominal stuffing rate]**

F: débit nominal de justification

S: velocidad nominal de justificación [velocidad nominal de relleno]

The justification rate that occurs when the digit rates of both the original signal and the justified signal are at their nominal values.

4031 **maximum justification rate [maximum stuffing rate]**

F: débit maximal de justification

S: velocidad máxima de justificación [velocidad máxima de relleno]

The maximum possible justification rate that can be accommodated by a justification process.

Note – In practice the tolerance limits of the original signal and of the system used to convey the justified signal might be such that the maximum justification rate is never realized.

4032 **justification ratio [stuffing ratio]**

F: taux de justification

S: relación de justificación [relación de relleno]

The ratio of the actual justification rate to the maximum justification rate.

4033 **nominal justification ratio [nominal stuffing ratio]**

F: taux nominal de justification

S: relación nominal de justificación [relación nominal de relleno]

The ratio of the nominal justification rate to the maximum justification rate.

2.5 *Frame alignment*

5001 **frame alignment**[3)]

F: verrouillage de trame

S: alineación de trama

The state in which the frame of the receiving equipment is synchronized with that of the received signal.

3) Similar definitions are applicable to multiframe alignment.

5002 **frame alignment signal** [4)]

F: signal de verrouillage de trame

S: señal de alineación de trama

The distinctive signal inserted in every frame or once in every *n* frames, always occupying the same relative position within the frame, and used to establish and maintain frame alignment.

5003 **bunched frame alignment signal** [4)]

F: signal de verrouillage de trame concentré

S: señal de alineación de trama concentrada

A frame alignment signal whose signal elements occupy consecutive digit time slots.

5004 **distributed frame alignment signal** [4)]

F: signal de verrouillage de trame réparti [signal de verrouillage de trame distribué]

S: señal de alineación de trama distribuida

A frame alignment signal whose signal elements occupy non-consecutive digit time slots.

5005 **frame alignment recovery time** [4)]

F: temps de reprise du verrouillage de trame

S: tiempo de recuperación de la alineación de trama

The time that elapses between a valid frame alignment signal being available at the receive terminal equipment and frame alignment being established.

Note – The frame alignment recovery time includes the time required for replicated verification of the validity of the frame alignment signal.

5006 **out-of-frame alignment time** [4)]

F: durée de perte du verrouillage de trame

S: duración de la pérdida de la alineación de trama

The time during which frame alignment is effectively lost.

Note – That time includes the time to detect loss of frame alignment and the frame alignment recovery time.

2.6 *Timing*

6001 **timing signal**

F: signal de rythme

S: señal de temporización

A cyclic signal used to control the timing of operations.

6002 **timing recovery [timing extraction]**

F: récupération du rythme

S: recuperación de la temporización [extracción de la temporización]

The derivation of a timing signal from a received signal.

4) Similar definitions are applicable to multiframe alignment.

6003 **retiming**

F: réajustement du rythme

S: reajuste de la temporización

Adjustment of the intervals between the significant instants of a digital signal, by reference to a timing signal.

6004 **time-slot**

F: créneau temporel [intervalle de temps]

S: intervalo de tiempo [sector de tiempo, celda de tiempo]

Any cyclic time interval that can be recognized and defined uniquely.

6005 **digit time-slot**

F: créneau temporel élémentaire [intervalle de temps élémentaire]

S: intervalo de tiempo de dígito

A time slot allocated to a single digit.

6006 **channel time-slot**

F: créneau temporel de voie

S: intervalo de tiempo de canal

A time slot occupying a specific position in a frame and allocated to a particular time-derived channel.

Note 1 – Where appropriate a description may be added, for example "telephone channel time slot".

Note 2 – In addition to its main function of transmitting a character signal, a channel time slot may also be used for in-slot signalling or for transmitting other information.

6007 **signalling time-slot**

F: créneau temporel de signalisation

S: intervalo de tiempo de señalización

A time slot occupying a specific position in a frame and allocated to the transmission of signalling.

6008 **frame alignment time-slot**

F: créneau temporel de verrouillage de trame

S: intervalo de tiempo de alineación de trama

A time slot occupying the same relative position in every frame and used to transmit the frame alignment signal.

6009 **clock**

F: horloge

S: reloj

Equipment that provides a timing signal.

Note – Where replicated sources are used for security reasons, the assembly of these is regarded as single clock.

6010 **reference clock**

F: horloge de référence

S: reloj de referencia

A clock of very high stability and accuracy that may be completely autonomous and whose frequency serves as a basis of comparison for the frequency of other clocks.

6011 **master clock**

F: horloge maîtresse

S: reloj maestro

A clock that is used to control the frequency of other clocks.

6012 **time interval error**

F: dérive temporelle

S: error de intervalo de tiempo

The total difference over a specified interval of time in the significant instants of a digital signal from their ideal positions in time.

6013 **relative time interval error**

F: dérive temporelle relative

S: error de intervalo de tiempo relativo

The total difference over a specified interval of time in the corresponding significant instants of two digital signals.

6014 **isochronous**

F: isochrone

S: isócrono

The essential characteristic of a time-scale or a signal such that the time intervals between consecutive significant instants either have the same duration or durations that are integral multiples of the shortest duration.

Note – In practice, variations in the time intervals are constrained within specified limits.

6015 **anisochronous**

F: anisochrone

S: anisócrono

The essential characteristic of a time-scale or a signal such that the time intervals between consecutive significant instants do not necessarily have the same duration or durations that are integral multiples of the shortest duration.

6016 **synchronous [mesochronous]**

F: synchrone [mésochrone]

S: síncrono [mesócrono]

The essential characteristic of time-scales or signals such that their corresponding significant instants occur at precisely the same average rate.

Note – The timing relationship between corresponding significant instants usually varies between specified limits.

6017 **homochronous**

F: homochrone

S: homócrono

The essential characteristic of time-scales or signals such that their corresponding significant instants have a constant, but uncontrolled, time relationship with each other.

6018 **non-synchronous [asynchronous/heterochronous]**

F: nonsynchrone [asynchrone/hétérochrone]

S: no-síncrono [asícrono/heterócrono]

The essential characteristic of time-scales or signals such that their corresponding significant instants do not necessarily occur at the same average rate.

6019 **plesiochronous**

F: plésiochrone

S: plesióchrono

The essential characteristic of time-scales or signals such that their corresponding significant instants occur at nominally the same rate, any variation in rate being constrained within specified limits.

Note 1 – Two signals having the same nominal digit rate, but not stemming from the same clock or homochronous clocks, are usually plesiochronous.

Note 2 – There is no limit to the time relationship between corresponding significant instants.

6020 **heterochronous**

F: hétérochrone

S: heterócrono

The essential characteristic of time-scales or signals such that their corresponding significant instants occur at different nominal rates.

Note 1 – Two signals having different nominal digit rates, and not stemming from the same clock or from homochronous clocks are usually heterochronous.

Note 2 – Terms 6015 to 6020 are based on the following Greek roots:

iso = equal
homo = same
plesio = near
hetero = different

6021 **codirectional interface**

F: interface codirectionnelle

S: interfaz codireccional

An interface across which the signals to be transferred and their associated timing signals are transmitted in the same direction.

6022 **centralized-clock interface**

F: interface à horloge centralisée

S: interfaz de reloj centralizado

An interface across which, for both directions of transmission of the signals to be transferred, the associated timing signals of both the exchange terminal on the line side and the exchange terminal on the service side are supplied from a centralized clock.

Note – The timing of the centralized clock may be derived from a nominated incoming line signal.

6023 **contradirectional interface**

F: interface contradirectionnelle

S: interfaz contradireccional

An interface across which the timing signals associated with both directions of transmission of the signals to be transferred, are directed towards the same side of the interface.

2.7 *Synchronization*

7001 **synchronization**

F: synchronisation

S: sincronización

The process of adjusting the corresponding significant instants of signals to make them synchronous.

7002 **timing information**

F: information de rythme

S: información de temporización

Information contained in a signal relating to the timing of another signal.

7003 **synchronization information**

F: information de synchronisation

S: información de sincronización

Information that indicates the relationship between the timing of two or more signals.

7004 **clock control signal**

F: signal de commande d'horloge

S: señal de control de reloj

A signal that directly controls the phase or frequency of a clock.

7005 **synchronization node**

F: nœud de synchronisation

S: nodo de sincronización

A point in a synchronized network at which synchronization information is derived, sent or received.

7006 **synchronization link**

F: liaison de synchronisation

S: enlace de sincronización

A link between two synchronization nodes over which synchronization information is transmitted.

7007 **synchronization network**

F: réseau de synchronisation

S: red de sincronización

An arrangement of synchronization nodes and synchronization links provided in order to synchronize the clocks at, or connected to, those nodes.

7008 **single-ended synchronization**

F: synchronisation locale [synchronisation unilatérale]

S: sincronización uniterminal

A method of synchronizing a specified synchronization node with respect to another synchronization node in which synchronization information at the specified node is derived from the phase difference between the local clock and the incoming digital signal from the other node.

7009 **double-ended synchronization**

F: synchronisation locale et distante [synchronisation bilatérale]

S: sincronización biterminal

A method of synchronizing a specified synchronization node with respect to another synchronization node in which synchronization information at the specified node is derived by comparing the phase difference between the local clock and the incoming digital signal from the other node, with the phase difference at the other node between its local clock and the digital signal incoming from the specified node.

7010 **unilateral control**

F: synchronisation unilatérale [commande unilatérale]

S: control unilateral

Control between two synchronization nodes such that the frequency of the clock of only one of these nodes is influenced by timing information derived from the clock of the other node.

7011 **bilateral control**

F: synchronisation bilatérale [commande bilatérale]

S: control bilateral

Control between two synchronization nodes such that the frequency of the clock of each of these nodes is influenced by timing information derived from the clock of the other node.

7012 **analogue control**

F: synchronisation analogique [mode analogique]

S: control analógico

A method of controlling clocks in which the clock control signal is a continuous (monotonic) function of the phase difference between clocks, at least over a limited range.

7013 **linear analogue control**

F: synchronisation analogique linéaire [mode analogique linéaire]

S: control analógico lineal

Analogue control in which the clock control signal is proportional to the phase difference between clocks, at least over a limited range.

7014 **amplitude quantized control**

F: synchronisation quantifiée [mode à quantification d'amplitude]

S: control por cuantificación de amplitud

A method of controlling clocks in which the clock control signal is a quantized function of the phase difference between clocks.

Note – In practice this implies that the working range of phase errors is divided into a finite number of subranges and that a unique signal is derived for each subrange whenever the error falls within a subrange.

7015 **time quantized control**

F: synchronisation échantillonnée [mode à quantification temporelle]

S: control por cuantificación temporal

A method of controlling clocks in which each clock control signal is derived or utilized only at a number of discrete instants, which may or may not be equally separated in time.

7016 **synchronized network [synchronous network]**

F: réseau synchronisé [réseau synchrone]

S: red sincronizada [red sincrona]

A network in which the corresponding significant instants of nominated signals are adjusted to make them synchronous.

7017 **non-synchronized network**

F: réseau non synchronisé

S: red no sincronizada

A network in which signals need not be synchronous.

7018 **mutually synchronized network**

F: réseau à synchronisation mutuelle

S: red mutuamente sincronizada

A synchronized network in which each clock exerts a degree of control on all others.

7019 **democratic network, democratic mutually synchronized network**

F: réseau démocratique, réseau à synchronisation mutuelle démocratique

S: red democrática, red democrática mutuamente sincronizada

A mutually synchronized network in which all clocks are of equal status and exert equal amounts of control on the others; the network operating frequency (digit rate) being the mean of the natural (uncontrolled) frequencies of all the clocks.

7020 **hierarchic network, hierarchic synchronized network**

F: réseau hiérarchisé, réseau à synchronisation hiérarchisée

S: red jerárquica, red con sincronización jerárquica

A synchronized network in which each clock is assigned a particular status which determines the degree of control it exerts over the other clocks.

7021 **hierarchic mutually synchronized network**

F: réseau hiérarchisé à synchronisation mutuelle

S: red jerárquica mutuamente sincronizada

A mutually synchronized network in which each clock is assigned a particular status which determines the degree of control it exerts over other clocks; the network operating frequency being a weighted mean of the natural frequencies of all the clocks.

7022 **monarchic network, monarchic synchronized network [despotic network, despotic synchronized network]**

F: réseau despotique, réseau à synchronisation despotique

S: red despótica, red con sincronización despótica [red monárquica, red con sincronización monárquica]

A synchronized network in which a single clock exerts control over all the other clocks.

7023 **oligarchic network, oligarchic synchronized network**

F: réseau oligarchique, réseau à synchronisation oligarchique

S: red oligárquica, red con sincronización oligárquica

A synchronized network in which a few selected clocks are mutually synchronized and exert control over all the other clocks.

2.8 *Pulse Code Modulation*

8001 **pulse code modulation (PCM)**

F: modulation par impulsions et codage (MIC)

S: modulación por impulsos codificados (MIC)

A process in which a signal is sampled, and each sample is quantized independently of other samples and converted by encoding to a digital signal.

8002 **differential pulse code modulation (DPCM)**

F: modulation par impulsions et codage différentiel (MICD)

S: modulación por impulsos codificados diferencial (MICD)

A process in which a signal is sampled, and the difference between each sample of this signal and its estimated value is quantized and converted by encoding to a digital signal.

Note – The estimated values of the signal are calculated by a predictor from the quantized difference signal.

8003 **delta modulation**

F: modulation delta

S: modulación delta

A form of differential pulse code modulation in which only the sign of the difference between each sample and its predicted value is detected and encoded by a single bit.

8004 **adaptive differential pulse code modulation (ADPCM)**

F: modulation par impulsions et codage différentiel adaptatif (MICDA)

S: modulación por impulsos y código diferencial adaptativo (MICDA)

A form of differential pulse code modulation that uses adaptive quantizing.

Note 1 – The predictor may be either fixed (time invariant) or variable.

Note 2 – When the predictor is adaptive, the adaption of its coefficients is made from the quantized difference signal.

8005 **predictor**

F: prédicteur

S: predictor

A device that provides an estimated value of a sampled signal derived from previous samples of the same signal or from a quantized version of those samples.

8006 **adaptive predictor**

F: prédicteur adaptatif

S: predictor adaptativo

A predictor whose estimating function is made variable according to the short term spectral characteristics of the sampled signal.

8007 **sample**

F: échantillon

S: muestra

A representative value of a signal at a chosen instant, derived from a portion of that signal.

8008 **sampling**

F: échantillonnage

S: muestreo

The process of taking samples of a signal, usually at equal time intervals.

8009 **sampling rate**

F: fréquence d'échantillonnage [taux d'échantillonnage]

S: velocidad de muestreo [frecuencia de muestreo]

The number of samples taken of a signal per unit time.

8010 **working range**

F: plage de fonctionnement [gamme de fonctionnement]

S: gama de funcionamiento

The range of values of an input signal over which an equipment is designed to operate with a specified performance. (See Figure 2/G.701.)

8011 **quantizing**

F: quantification

S: cuantificación

A process in which a continuous range of values is divided into a number of adjacent intervals, and any value within a given interval is represented by a single predetermined value within the interval. (See Figure 2/G.701.)

8012 **adaptive quantizing**

F: quantification adaptative

S: cuantificación adaptativa

Quantizing in which some parameters are made variable according to the short term statistical characteristics of the quantized signal.

8013 **uniform quantizing**

F: quantification uniforme

S: cuantificación uniforme

Quantizing in which all the quantizing intervals lying entirely with the working range are equal. (See Figure 2/G.701.)

8014 **non-uniform quantizing**

F: quantification non uniforme

S: cuantificación no uniforme

Quantizing in which not all the quantizing intervals lying entirely with the working range are equal. (See Figure 2/G.701.)

8015 **quantizing interval**

F: intervalle de quantification

S: intervalo de cuantificación

One of the intervals used in quantizing. (See Figure 2/G.701.)

8016 **decision value**

F: valeur de décision [amplitude de décision]

S: valor de decisión

A value defining the boundary between adjacent quantizing intervals. (See Figures 2/G.701 and 4/G.701.)

8017 **virtual decision value**

F: valeur virtuelle de décision [amplitude virtuelle de décision]

S: valor virtual de decisión

Each of the two defined values, that provide conventional bounds for the working range in quantizing. (See Figure 2/G.701.)

Note – These values are taken to represent hypothetical outer bounds for the two extreme quantizing intervals of the quantizing law.

8018 **quantized value**

F: valeur quantifiée [amplitude quantifiée]

S: valor cuantificado

The single discrete value used to represent any value in a particular quantizing interval. (See Figure 2/G.701.)

8019 **load capacity [overload point]**

F: capacité de charge [point de surcharge]

S: capacidad de carga [punto de sobrecarga]

The level of a sinusoidal signal whose positive and negative peaks coincide with the virtual decision values.

8020 **peak limiting, peak limiting in quantizing**

F: écrêtage

S: limitación de cresta (en cuantificación)

The effect whereby any value to be quantized lying outside the working range is replaced by the nearest quantized value. (See Figure 2/G.701.)

8021 **quantizing distortion**

F: distorsion de quantification

S: distorsión de cuantificación

The distortion resulting from the process of quantizing samples within the working range.

8022 **quantizing distortion power**

F: puissance de distorsion de quantification

S: potencia de la distorsión de cuantificación

The power of the distortion component of the output signal resulting from the process of quantizing.

8023 **encoding [coding, coding in PCM]**

F: codage

S: codificación [codificación en MIC]

The generation of a code word to represent a quantized value.

8024 **encoder [coder]**

F: codeur

S: codificador

A device that performs encoding.

8025 **uniform encoding**

F: codage uniforme

S: codificación uniforme

The generation of code words to represent uniformly quantized values.

8026 **non-uniform encoding**

F: codage non uniforme

S: codificación no uniforme

The generation of code words to represent non-uniformly quantized values. (See Figure 3/G.701.)

8027 **encoding law**

F: loi de quantification [loi de codage]

S: ley de codificación

The law defining the relative values of the quantizing intervals used in quantizing and encoding. (See Figure 4/G.701.)

8028 **segmented encoding law**

F: loi de quantification à segments [loi de codage à segments]

S: ley de codificación por segmentos

An encoding law in which an approximation to a smooth law is obtained by a number of linear segments. (See Figures 3a/G.701 and 3b/G.701.)

8029 **decoding**

F: décodage

S: decodificación

The generation of reconstructed samples.

8030 **decoder**

F: décodeur

S: decodificador

A device that performs decoding.

8031 **reconstructed sample**

F: échantillon reconstitué

S: muestra reconstruida

The signal generated at the output of a decoder when a specified digital signal representing a quantized value is applied to its input.

8032 **codec**

F: codec

S: códec

A combination of an encoder and a decoder operating in opposite directions of transmission in the same equipment.

Note – When used to describe an equipment the function of the equipment should qualify the title, for example: supergroup codec, hypergroup codec.

8033 **digilogue channel**

F: voie digilogue

S: canal digi-analógico

A channel in which information is represented by a digital signal at one end and the same information is represented by the corresponding analogue signal at the other end.

Note – The term may be qualified by "A to D" or "D to A" to indicate whether encoding or decoding is being performed.

8034 **digilogue circuit**

F: circuit digilogue

S: circuito digi-analógico

A circuit in which transmission is provided in one direction by an A to D digilogue channel and in the other direction by a D to A digilogue channel.

Note – Because the digital interface is inherently 4-wire, the term may be qualified by "2-W" or "4-W" to indicate whether the analogue interface is 2-wire or 4-wire.

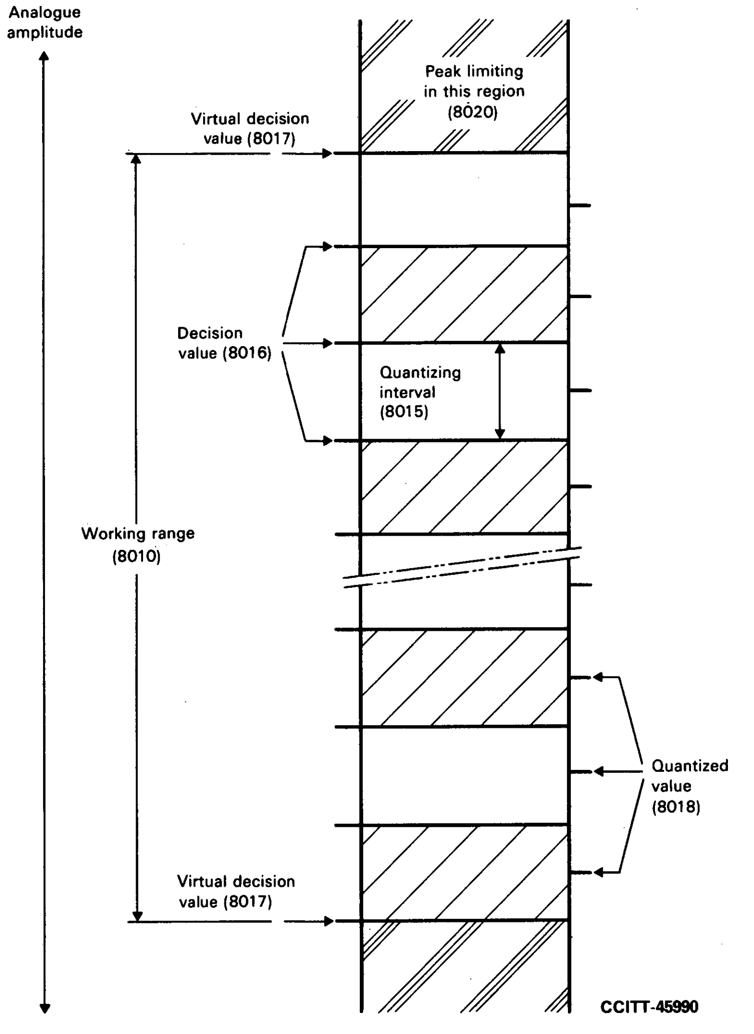
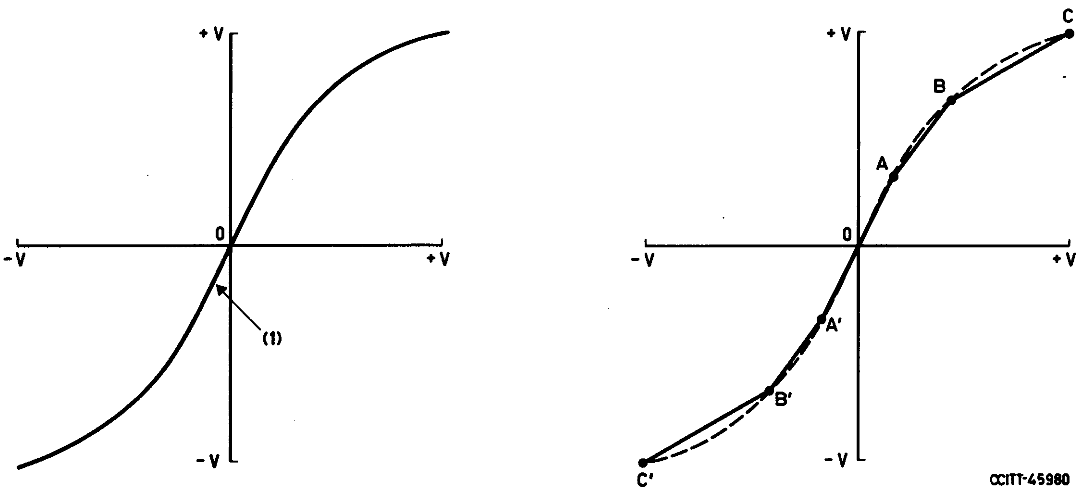


FIGURE 2/G.701

Illustration of terms associated with quantizing (8011)



a) Smooth characteristic

Note – A central linear section (1), if present, must tangentially join on to the curved end-section.

b) Segmented characteristic

Note – This particular characteristic has 5 linear segments: C′B′, B′A′, A′A, AB, BC.

FIGURE 3/G.701

Non-uniform encoding laws

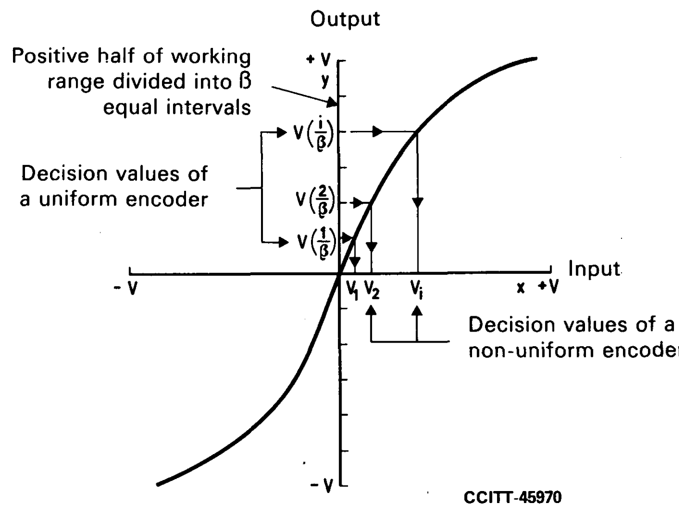


FIGURE 4/G.701

Relationship between the decision values of a uniform and a non-uniform encoding law

2.9 *Codes*

9001 **pulse code**

F: code d'impulsions (code de modulation d'impulsions)

S: código de impulsos

A set of rules giving the equivalence between each quantized value and its corresponding code word.

9002 **line code**

F: code en ligne

S: código de línea, código en línea

A code chosen to suit the characteristics of a channel, that defines the equivalence between sets of digits presented for transmission and the corresponding sequence of signal elements transmitted over that channel.

9003 **redundant line code**

F: code en ligne redondant

S: código de línea redundante

A line code that uses more encoded signal elements than strictly necessary to represent groups of digits of the original signal.

9004 **alternate mark inversion code (AMI code)**

F: code bipolaire [code bipolaire alternant, code bipolaire strict]

S: codigo de inversión de marcas alternada (codigo AMI) [código bipolar]

A line code that employs a ternary signal to convey binary digits, in which successive binary ones are represented by signal elements that are normally of alternating, positive and negative polarity but equal in amplitude, and in which binary zeros are represented by signal elements that have zero amplitude.

9005 **modified alternate mark inversion code**

F: code bipolaire alternant modifié

S: código de inversión de marcas alternada modificado

A line code that is based on an alternate mark inversion code, in which alternate mark inversion violations occur in accordance with a defined set of rules.

9006 **alternate mark inversion signal [bipolar signal]**

F: signal bipolaire [signal bipolaire alternant]

S: señal de inversión de marcas alternada [señal bipolar]

The encoded signal produced by alternate mark inversion code.

9007 **alternate mark inversion violation [bipolar violation]**

F: violation de bipolarité

S: violación de inversión de marcas alternada [violación bipolar]

A non-zero signal element in an alternate mark inversion signal that has the same polarity as the previous non-zero signal element.

9008 **disparity**

F: disparité

S: disparidad

The algebraic sum of the values of the departure from notional zero level of one or more consecutive signal elements forming a defined group.

9009 **digital sum**

F: somme numérique

S: suma digital

The algebraic sum of the disparities of a sequence of consecutive defined groups of signal elements.

9010 **digital sum variation**

F: variation de la somme numérique

S: variación de la suma digital

The difference between the maximum possible digital sum and the minimum possible digital sum of a specified number of groups of signal elements.

9011 **balanced code**

F: code à somme bornée

S: código equilibrado

A code that generates only groups of signal elements that have zero digital sum.

9012 **paired-disparity code [alternate code, alternating code]**

F: code à disparité compensée

S: código con disparidad compensada [código alternado, código alternante]

A code in which some or all of the digits in the original signal are represented by two assemblies of digits, of opposite disparity, which are used in a sequence to minimize the digital sum of a longer sequence of digits.

Note – An alternate mark inversion signal is an example of a paired-disparity code.

9013 **PCM binary code**

F: code binaire MIC

S: código binario MIC

A pulse code in which all the quantized values are identified by binary numbers taken in order.

Note – This term should not be used for line transmission.

9014 **symmetrical binary code**

F: code binaire symétrique

S: código binario simétrico

A pulse code in which the sign of the quantized value, is represented by one digit, and in which the remaining digit constitute a binary number representing the magnitude.

Note 1 – In a particular symmetrical binary code, the order of the digits and the use made of the symbols 0 and 1 in the various digit positions must be specified.

Note 2 – This term should not be used for line transmission.

9015 **code conversion**

F: transcodage

S: conversión de código

The conversion of digital signals in one code to the corresponding signals in a different code.

ANNEX A

(to Recommendation G.701)

Alphabetical list of terms defined in this Recommendation

8004	adaptive differential pulse code modulation (ADPCM)
8006	adaptive predictor
8012	adaptive quantizing
3023	alarm indication signal (AIS)
9012	[alternate code]
9004	alternate mark inversion code (AMI code)
9012	[alternating code]
9006	alternate mark inversion signal
9007	alternate mark inversion violation
7014	amplitude quantized control
7012	analogue control
1002	analogue signal
6015	anisochronous
6018	[asynchronous/heterochronous]
9011	balanced code
7011	bilateral control
2003	binary digit
2002	binary figure
9006	[bipolar signal]
9007	[bipolar violation]
3019	bit sequence independence
5003	bunched frame alignment signal
4001	(bus: American)
6022	centralized-clock interface
1005	channel, transmission channel
4002	channel gate
6006	channel time-slot
2005	[character signal]
1007	circuit, telecommunication circuit
6009	clock
7004	clock control signal
2005	code word
8032	codec
8024	[coder]
8023	[coding, coding in PCM]
6021	codirectional interface
6023	contradirectional interface
2026	controlled slip
2020	decision circuit
2019	decision instant, decision instant of a digital signal
8016	decision value
8030	decoder
8029	decoding
8003	delta modulation
7019	democratic network, democratic mutually synchronized network
2029	descrambler

Reference

[1] CCITT Recommendation *Definitions relating to national and international numbering plans*, Vol. VI, Rec. Q.10.

DIGITAL HIERARCHY BIT RATES

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

The CCITT,

considering

(a) that digital hierarchy bit rates are those bit rates which are or will be used as the basis for higher digital hierarchy levels if such levels exist (see Recommendation G.701, definition 4003);

(b) that the specification of hierarchical bit rates is necessary to prevent the proliferation of interface standards used in digital networks;

(c) that international interconnections of digital network components are preferably carried out at hierarchical bit rates;

(d) that when determining hierarchical bit rates a number of factors relating to services, transmission media and networking need to be taken into account, for example:

- characteristics of and suitable coding method for analogue source signals;
- bit rates of digital source signals;
- use of available transmission media;
- compatibility with analogue multiplex systems;
- modularity and flexibility in assembling and routing groups of source signals,

recommends

that the following bit rates should be used as hierarchical bit rates in digital networks:

Digital Hierarchy Level	Hierarchichal bit rates (kbit/s) for networks with the digital hierarchy based on a first level bit rate of		
	1544 kbit/s		2048 kbit/s
	64		64
1	1544		2 048
2	6312		8 448
3	32 064	44 736	34 368
4	97 728		139 264

Figure 1/G.702 and Figure 2/G.702 show the recommended hierarchical bit rates only, including references to related Recommendations on network interfaces, multiplex equipments, digital sections/systems.

Recommendations on the following may also exist, but are not identified in Figure 1/G.702 and Figure 2/G.702:

- multiplex equipments operating between non-adjacent levels of the digital hierarchy;
- network interfaces, multiplex equipments and digital sections/systems at non-hierarchical bit rates.

Annex A to this Recommendation provides guidelines on usable bit rates available for services.

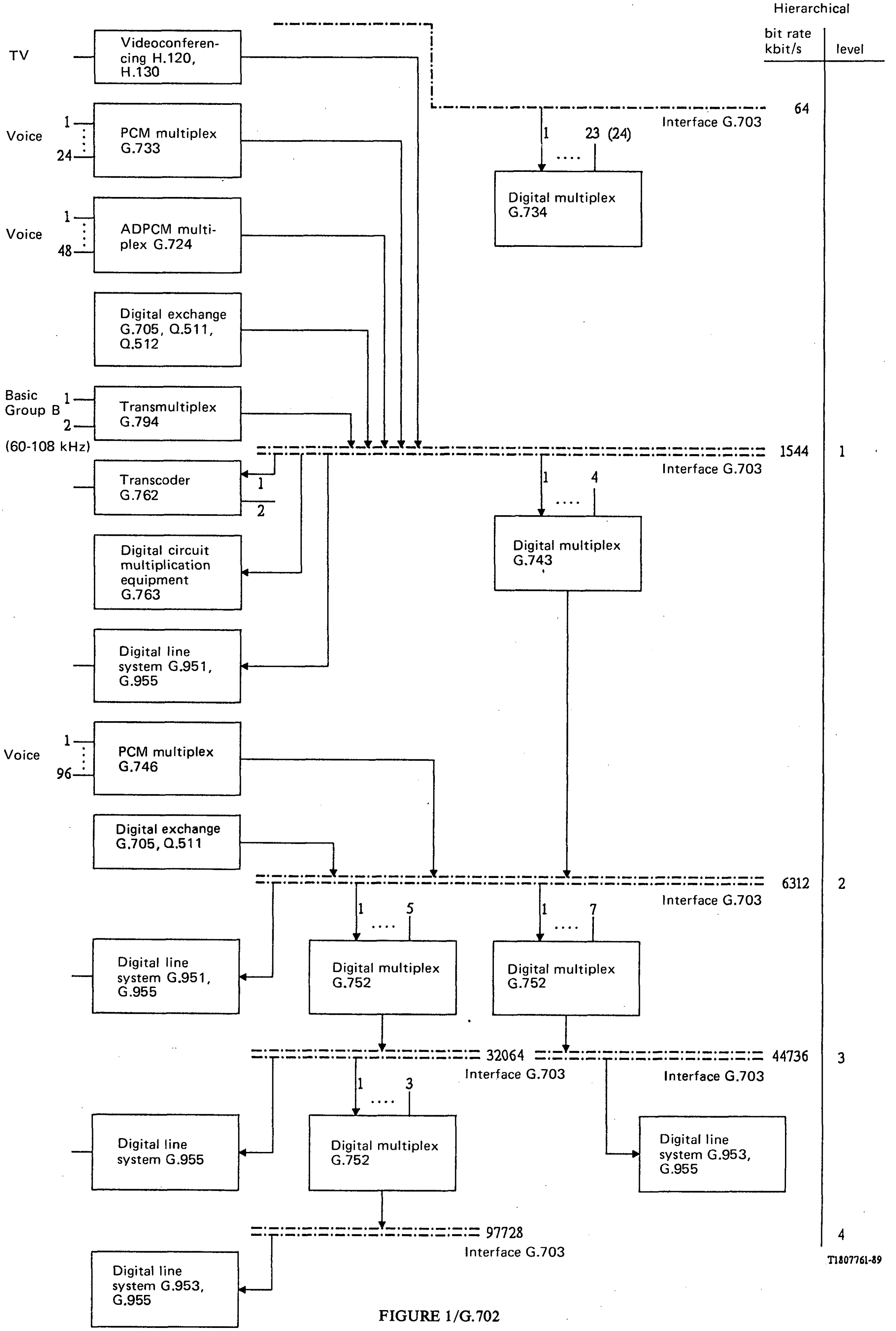


FIGURE 1/G.702

Hierarchical bit rates for networks with the digital hierarchy based on the first level bit rate of 1544 kbit/s

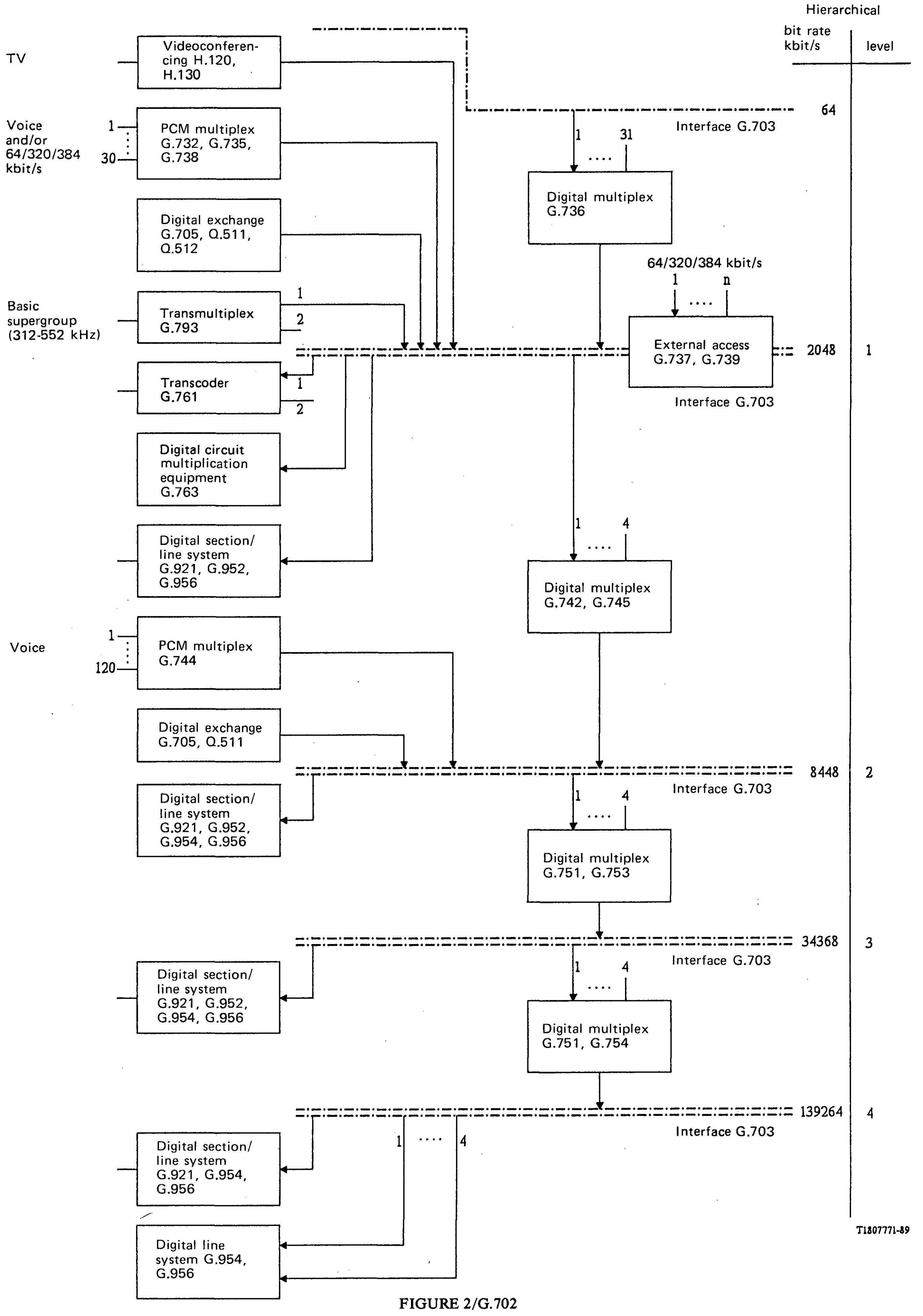


FIGURE 2/G.702

Hierarchical bit rates for networks with the digital hierarchy based on the first level bit rate of 2048 kbit/s

ANNEX A

(to Recommendation G.702)

Usable bit rates available for services

In the case of access to the ISDN for broadband services, bit rates up to the primary hierarchy level are specified in the I.200 series of Recommendations.

In general, with regard to bit rates available for transport of service signals, the following guidelines apply:

A.1 For the hierarchies based on the 1544 kbit/s primary rate, the principle has been established that some bits in the frame should be reserved, in particular to perform quality control of the digital paths when several digital sections in tandem are involved. Table A-1/G.702 provides the necessary information.

TABLE A-1/G.702

Bit rates available for services and frame structures required at hierarchical interfaces

Hierarchy bit rate (kbit/s)	Frame structure as per Recommendations	Reserved bits	Bit rate available for services (kbit/s)
1 544	G.704	F [a]	1 536
6 312 [b]	Not applicable	None	6 312
6 312 [c]	G.704	F bits and bits in time slots 97 and 98	6 144
44 736	G.752	M_j [d] F_0, F_{11}, F_{12}	44 407 [d]

[a] The use of the F-bit for purposes additional to framing is under study.

[b] In networks with asynchronous operation.

[c] In networks with synchronous operation.

[d] In some applications, the *C*-bits (C_{j1}, C_{j2} and C_{j3}) may also need to be reserved. In this case, the bit rate available for services becomes 44 209 kbit/s.

A.2 In case of networks using 2048 kbit/s based hierarchy there is in principle no basic restriction on the use of full capacity of the digital path. However, it is recognized that compatibility with recommended frame structures at the various levels of the 2 Mbit/s hierarchy (e.g. the use of the same frame alignment pattern) could be a preferred solution since it offers the following advantages:

- use of the same framing devices for switched and non-switched applications;
- end-to-end quality control performed in a unique way by the network when the maintenance entity that terminates the service (e.g. the encoding device) does not belong to the network;
- possibility of performing additional network management functions that could be required, depending on the applications.

The preference for compatibility with recommended frame structures could be reconsidered for the applications where significant restrictions on the efficient use of the digital path capability can be identified.

PHYSICAL/ELECTRICAL CHARACTERISTICS OF HIERARCHICAL DIGITAL INTERFACES

(Geneva, 1972; further amended)

The CCITT,

considering

that interface specifications are necessary to enable the interconnection of digital network components (digital sections, multiplex equipment, exchanges) to form an international digital link or connection;

that Recommendation G.702 defines the hierarchical levels;

that Recommendation G.704 deals with the functional characteristics of interfaces associated with network nodes;

that I.430 series Recommendations deal with the layer 1 characteristics for ISDN user-network interfaces;

recommends

that physical and electrical characteristics of the interfaces at hierarchical bit rates should be as described in this Recommendation.

Note 1 – The characteristics of interfaces at non-hierarchical bit rates, except $n \times 64$ kbit/s interfaces conveyed by 1544 kbit/s or 2048 kbit/s interfaces, are specified in the respective equipment Recommendations.

Note 2 – The jitter specifications contained in the following §§ 6, 7, 8 and 9 are intended to be imposed at international interconnection points.

Note 3 – The interfaces described in §§ 2 to 9 correspond to the ports T (output port) and T′ (input port) as recommended for interconnection in CCIR Recommendation AC/9 with reference to Report AH/9 of CCIR Study Group 9. (This Report defines the points T and T′.)

Note 4 – For signals with bit rates of $n \times 64$ kbit/s ($n = 2$ to 31) which are routed through multiplexing equipment specified for the 2048 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2048 kbit/s interface specified in § 6. For signals with bit rates of $n \times 64$ kbit/s ($n = 2$ to 23) which are routed through multiplexing equipment specified for the 1544 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 1544 kbit/s interface specified in § 2.

1 Interface at 64 kbit/s

1.1 *Functional requirements*

1.1.1 The following basic requirements for the design of the interface are recommended:

1.1.2 In both directions of transmission, three signals can be carried across the interface:

- 64 kbit/s information signal,
- 64 kHz timing signal,
- 8 kHz timing signal.

Note 1 – The 64 kbit/s information signal and the 64 kHz timing signal are mandatory. However, although an 8 kHz timing must be generated by the controlling equipment (e.g. PCM multiplex or time slot access equipment), it should not be mandatory for the subordinate equipment on the other side of the interface to either utilize the 8 kHz timing signal from the controlling equipment or to supply an 8 kHz timing signal.

Note 2 – The detection of an upstream fault can be transmitted across the 64 kbit/s interface by transmitting an alarm indication signal (AIS) towards the subordinate equipment.

1.1.3 The interface should be bit sequence independent at 64 kbit/s.

Note 1 – An unrestricted 64-kbit/s signal can be transmitted across the interface. However, this does not imply that unrestricted 64-kbit/s paths are realizable on a global basis. This is because some Administrations presently have or are continuing to install extensive networks composed of digital line sections whose characteristics do not permit the transmission of long sequences of 0s. (Recommendation G.733 provides for PCM multiplexes with characteristics appropriate for such digital line sections.) Specifically for octet timed sources, in 1544-kbit/s digital networks it is required that at least one binary 1 should be contained in any octet of a 64-kbit/s digital signal. For a bit stream which is not octet timed no more than 7 consecutive 0s should appear in the 64-kbit/s signal.

Note 2 – Although the interface is bit sequence independent, the use of the AIS (all 1s bit pattern) may result in some minor restrictions for the 64-kbit/s source. For example, an all 1s alignment signal could result in problems.

1.1.4 *Three types of envisaged interfaces*

1.1.4.1 *Codirectional interface*

The term codirectional is used to describe an interface across which the information and its associated timing signal are transmitted in the same direction (see Figure 1/G.703).

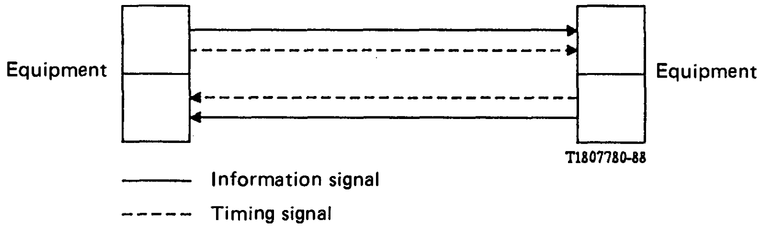


FIGURE 1/G.703

Codirectional interface

1.1.4.2 *Centralized clock interface*

The term centralized clock is used to describe an interface wherein for both directions of transmission of the information signal, the associated timing signals are supplied from a centralized clock, which may be derived for example from certain incoming line signals (see Figure 2/G.703).

Note – The codirectional interface or centralized clock interface should be used for synchronized networks and for plesiochronous networks having clocks of the stability required (see Recommendation G.811) to ensure an adequate interval between the occurrence of slips.

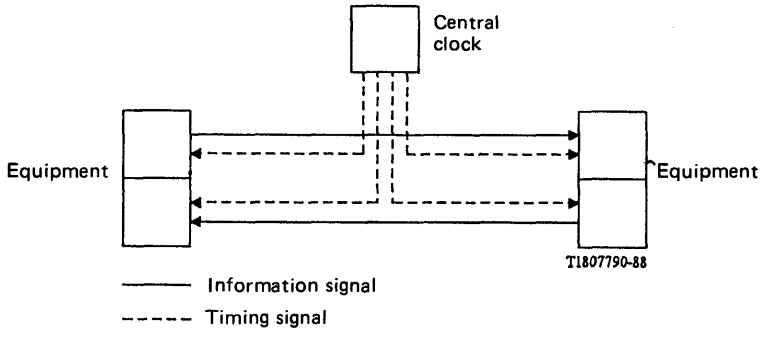


FIGURE 2/G.703

Centralized clock interface

1.1.4.3 *Contradirectional interface*

The term contradirectional is used to describe an interface across which the timing signals associated with both directions of transmission are directed towards the subordinate equipment (see Figure 3/G.703.)

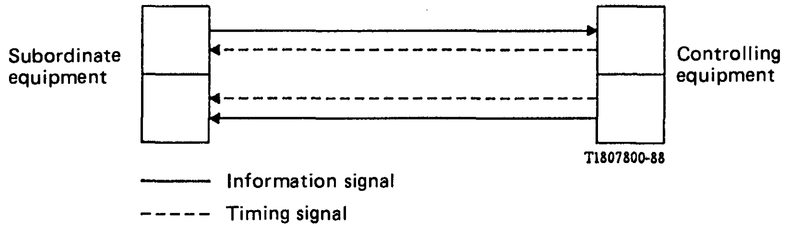


FIGURE 3/G.703

Contradirectional interface

1.2 *Electrical characteristics*

1.2.1 *Electrical characteristics of 64-kbit/s codirectional interface*

1.2.1.1 *General*

1.2.1.1.1 Nominal bit rate: 64 kbit/s.

1.2.1.1.2 Maximum tolerance of signals to be transmitted through the interface: ± 100 ppm.

1.2.1.1.3 64-kHz and 8-kHz timing signal to be transmitted in a codirectional way with the information signal.

1.2.1.1.4 One balanced pair for each direction of transmission; the use of transformers is recommended.

1.2.1.1.5 *Code conversion rules*

Step 1 – A 64-kbit/s bit period is divided into four unit intervals.

Step 2 – A binary one is coded as a block of the following four bits:

1 1 0 0

Step 3 – A binary zero is coded as a block of the following four bits:

1 0 1 0

Step 4 – The binary signal is converted into a three-level signal by alternating the polarity of consecutive blocks.

Step 5 – The alternation in polarity of the blocks is violated every 8th block. The violation block marks the last bit in an octet.

These conversion rules are illustrated in Figure 4/G.703.

1.2.1.1.6 *Overvoltage protection requirement*

See Annex B.

1.2.1.2 *Specifications at the output ports* (see Table 1/G.703)

1.2.1.3 *Specifications at the input ports*

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 128 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

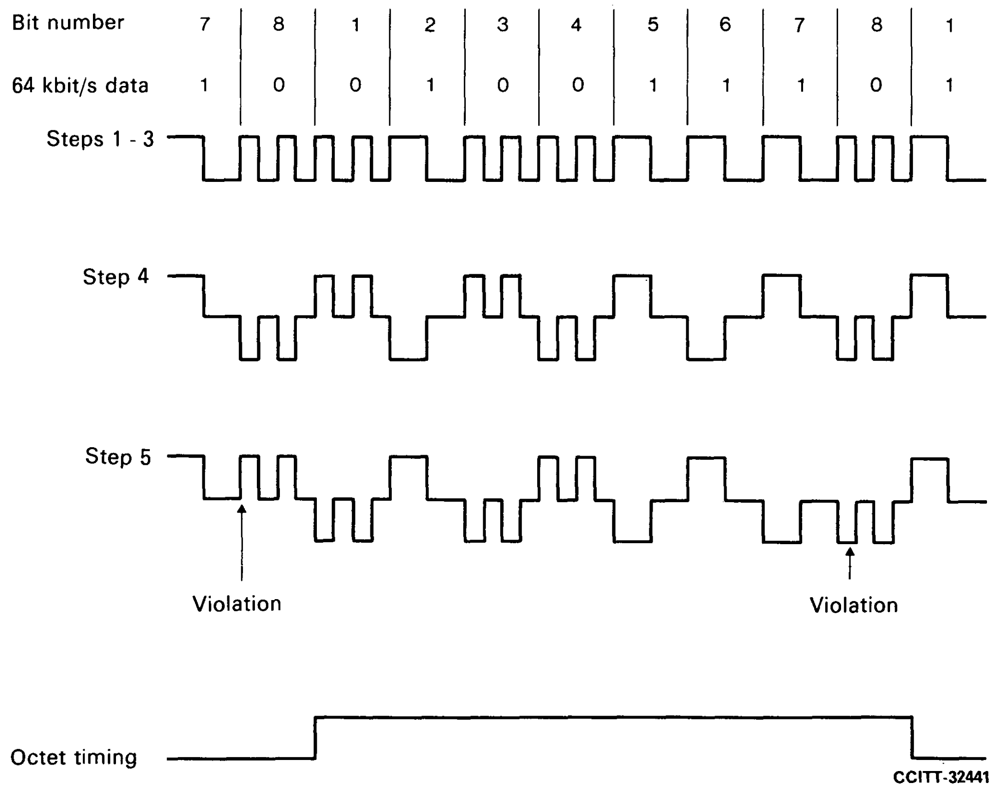


FIGURE 4/G.703

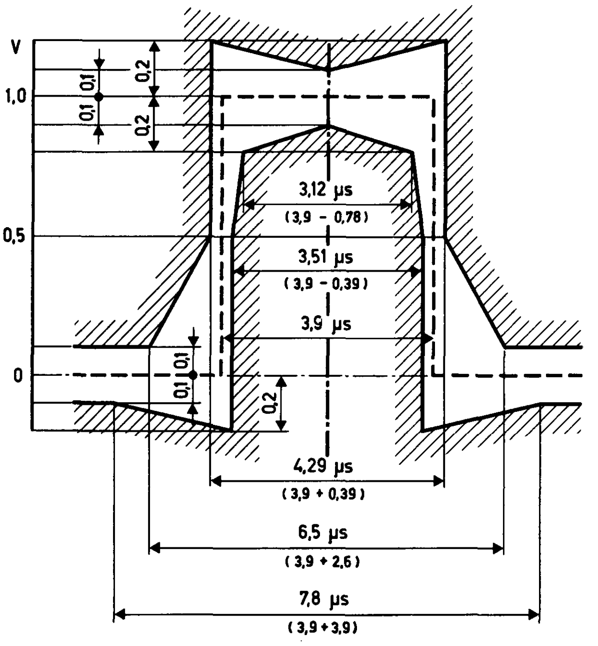
The return loss at the input ports should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
4 to 13	12
13 to 256	18
256 to 384	14

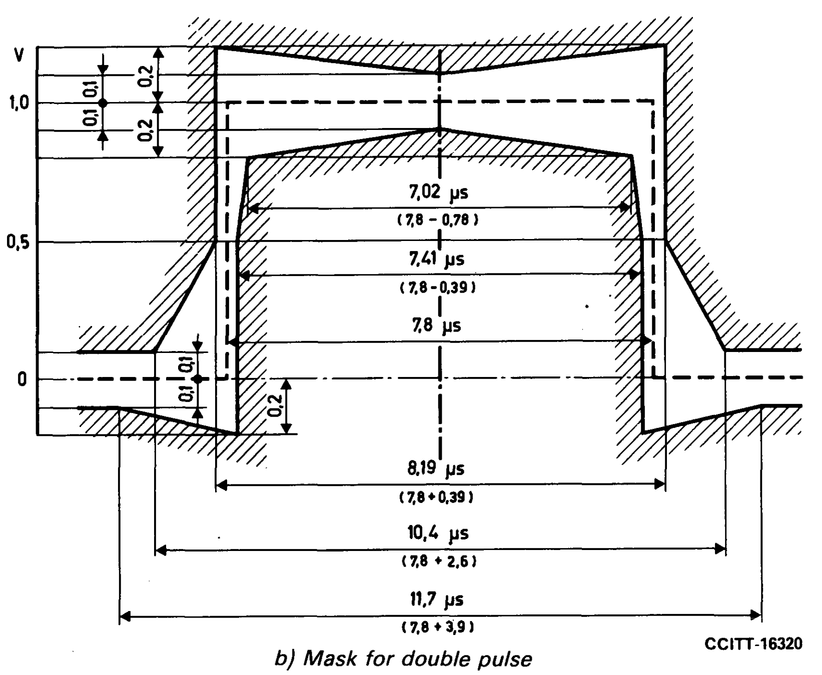
To provide nominal immunity against interference, input ports are required to meet the following requirements:

A nominal aggregate signal, encoded as a 64 kbit/s co-directional signal and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.152 ($2^{11} - 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

Note – If the symmetrical pair is screened, the screen shall be connected to the earth at the output port, and provision shall be made for connecting the screen of the symmetrical pair to earth, if required, at the input port.



a) Mask for single pulse



b) Mask for double pulse

Note – The limits apply to pulses of either polarity.

FIGURE 5/G.703

Pulse masks of the 64 kbit/s codirectional interface

TABLE 1/G.703

Symbol rate	256 kbauds
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the masks in Figure 5/G.703, irrespective of the polarity
Pair for each direction	One symmetric pair
Test load impedance	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.10 V
Nominal pulse width	3.9 μs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulses interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to § 2 of Recommendation G.823

Note – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.

1.2.2 *Electrical characteristics of the 64-kbit/s centralized clock interface*

1.2.2.1 *General*

1.2.2.1.1 Nominal bit rate: 64 kbit/s. The tolerance is determined by the network clock stability (see Recommendation G.811).

1.2.2.1.2 For each direction of transmission there should be one symmetrical pair of wires carrying the data signal. In addition, there should be symmetrical pairs of wires carrying the composite timing signal (64 kHz and 8 kHz) from the central clock source to the office terminal equipment. The use of transformers is recommended.

1.2.2.1.3 *Overvoltage protection requirement*

See Annex B.

1.2.2.1.4 *Code conversion rules*

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64-kHz bit-timing information using AMI code with a 50% to 70% duty ratio and the 8-kHz octet-phase information by introducing violations of the code rule. The structure of the signals and their nominal phase relationships are shown in Figure 6/G.703.

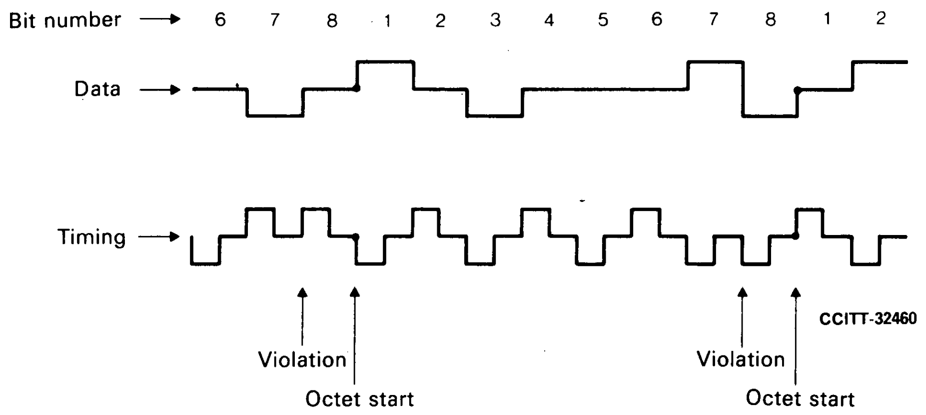


FIGURE 6/G.703

Signal structures of the 64-kbit/s central clock interface at office terminal output ports

The data stream at the output ports should be timed by the leading edge of the timing pulse and the detection instant at the input ports should be timed by the trailing edge of each timing pulse.

1.2.2.2 *Characteristics at the output ports* (see Table 2/G.703)

TABLE 2/G.703

Parameters	Data	Timing
Pulse shape	Nominally rectangular, with rise and fall times less than 1 μsec	Nominally rectangular, with rise and fall times less than 1 μsec
Nominal test load impedance	110 ohms resistive	110 ohms resistive
Peak voltage of a "mark" (pulse) (See Note 1)	a) 1.0 ± 0.1 V b) 3.4 ± 0.5 V	a) 1.0 ± 0.1 V b) 3.0 ± 0.5 V
Peak value of a "space" (no pulse) (See Note 1)	a) 0 ± 0.1 V b) 0 ± 0.5 V	a) 0 ± 0.1 V b) 0 ± 0.5 V
Nominal pulse width (See Note 1)	a) 15.6 μs b) 15.6 μs	a) 7.8 μs b) 9.8 to 10.9 μs
Maximum peak-to-peak jitter at the output port (Note 2)	Refer to § 2 of Recommendation G.823	

Note 1 – The choice between the set of parameters a) and b) allows for different office noise environments and different maximum cable lengths between the three involved office equipments.

Note 2 – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.

1.2.2.3 *Characteristics at the input ports*

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The varying parameters in Table 2/G.703 will allow typical maximum interconnecting distances of 350 to 450 m.

1.2.2.4 *Cable characteristics*

The transmission characteristics of the cable to be used are subject to further study.

1.2.3 *Electrical characteristics of 64-kbit/s contradirectional interface*

1.2.3.1 *General*

1.2.3.1.1 Bit rate: 64 kbit/s.

1.2.3.1.2 Maximum tolerance for signals to be transmitted through the interface: ± 100 ppm.

1.2.3.1.3 For each direction of transmission there should be two symmetrical pairs of wires, one pair carrying the data signal and the other carrying a composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.

Note – If there is a national requirement to provide a separate alarm signal across the interface, this can be done by cutting the 8-kHz timing signal for the transmission direction concerned, i.e., by inhibiting the code violations introduced in the corresponding composite timing signal (see below).

1.2.3.1.4 *Code conversion rules*

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64-kHz bit-timing information using AMI code with a 50% duty ratio and the 8-kHz octet-phase information by introducing violations of the code rule. The structures of the signals and their phase relationships at data output ports are shown in Figure 7/G.703.

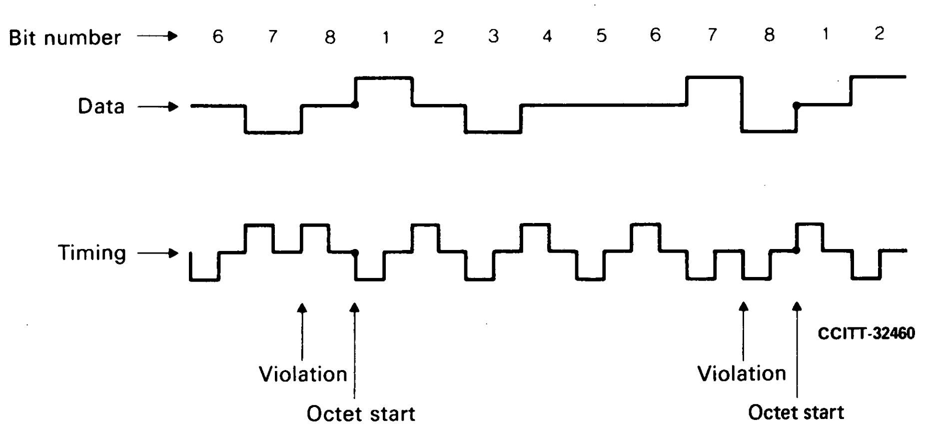


FIGURE 7/G.703

Signal structures of the 64-kbit/s contradirectional interface at data output ports

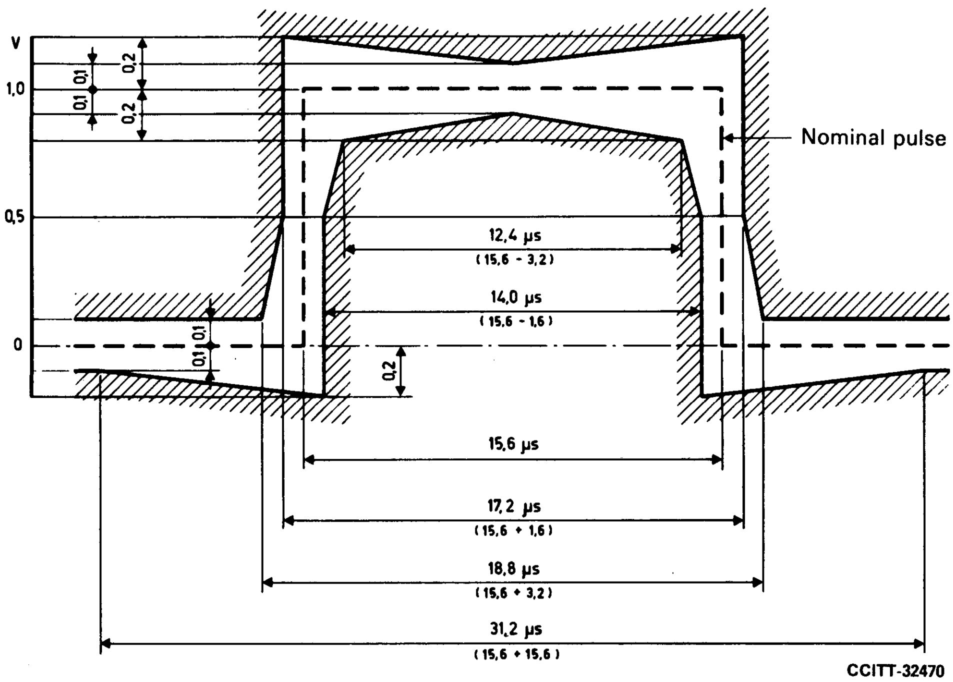
The data pulses received from the service (e.g. data or signalling) side of the interface will be somewhat delayed in relation to the corresponding timing pulses. The detection instant for a received data pulse on the line side (e.g. PCM) of the interface should therefore be at the leading edge of the next timing pulse.

1.2.3.1.5 *Specifications at the output ports* (see Table 3/G.703)

TABLE 3/G.703

Parameters	Data	Timing
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the mask in Figure 8/G.703 irrespective of the polarity	All pulses of a valid signal must conform to the mask in Figure 9/G.703, irrespective of the polarity
Pairs in each direction of transmission	One symmetric pair	One symmetric pair
Test load impedance	120 ohms resistive	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.1 V	0 V ± 0.1 V
Nominal pulse width	15.6 μs	7.8 μs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to § 2 of Recommendation G.823	

Note – For the time being these values are valid only for equipments of the 2 Mbit/s.



Note 1 – When one pulse is immediately followed by another pulse of the opposite polarity, the time limits at the zero-crossing between the pulses should be ± 0.8 μs.

Note 2 – The time instants at which a transition from one state to another in the data signal may occur are determined by the timing signal. On the service (e.g. data or signalling) side of the interface it is essential that these transitions are not initiated in advance of the timing instants given by the received timing signal.

FIGURE 8/6.703

Mask of the data pulse of the 64-kbit/s contradirectional interface

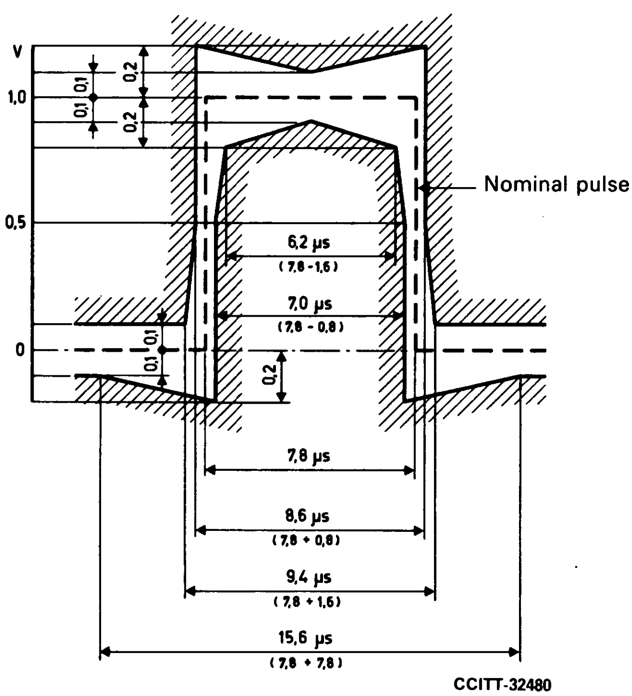


FIGURE 9/G.703

Mask of the timing pulse of the 64-kbit/s contradirectional interface

1.2.3.1.6 *Specifications at the input ports*

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 32 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The return loss at the input ports should have the following minimum values:

Frequency range (kHz)		Return loss (dB)
Data signal	Composite timing signal	
1.6 to 3.2	3.2 to 6.4	12
3.2 to 64	6.4 to 128	18
64 to 96	128 to 192	14

To provide nominal immunity against interference, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded as a 64 kbit/s contra-directional signal and having a pulse shape as defined in the pulse mask, shall have added to it an intefering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.152 (2^{11} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

Note 1 – The return loss specification for both the data signal and the composite timing signal input ports.

Note 2 – If the symmetrical pairs are screened, the screens shall be connected to the earth at the output port, and provision shall be made for connecting the screens of the symmetrical pairs to earth, if required, at the input port.

1.2.3.1.7 *Overvoltage protection requirement*

See Annex B.

2 Interface at 1544 kbit/s

2.1 Interconnection of 1544-kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

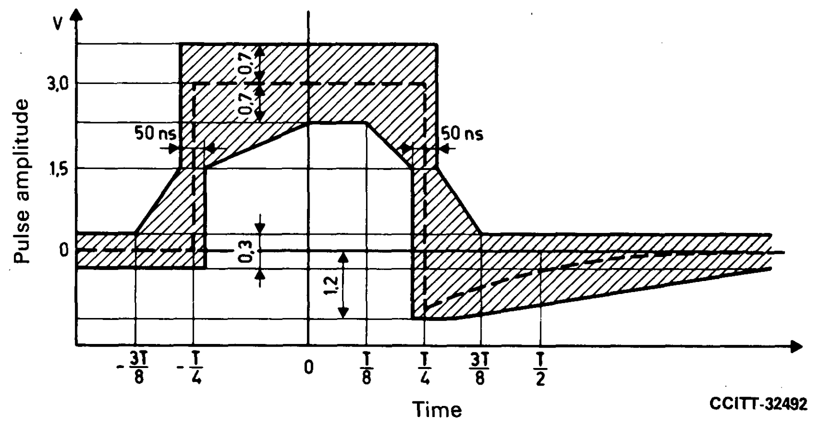
2.2 The signal shall have a bit rate of 1544 kbit/s ± 50 parts per million (ppm).

2.3 One symmetrical pair shall be used for each direction of transmission.

2.4 Test load impedance shall be 100 ohms, resistive.

2.5 An AMI (bipolar) code or B8ZS code shall be used. Connecting line systems require suitable signal content to guarantee adequate timing information. This can be accomplished either by use of B8ZS code, scrambling or by permitting not more than 15 spaces between successive marks and having an average mark density of at least 1 in 8.

2.6 The shape for an isolated pulse measured at the distribution frame shall fall within the mask in Figure 10/G.703 and meet the other requirements of Table 4/G.703. For pulse shapes within the mask, the peak undershoot should not exceed 40% of the peak pulse (mark).



T Time-slot width

FIGURE 10/G.703

Pulse mask for interface at 1544 kbit/s

2.7 The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 10/G.703 or ± 0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

TABLE 4/G.703

Digital interface at 1544 kbit/s [a)]

Location		Digital distribution frame
Bit rate		1544 kbit/s
Pair(s) in each direction of transmission		One symmetric pair
Code		AMI [b)] or B8ZS [c)]
Test load impedance		100 ohms resistive
Nominal pulse shape		Rectangular
Signal level [d)]	Power at 772 kHz	+12 dBm to +19 dBm
	Power at 1544 kHz	At least 25 dB below the power at 772 kHz

a) The pulse mask for 1st order digital interface is shown in Figure 10/G.703

b) See § 2.5 in the text.

c) See Annex A.

d) The signal level is the power level measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame for an all 1s pattern transmitted.

3 Interface at 6312 kbit/s

3.1 Interconnection of 6312 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

3.2 The signal shall have a bit rate of 6312 kbit/s ± 30 ppm.

3.3 One symmetrical pair of characteristic impedance of 110 ohms, or one coaxial pair of characteristic impedance of 75 ohms shall be used for each direction of transmission.

3.4 Test load impedance shall be 110 ohms resistive or 75 ohms resistive as appropriate.

3.5 A pseudo-ternary code shall be used as indicated in Table 5/G.703.

3.6 The shape for an isolated pulse measured at the distribution frame shall fall within the mask either of Figure 11/G.703 or of Figure 12/G.703 and meet the other requirements of Table 5/G.703.

3.7 The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 11/G.703, or ± 0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

TABLE 5/G.703

Digital interface at 6312 kbit/s [a)]

Location	Digital distribution frame	
Bit rate	6312 kbit/s	
Pair(s) in each direction of transmission	One symmetric pair	One coaxial pair
Code	B6ZS [b)]	B8ZS [b)]
Test load impedance	110 ohms resistive	75 ohms resistive
Nominal pulse shape [a)]	Rectangular, shaped by cable loss (see Figure 11/G.703)	Rectangular (see Figure 12/G.703)
Signal level	For an all 1s pattern transmitted, the power measured in a 3-kHz bandwidth should be as follows: 3156 kHz: 0.2 to 7.3 dBm 6312 kHz: −20 dBm or less	3156 kHz: 6.2 to 13.3 dBm 6312 kHz: −14 dBm or less

[a)] The pulse mask for 2nd order digital interface is shown in Figures 1/G.703 and 12/G.703.

[b)] See Annex A.

	T	Value of curve
Lower curve	$T \leqslant -0.41$ $-0.41 \leqslant T \leqslant 0.24$ $0.24 \leqslant T$	0 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.205}\right)\right]$ $0.331\, e^{-1.9\,(T-0.3)}$
Upper curve	$T \leqslant -0.72$ $-0.72 \leqslant T \leqslant 0.2$ $0.2 \leqslant T$	0 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.36}\right)\right]$ $0.1+0.72\, e^{-2.13\,(T-0.2)}$

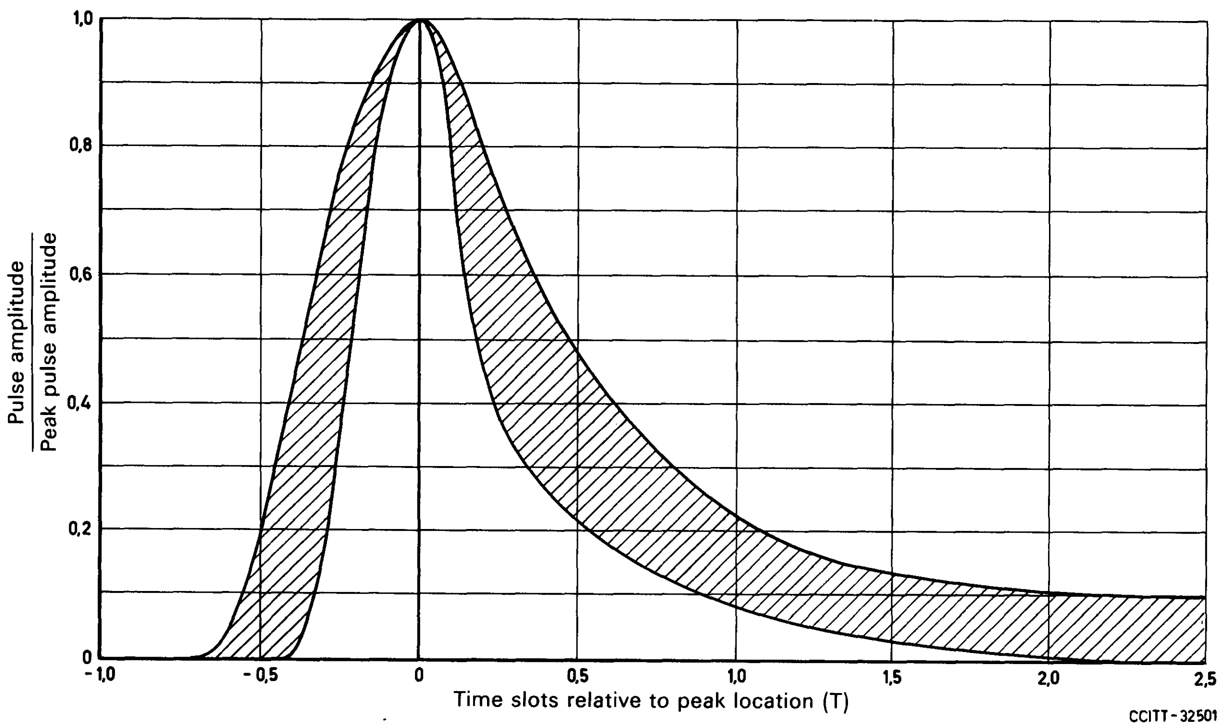
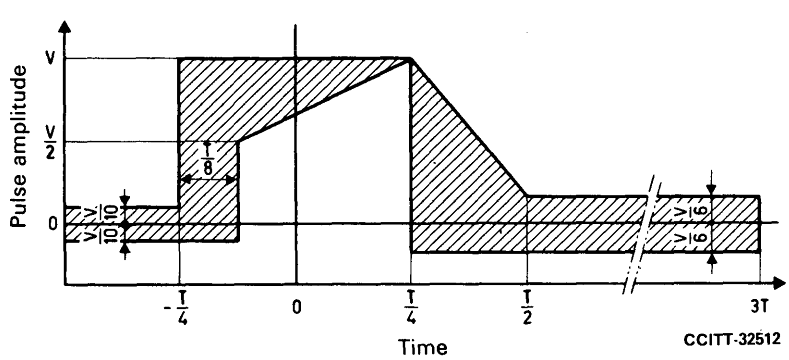


FIGURE 11/G.703

Pulse mask for the symmetric pair interface at 6312 kbit/s



T Time-slot width

FIGURE 12/G.703

Pulse mask for the coaxial pair interface at 6312 kbit/s

4 Interface at 32 064 kbit/s

4.1 Interconnection of 32 064 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

4.2 The signal shall have a bit rate of 32 064 kbit/s ± 10 ppm.

4.3 One coaxial pair shall be used for each direction of transmission.

4.4 The test load impedance shall be 75 ohms ± 5 per cent resistive and the test method shall be direct.

4.5 A scrambled AMI code shall be used.

4.6 The shape for an isolated pulse measured at the point where the signal arrives at the distribution frame shall fall within the mask in the Figure 13/G.703.

4.7 The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 13/G.703 or ± 0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

	T	Value of curve
Lower curve	$-0.36 \leqslant T < -0.30$	$5.76\,T + 2.07$
	$-0.30 \leqslant T < 0$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.25}\right)\right]$
	$0 \leqslant T < 0.22$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.16}\right)\right]$
	$0.22 \leqslant T$	$0.11\,e^{-3.42\,(T-0.3)}$
Upper curve	$-0.65 \leqslant T < 0$	$1.05\,[1 - e^{-4.6\,(T+0.65)}]$
	$0 \leqslant T < 0.25$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.28}\right)\right]$
	$0.25 \leqslant T$	$0.11 + 0.407\,e^{-2.1\,(T-0.29)}$

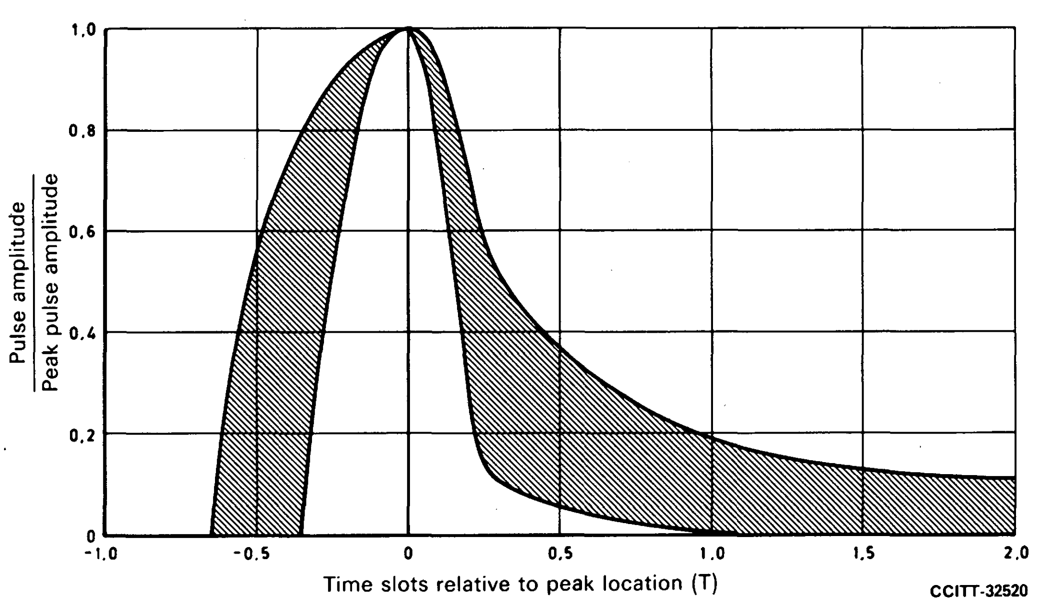


FIGURE 13/G.703

Pulse mask for the coaxial pair interface at 32064 kbit/s

4.8 For an all 1s pattern transmitted, the power measured in a 3-kHz bandwidth at the point where the signal arrives at the distribution frame shall be as follows:

16 032 kHz: +5 dBm to +12 dBm
32 064 kHz: at least 20 dB below the power at 16 032 kHz

4.9 The connectors and coaxial cable pairs in the distribution frame shall be 75 ohms ± 5 per cent.

5 Interface at 44 736 kbit/s

5.1 Interconnection of 44 736 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

5.2 The signal shall have a bit rate of 44 736 kbit/s ± 20 ppm.

The signal shall have a frame structure consistent with Recommendation G.752. Specifically, it shall contain the frame alignment bits F_0, F_{11}, F_{12} and the multi-frame alignment bits M_1 to M_7, as defined in Table 2/G.752.

5.3 One coaxial pair shall be used for each direction of transmission.

5.4 Test load impedance shall be 75 ohms ± 5 per cent resistive, and the test method shall be direct.

5.5 The B3ZS code shall be used. This code is defined in Annex A.

5.6 The transmitted pulses have a nominal 50 per cent duty cycle.

The shape for an isolated pulse measured at the point where the signal arrives at the distribution frame shall fall within the mask in Figure 14/G.703.

5.7 The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 14/G.703, or ± 0.05 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

5.8 For an all 1s pattern transmitted, the power measured in a 3-kHz bandwidth at the point where the signal arrives at the distribution frame shall be as follows:

22 368 kHz: −1.8 to +5.7 dBm
44 736 kHz: at least 20 dB below the power at 22 368 kHz

5.9 The digital distribution frame for 44 736 kbit/s signals shall have the characteristics specified in §§ 5.9.1 and 5.9.2 below.

5.9.1 The loss between the points where the signal arrives and leaves at the distribution frame shall be as follows:

0.60 ± 0.55 dB at 22 368 kHz
(comprised of any combination of flat and shaped losses).

5.9.2 The connectors and coaxial pair cables in the distribution frame shall be 75 ohms ± 5 per cent.

6 Interface at 2048 kbit/s

6.1 *General characteristics*

Bit rate: 2048 kbit/s ± 50 ppm
Code: HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirement: see Annex B.

6.2 *Specifications at the output ports* (see Table 6/G.703)

6.3 *Specifications at the input ports*

6.3.1 The digital signal presented at the input port shall be as defined above but modified by the characteristic of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 1024 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

6.3.2 For the jitter to be tolerated at the input port, refer to § 3 of Recommendation G.823.

	T	Value of curve
Lower curve	$T \leqslant -0.36$ $-0.36 \leqslant T \leqslant 0.28$ $0.28 \leqslant T$	0 $0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right]$ $0.11\ e^{-3.42\,(T - 0.3)}$
Upper curve	$T \leqslant -0.65$ $-0.65 \leqslant T \leqslant 0$ $0 \leqslant T \leqslant 0.36$ $0.36 \leqslant T$	0 $1.05\left[1 - e^{-4.6\,(T + 0.65)}\right]$ $0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right]$ $0.05 + 0.407\ e^{-1.84\,(T - 0.36)}$

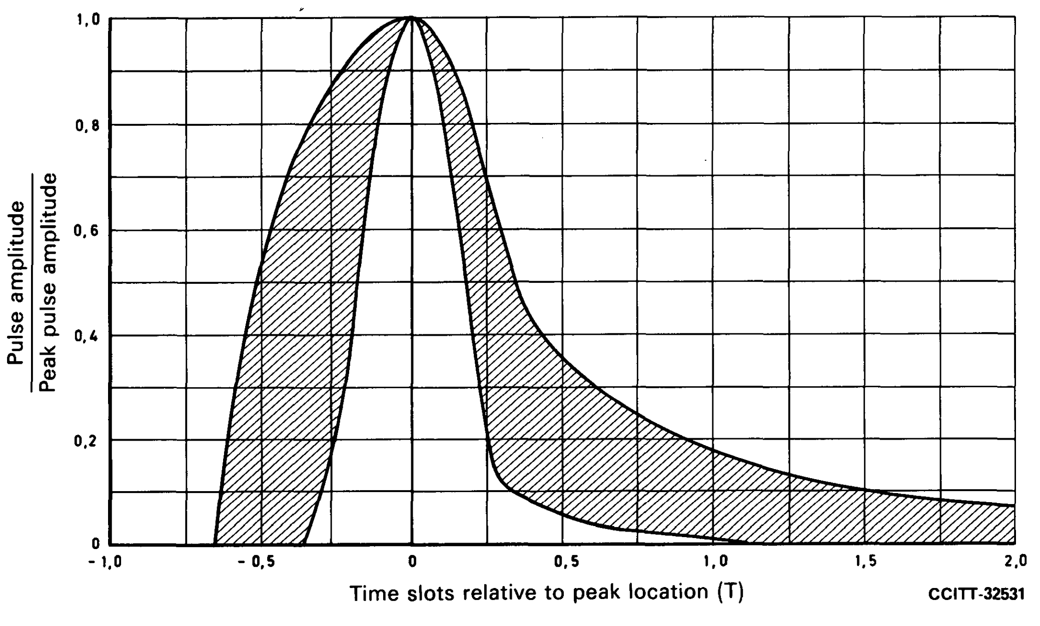


FIGURE 14/G.703

Pulse mask for the coaxial pair interface at 44 736 kbit/s

TABLE 6/G.703

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 15/G.703) irrespective of the sign. The value V corresponds to the nominal peak value	
Pair(s) in each direction	One coaxial pair (see § 6.4)	One symmetrical pair (see § 6.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	
Maximum peak-to-peak jitter at an output port	Refer to § 2 of Recommendation G.823	

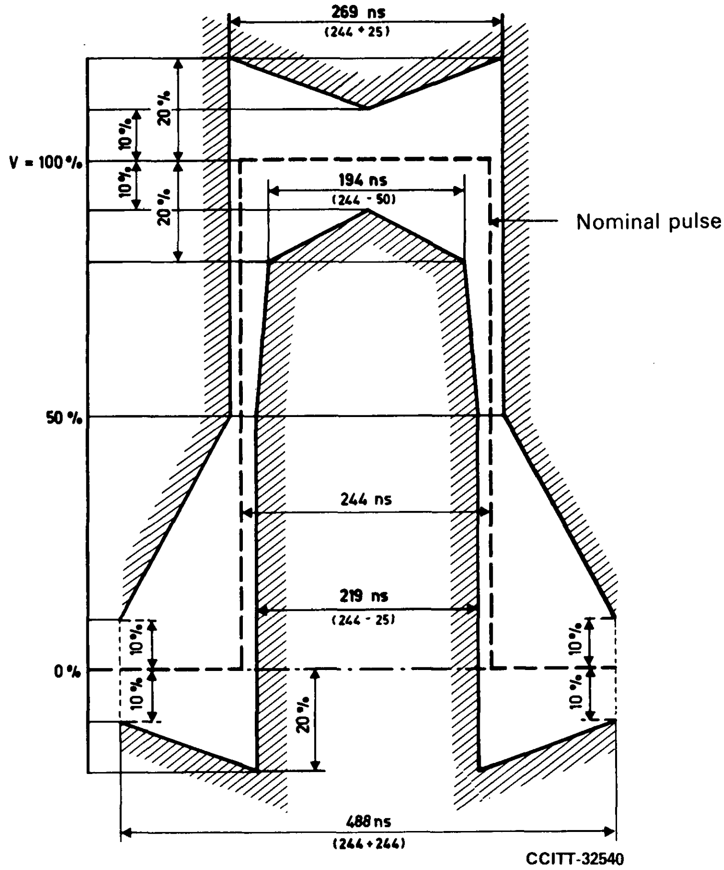
6.3.3 The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
51 to 102	12
102 to 2048	18
2048 to 3072	14

6.3.4 To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms (in the case of coaxial-pair interface) or 120 ohms (in the case of symmetrical-pair interface), to give a signal-to-interference ratio of 18 dB. The binary content of the interfering signal should comply with Recommendation O.151 (2^{15} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

Note – A receiver implementation providing an adaptive rather than a fixed threshold is considered to be more robust against reflections and should therefore be preferred.



Note – V corresponds to the nominal peak value.

FIGURE 15/G.703

Mask of the pulse at the 2048 kbit/s interface

6.4 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to the earth at the output port and provision shall be made for connecting the outer conductor of the coaxial pair or the screen of the symmetrical pair to earth if required, at the input port.

7 Interface at 8448 kbit/s

7.1 *General characteristics*

Bit rate: 8448 kbit/s ± 30 ppm
Code: HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirement: see Annex B.

7.2 *Specification at the output ports* (see Table 7/G.703)

TABLE 7/G.703

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (Figure 16/G.703) irrespective of the sign
Pair(s) in each direction	One coaxial pair (see § 7.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V
Peak voltage of a space (no pulse)	0 V ± 0.237 V
Nominal pulse width	59 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05
Ratio of widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to § 2 of Recommendation G.823

7.3 *Specifications at the input ports*

7.3.1 The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 4224 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

7.3.2 For the jitter to be tolerated at the input port, refer to § 3 of Recommendation G.823.

7.3.3 The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
211 to 422	12
422 to 8 448	18
8448 to 12 672	14

7.3.4 To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.151 ($2^{15} - 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

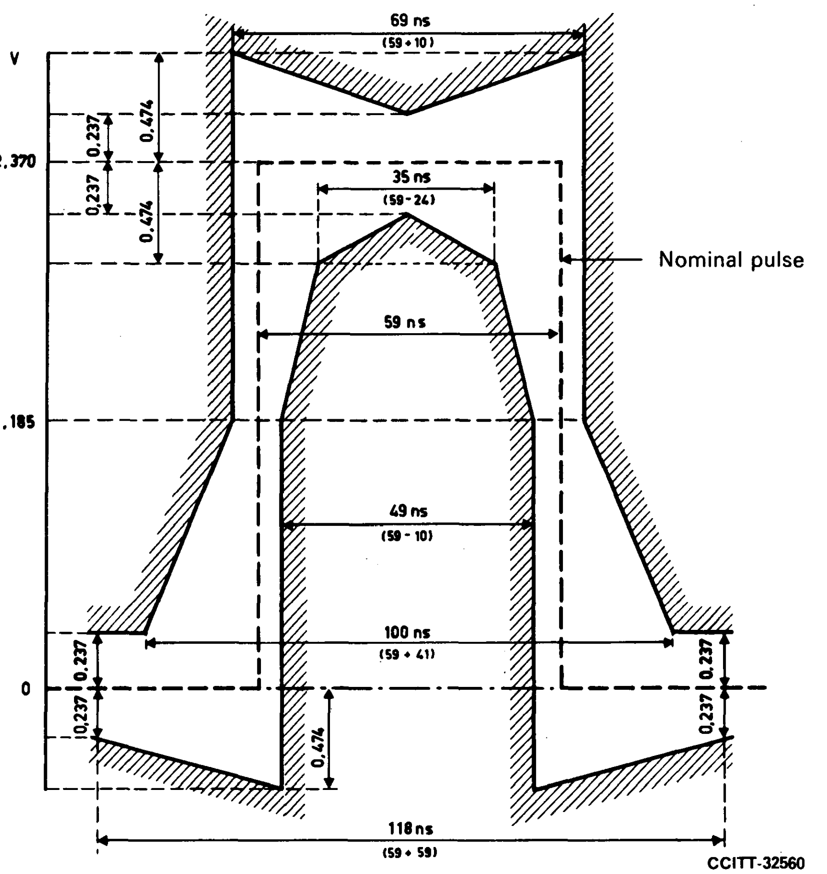


FIGURE 16/G.703

Pulse mask at the 8448-kbit/s interface

7.4 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair shall be connected to the earth at the output port, and provision shall be made for connecting this conductor to earth, if required, at the input port.

8 Interface at 34 368 kbit/s

8.1 *General characteristics*

Bit rate: 34 368 kbit/s ± 20 ppm
Code: HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirement: see Annex B.

8.2 *Specification at the output ports* (see Table 8/G.703)

8.3 *Specifications at the input ports*

8.3.1 The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pair. The attenuation of this cable shall be assumed to follow approximately a $\sqrt{f}$ law and the loss at a frequency of 17 184 kHz shall be in the range 0 to 12 dB.

8.3.2 For the jitter to be tolerated at the input port, refer to § 3 of Recommendation G.823.

8.3.3 The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
860 to 1 720	12
1 720 to 34 368	18
34 368 to 51 550	14

8.3.4 To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.151 ($2^{23} - 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

8.4 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair shall be connected to the earth at the output port, and provision shall be made for connecting this conductor to earth, if required, at the input port.

TABLE 8/G.703

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 17/G.703), irrespective of the sign
Pair(s) in each direction	One coaxial pair (see § 8.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V ± 0.1 V
Nominal pulse width	14.55 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to § 2 of Recommendation G.823

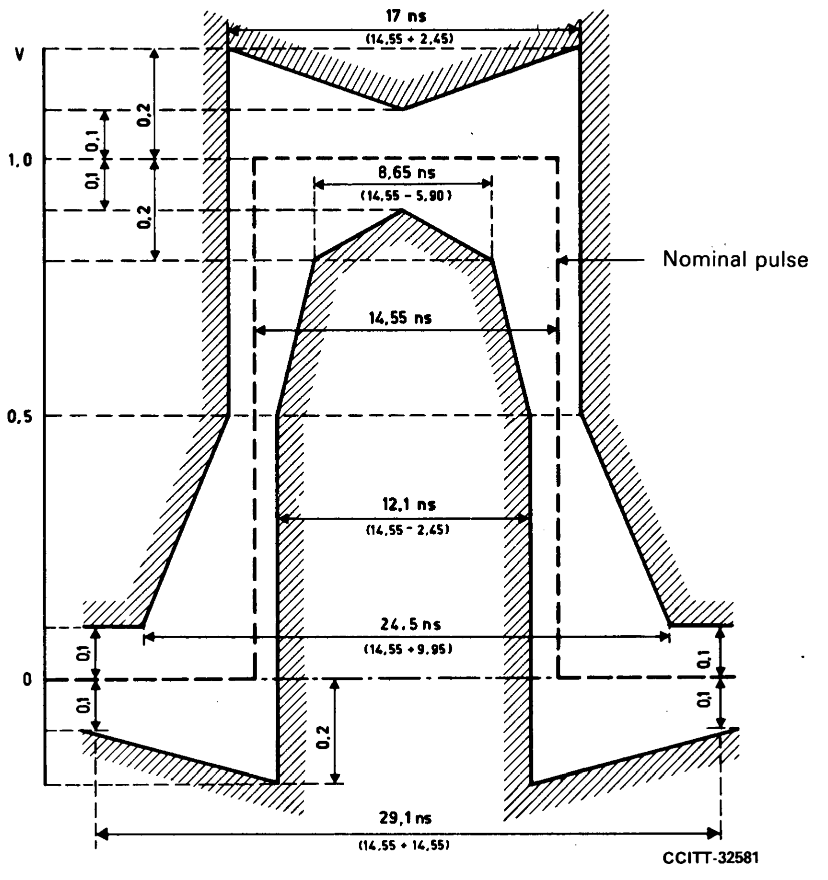


FIGURE 17/G.703

Pulse mask at the 34 368-kbit/s interface

9 Interface at 139 264 kbit/s

9.1 *General characteristics*

Bit rate: 139 264 kbit/s ± 15 ppm
Code: **coded mark inversion (CMI)**

Overvoltage protection requirement: see Annex B.

CMI is a 2-level non-return-to-zero code in which binary 0 is coded so that both amplitude levels, A_1 and A_2, are attained consecutively, each for half a unit time interval (T/2).

Binary 1 is coded by either of the amplitude levels A_1 or A_2, for one full unit time interval (T), in such a way that the level alternates for successive binary 1s.

An example is given in Figure 18/G.703.

Note 1 – For binary 0, there is always a positive transition at the midpoint of the binary unit time interval.

Note 2 – For binary 1,

a) there is a positive transition at the start of the binary unit time interval if the proceeding level was A_1;

b) there is a negative transition at the start of the binary unit time interval if the last binary 1 was encoded by level A_2.

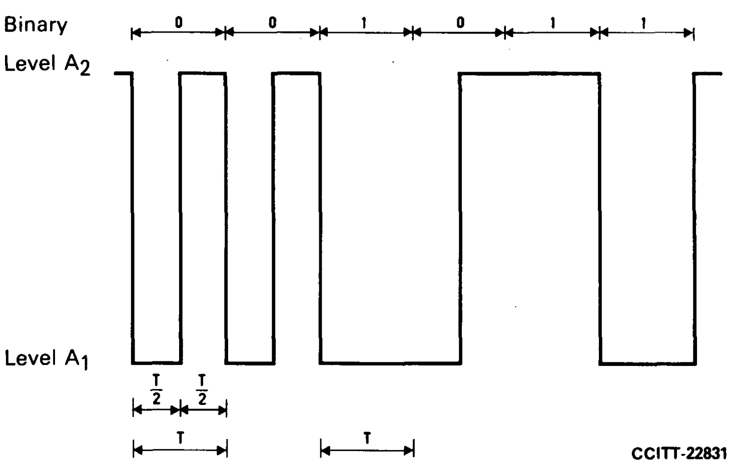


FIGURE 18/G.703
Example of CMI coded binary signal

9.2 *Specifications at the output ports* (see Table 9/G.703 and Figures 19/G.703 and 20/G.703)

Note 1 – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 9/G.703 have been met.

The relevant values are under study.

9.3 *Specifications at the input ports*

The digital signal presented at the input port should conform to Table 9/G.703 and Figures 19/G.703 and 20/G.703 modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12 dB at a frequency of 70 MHz.

For the jitter to be tolerated at the input port refer to § 3 of Recommendation G.823.

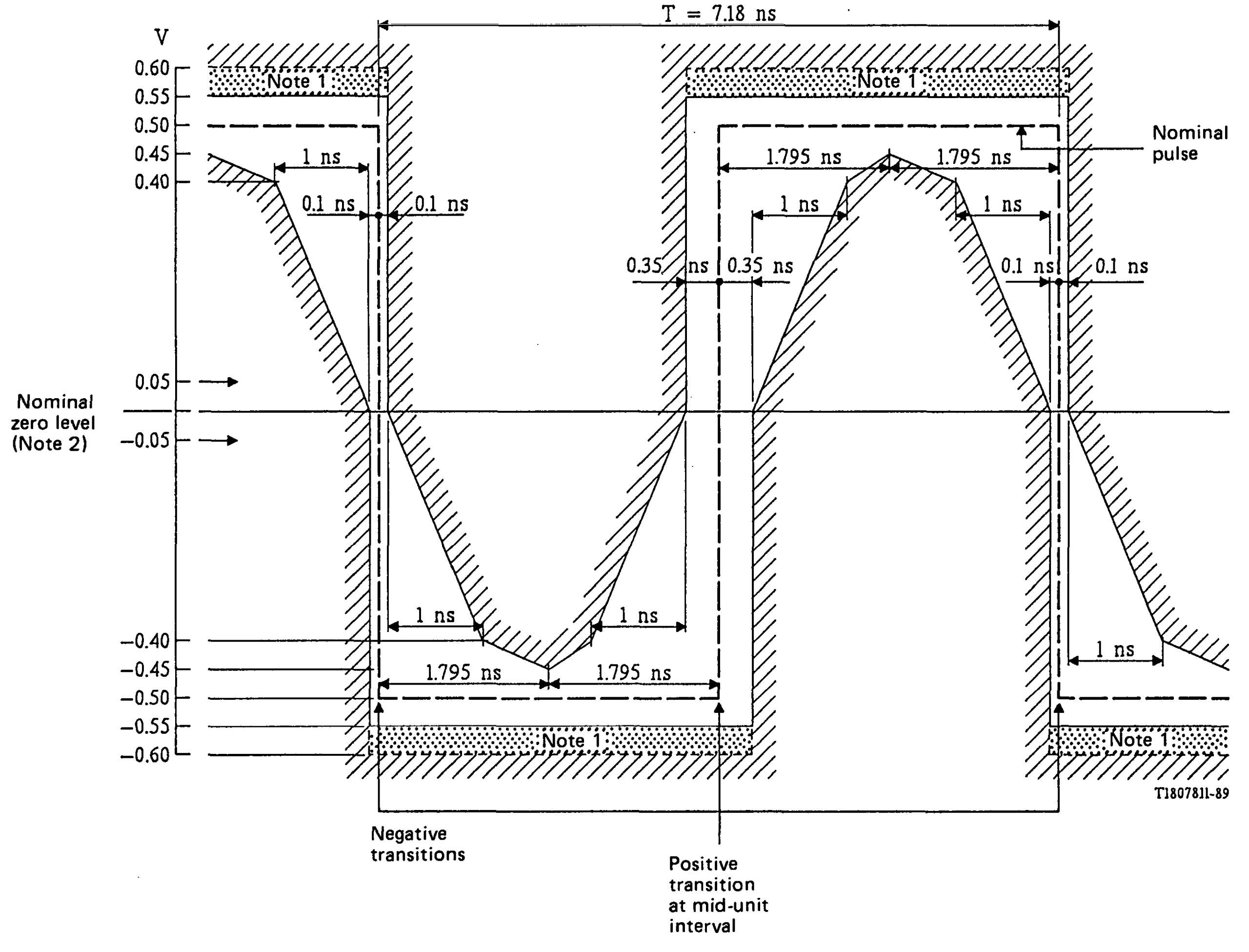
The return loss characteristics should be the same as that specified for the output port.

TABLE 9/G.703

Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 19/G.703 and 20/G.703
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	$\leqslant$ 2 ns
Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transitions)	Negative transitions: ± 0.1 ns Positive transitions at unit interval boundaries: ± 0.5 ns Positive transitions at mid-interval: ± 0.35 ns
Return loss	$\geqslant$ 15 dB over frequency range 7 MHz to 210 MHz
Maximum peak-to-peak jitter at an output port	Refer to § 2 of Recommendation G.823

9.4 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair shall be connected to the earth at the output port, and provision shall be made for connecting this conductor to earth, if required, at the input port.



Note 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

Note 2 – For all measurements using these masks, the signal should by AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.

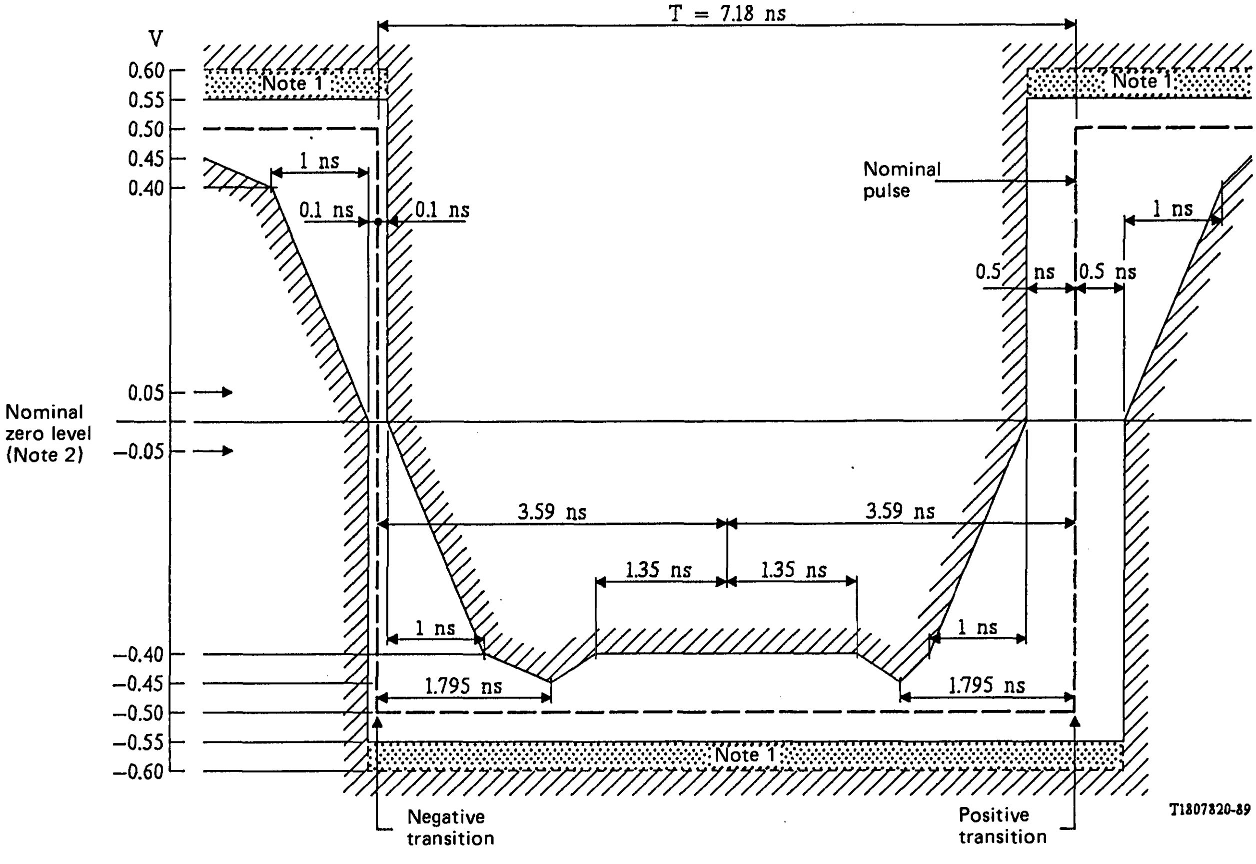
The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0.05 V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a 139 264 kHz timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all-0s and all-1s signals, respectively. (In practice, the signal may contain frame alignment bits per Rec. G.751.)

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between −0.4 V and 0.4 V, and should not exceed 2 ns.

FIGURE 19/G.703

Mask of a pulse corresponding to a binary 0



Note 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

Note 2 – For all measurements using these masks, the signal should by AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0.05 V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a 139 264 kHz timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all-0s and all-1s signals, respectively. (In practice, the signal may contain frame alignment bits per Rec. G.751.)

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between −0.4 V and 0.4 V, and should not exceed 2 ns.

Note 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the zero level of the negative and positive transitions are ± 0.1 ns and ± 0.5 ns respectively.

FIGURE 20/G.703

Mask of a pulse corresponding to a binary 1

10 2048 kHz synchronization interface

10.1 *General*

The use of this interface is recommended for all applications where it is required to synchronize a digital equipment by an external 2048 kHz synchronization signal.

Overvoltage protection requirement: see Annex B.

10.2 *Specifications at the output port* (see Table 10/G.703)

TABLE 10/G.703

Frequency	2048 kHz ± 50 ppm	
Pulse shape	The signal must conform with the mask (Figure 21/G.703) The value V corresponds to the maximum peak value The value V_l corresponds to the minimum peak value	
Type of pair	Coaxial pair (see Note in § 10.3)	Symmetrical pair (see Note in § 10.3)
Test load impedance	75 ohms resistive	120 ohms resistive
Maximum peak volatge (V_{op})	1.5	1.9
Minimum peak voltage (V_{op})	0.75	1.0
Maximum jitter at an output port	0.05 UI peak-to-peak, measured within the frequency range f_1 = 20 Hz to f_4 = 100 kHz (Note)	

Note – This value is valid for network timing distribution equipments. Other values may be specified for timing output ports of digital links carrying the network timing.

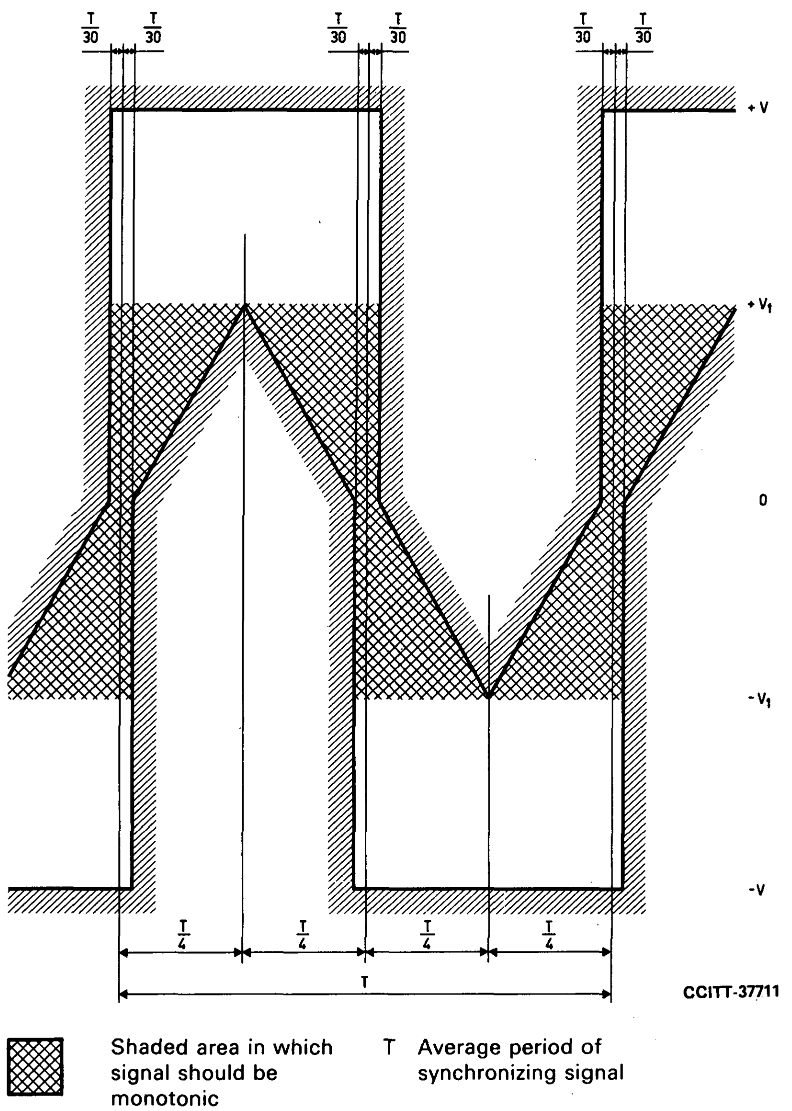


FIGURE 21/G.703

Wave shape at an output port

10.3 *Specifications at the input ports*

The signal presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 2048 kHz should be in the range 0 to 6 dB (minimum value). This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The input port shall be able to tolerate a digital signal with these electrical characteristics but modulated by jitter. The jitter values are under study.

The return loss at 2048 kHz should be $\geqslant$ 15 dB.

Note – The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to earth at the output port, and provision shall be made for connecting the outer conductor of the coaxial pair or the screen of the symmetrical pair to earth if required, at the input port.

11 Interface at 97 728 kbit/s

11.1 Interconnection of 97 728 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

11.2 The signal shall have a bit rate of 97 728 kbit/s + 10 ppm.

11.3 One coaxial pair shall be used for each direction of transmission.

11.4 The test load impedance shall be 75 ohms ± 5% resistive.

11.5 A scrambled AMI code[1)] shall be used.

11.6 The shape for the 97 728 kbit/s output port shall fall within the mask in Figure 22/G.703. The shape at the point where the signal arrives at the distribution frame will be modified by the characteristics of the interconnecting cable.

11.7 The connectors and cable pairs in the distribution frame shall be 75 ohms ± 5%.

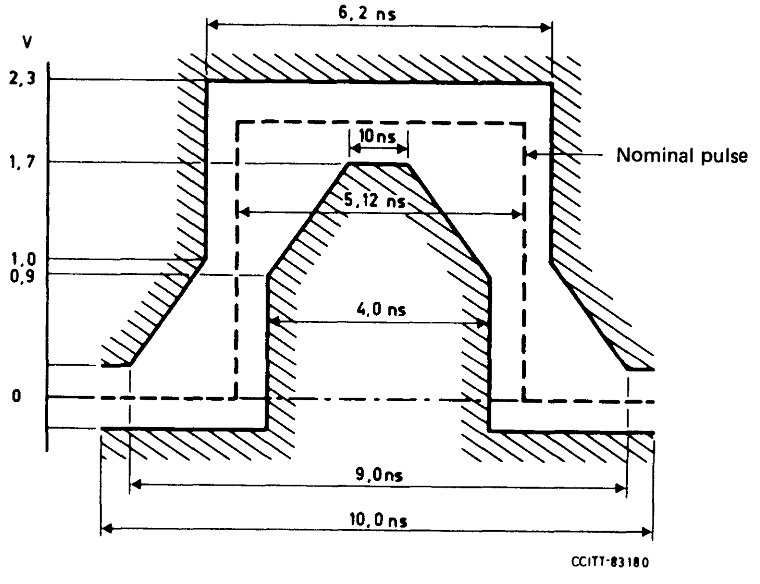


FIGURE 22/G.703

Pulse mask at the 97 728 kbit/s output port

ANNEX A

(to Recommendation G.703)

Definition of codes

This annex defines the modified alternate mark inversion codes (see Recommendation G.701, item 9005) whose use is specified in Recommendation G.703.

In these codes, binary 1 bits are generally represented by alternate positive and negative pulses, and binary 0 bits by spaces. Exceptions, as specified for the individual codes, are made when strings of successive 0 bits occur in the binary signal.

In the definitions below, B represents an inserted pulse conforming to the AMI rule (Rec. G.701, 9004), and V represents an AMI violation (Rec. G.701, 9007).

The encoding of binary signals in accordance with the rules given in this annex includes frame alignment bits, etc.

---

1) An AMI code is scrambled by a five-stage reset-type scrambler with the primitive polynominal of $x^5 + x^3 + 1$.

A.1 *Definition of B3ZS (also designated HDB2) and HDB3*

Each block of 3 (or 4) successive zeros is replaced by 00V (or 000V respectively) or B0V (B00V). The choice of 00V (000V) or B0V (B00V) is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no d.c. component is introduced.

Note – The abbreviations stand for the following:

HDB2 (HDB3) high density bipolar of order 2 (3)

B3ZS bipolar with three-zero substitution.

A.2 *Definition of B6ZS and B8ZS*

Each block of 6 (or 8) successive zeros is replaced by 0VB0VB (or 000VB0VB respectively).

ANNEX B

(to Recommendation G.703)

Specification of the overvoltage protection requirement

The input and output ports should withstand without damage the following tests:

- 10 standard lightning impulses (1.2/50 μs) with a maximum amplitude of U (5 negative and 5 positive impulses). For the definition of this impulse see Ref. [1].
- at the interface for coaxial pairs:
  i) differential mode: with a pulse generator of Figure B-1/G.703, the value of U is under study;
  ii) common mode – under study;
- at the interface for symmetrical pairs:
  i) differential mode: with a pulse generator of Figure B-1/G.703, the value of U is under study (a value of 20 V has been mentioned);
  ii) common mode: with a pulse generator of Figure B-2/G.703, U = 100 V_{dc};

Possible pulse generators are described in Figures B-1/G.703 and B-2/G.703.

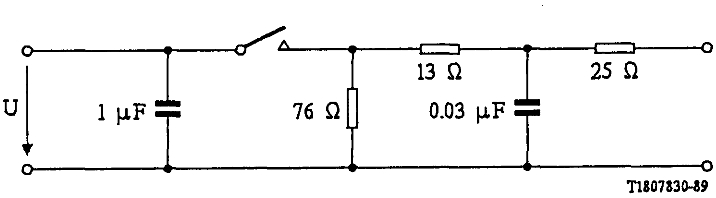


FIGURE B-1/G.703

Pulse generator 1.2/50 μs for differential mode voltages

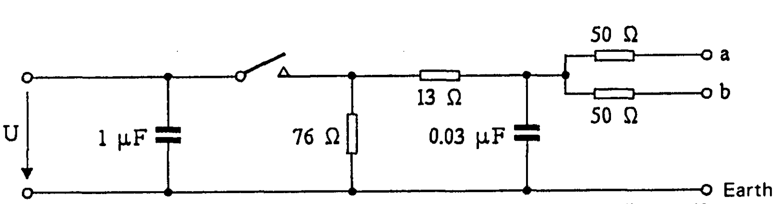


FIGURE B-2/G.703

Pulse generator 1.2/50 μs for common mode voltages at symmetrical interfaces

References

[1] IEC publication No. 60-2 *High-voltage test techniques, Part 2: Test procedures*, Geneva, 1973.

SYNCHRONOUS FRAME STRUCTURES USED AT PRIMARY AND SECONDARY HIERARCHICAL LEVELS

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

1 General

This Recommendation gives functional characteristics of interfaces associated with:

- network nodes, in particular, synchronous digital multiplex equipment and digital exchanges in IDNs for telephony and ISDNs, and
- PCM multiplexing equipment.

Paragraph 2 deals with basic frame structures, including details of frame length, frame alignment signals, cyclic redundancy check (CRC) procedures and other basic information.

Paragraphs 3 to 6 contain more specific information about how certain channels at 64 kbit/s and at other bit rates are accomodated within the basic frame structures described in § 2.

Electrical characteristics for these interfaces are defined in Recommendation G.703.

Note 1 – This Recommendation does not necessarily apply to those cases where the signals that cross the interfaces are devoted to non-switched connections, such as those for the transport of encoded wideband signals (e.g. broadcast TV signals or multiplexed sound-programme signals which need not be individually routed via the ISDN), see also Annex A to Recommendation G.702.

Note 2 – The frame structures recommended in this Recommendation do not apply to certain maintenance signals, such as the all 1s signals transmitted during fault conditions or other signals transmitted during out-of-service conditions.

Note 3 – Frame structures associated with digital multiplexing equipments using justification are covered in each corresponding equipment Recommendation.

Note 4 – Inclusion of channel structures at other bit rates than 64 kbit/s is a matter for further study. Recommendations G.761 and G.763 dealing with the characteristics of PCM/ADPCM transcoding equipment contain information about channel structures at 32 kbit/s. The more general use of those particular structures is a subject of further study.

2 Basic frame structures

2.1 *Basic frame structure at 1544 kbit/s*

2.1.1 *Frame length*:

193 bits, numbered 1 to 193. The frame repetition rate is 8000 Hz.

2.1.2 *F-bit*

The first bit of a frame is designated an F-bit, and is used for such purposes as frame alignment, performance monitoring and providing a data link.

2.1.3 *Allocation of F-bit*

Two alternative methods as given in Tables 1/G.704 and 2/G.704 for allocation of F-bits are recommended.

TABLE 1/G.704

Multiframe structure for the 24 frame multiframe

Frame number within multiframe	F-bit				Bit number(s) in each channel time slot		Signalling channel designation a)
	Bit number within multiframe	Assignements					
		FAS	DL	CRC	For character signal a)	For signalling a)	
1	1	–	m	–	1-8	–	
2	194	–	–	e_1	1-8	–	
3	387	–	m	–	1-8	–	
4	580	0	–	–	1-8	–	
5	773	–	m	–	1-8	–	
6	966	–	–	e_2	1-7	8	A
7	1159	–	m	–	1-8	–	
8	1352	0	–	–	1-8	–	
9	1545	–	m	–	1-8	–	
10	1738	–	–	e_3	1-8	–	
11	1931	–	m	–	1-8	–	
12	2124	1	–	–	1-7	8	B
13	2317	–	m	–	1-8	–	
14	2510	–	–	e_4	1-8	–	
15	2703	–	m	–	1-8	–	
16	2896	0	–	–	1-8	–	
17	3089	–	m	–	1-8	–	
18	3282	–	–	e_5	1-7	8	C
19	3475	–	m	–	1-8	–	
20	3668	1	–	–	1-8	–	
21	3861	–	m	–	1-8	–	
22	4054	–	–	e_6	1-8	–	
23	4247	–	m	–	1-8	–	
24	4440	1	–	–	1-7	8	D

FAS Frame alignement signal (... 001011 ...).

DL 4 kbit/s data link (message bits m).

CRC CRC-6 (block check field (check bits $e_1 \dots e_6$).

a) Only applicable in the case of channel associated signalling see (§ 3.1.3.2.)

TABLE 2/G.704

Allocation of F-bit for the 12-frame multiframe

Frame number	Frame alignment signal	Multiframe alignment signal or signalling
1	1	–
2	–	S
3	0	–
4	–	S

Note – For multiframe structure, see § 3.1.3.2.2.

2.1.3.1 *Method 1: Twenty-four-frame multiframe*

Allocation of the F-bit to the multiframe alignment signal, the CRC check bits and the data link is given in Table 1/G.704.

2.1.3.1.1 *Multiframe alignment signal*

The F-bit of every fourth frame forms the pattern 001011 ... 001011. This multiframe alignment signal is used to identify where each particular frame is located within the multiframe in order to extract the cyclic redundancy check code, CRC-6, and the data link information, as well as to identify those frames that contain signalling (frames 6, 12, 18 and 24), if channel associated signalling is used.

2.1.3.1.2 *Cyclic redundancy check*

The CRC-6 is a method of performance monitoring that is contained within the F-bit position of frames 2, 6, 10, 14 18 and 22 of every multiframe (see Table 1/G.704).

The CRC-6 message block check bits e_1, e_2, e_3, e_4, e_5, and e_6 are contained within multiframe bits 194, 966, 1738, 2510, 3282 and 4054 respectively, as shown in Table 1/G.704. The CRC-6 Message Block (CMB) is a sequence of 4632 serial bits that is coincident with a multiframe. By definition, CMB N begins at bit position 1 of multiframe N and ends at bit position 4632 of multiframe N. The first transmitted CRC bit of a multiframe is the most significant bit of the CMB polynomial.

In calculating the CRC-6 bits, the F-bits are replaced by binary 1s. All information in the other bit positions will be identical to the information in the corresponding multiframe bit positions.

The check-bit sequence e_1 through e_6 transmitted in multiframe $N+1$, is the remainder after multiplication by x^6 and then division (modulo-2) by the generator polynomial x^6+x+1 of the polynomial corresponding to CMB N. The first check bit (e_1) is the most significant bit of the remainder; the last check bit (e_6) is the least significant bit of the remainder. Each multiframe contains the CRC-6 check bits generated for the preceding CMB.

At the receiver, the received CMB, with each F-bit having first been replaced by a binary 1, is acted upon by the multiplication/division process described above. The resulting remainder is compared on a bit-by-bit basis, with the CRC-6 check bits contained in the subsequently received multiframe. The compared check bits will be identical in the absence of transmission errors.

2.1.3.1.3 *4 kbit/s data link*

Beginning with frame 1 of the multiframe (see Table 1/G.704) the first bit of every other frame is part of the 4 kbit/s data link. This data link provides a communication path between primary hierarchical level terminals and will contain data, an idle data link sequence or a loss of frame alignment alarm sequence.

The format to be used for the transmission of data over the *m*-bits of the data link is still under study.

The idle data link pattern is also under study.

A loss of frame alignment alarm sequence is used when a loss of frame alignment (LFA) condition has been detected. After a loss of frame alignment condition is detectd at local end A, a 16-bit LFA sequence of eight 1s eight 0s (1111111100000000) will be transmitted in the *m*-bits of the 4 kbit/s data link continuously to remote end B.

2.1.3.2 *Method 2: Twelve-frame multiframe*

Allocation of the F-bit to the frame alignment signal, multiframe alignment signal and signalling is given in Table 2/G.704.

2.2 *Basic frame structure at 6312 kbit/s*

2.2.1 *Frame length*

The number of bits per frame is 789. The frame repetition rate is 8000 Hz.

2.2.2 *F-bits*

The last five bits of a frame are designated as F-bits, and are used for such purposes as frame alignment, performance monitoring and providing a data link.

2.2.3 *Allocation of F-bits*

Allocation of the F-bits is given in Table 3/G.704.

TABLE 3/G.704

Allocation of F-bits

Frame number	Bit number				
	785	786	787	788	789
1	1	1	0	0	m
2	1	0	1	0	0
3	x	x	x	a	m
4	e_1	e_2	e_3	e_4	e_5

m Data link bit.

a Remote end alarm bit (1 state = alarm, 0 state = no alarm).

e_i CRC-5 check bit (i = 1 to 5).

x Spare bits, to be set at state 1 if not used.

2.2.3.1 *Frame alignment signal*

The frame and multiframe alignment signal is 110010100, and is carried on the F-bits in frames 1 and 2, excluding bit 789 of frame 1.

2.2.3.2 *Cyclic redundancy check*

The cyclic redundancy check 5 (CRC-5) message block (CMB) is a sequence of 3151 serial bits which starts at bit number 1 of frame number 1 and ends at bit number 784 of frame number 4. The CRC-5 message block check bits e_1, e_2, e_3, e_4 and e_5 occupy the last five bits of the multiframe as shown in Table 3/G.704.

The check-bit sequence e_1 through e_5 transmitted in multiframe N is the remainder after multiplication by x^5 and then division (modulo-2) by the generator polynomial $x^5+x^4+x^2+1$ of the polynomial corresponding to CMB N. The first check bit (e_1) is the most significant bit of the remainder; the last check bit (e_5) is the least significant bit of the remainder. Each multiframe contains the CRC-5 check bits generated for the corresponding CMB.

At the receiver the incoming sequence of 3156 serial bits (i.e. 3151 bits of CMB and 5 CRC bits), when divided by the generator polynomials, will result in a remainder of 00000 in the absence of transmission errors.

2.2.3.3 *4 kbit/s data link*

The bit m shown in Table 3/G.704 is used as a data link bit. These bits provide 4 kbit/s data transmission capability associated with the 6312 kbit/s digital path.

2.2.3.4 *Remote end alarm indication*

After a loss of frame alignment condition is detected at local end A, remote end alarm signal bit a, shown in Table 3/G.704, will be transmitted to remote end B.

2.3 *Basic frame structure at 2048 kbit/s*

2.3.1 *Frame length*

256 bits, numbered 1 to 256. The frame repetition rate is 8000 Hz.

2.3.2 *Allocation of bits number 1 to 8 of the frame*

Allocation of bits number 1 to 8 of the frame is shown in Table 4a/G.704.

TABLE 4a/G.704

Allocation of bits 1 to 8 of the frame

Alternate frames \ Bit number	1	2	3	4	5	6	7	8
Frame containing the frame alignment signal	S_i	0	0	1	1	0	1	1
	Note 1	Frame alignment signal						
Frame not containing the frame alignment signal	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	Note 1	Note 2	Note 3	Note 4				

Note 1 – S_i = bits reserved for international use. One specific use is described in § 2.3.3. Other possible uses may be defined at a later stage. If no use is realized, these bits should be fixed at 1 on digital paths crossing an international border. However, they may be used nationally if the digital path does not cross a border.

Note 2 – This bit is fixed at 1 to assist in avoiding simulations of the frame alignement signal.

Note 3 – A = Remote alarm indication. In undisturbed operation, set to 0; in alarm condition, set to 1.

Note 4 – S_{a4} to S_{a8} = Additional spare bits whose use may be as follows:

i) Bits S_{a4} to S_{a8} may be recommended by CCITT for use in specific point-to-point applications (e.g. transcoder equipments conforming to Recommendation G.761;

ii) Bit S_{a4} may be recommended by CCITT as a message-based data link for operations, maintenance and performance monitoring. This channel originates at the point where the frame is generated and terminates where the frame is split up. This requires further study;

iii) Bits S_{a5} to S_{a7} are for national usage where there is no demand on them for specific point-to-point applications (see i) above.

Bits S_{a4} to S_{a8} (where these are not used) should be set to 1 on links crossing an international border.

2.3.3 *Description of the CRC-4 procedure in bit 1 of the frame*

2.3.3.1 *Special use of bit 1 of the frame*

Where there is a need to provide additional protection against simulation of the frame alignment signal, and/or where there is a need for an enhanced error monitoring capability, then bit 1 should be used for a Cyclic Redundancy Check-4 (CRC-4) procedure as detailed below.

Note – Equipment incorporating the CRC-4 procedure should be designed to be capable of interworking with equipment which does not incorporate the CRC procedure, with the option being manually selectable (e.g. by straps). For such interworking, bit 1 of the frame should be fixed at 1 in both directions (see Table 4a/G.704, Note 1).

2.3.3.2 The allocation of bits 1 to 8 of the frame is shown in Table 4b/G.704 for a complete CRC-4 multiframe.

TABLE 4b/G.704

CRC-4 multiframe structure

	Sub-multiframe (SMF)	Frame number	Bits 1 to 8 of the frame							
			1	2	3	4	5	6	7	8
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

Note 1 – E = CRC-4 error indication bits (see § 2.3.3.4).

Note 2 – S_{a4} to S_{a8} = Spare bits (see Note 4 to Table 4a/G.704).

Note 3 – C_1 to C_4 = Cyclic Redundancy Check-4 (CRC-4) bits (see §§ 2.3.3.4 and 2.3.3.5).

Note 4 – A = Remote alarm indication (see Table 4a/G.704).

2.3.3.3 Each CRC-4 multiframe, which is composed of 16 frames numbered 0 to 15, is divided into two 8-frame sub-multiframes (SMF), designated SMF I and SMF II which signifies their respective order of occurrence within the CRC-4 multiframe structure. The SMF is the Cyclic Redundancy Check-4 (CRC-4) block size (i.e. 2048 bits).

The CRC-4 multiframe structure is not related to the possible use of a multiframe structure in 64 kbit/s channel time slot 16 (see § 5.1.3.2).

2.3.3.4 *Use of bit 1 in 2048 kbit/s CRC-4 multiframe*

In those frames containing the frame alignment signal (defined in § 2.3.2), bit 1 is used to transmit the CRC-4 bits. There are four CRC-4 bits, designated C_1, C_2, C_3 and C_4 in each SMF.

In those frames not containing the frame alignment signal (see § 2.3.2), bit 1 is used to transmit the 6-bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E).

The CRC multiframe alignment signal has the form 001011.

The E-bits should be used to indicate received errored sub-multiframes by setting the binary state of one E-bit from 1 to 0 for each errored sub-multiframe. Any delay between the detection of an errored sub-multiframe and the setting of the E-bit that indicates the error state must be less than 1 second.

Note 1 – The E-bits will always be taken into account even if the SMF which contains them is found to be errored, since there is little likelihood that the E-bits themselves will be errored.

Note 2 – In the short term, there may exist equipments which do not use the E-bits; in this case the E-bits are set to binary 1.

2.3.3.5 *Cyclic Redundancy Check*

2.3.3.5.1 *Multiplication/division process*

A particular CRC-4 word, located in sub-multiframe N, is the remainder after multiplication by x^4 and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of sub-multiframe $N - 1$).

Note – When representing the contents of the check block as a polynomial, the first bit in the block, i.e. frame 0, bit 1 or frame 8, bit 1, should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_4 the least significant bit of the remainder.

2.3.3.5.2 *Encoding procedure*

i) The CRC-4 bits in the SMF are replaced by binary 0s.

ii) The SMF is then acted upon by the multiplication/division process referred to in § 2.3.3.5.1.

iii) The remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

Note – The CRC-4 bits thus generated do not affect the result of the multiplication/division process in the next SMF because, as indicated in i) above, the CRC-4 bit positions in an SMF are initially set to 0 during the multiplication/division process.

2.3.3.5.3 *Decoding procedure*

i) A received SMF is acted upon by the multiplication/division process referred to in § 2.3.3.5.1, after having its CRC-4 bits extracted and replaced by 0s.

ii) The remainder resulting from this division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.

iii) If the remainder calculated in the decoder exactly corresponds to the CRC-4 bits received in the next SMF, it is assumed that the checked SMF is error free.

2.4 *Basic frame structure at 8448 kbit/s*

2.4.1 *Frame length*

The number of bits per frame is 1056. They are numbered from 1 to 1056. The frame repetition rate is 8000 Hz.

2.4.2 *Frame alignment signal*

The frame alignment signal is 11100110 100000 and occupies the bit-positions 1 to 8 and 529 to 534.

2.4.3 *Service digits*

Bit 535 is used to convey alarm indication (bit 535 at 1 state – alarm; bits 535 at 0 state = no alarm).

Bit 536 is left free for national use and should be fixed at 1 on paths crossing the international border. The same applies to bits 9-40 in the case of channel-associated signalling.

3 Characteristics of frame structure carrying channels at various bit rates in 1544 kbit/s

3.1 *Interface at 1544 kbit/s carrying 64 kbit/s channels*

3.1.1 *Frame structure*

3.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

3.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 2 to 193 in the basic frame carry 24 octet interleaved 64 kbit/s channel time slots, numbered 1 to 24.

3.1.1.3 *Allocation of F-bit*

Refer to § 2.1.3.

3.1.2 *Use of 64 kbit/s channel time slots*

Each 64 kbit/s channel time slot can accommodate e.g., a PCM encoded voiceband signal conforming to Rec. G.711 or data information with a bit rate up to 64 kbit/s.

3.1.3 *Signalling*

Two alternative methods as given in §§ 3.1.3.1 and 3.1.3.2 are recommended:

3.1.3.1 *Common channel signalling*

One 64 kbit/s channel time slot is used to provide common channel signalling at a rate of 64 kbit/s. In the case of the 12-frame multiframe method of § 2.1.3.2, the pattern of the S-bit may be arranged to carry common channel signalling at a rate of 4 kbit/s or a sub-multiple of this rate.

3.1.3.2 *Channel associated signalling*

3.1.3.2.1 *Allocation of signalling bits for the 24-frame multiframe*

As can be seen in Table 1/G.704, there are four different signalling bits (A, B, C and D) in the multiframe. This channel associated signalling can provide four independent 333-bit/s signalling channels designated A, B, C and D, two independent 667-bit/s signalling channels designated A and B (see Note,) or one 1333-bit/s signalling channel.

Note – When only four state signalling is required, the A, B signalling bits previously associated with frames 6 and 12 respectively should be mapped into the A, B, C, D signalling bits of frames 6, 12, 18 and 24 respectively as follows: A = A, B = B, C = A, D = B. In this case the ABCD signalling is the same as the AB signalling specified in § 3.1.3.2.2.

3.1.3.2.2 *Allocation of signalling bits for the 12-frame multiframe*

Based on agreement between the Administrations involved, channel-associated signalling is provided for intra-regional circuits according to the following arrangement:

A multiframe comprises 12 frames as shown in Table 5/G.704. The multiframe alignment signal is carried on the S-bit as shown in the table.

Frames 6 and 12 are designated as signalling frames. The eight bit in each channel time slot is used in every signalling frame to carry the signalling associated with that channel.

TABLE 5/G.704

Multiframe structure

Frame number	Frame alignment signal (see Note 1)	Multiframe alignment signal (S bit)	Bit number(s) in each channel time slot		Signalling channel designation (see Note 2)
			For character signal	For signalling	
1	1	–	1-8	–	
2	–	0	1-8	–	
3	0	–	1-8	–	
4	–	0	1-8	–	
5	1	–	1-8	–	
6	–	1	1-7	8	A
7	0	–	1-8	–	
8	–	1	1-8	–	
9	1	–	1-8	–	
10	–	1	1-8	–	
11	0	–	1-8	–	
12	–	0	1-7	8	B

Note 1 – When the S-bit is modified to signal the alarm indications to the remote end, the S-bit in frame 12 is changed from state 0 to 1.

Note 2 – Channel associated signalling provides two independent 667-bit/s signalling channels designated A and B or one 1333-bit/s signalling channel.

3.2 *Interface at 1544 kbit/s carrying 32 kbit/s channel time slots* (see Note)

Note – This interface provides for the carrying of 32 kbit/s information. The interface will be used between network nodes and will apply to primary rate multiplexing equipment, digital cross-connect equipment, transcoder and other equipment relevant to the network nodes. Switching in this case is assumed to take place on a 64 kbit/s basis.

3.2.1 *Frame structure*

3.2.1.1 *Number of bits per 32 kbit/s channel time slot*

Four, numbered 1 to 4.

3.2.1.2 *Number of 32 kbit/s channel time slots per frame*

Bits 2 to 193 in the basic frame can carry forty-eight 4-bit interleaved 32 kbit/s channel time slots, numbered 1 to 48.

3.2.1.3 *Allocation of F-bits*

Refer to § 2.1.3.

3.2.2 *Use of 32 kbit/s channel time slot*

Each 32 kbit/s channel time slot can accomodate an ADPCM-encoded voiceband signal conforming to Rec. G.721, or data with a bit rate up to 32 kbit/s.

3.2.3 *384 kbit/s 12-channel time slot grouping*

3.2.3.1 *Structure of 12-channel time slot grouping*

The 1544 kbit/s frame for 32 kbit/s channel time slots shown in Table 6/G.704 is structured to provide four independent 384 kbit/s 12-channel time slot groupings. These are numbered 1-4, and transmitted in numbered order starting with time slot grouping number 1.

The signalling grouping channels (SGC) for time slot groupings 1-4, occupy time slots 12, 24, 36 and 48 respectively. Each time slot grouping can be independently configured for situations requiring channel associated signalling or situations with no signalling requirement (e.g. external common signalling). (See § 3.2.3.1.1.)

TABLE 6/G.704

32 kbit/s channel time slots frame structure for 1544 kbit/s interface

Time slot grouping	Time slots												
No. 1	1	2	3	4	5	6	7	8	9	10	11	12	(SGC)
No. 2	13	14	15	16	17	18	19	20	21	22	23	24	(SGC)
No. 3	25	26	27	28	29	30	31	32	33	34	35	36	(SGC)
No. 4	37	38	39	40	41	42	43	44	45	46	47	48	(SGC)

Note 1 – Each time slot signifies a 32 kbit/s channel.

Note 2 – The signalling grouping channel (SGC) occupies the twelfth 32 kbit/s time slot of each time slot grouping.

3.2.3.1.1 *Use of a 384 kbit/s time slot grouping*

Use of a 384 kbit/s time slot grouping is categorized into two possible configurations:

– When no signalling capabilities are required, a 384 kbit/s time slot grouping can carry twelve 32 kbit/s channel time slots;

– When channel associated signalling capabilities are required, a 384 kbit/s time slot grouping will consist of eleven 32 kbit/s channel time slots and a 32 kbit/s channel time slot defined as a signalling grouping channel.

3.2.3.1.2 *Use of a signalling grouping channel*

A signalling grouping channel is used for the transmission of channel associated A-B-C-D signalling information, signalling grouping channel alarm information, the signalling grouping channel multiframe alignment signal, and CRC-6 error detection information between network nodes.

3.2.4 *32 kbit/s signalling grouping channel multiframe structure*

3.2.4.1 *Number of bits per 32 kbit/s signalling grouping channel time slot*

Four, numbered 1 to 4.

3.2.4.2 *Bit allocation of 32 kbit/s signalling grouping channel time slot*

Allocated to the last four bits of each time slot grouping.

3.2.4.3 *Multiframe structure*

The signalling grouping channel multiframe structure consists of 24 consecutive frames numbered 1 to 24. Table 7/G.704 shows the signalling grouping channel multiframe structure.

TABLE 7/G.704

32 kbit/s signalling grouping channel multiframe structure

Time slot grouping frame number	Signalling grouping channel bit number			
	1	2	3	4
1	A_j	A_{j+1}	0	S_1
2	A_{j+2}	A_{j+3}	1	S_2
3	A_{j+4}	A_{j+5}	0	CRC-1
4	A_{j+6}	A_{j+7}	1	S_4
5	A_{j+8}	A_{j+9}	0	S_5
6	A_{j+10}	M_1	1	S_6
7	B_j	B_{j+1}	0	CRC-2
8	B_{j+2}	B_{j+3}	1	S_8
9	B_{j+4}	B_{j+5}	0	S_9
10	B_{j+6}	B_{j+7}	1	S_{10}
11	B_{j+8}	B_{j+9}	0	CRC-3
12	B_{j+10}	M_2	1	S_{12}
13	C_j	C_{j+1}	1	S_{13}
14	C_{j+2}	C_{j+3}	0	S_{14}
15	C_{j+4}	C_{j+5}	1	CRC-4
16	C_{j+6}	C_{j+7}	0	S_{16}
17	C_{j+8}	C_{j+9}	1	S_{17}
18	C_{j+10}	M_2	0	S_{18}
19	D_j	D_{j+1}	1	CRC-5
20	D_{j+2}	D_{j+3}	0	S_{20}
21	D_{j+4}	D_{j+5}	1	S_{21}
22	D_{j+6}	D_{j+7}	0	S_{22}
23	D_{j+8}	D_{j+9}	1	CRC-6
24	D_{j+10}	M_4	0	S_{24}

Note 1 – $_j$ = 1 for 12th 32 kbit/s channel time slot
$_j$ = 13 for 24th 32 kbit/s channel time slot
$_j$ = 25 for 36th 32 kbit/s channel time slot
$_j$ = 37 for 48th 32 kbit/s channel time slot

Note 2 – (A_j, B_j, C_j, D_j): A, B, C, D signalling bits
M_j: Signalling grouping channel alarm indication bits
S_k: Spare bits

Note 3 – The signalling grouping channel provides A, B, C, D signalling capability for 11 channels within each time slot grouping.

3.2.4.4 *Signalling grouping channel multiframe alignment signal*

Bit 3 of the signalling grouping channel, as shown in Table 7/G.704, contains the signal grouping channel multiframe alignment signal used to associate the signalling bits in the signal grouping channel with the proper channels of the associated time slot grouping.

Note – The signalling grouping channel multiframe alignment signal is independent of, and different from, the framing bit of the 1544 kbit/s frame.

3.2.4.5 *CRC-6 error detection information for the time slot grouping*

An optional 2 kbit/s CRC-6 error detection code word may be transmitted in the bit position indicated by CRC-1 through CRC-6 in Table 7/G.704.

The CRC-6 message block (CMB) is a sequence of 1152 serial bits that is concident with a time slot grouping multiframe. By definition, CMB N begins at bit position 0 of time slot grouping multiframe N and ends at bit position 1151 of time slot grouping multiframe N.

The check-bit sequence CRC-1 through CRC-6 transmitted in multiframe $N + 1$ is the remainder after multiplication by x^6, and then division (modulo 2) by the generator polynomial $x^6 + x + 1$ of the the polynomial corresponding to CMB N. The first check bit, CRC-1, is the most significant bit of the remainder; the last check bit CRC-6, is the least significant bit. The time slot grouping channel is included in this calculation with bit 4 of the time slot grouping channel being set to 1.

When not utilizing the option to transmit the CRC-6 error detection signal, CRC-1 through CRC-6 shall be set to 1.

3.2.4.6 *Signalling*

Two alternative methods as given in §§ 3.2.4.6.1 and 3.2.4.6.2 are recommended.

3.2.4.6.1 *Common channel signalling*

Refer to § 3.1.3.1. Two successive 32 kbit/s channel time slots are used for 64 kbit/s common channel signalling transmission.

3.2.4.6.2 *Channel associated signalling*

As indicated in Table 7/G.704, bits 1 and 2 of the signalling grouping channel convey the channel associated signalling information for the channels of the associated time slot grouping.

The signalling grouping channel can provide four independent 333 bit/s signalling channels designated A, B, C and D, two independent 667 bit/s signalling channels designated A and B, or one 1333 bit/s signalling channel designated A. Where only A-B signalling is used, the A-B signalling is repeated for the C-D positions respectively. Where only A signalling is used, the A signalling is repeated for the B-C-D positions respectively.

3.2.4.7 *Signalling grouping channel alarm indication signals*

As indicated in Table 7/G.704, the signalling grouping channel contains four alarm indication bits, M_1, M_2, M_3 and M_4.

M_1 provides the capability to transmit through the interface a remote time slot grouping alarm indication of a failure in the opposite direction of transmission.

M_2 provides the capability to transmit through the interface an indication of a failure in tributary input signals to the network node.

M_3 provides the capability to transmit through the interface an indication of a failure in tributary output signals from the network node.

M_4 is set to 1 whenever M_1 and/or M_2 and/or M_3 are set to 1.

3.2.5 *Signal grouping channel unused bits*

The bits marked S in Table 7/G.704 are currently unused and set to 1. The definition and allocation of the S-bits are for further study.

3.2.6 *Loss and recovery of signalling channel multiframe alignment*

Loss of the signalling grouping channel multiframe alignment signal is declared when two out of four signalling grouping channel framing bits are in error. The rare occurrence of a single instantaneous slip of ± 11 frames is undetected by the two-out-of-four algorithm. Signalling grouping channel multiframe alignment shall be declared when the correct sequence of 24 valid signalling grouping channel framing bits is detected, beginning with the first frame of the multiframe.

3.3 *Interface at 1544 kbit/s carrying n × 64 kbit/s*

Electrical characteristics should follow Recommendation G.703.

The time slot mapping to the 1544 kbit/s interface is for further study.

4 Characteristics of frame structures carrying channels at various bit rates in 6312 kbit/s interfaces

4.1 *Interface at 6312 kbit/s carrying 64 kbit/s channels*

4.1.1 *Frame structure*

4.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

4.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 1 to 784 in the basic frame carry 98 octet interleaved 64 kbit/s channel time slots, numbered 1 to 98. Five bits per frame (F-bits) are added at the end of the frame for the frame alignment signal and for other signals.

4.1.1.3 *Allocation of the F-bits*

Refer to Table 3/G.704.

4.1.2 *Use of 64 kbit/s channel time slots*

Each 64 kbit/s channel time slot can accomodate e.g., a PCM-encoded voiceband signal conforming to Recommendation G.711 or data information with a bit rate up to 64 kbit/s. 64 kbit/s channel time slots 97, 98 may be used for signalling.

4.1.3 *Signalling*

Two alternative methods as given in §§ 4.1.3.1 and 4.1.3.2 are recommended.

4.1.3.1 *Common channel signalling*

Use of 64 kbit/s channel time slots 97 and 98 for common channel signalling is under study.

4.1.3.2 *Channel associated signalling*

Based on agreement between the Administrations concerned, channel associated signalling is provided for intra-regional circuits according to the following arrangement:

4.1.3.2.1 *Allocation of signalling bit*

Sixteen signalling bits (bit positions 769 to 784) are designated as ST_1 to ST_{16}. One ST_i-bit ($i = 1$ to 16) accomodates signalling information corresponding to six channel time slots i, $16 + i$, $32 + i$, $48 + i$, $64 + i$ and $80 + i$ in a manner described in § 4.1.3.2.2 below.

4.1.3.2.2 *Signalling multiframe structure*

Each ST-bit constitutes an independent signalling multiframe over eight frames as shown in Table 8/G.704.

TABLE 8/G.704

Signalling multiframe structure

Frame number	n	$n+1$	$n+2$	$n+3$	$n+4$	$n+5$	$n+6$	$n+7$
Use of ST-bit	F_s	S_1	S_2	S_3	S_4	S_5	S_6	S_p
	(See Note 1)	(See Note 2)						(See Note 4)

Note 1 – The F_s-bit is either alernate 0, 1 or the following 48 bit digital pattern:

A101011011 0000011001 1010100111 0011110110 10000101.

For the 48 bit digital pattern, the A-bit is usually fixed to state 1 and is reserved for optional use. The pattern is generated according to the following primitive polynomial (refer to Recommendation X.50):

$$x^7 + x^4 + 1$$

Note 2 – S_j-bits ($j = 1$ to 6) carry channel associated signalling or maintenance information. When the 48 bit pattern is adopted as the F_s frame alignment signal, each S_j-bit ($j = 1$ to 6) can be multiframed, as follows:

$$S_{j1}, S_{j2}, \ldots, S_{j12}$$

The S_{j1}-bit carries the following 16 bit frame alignment pattern generated according to the same primitive polynomial as for the 48 bit pattern.

A011101011011000

The A-bit is usually fixed to 1 and is reserved for optional use. Each S_{ji}-bit ($i = 2$ to 12) carries channel associated signalling for sub-rate circuits and/or maintenance information.

Note 3 – ST-bits (F_s, S_1, ..., S_6 and S_p) all at state 1 indicate Alarm Indication Signal (AIS) for six 64 kbit/s channels.

Note 4 – The S_p-bit is usually fixed to state 1. When backward AIS for six 64 kbit/s channels is required to be sent, the S_p is set to state 0.

4.2 *Interfaces at 6312 kbit/s carrying other channels than 64 kbit/s*

For further study.

5 Characteristics of frame structures carrying channels at various bit rates in 2048 kbit/s interfaces

5.1 *Interface at 2048 kbit/s carrying 64 kbit/s channels*

5.1.1 *Frame structure*

5.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

5.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 1 to 256 in the basic frame carry 32 octet interleaved time slots numbered 0 to 31.

5.1.1.3 *Allocation of the bits of 64 kbit/s channel time slot 0*

See Table 4a/G.704 (§ 2.3.2).

5.1.2 *Use of other 64 kbit/s channel time slots*

Each of the 64 kbit/s channel time slots 1 to 15 and 17 to 31 can accomodate e.g., a PCM-encoded voiceband signal according to Recommendation G.711 or a 64 kbit/s digital signal.

The 64 kbit/s channel time slot 16 may be used for signalling. If not needed for signalling, in some cases it may be used for a 64 kbit/s channel in the same way as time slots 1 to 15 and 17 to 31.

5.1.3 *Signalling*

The use of 64 kbit/s channel time slot 16 is recommended for either common channel or channel associated signalling as required.

The detailed requirements for the organization of particular signalling systems will be included in the specifications for those signalling systems.

5.1.3.1 *Common channel signalling*

The 64 kbit/s channel time slot 16 may be used for common channel signalling systems up to a rate of 64 kbit/s. The method of obtaining signal alignent will form part of the particular common channel signallling specification.

5.1.3.2 *Channel associated signalling*

This section contains the recommended arrangement for the use of the 64 kbit/s capability of channel time slot 16 for channel associated signalling.

5.1.3.2.1 *Multiframe structure*

A multiframe comprises 16 consecutive frames (whose structure is given in § 5.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of 64 kbit/s channel time slot 16 in frame 0.

5.3.1.2.2 *Allocation of 64-kbit/s channel time slot 16*

When 64 kbit/s channel time slot 16 is used for channel associated signalling, the 64-kbit/s capacity is sub-multiplexed into lower-rate signalling channels using the multiframe alignement signal as a reference.

Details of the bit allocation are given in Table 9/G.704.

5.2 *Interface at 2048 kbit/s carrying n × 64 kbit/s*

Electrical characteristics should follow Recommendation G.703 (see Note 4 of Preamble to G.703). For the accomodation of $n \times 64$ kbit time slots in the 2048 kbit/s frame, two situations are envisaged.

5.2.1 *One n × 64 kbit/s signal on the tributary side of a multiplex equipment*

Time slots of the 2048 kbit/s frame are filled as follows:

TS0: according to § 2.3;

TS16: reserved for the accomodation, if required, of a 64 kbit/s signalling channel.

- If $2 \leq n \leq 15$, TS1 to TSn are filled with $n \times 64$ kbit/s data [see a) of Figure 1/G.704];
- If $15 < n \leq 30$, TS1 to TS15 and TS17 to TS(n+1) are filled with $n \times 64$ kbit/s data [see b) of Figure 1/G.704].
- Remaining time slots are filled with all 1s.

TABLE 9/G.704

Bit allocation of channel associated 64 kbit/s time slot 16 for channel associated signalling

Time slot 16 of frame 0	Time slot 16 of frame 1		Time slot 16 of frame 2		– – –	Time slot 16 of frame 15	
0000 xyxx	abcd Channel 1	abcd Channel 16	abcd Channel 2	abcd Channel 17	– – –	abcd Channel 15	abcd Channel 30

Note 1 – Channel numbers refer to telephone channel numbers. 64 kbit/s channel time slots 1 to 15 and 17 to 31 are assigned to telephone channels numbered from 1 to 30.

Note 2 – This bit allocation provides four 500-bit/s signalling channels designated a, b, c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the PCM transmission system, will not exceed ± 2 ms.

Note 3 – When bits b, c or d are not used they should have the values: b = 1, c = 0, d = 1.

It is recommended that the combination 0000 of bits a, b, c and d should not be used for signalling purposes for channels 1-15.

Note 4 – x = spare bit, to be set to 1 if not used.

y = bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in an alarm condition, set to 1.

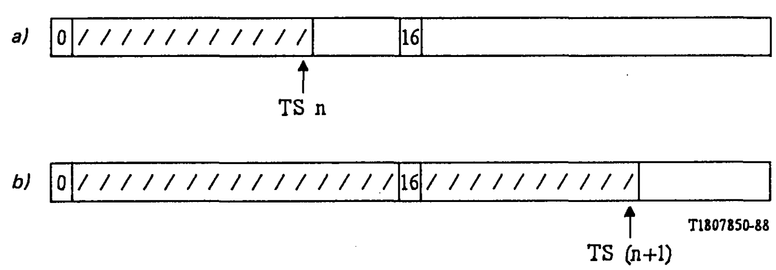


FIGURE 1/G.704

5.2.2 *One or more n × 64 kbit/s signal on the multiplexed signal side of a multiplexing equipment*

For any one $n \times 64$ kbit/s signal, time slots of the 2048 kbit/s frame are filled as follows:

TS0: according to § 2.3;

TS16: reserved for the accomodation, if required, of a 64 kbit/s signalling channel.

TS(x) of the 2048 kbit/s frame is designated as the time slot into which the first time slot of the $n \times 64$ kbit/s is accomodated.

– If $x \leqslant 15$ and $x + (n-1) \leqslant 15$, or, if $x \geqslant 17$ and $x + (n-1) \leqslant 31$, then the filling of time slots is from TS (x) to TS $(x+n-1)$ [see a)and b) of Figure 2/G.704];

– If $x + (n-1) \geqslant 16$, then the filling of time slots is from TS (x) to TS15 and TS17 to TS $(x+n)$ (see c) of Figure 2/G.704).

Note – Once $n \times 64$ kbit/s signal has been accomodated into the multiplexed signal, care should be taken in the interpretation of the above rules to ensure that further such signals only use the time slots which remain spare.

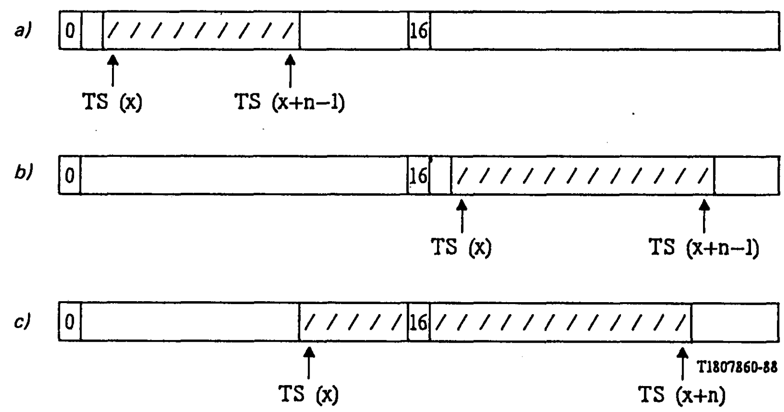


FIGURE 2/G.704

6 Characteristics of frame structures carrying channels at various bit rates in 8448 kbit/s interface

6.1 *Interface at 8448 kbit/s carrying 64 kbit/s channels*

6.1.1 *Frame structure*

6.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered from 1 to 8.

6.1.1.2 *Number of 64 kbit/s channel time time slots per frame*

Bits 1 to 1056 in the basic frame carry 132 octet interleaved 64 kbit/s channel time slots, numbered form 0 to 131.

6.1.2 *Use of 64 kbit/s channel time slots*

6.1.2.1 *64 kbit/s channel time slot assignment in case of channel associated signalling*

64 kbit/s channel time slots 5 to 32, 34 to 65, 71 to 98 and 100 to 131 are assigned to 120 telephone channels from 1 to 120.

64 kbit/s channel time slot 0 and the first 6 bits in 64 kbit/s channel time slot 66 are assigned to framing: the remaining 2 bits in 64 kbit/s channel time slot 66 are devoted to services.

64 kbit/s channel time slots 67 to 70 are assigned to channel associated signalling as covered in § 6.1.4.2 below.

64 kbit/s channel time slots 1 to 4, 33 are left free for national use.

6.1.2.2 *64 kbit/s channel time slot assignment in case of common channel signalling*

64 kbit/s channel time slots 2 to 32, 34 to 65, 67 to 98 and 100 to 131 are available for 127 telephone, signalling or other service channels. By bilateral agreement between the Administrations concerned, 64 kbit/s channel time slot 1 may either be used to ‘provide another telephone or service channel or left free for service purposes within a digital exchange.

The 64 kbit/s channels corresponding to 64 kbit/s channel time slot 1 to 32, 34 to 65 (etc. as above) are numbered 0 to 127.

64 kbit/s channel time slot 0 and the first 6 bits in channel time slot 66 are assigned to framing, the remaining 2 bits in 64 kbit/s channel time slot 66 are assigned to service.

64 kbit/s channel time slots 67 to 70 are, in descending order of priority, available for common channel signalling as covered in § 6.1.4.1 below.

64 kbit/s channel slot 33 is left free for national use.

6.1.3 *Description of the CRC procedure in 64 kbit/s channel time slot 99*

In order to provide an end-to-end quality monitoring of the 8 Mbit/s link, a CRC-6 procedure is used and the six bits C_1 to C_6 computed at the source location are inserted in bit positions 1 to 6 of the time slot 99 (see Figure 3/G.704).

In addition, bit 7 of this time slot, denoted E, is used to send in the transmitting direction an indication about the received signal arriving from the opposite direction. Bit E indicates whether or not the most recent CRC block arriving at the opposite end had errors.

The CRC-6 bits C_1 to C_6 are computed for each frame. The CRC-6 block size is then 132 octets, i.e. 1056 bits, and the computation is made 8000 times per second.

C_1	C_2	C_3	C_4	C_5	C_6	E	S
1							8

T1807870-88

FIGURE 3/G.704

Time slot 99

6.1.3.1 *Multiplication/division process*

A given C_1-C_6 word located in frame N is the remainder after multiplication by x^6 and then division (modulo 2) by the generator polynomial $x^6 + x + 1$ of the polynomial representation of frame $(N-1)$.

Note – When representing the contents of a frame as a polynomial, the first bit in the frame should be taken as being the most significant bit. Similarly C_1 is defined to be the most significant bit of the remainder and C_6 the least significant bit of the remainder.

6.1.3.2 *Encoding procedure*

The CRC bit positions are initially set at 0 i.e.:

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = 0$$

The frame is then acted upon by the multiplication/division process referred to above in § 6.1.3.1.

The remainder resulting from the multiplication/division process is stored ready for insertion into the respective CRC locations of the next frame.

Note – These CRC bits do not affect the computation of the CRC bits in the next frame since the corresponding locations are set to 0 before the computation.

6.1.3.3 *Decoding procedure*

A received frame is acted upon by the multiplication/division process, referred to above in § 6.1.3.1, after having its CRC bits extracted and replaced by 0s.

The remainder resulting from this multiplication/division process is then stored and subsequently compared on a bit by bit basis with the CRC received in the next frame.

If the decoder-calculated remainder exactly corresponds to the CRC bits sent from the encoder, it is assumed that the checked frame is error free.

6.1.3.4 *Action on bit E*

Bit E of frame N is set to 1 in the transmitting direction if bits C_1 to C_6 detected in the most recent frame at the opposite end have been found in error (at least one bit in error). If no errors, E is set to 0.

6.1.4 *Signalling*

The use of channel time slots 67 to 70 is recommended for either common channel or channel-associated signalling as required. The detailed requirements for the organization of particular signalling systems will be included in the specifications for those signalling systems.

6.1.4.1 *Common channel signalling*

64 kbit/s channel time slots 67 to 70 may be used for common channel signalling in a descending order of priority up to a rate of 64 kbit/s. The method of obtaining signal alignment will form part of the particular common channel signalling specification.

6.1.4.2 *Channel associated signalling*

The recommended arrangement for the use of the 64 kbit/s capacity in each 64 kbit/s channel time slot 67 to 70 for channel associated signalling is as follows:

6.1.4.2.1 *Multiframe structure*

A multiframe for each 64 kbit/s bit-stream comprises 16 consecutive frames (whose structure is given in § 6.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of channel time slots 67 to 70 in frame 0.

6.1.4.2.2 *Allocation of 64 kbit/s channel time slots 67 to 70*

When 64 kbit/s channel time slots 67 to 70 are used for channel associated signalling, the 64 kbit/s capacity of each of the four 64 kbit/s channel time slots is sub-multiplexed into lower rate signalling channels using the multiframe alignment signal as a reference. Details of the bit allocation are given in Table 10/G.704.

6.2 *Interface at 8448 kbit/s carrying other channels than 64 kbit/s*

For further study.

TABLE 10/G.704

Bit allocation of 64 kbit/s channel time slots 67 to 70

64 kbit/s channel time slot / Frame	67		68		69		70	
0	0000*xyxx*		0000*xyxx*		0000*xyxx*		0000*xyxx*	
1	*abcd* Channel 1	*abcd* Channel 16	*abcd* Channel 31	*abcd* Channel 46	*abcd* Channel 61	*abcd* Channel 76	*abcd* Channel 91	*abcd* Channel 106
. .	. .	. .	. .	. .	. .	. .	. .	. .
15	*abcd* Channel 15	*abcd* Channel 30	*abcd* Channel 45	*abcd* Channel 60	*abcd* Channel 75	*abcd* Channel 90	*abcd* Channel 105	*abcd* Channel 120

Note 1 – Channel numbers refer to telephone channel numbers. Refer to § 6.1.2.1 for the assignment of 64 kbit/s channel time slots to the telephone channels.

Note 2 – This bit allocation provides four 500-bit/s signalling channels designated a, b, c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the PCM transmission system, will not exceed ± 2 ms.

Note 3 – When bits b, c or d are not used they should have the values: b = 1, c = 0, d = 1.

It is recommended the the combination 0000 of bits *a*, *b*, *c* and *d* should not be used for signalling purposes for channels 1-15, 31-45, 61-75 and 91-125.

Note 4 – x = spare bit, to be set to 1 if not used.

y = bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in an alarm condition, set to 1.

ANNEX A

(to Recommendation G.704)

Examples of CRC implementations using shift registers

A.1 *CRC-6 procedure for interface at 1544 kbit/s* (Reference: § 2.1.3.1.2)

See Figure A-1/G.704.

Input I to the shift register: CMB *N* with F bits set to 1.

Generator polynomial of the shift register: $x^6 + x + 1$.

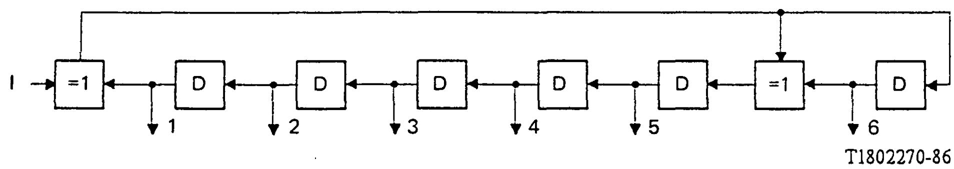


FIGURE A-1/G.704

At I, the CMB is fed serially (i.e. bit by bit) into the circuit, starting with bit number 1 of the multiframe (see Table 1/G.704). When the last bit of the CMB (i.e. bit number 4632 within the multiframe has been fed into the shift register, the CRC bits e_1 to e_6 are available at the outputs 1 to 6. (Output 1 provides the most significant bit, e_1, and output 6 the least significant bit, e_6). Bits e_1 to e_6 are transmitted in the next CMB (c.f. Table 1/G.704).

Note – The outputs (1 to 6) of the shift register stages are reset to 0 after each CMB.

A.2 *CRC-5 procedure for interface at 6312 kbit/s* (Reference: § 2.2.3.2)

Input I to the shift register: CMB *N*.

Generator polynomial of the shift register: $x^5 + x^4 + x^2 + 1$.

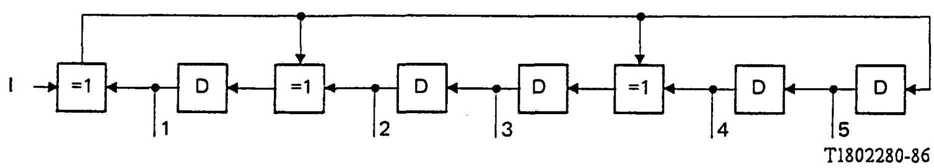


FIGURE A-2/G.704

At I, the CMB is fed serially (i.e. bit by bit) into the circuit, starting with bit number 1 of frame number 1 (see Table 3/G.704). When the last bit of the CMB (i.e. bit number 784 of frame number 4) has been fed into the the shift register, the CRC bits e_1 to e_5 are available at the outputs 1 to 5. (Output 1 provides the most significant bit, e_1, and output 5 the least significant bit, e_5). Bits e_1 to e_5 are transmitted in the corresponding multiframe (see Table 3/G.704).

Note – The outputs (1 to 5) of the shift register stages are reset to 0 after each CMB.

A.3 *CRC-4 procedure for interface at 2048kbit/s* (Reference: § 2.3.3.5)

See Figure A-3/G.704.

Input I to the shift register: SMF (*N*) with C_1, C_2, C_3, C_4 set to 0.

Generator polynomial of the shift register: $x^4 + x + 1$.

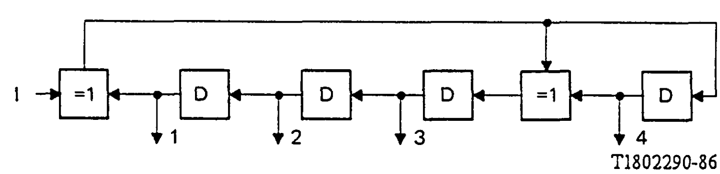


FIGURE A-3/G.704

At I, the SMF is fed serially (i.e. bit by bit) into the circuit, starting with bit $C_1 = 0$ (see Table 4b/G.704). When the last bit of the SMF (i.e. bit number 256 of frame number 7, respectively of frame number 15) has been fed into the shift register, the CRC bits C_1 to C_4 are available at the outputs 1 to 4. (Output 1 provides the most significant bit, C_1, and output 4 the least significant bit, C_4). Bits C_1 to C_4 are transmitted in the next SMF, i.e. SMF($N+1$).

Note – The outputs (1 to 4) of the shift register stages are reset to 0 after each SMF.

CHARACTERISTICS REQUIRED TO TERMINATE DIGITAL LINKS ON A DIGITAL EXCHANGE

(Malaga-Torremolinos, 1984)

This Recommendation defines interface conditions and fundamental functions of digital exchange terminal equipments used to terminate digital paths. The multiplex structures are compatible with those described in Recommendation G.704, and are applicable to digital paths which connect PCM multiplex equipments to exchanges and to digital paths which interconnect digital exchanges. The locations of these interfaces are described in Recommendations Q.502 and Q.512 for digital transit and digital local exchanges.

The digital exchange terminal is a synchronous equipment which has a frame aligner circuit. In order to meet the network performance objectives of Recommendation G.822, the digital exchange terminal should fulfil the synchronization performance as described below.

1 1544 kbit/s digital path

1.1 *General characteristics*

1.1.1 *Bit rate*

The nominal bit rate is 1544 kbit/s.

Note – The tolerance on this bit rate should be further studied and specified.

1.1.2 *Timing signal*

It should be possible to derive the transmitting timing signal from an external source as specified below.

Note – For PCM multiplex equipment at the remote end, the timing signal will be derived from the incoming signal at the receive end.

1.1.2.1 *Timing in a non-synchronized network*

For a digital exchange the transmitting timing signal will be derived from an office clock.

1.1.2.2 *Timing in a synchronized network*

In case of synchronous operation of the network, a network synchronization system will maintain the signal or clocks within agreed timing limits.

1.1.3 *Interfaces*

Refer to § 2 of Recommendation G.703. No interface internal to the switch will be recommended.

1.1.4 *Transmission performance*

Transmission performance of the digital path should be the same as that for 1544 kbit/s digital paths between primary PCM multiplex equipment.

1.2 *Frame strusture*

Refer to § 3.1 of Recommendation G.704.

1.3 *Synchronization performances*

1.3.1 *Wander at the input*

Refer to § 4 of Recommendation G.824.

1.3.2 *Jitter at the input*

Refer to § 4 of Recommendation G.824.

1.3.3 *Jitter at the output*

Jitter at the output is under study.

1.3.4 *Slips*

Refer to §§ 3 and 4 of Recommendation G.822.

1.3.5 *Forms of frame aligner*

Refer to § 8 of Recommendation G.811.

2 6312 kbit/s digital path

2.1 *General characteristics*

2.1.1 *Bit rate*

The nominal bit rate is 6312 kbit/s.

Note – The tolerance on this bit rate should be further studied and specified.

2.1.2 *Timing signal*

It should be possible to derive the transmitting timing signal from an external source as specified below.

Note – For PCM multiplex equipment at the remote end, the timing signal will be derived from the incoming signal at the receive end.

2.1.2.1 *Timing in a non-synchronized network*

For a digital exchange the transmitting timing signal will be derived from an office clock.

2.1.2.2 *Timing in a synchronized network*

In case of synchronous operation of the network, a network synchronization system will maintain the signal or clocks within agreed timing limits.

2.1.3 *Interfaces*

Refer to § 3 of Recommendation G.703. No interface internal to the switch will be recommended.

2.1.4 *Transmission performance*

Transmission performance of the digital path should be the same as that for 6312 kbit/s digital paths between primary PCM multiplex equipment.

2.2 *Frame structure*

Refer to § 3.2 of Recommendation G.704.

2.3 *Synchronization performances*

2.3.1 *Wander at the input*

Refer to § 4 of Recommendation G.824.

2.3.2 *Jitter at the input*

Refer to § 4 of Recommendation G.824.

2.3.3 *Jitter at the output*

Jitter at the output is under study.

2.3.4 *Slips*

Refer to §§ 3 and 4 of Recommendation G.822.

2.3.5 *Forms of frame aligner*

Refer to § 8 of Recommendation G.811.

3 2048 kbit/s digital path

3.1 *General characteristics*

3.1.1 *Bit rate*

The nominal bit rate is 2048 kbit/s. This rate will be controlled to within at least ± 50 parts per million (ppm) at the transmitting end for each direction of transmission.

3.1.2 *Timing signal*

The timing signal is a 2048 kHz signal from which the bit rate is derived.

3.1.2.1 *Timing in a non-synchronized network*

For a PCM multiplex equipment, the timing signal will be derived from the incoming timing signal at the receive side. For a digital exchange, the transmitting timing signal will be derived from a clock within the digital exchange.

3.1.2.2 *Timing in a synchronized network*

In case of synchronous operation of the network, a network synchronization system will maintain the timing signal or clocks within agreed timing limits.

3.1.3 *Interfaces*

Refer to § 6 of Recommendation G.703. No interface, internal to the switch, will be recommended.

3.1.4 *Transmission performance*

The transmission performance of the digital path will be the same as that for 2048 kbit/s digital paths between primary PCM multiplex equipments.

3.2 *Frame structure*

Refer to § 3.3 of Recommendation G.704.

Where more signalling capacity is required between exchanges, additional time slots may be utilized for common channel signalling. They should be selected from the slots allocated in PCM multiplexes for data purposes. On routes between exchanges comprising more than one 2048-kbit/s digital path, it may be possible to provide an adequate signalling capacity without using time slot 16 of all systems on the route. In these circumstances time slot 16 in those systems not carrying signalling can be allocated to speech or other services. Time slot 0 is reserved for frame alignment, alarms and network synchronization information and should not be used for signalling or speech purposes.

3.3 *Synchronization performances*

3.3.1 *Wander at the input*

Refer to § 3 of Recommendation G.823.

3.3.2 *Jitter at the input*

Refer to § 3 of Recommendation G.823.

3.3.3 *Jitter at the output*

Jitter at the output is under study.

3.3.4 *Slips*

Refer to §§ 3 and 4 of Recommendation G.822.

3.3.5 *Forms of frame aligner*

Refer to § 8 of Recommendation G.811.

4 8448 kbit/s digital path

4.1 *General characteristics*

4.1.1 *Bit rate*

The nominal bit rate is 8448 kbit/s. This rate will be controlled to within at least ± 30 parts per million at the transmitting end for each direction of transmission.

4.1.2 *Timing signal*

The timing signal is an 8448 kHz signal from which the bit rate is derived.

4.1.2.1 *Timing in a non-synchronous network*

For a PCM multiplex equipment, the timing signal will be derived from the incoming timing signal at the receive side. For a digital exchange, the transmitting timing will be derived from a clock within the digital exchange.

4.1.2.2 *Timing in a synchronous network*

In case of synchronous operation of the network, a network synchronization system will maintain the timing signal or clocks within agreed timing limits.

4.1.3 *Interfaces*

Refer to § 7 of Recommendation G.703. No interface, internal to the switch, will be recommended.

4.1.4 *Transmission performance*

The transmission performance of the digital path will be the same as that for 8448 kbit/s digital paths between secondary PCM and/or digital multiplex equipments.

4.2 *Frame structure*

Refer to § 3.4 of Recommendation G.704.

Where signalling capacity is required between exchanges, time-slots 67, 68, 69 and 70 may be utilized for common channel signalling in this order of descending priority. Those channels not used for common channel signalling can be used for speech or other purposes.

4.3 *Synchronization performance*

4.3.1 *Wander at the input*

Refer to § 3 of Recommendation G.823.

4.3.2 *Jitter at the input*

Refer to § 3 of Recommendation G.823.

4.3.3 *Jitter at the output*

Jitter at the output is under study.

4.3.4 *Slips*

Refer to §§ 3 and 4 of Recommendation G.822.

4.3.5 *Forms of frame aligner*

Refer to § 8 of Recommendation G.811.

Recommendation G.706

FRAME ALIGNMENT AND CYCLIC REDUNDANCY CHECK (CRC) PROCEDURES RELATING TO BASIC FRAME STRUCTURES DEFINED IN RECOMMENDATION G.704

(Melbourne, 1988)

1 General

This Recommendation relates to equipment which receives signals with basic frame structures as defined in Recommendation G.704. It defines the frame alignment, the cyclic redundancy check (CRC) multiframe alignment and CRC bit error monitoring procedures to be used by such equipment. Annex A contains background information about the use of the CRC procedures and their limitations.

2 Frame alignment and CRC procedures at 1544 kbit/s interface

2.1 *Loss and recovery of frame alignment*

There are two alternative multiframe structures at the 1544 kbit/s interface:

a) 24-frame multiframe, and

b) 12-frame multiframe.

2.1.1 *Loss of frame alignment*

The frame alignment signal should be monitored to determine if frame alignment has been lost. Loss of frame alignment should be detected within 12 ms. Loss of frame alignment must be confirmed over several frames to avoid the unnecessary initiation of the frame alignment recovery procedure due to transmission bit errors. The frame alignment recovery procedure should commence immediately once loss of frame alignment has been confirmed.

Note – For the 12-frame multiframe described in Recommendation G.704, loss of multiframe alignment is deemed to occur when loss of frame alignment occurs.

2.1.2 *Recovery of frame alignment*

2.1.2.1 *Frame alignment recovery time*

The frame alignment recovery time is specified in terms of the maximum average reframe time in the absence of errors. The maximum average reframe time is the average time to reframe when the maximum number of bit positions must be examined for locating the frame alignment signal.

a) *24-frame multiframe*

The maximum average reframe time should not exceed 15 ms.

Note – Some existing designs of equipment were designed to a limit of 50 ms.

b) *12-frame multiframe*

The maximum average reframe time should not exceed 50 ms.

Note – These times do not include the time required for the CRC procedure for false frame alignment verification defined in § 2.2.2.

2.1.2.2 *Strategy for frame alignment recovery*

a) *24-frame multiframe*

Frame alignment should be recovered by detecting the valid frame alignment signal. When the CRC-6 code is utilized for error performance monitoring (see § 2.2.3), the CRC-6 information may be coupled with the framing algorithm to ensure that a valid frame alignment signal contained within the 24 F-bits is the only pattern onto which the reframe circuit can permanently lock. This procedure is illustrated in Figure 1/G.706.

b) *12-frame multiframe*

Overall frame alignment should be recovered by way of simultaneous detection of the frame alignment signal and the multiframe alignment signal, or of frame alignment followed by multiframe alignment.

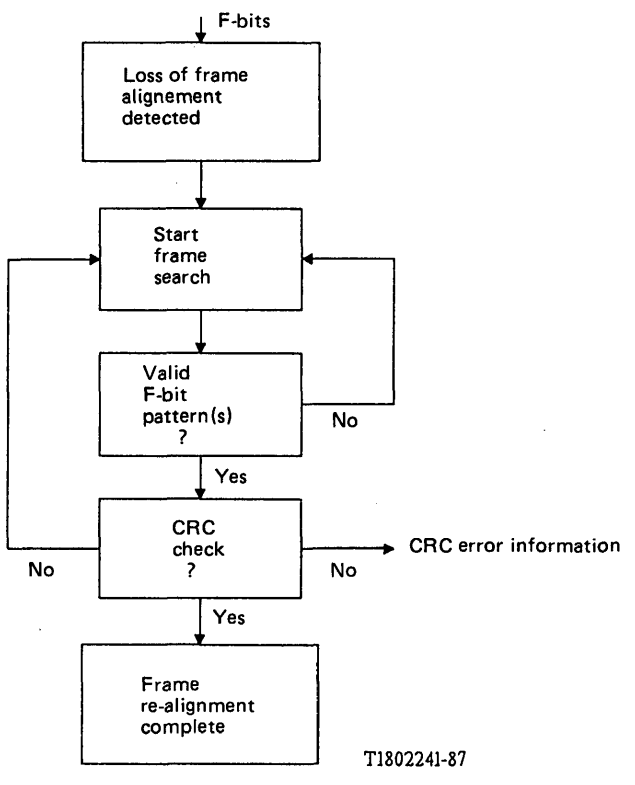


FIGURE 1/G.706

False frame alignment protection using a cyclic redundancy check (CRC) (1544 and 6312 kbit/s)

2.2 *CRC bit monitoring*

Error monitoring by CRC-6 assumes a signal quality sufficient for frame alignment to be established so that CRC-6 bits can be correctly accessed.

2.2.1 *Monitoring procedure*

i) A received CRC Message Block (CMB) is acted upon by the multiplication/division process defined in Recommendation G.704 after having its F-bits replaced by binary 1s.

ii) The remainder resulting from the division process is then stored and compared on a bit-by-bit basis with the CRC bits received in the next CMB.

iii) If the remainder exactly corresponds to the CRC bits contained in the next CMB of the received signal, it is assumed that the checked CMB is error-free.

2.2.2 *Monitoring for false frame alignment* (see § A.1.1)

In the case of the 24-frame multiframe, when the CRC-6 code is utilized for error performance monitoring, it may also be used to provide immunity against spurious frame alignment signals. The procedure described in § 2.1.2.2 a) should be followed.

2.2.3 *Error performance monitoring using CRC-6* (see § A.1.2)

For the purpose of error performance monitoring, it should be possible to obtain indications of each CRC message block which is received in error. The consequent error information should be used in accordance with the requirements to be defined in respective equipment Recommendations.

3 Frame alignment and CRC procedures at 6312 kbit/s interface

3.1 *Loss and recovery of frame alignment*

For the 6312 kbit/s hierarchical level, the term "frame alignment" is synonymous with "multiframe alignment". The last five bits of the 789-bit frame are designated as the F-bits (see Recommendation G.704) and are time-shared as a frame alignment signal and for other purposes.

3.1.1 *Loss of frame alignment*

The frame alignment signal should be monitored to determine if frame alignment has been lost. The loss of frame alignment is declared when seven consecutive incorrect frame alignment signals have been received.

The recovery of frame alignment procedure should start immediately once loss of frame alignment has been confirmed.

3.1.2 *Recovery of frame alignment*

3.1.2.1 *Frame alignment recovery time*

The frame alignment recovery time is specified in terms of the maximum average reframe time in the absence of errors. The maximum average reframe time is the average time to reframe when the maximum number of bit positions must be examined for locating the frame alignment signal.

The maximum average reframe time should be less than 5 ms.

3.1.2.2 *Strategy for frame alignment recovery*

Frame alignment should be recovered by detecting three consecutive correct frame alignment signals. In addition to this, the CRC-5 code (see § 3.2) should be coupled with the framing algorithm to ensure that a valid frame alignment signal contained within the F-bits is the only pattern onto which the reframe circuit can permanently lock. This procedure is illustrated in Figure 1/G.706.

3.2 *CRC bit monitoring*

Error monitoring by CRC-5 assumes a signal quality sufficient for frame alignment to be established so that the CRC-5 bits can be correctly accessed.

3.2.1 *Monitoring procedure*

i) A received sequence of 3156 serial bits (i.e. 3151 bits of CMB and 5 CRC bits) is divided by the generator polynomial defined in Recommendation G.704.

ii) If the remainder resulting from the division process is 00000, it is assumed that the checked CMB is error-free.

3.2.2 *Monitoring for false frame alignment* (see § A.1.1)

The procedure in § 3.1.2.2 should be followed when the CRC-5 code is used to provide immunity against false frame alignment signal.

Using the CRC-5 code, it should be possible to detect false frame alignment within 1 second and with greater than 0.99 probability. On detection of such an event, a re-search for correct frame alignment should be initiated.

With a random error ratio of 10^{-4}, the mean time between two events of falsely initiating a search for frame alignment due to an excessive number of errored CRC message blocks should be more than one year.

Note 1 – With a random error ratio of approximately 10^{-3}, it is almost impossible to distinguish whether CRC errors are caused by the false frame alignment or by transmission bit errors.

Note 2 – To achieve the probability bounds stated above, one method is to count the errored CRC-5 message blocks with the understanding that a count of 32 consecutive errored CRC-5 blocks indicates false frame alignment.

3.2.3 *Error performance monitoring using CRC-5* (see § A.1.2)

For the purpose of error performance monitoring, it should be possible to obtain indications for each CRC message block which is received in error. The consequent error information should be used in accordance with the requirements to be defined in the respective equipment Recommendations.

4 Frame alignment and CRC procedures at 2048 kbit/s interface

4.1 *Loss and recovery of frame alignment*

4.1.1 *Loss of frame alignment*

Frame alignment will be assumed to have been lost when three consecutive incorrect frame alignment signals have been received.

Note 1 – In addition to the preceding, in order to limit the effect of spurious frame alignment signals, the following procedure may be used:

Frame alignment will be assumed to have been lost when bit 2 in time slot 0 in frames not containing the frame alignment signal has been received with an error on three consecutive occasions.

Note 2 – Loss of frame alignment can also be invoked by an inability to achieve CRC multiframe alignment in accordance with § 4.2, or by exceeding a specified count of errored CRC message blocks as indicated in § 4.3.2.

4.1.2 *Strategy for frame alignment recovery*

Frame alignment will be assumed to have been recovered when the following sequence is detected:

– for the first time, the presence of the correct frame alignment signal;
– the absence of the frame alignment signal in the following frame detected by verifying that bit 2 of the basic frame is a 1;
– for the second time, the presence of the correct frame alignment signal in the next frame.

Note – To avoid the possibility of a state in which no frame alignment can be achieved due to the presence of a spurious frame alignment signal, the following procedure may be used:

When a valid frame alignment signal is detected in frame n, a check should be made to ensure that a frame alignment signal does not exist in frame $n + 1$, and also that a frame alignment signal exists in frame $n + 2$. Failure to meet one or both of these requirements should cause a new search to be initiated in frame $n + 2$.

4.2 *CRC multiframe alignment using information in bit 1 of the basic frame*

If a condition of assumed frame alignment has been achieved, CRC multiframe alignment should be deemed to have occurred if at least two valid CRC multiframe alignment signals can be located within 8 ms, the time separating two CRC multiframe alignment signals being 2 ms or a multiple of 2 ms. The search for the CRC multiframe alignment signal should be made only in basic frames not containing the frame alignment signal.

If multiframe alignment cannot be achieved within 8 ms, it should be assumed that frame alignment is due to a spurious frame alignment signal and a re-search for frame alignment should be initiated.

Note 1 – The re-search for frame alignment should be started at a point just after the location of the assumed spurious frame alignment signal. This will usually avoid realignment onto the spurious frame alignment signal.

Note 2 – Consequent actions taken as a result of loss of frame alignment should no longer be applied once frame alignment has been recovered. However, if CRC multiframe alignment cannot be achieved within a time limit in the range of 100 ms to 500 ms, e.g. owing to the CRC procedure not being implemented at the transmitting side, consequent actions should be taken equivalent to those specified for loss of frame alignment.

4.3 *CRC bit monitoring*

If frame and CRC multiframe alignment have been achieved, the monitoring of the CRC bits in each sub-multiframe should commence.

4.3.1 *Monitoring procedure*

i) A received CRC sub-multiframe (SMF) is acted upon by the multiplication/division process defined in Recommendation G.704 after having its CRC bits extracted and replaced by 0s.

ii) The remainder resulting from the division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.

iii) If the remainder exactly corresponds to the CRC bits contained in the next SMF of the received signal, it is assumed that the checked SMF is error-free.

4.3.2 *Monitoring for false frame alignment* (see § A.1.1)

It should be possible to detect a condition of false frame alignment within 1 second and with a probability greater than 0.99. On detection of such an event, a re-search for frame alignment should be initiated.

With a random error ratio of 10^{-3} the probability of falsely initiating a search for frame alignment due to an excessive number of errored CRC blocks should be less than 10^{-4} over a 1 second period.

Figure 2/G.706 shows an illustration of the procedure to be followed in passing from the frame alignment search to error monitoring using CRC.

Note 1 – The re-search for frame alignment should be started at a point just after the location of the assumed spurious frame alignment signal. This will usually avoid realignment onto the spurious frame alignment signal.

Note 2 – To achieve the probability bounds stated above, a preferred threshold count is 915 errored CRC blocks out of 1000, with the understanding that a count of $\geqslant 915$ errored CRC blocks indicates false frame alignment.

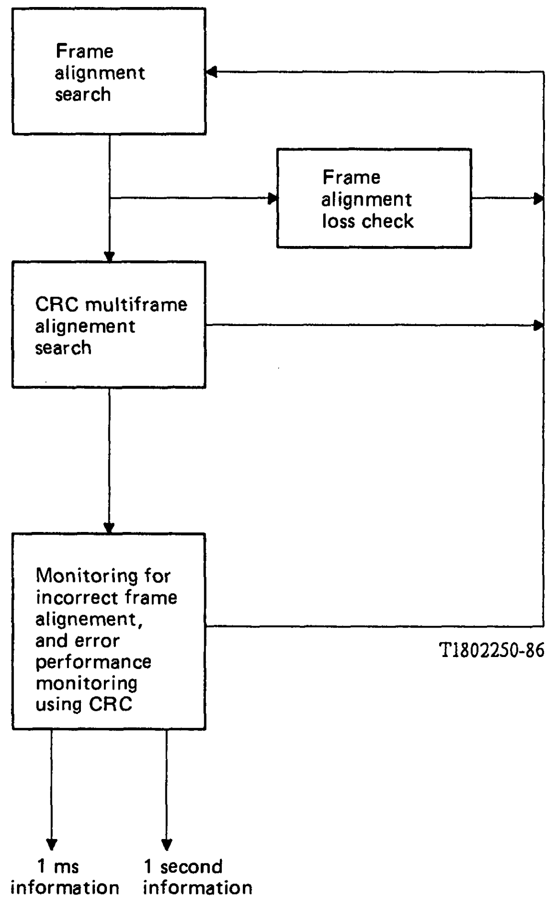


FIGURE 2/G.706

Procedure to be followed in passing from the frame alignment search to error monitoring using a cyclic redundancy check (CRC) (2048 kbit/s)

4.3.3 *Error performance monitoring using CRC-4* (see § A.1.2)

Information on the status of the CRC processing should be made available in two forms:

a) *Direct information*

Every time a CRC block is detected in error, it will be necessary to indicate this condition.

b) *Integrated information*

In consecutive 1 second periods, the number of errored CRC blocks should be made available. This number will be in the range 0 to 1000 (decimal).

5 Frame alignment and CRC procedures at 8448 kbit/s interface

For further study.

ANNEX A

(to Recommendation G.706)

Background information on the use of cyclic redundancy check (CRC) procedures

A.1 *Reasons for application of CRC*

CRC procedures can be used for both protection against false frame alignment and for bit error monitoring.

A.1.1 *Protection against false frame alignment*

The CRC procedures are used to protect against false frame alignment of receivers of multiplex signals. For example, false frame alignment could occur in an ISDN if a user imitates a frame alignment signal in his non-voice terminal. However, since a user is not controlling the composition of a multiplex frame, the addition of CRC bits, and evaluation of these bits in the receiver, leads to detection of the false frame alignment.

A.1.2 *Bit error monitoring*

The CRC procedure is also used for improved bit error ratio monitoring if low values of error ratio (e.g. 10^{-6}) are to be considered. CRC monitoring (like monitoring of the frame alignment signal) takes account of the entire digital link between the source and sink of a multiplex signal, as opposed to code violation monitoring (e.g. monitoring of AMI, HDB3 or B8ZS violations) which concerns only the digital line section nearest to the receiver, or in many cases only an interface line [e.g. between a digital multiplexer and an Exchange Terminal (ET)].

A.2 *Limitations of CRC procedures*

A.2.1 *Probability of undetected bit errors*

It can be estimated [1] that for CRC-*n*, and long message/check blocks, the probability that an error remains undetected approaches 2^{-n} even with a high bit error ratio; with a low bit error ratio, the probability is lower. The resulting inaccuracy (at most, with CRC-4, about 6% of blocks with undetected errors; similarly, with CRC-6, 1.6%) is tolerable for the required purpose.

A.2.2 *Limitation of application to bit error ratio measurement*

The CRC monitoring procedure is not well suited to measure values of bit error ratio that are so high that on average every message/check block contains at least one bit error (i.e. for BER = 10^{-3} or higher).

Reference

[1] LEUNG, C. and WITZKE, K.A. – A comparison of some error detecting CRC code standards. *IEEE Trans.* Vol. COM-33, pp. 996-998, 1985.

Recommendation G.707

SYNCHRONOUS DIGITAL HIERACHY BIT RATES

(Melbourne, 1988)

The CCITT,

considering

(a) that Recommendation G.702 specifies a number of digital hierarchy bit rates for 1544 kbit/s and 2048 kbit/s based digital networks;

(b) that the various hierarchy levels specified in Recommendation G.702 are interconnected by means of digital multiplexing employing justification methods;

(c) that synchronous digital multiplexing and a related synchronous digital hierarchy offer advantages such as:

- simplified multiplexing/demultiplexing techniques;
- direct access to lower speed tributaries, without need to multiplex/demultiplex the entire high speed signal;
- enhanced Operations, Administration and Maintenance (OAM) capabilities;
- easy growth to higher bit rates in step with the evolution of transmission technology;

(d) that the synchronous digital hierarchy rates need to be chosen such that they allow the transport of digital signals:

- at hierarchical bit rates as specified in Recommendation G.702;
- at broadband channel bit rates;

(e) that Recommendation G.708 specifies the Network Node Interface (NNI) for the synchronous digital hierarchy;

(f) that Recommendation G.709 specifies the synchronous multiplexing structure;

(g) that Recommendations G.707, G.708 and G.709 form a coherent set of specifications for the synchronous digital hierarchy and NNI.

recommends

(1) that the first level of the synchronous digital hierarchy shall be 155 520 kbit/s;

(2) that higher synchronous digital hierarchy bit rates shall be obtained as integer multiples of the first level bit rate;

(3) that higher synchronous digital hierachy levels should be denoted by the corresponding multiplication factor of the first level rate;

(4) that the following bit rates should constitute the synchronous digital hierarchy:

TABLE 1/G.707

Synchronous digital hierarchy level	Hierarchical bit rate kbit/s
1	155 520
4	622 080

Note – The specification of higher synchronous digital hierarchy levels requires further study. Possible candidates are:

Level	*Bit rate*
8	1 244 160 kbit/s
12	1 866 240 kbit/s
16	2 488 320 kbit/s

NETWORK NODE INTERFACE FOR THE SYNCHRONOUS DIGITAL HIERARCHY

(Melbourne, 1988)

The CCITT,

considering

(a) that network node interface (NNI) specifications are necessary to enable interconnection of synchronous digital network elements for transport of payloads, including digital signals of the asynchronous hierarchy defined in Recommendation G.702;

(b) that Recommendation G.707 describes the advantages offered by a synchronous digital hierarchy and multiplexing method and specifies a set of synchronous digital hierarchy bit rates;

(c) that Recommendation G.709 specifies the multiplexing structures;

(d) that Recommendations G.707, G.708 and G.709 form a coherent set of specifications for the synchronous digital hierarchy and NNI;

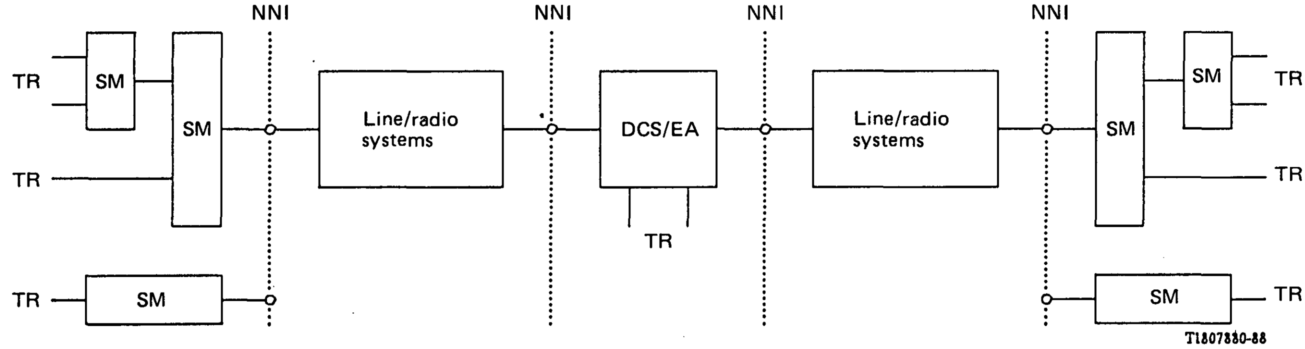
(e) that Recommendation G.802 specifies the interworking between networks based on different asynchronous digital hierarchies and speech encoding laws,

recommends

that the frame structure for multiplexed digital signals at the network node interface of a synchronous digital network including ISDN should be as described in this Recommendation.

1 Location of NNI

Figure 1-1/G.708 gives a possible network configuration to illustrate the location of the network node interface specified in this Recommendation.



DCS Digital crossconnect system
EA External access equipment
SM Synchronous multiplexer
TR Tributaries

FIGURE 1-1/G.708

Location of the NNI

2 Basic multiplexing principle and multiplexing elements

2.1 *General*

Frame structures and overheads in this Recommendation are mainly in the context of circuit mode connection types rather than asynchronous transfer mode (ATM). ATM based multiplexing principles are under study.

Figure 2-1/G.708 shows the relationship between various multiplexing elements that are defined below, and illustrates possible multiplexing structures.

Figures 2-2/G.708, 2-3/G.708 and 2-4/G.708 are examples of how various signals are multiplexed using these multiplexing elements.

The legends used in these figures are defined in § 2.2.

Details of the multiplexing method and mappings are given in Recommendation G.709.

Note – When signals at bit rates of the various multiplexing elements of the synchronous digital hierarchy (Recommendations G.707, G.708, G.709) are different from existing hierarchy levels in Recommendation G.702, the signals are not required to be transported via digital networks which are in line with Recommendation G.702.

2.2 *Definitions*

2.2.1 *Container, C-n (n = 1 to 4)*

This element is a defined unit of payload capacity which is dimensioned to carry any of the levels currently defined in Recommendation G.702 and may also provide capacity for transport of broadband signals which are not yet defined.

2.2.2 *Virtual container, VC-n*

Two types of virtual containers have been identified:

– *Basic virtual container, VC-n (n = 1, 2)*

  This element comprises a single C-*n (n = 1, 2)* plus the basic virtual container path overhead (POH) appropriate to that level.

– *Higher order virtual container to VC-n (n = 3, 4)*

  This element comprises a single C-*n (n = 3, 4)*, an assembly of tributary unit groups (TUG-2s) or an assembly of TU-3s, together with virtual container POH appropriate to that level.

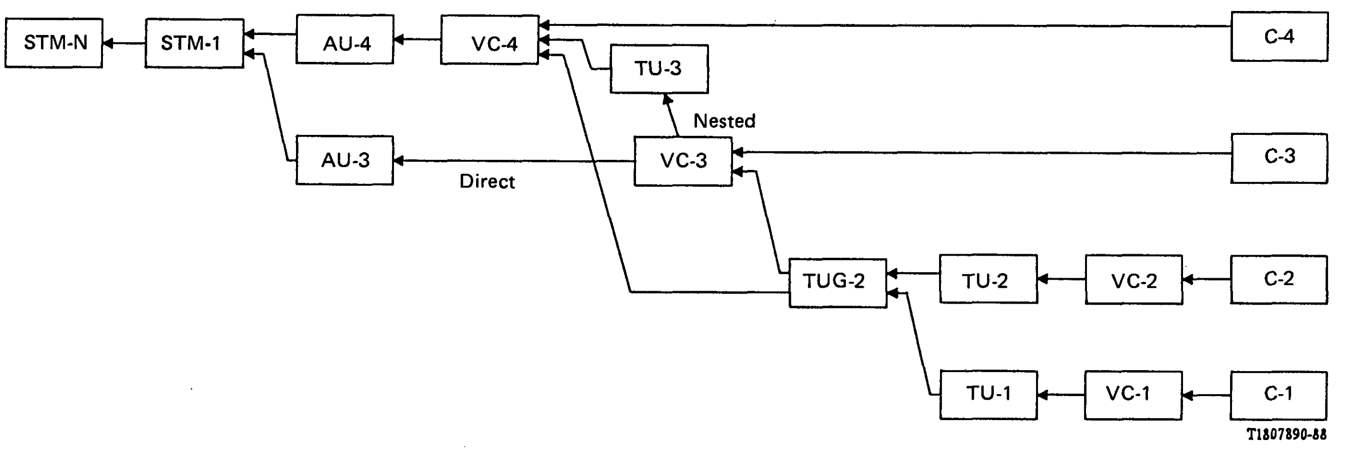
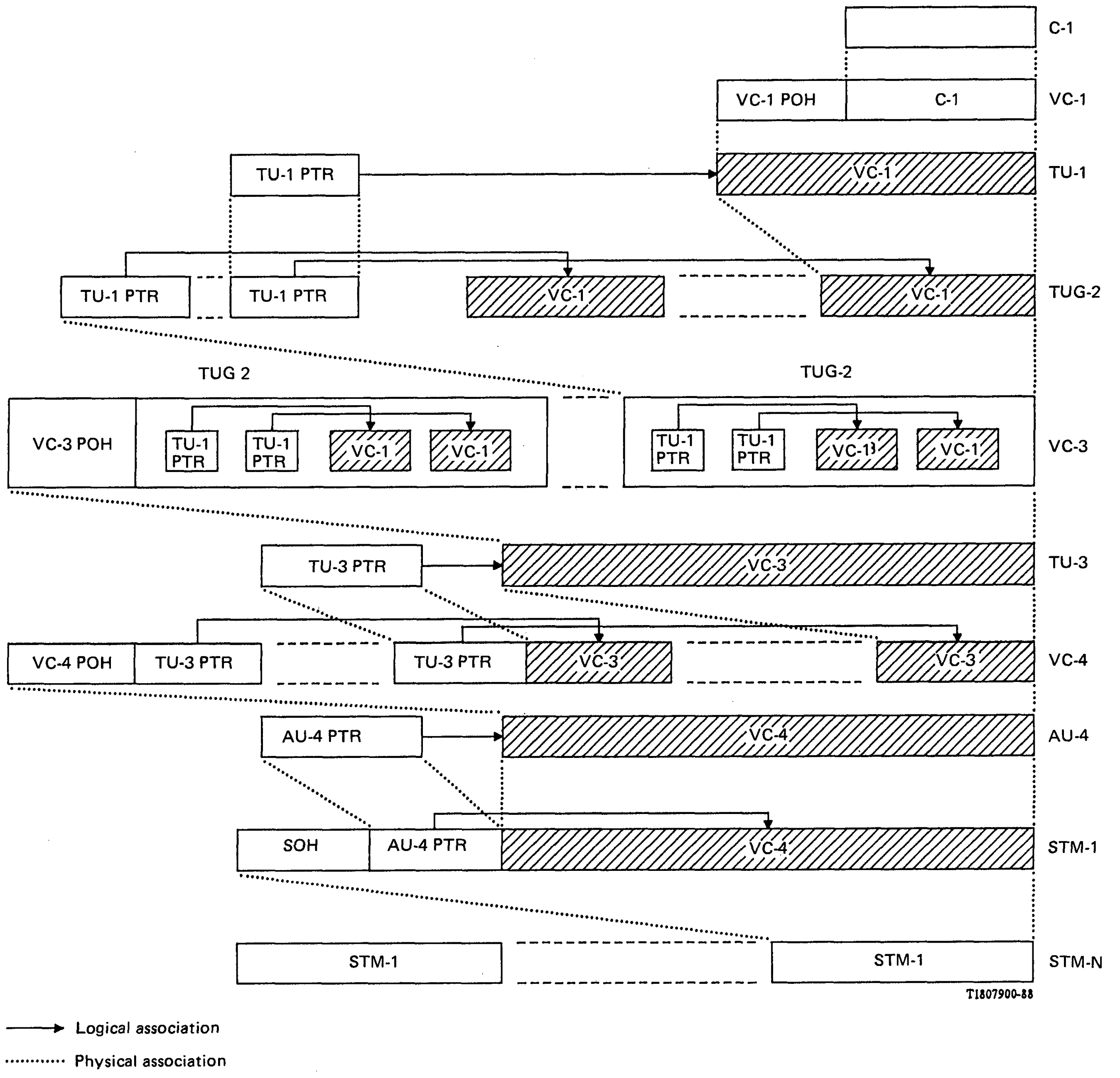


FIGURE 2-1/G.708

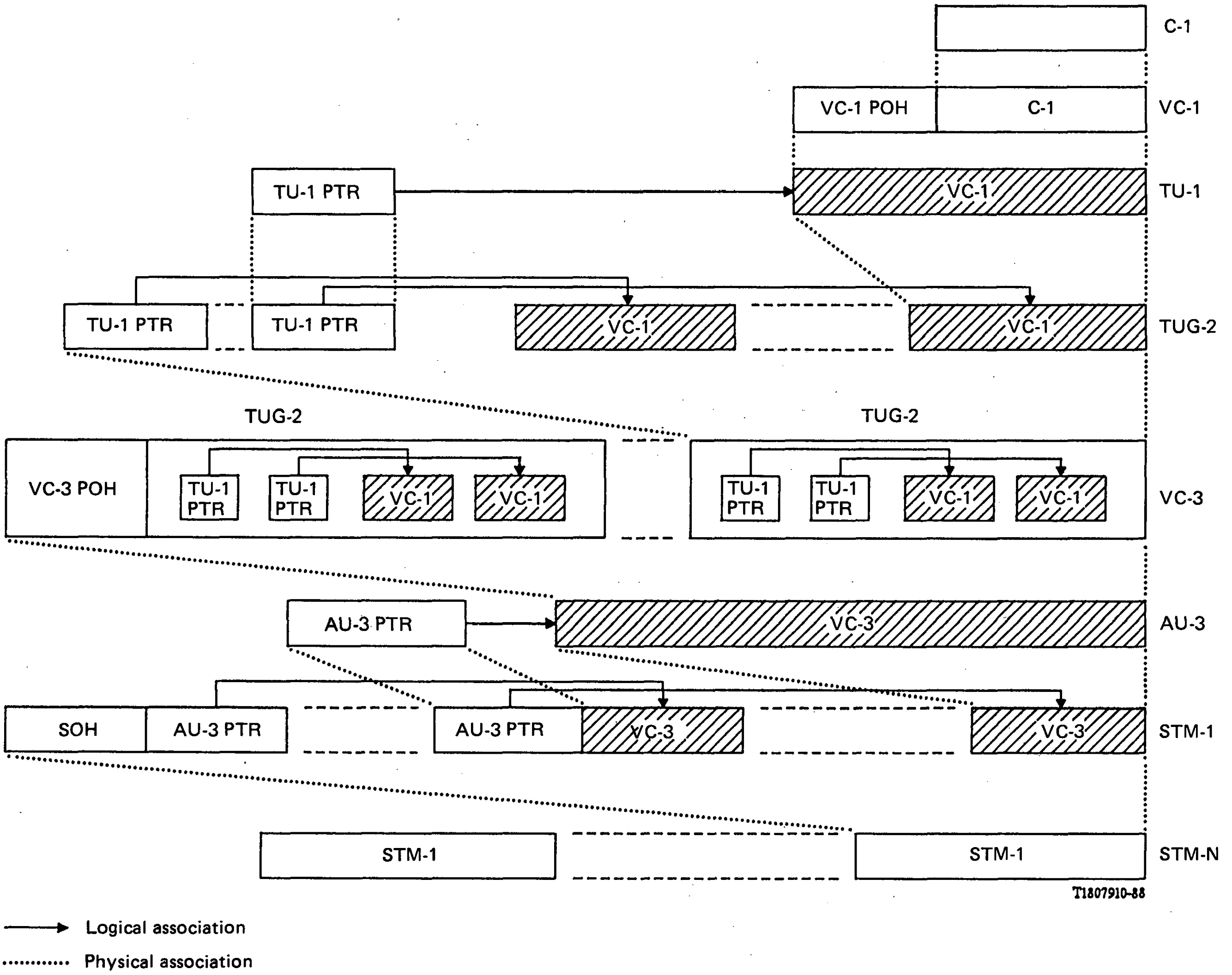
Generalized multiplexing structure



Note – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer and is indicated by the arrow.

FIGURE 2-2/G.708

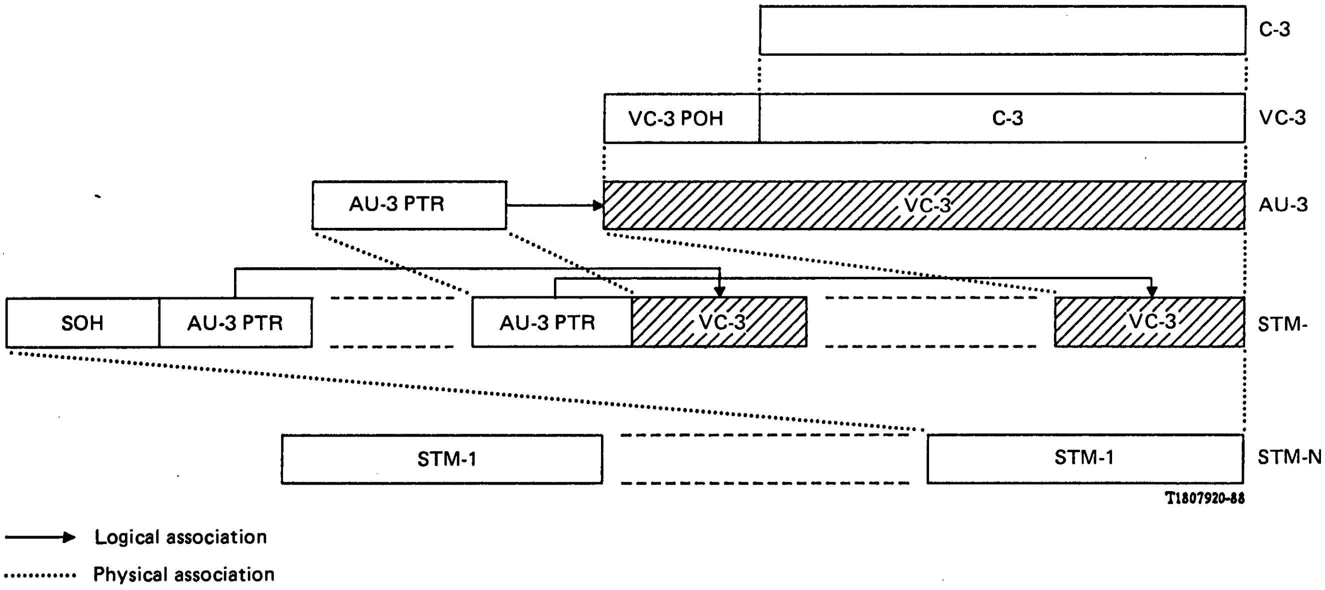
Multiplexing method: nested arrangement



Note — Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer and is indicated by the arrow.

FIGURE 2-3/G.708

Multiplexing method: directly from C-1



Note — Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer and is indicated by the arrow.

FIGURE 2-4/G.708

Multiplexing method: directly from C-1

2.2.3 *Tributary unit TU-n (n = 1 to 3)*

This element consists of a virtual container plus a tributary unit pointer. A tributary unit pointer indicates the phase alignment of the virtual container (VC-*n*) with respect to the POH of the next higher level virtual containers in which it resides. The tributary unit pointer location is fixed with respect to this higher level POH.

In certain applications (for example, synchronous mapping providing direct observability of 64 kbit/s channels) the basic virtual container has a fixed phase-alignment with respect to the higher level virtual container. In this case, the basic virtual container (VC-1) POH and TU-1 pointer are null.

2.2.4 *Tributary unit group, TUG-2*

This element consists of a homogeneous assembly of TU-1s or a single TU-2.

2.2.5 *Administrative unit, AU-n (n = 3, 4)*

This element consists of a VC-*n* (*n*= 3, 4) plus an administrative unit pointer (AU PTR). An administrative unit pointer indicates the phase alignment of the VC-*n (n = 3, 4)* with respect to the STM-1 frame. The administrative unit pointer location is fixed with respect to the STM-1 frame.

2.2.6 *Synchronous transport module level 1, STM-1*

This element is the basic building block of the synchronous digital hierarchy and it comprises either one AU-4 or multiple AU-3s, together with the section overhead (SOH).

2.2.7 *Synchronous transport module level N, STM-N*

This element defines the N-th level of the synchronous-digital hierarchy and contains N synchronously multiplexed STM-1 signals.

The STM-N-signal can be obtained via single-or multiple-stage multiplexing.

Values of N correspond to the synchronous digital hierarchy levels given in Recommendation G.707.

3 Frame structure

3.1 *Level 1: 155 520 kbit/s (STM-1)*

3.1.1 *Basic frame structure*

The STM-1 frame structure is shown in Figure 3-1/G.708. The three main areas of the STM-1 frame are indicated:

- section overhead;
- AU pointers;
- STM-1 payload.

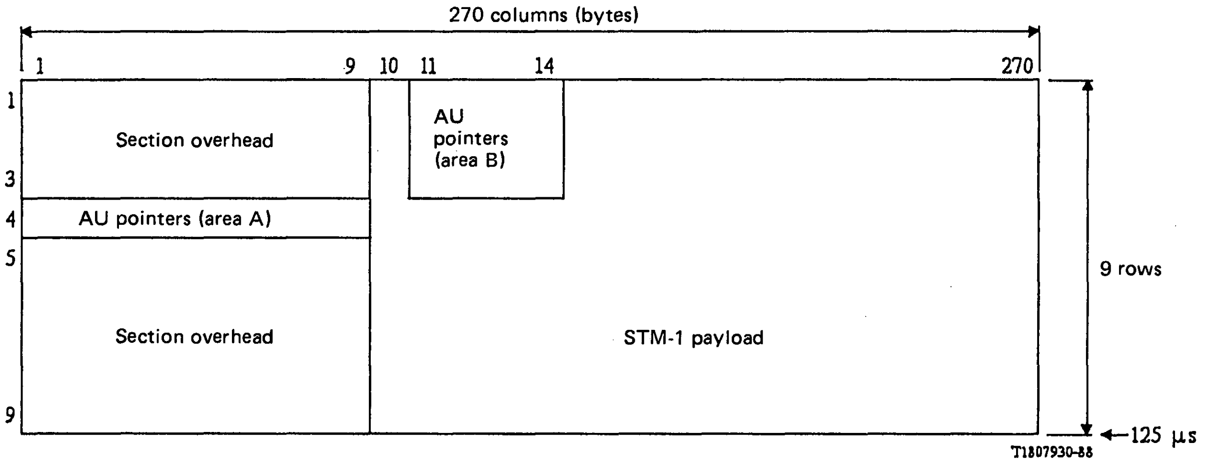


FIGURE 3-1/G.708

STM-1 frame structure

3.1.2 *Section overhead*

Rows 1-3 and 5-9 of columns 1-9 of the STM-1 in Figure 3-1/G.708 are dedicated to the section overhead.

The allocation of section overhead capacity and functions is given in Figure 3-4a/G.708. An explanation of the overhead functions is given in § 5.

3.1.3 *Administrative unit (AU) pointers*

Row 4 of columns 1-9 and row 1-3 of columns 11-14 in Figure 3-1/G.708 are available for AU pointers. The positions of the pointers of the AUs for different organizations of the STM-1 payload are shown in Table 3-1/G.708. The application of pointers and their detailed specifications are given in Recommendation G.709.

TABLE 3-1/G.708

Position of AU pointers

AU	Position of AU pointer
31	Areas A and B
32	Area A
4	Area A

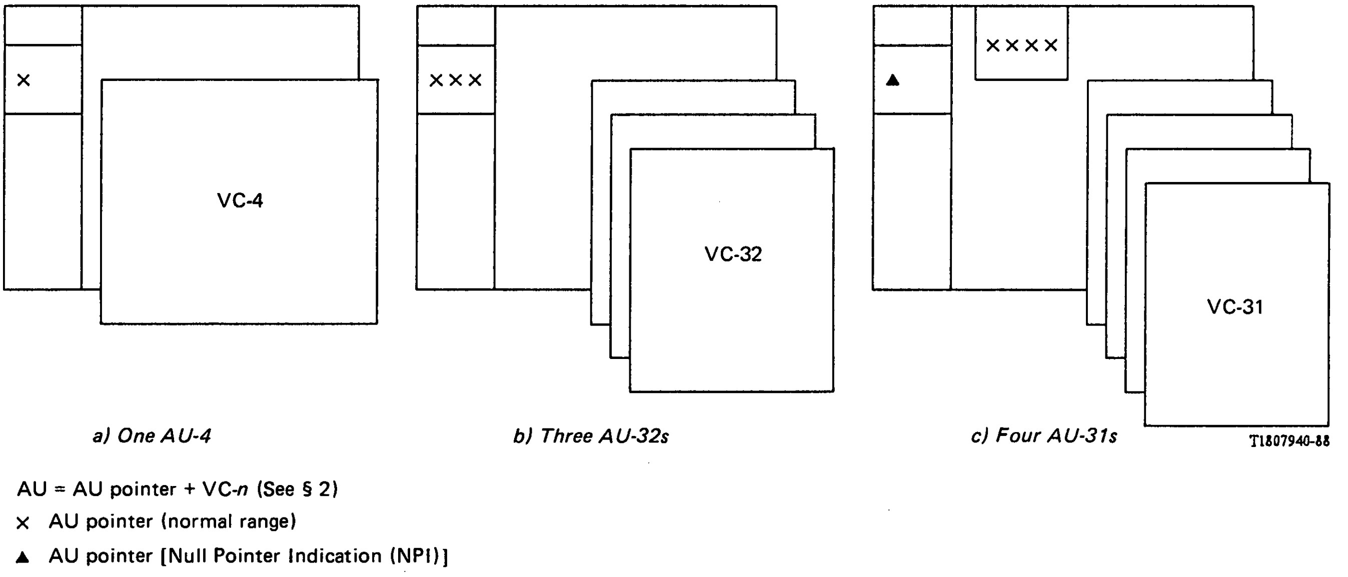
3.1.4 *Administrative units in the STM-1*

The STM-1 payload can suppport the following types and numbers of administrative units:

– one AU-4; or three AU-32s; or four AU-31s.

The VC-*n* associated with each AU-*n* does not have a fixed phase with respect to the STM-1 frame. The location of the first byte of the VC-*n* is indicated by the AU-*n* pointer. The AU-*n* pointer is in a fixed location in the STM-1 frame as illustrated in Figures 2-2/G.708 to 2-4/G.708 and 3-1/G.708 to 3-3/G.708.

The AU-4 may be used to carry, via the VC-4, three TU-32s or four TU-31s. This nested arrangement is illustrated in Figures 3-2/G.708 and 3-3/G.708. The VC-3 associated with each TU-3 does not have a fixed phase relationship with respect to the start of the VC-4. The TU-3 pointer is in a fixed location in the VC-4 and the location of the first byte of the VC-3 is indicated by the TU-3 pointer (illustrated in Figures 3-2/G.708 and 3-3/G.708).



Note – Definitions of pointer value (normal range and NPI) are given in Figure 3-4/G.709.

FIGURE 3-2/G.708

Administrative units in STM-1 frame

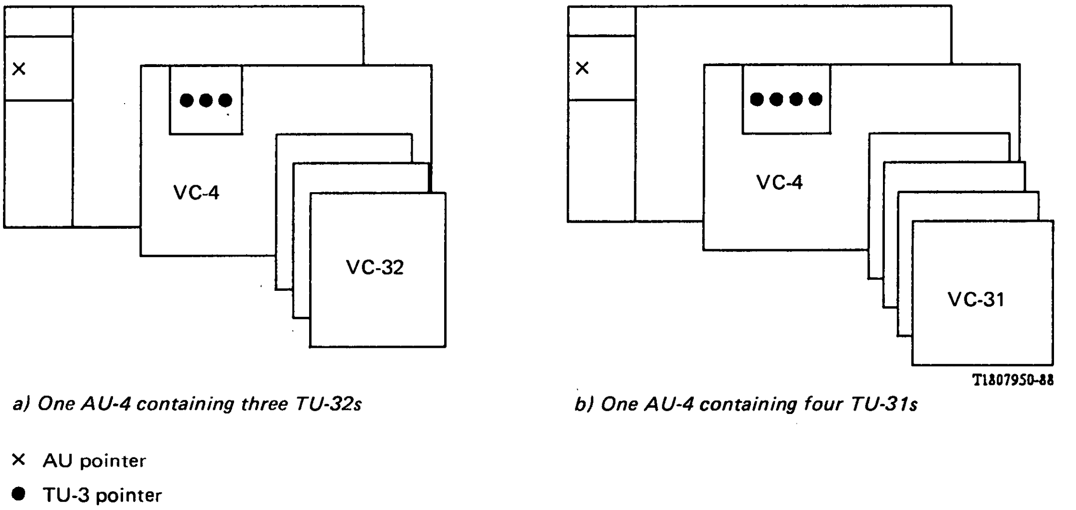


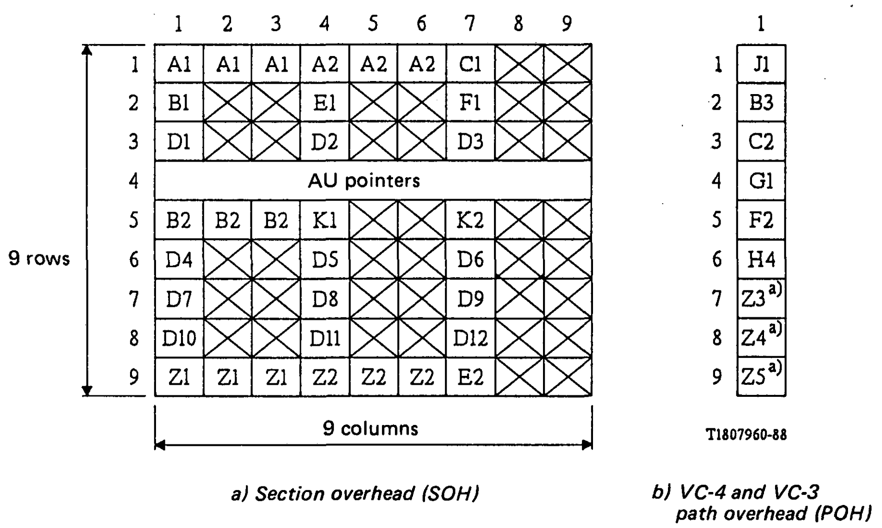
FIGURE 3-3/G.708

Use of the AU-4 to carry TU-3s

3.1.5 *VC-4 and VC-3 path overheads*

The allocation of the VC-4 and VC-3 path overhead capacity and functions is given in Figure 3-4/G.708. An explanation of the overhead functions is given in § 5.

The position of the VC-4 and VC-3 path overhead is specified in Recommendation G.709.



Bytes reserved for national use

a) These bytes are not included in the VC-31 POH.

Note – The use of some of the Z bytes for national purposes is for further study.

FIGURE 3-4/G.708

Overhead bytes assignment in the STM-1 frame

3.2 *Level 4: 622 080 kbit/s (STM-4)*

This level is obtained by one-byte interleaving of four STM-1s as illustrated in Figure 3-5/G.708.

The SOH of the STM-1s shall be 125 s phase aligned prior to multiplexing such that the SOH of the resulting STM-4 is contained in the first 36 columns. The AU pointer value(s) of each STM-1 is/are adjusted to indicate the start of the VC(s) with respect to this new position of the AU pointer(s) which is fixed relative to the STM-4 SOH.

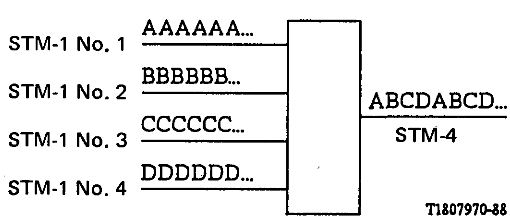


FIGURE 3-5/G.708

STM-1 to STM-4 synchronous multiplexing

4 Interconnection of STM-1s

The synchronous digital hierarchy, specified in Recommendations G.707, G.708 and G.709, is designed to be universal, allowing transport of a large variety of signals including those specified in Recommendation G.702.

However, there are a number of options for structuring an STM-1. This section provides guidelines for the interconnection of STM-1s. Two general cases are considered:

- Case 1: STM-1s having the same structure (detailed in § 4.1);
- Case 2: STM-1s having different structures (detailed in § 4.2).

4.1 *Interconnection of STM-1s having the same structure*

The interconnection unit used between STM-1s is the VC associated with the AU. This arrangement is shown in row i) of Table 4-1/G.708.

4.2 *Interconnection of STM-1s having different structures*

In the case of STM-1s having different structures, the following guidelines should be used to facilitate interconnection by bilateral agreement or to resolve contention.

The method of interconnection between STM-1s having different structures depends on whether the type of AU is different or whether the type of TUG is different. The cases are considered in three categories:

- different types of AU-3s carrying a C-3 payload;
- different types of AU carrying the same type of TUG-2;
- different types of TUG-2s.

4.2.1 *Different types of AU-3s carrying a C-3 payload*

For the interconnection of different types of AU-3s carrying a C-3 payload, the C-3 payload is transferred from the AU-3 to a corresponding TU-3. This TU-3 is then assembled into a VC-4 using the nested approach illustrated in Figure 3-3/G.708. This arrangement is shown in row ii) of Table 4-1/G.708, and is intended to facilitate the transit of C-3 in a VC-3 across a network which cannot support the associated AU-3.

4.2.2 *Different types of AU carrying the same type of TUG*

For the interconnection of a different type of AU carrying the same type of TUG-2, the TUG-2s are transferred between the dissimilar AUs. In the absence of bilateral agreement on an AU-3 type, the AU-4 shall be used. This arrangement is shown in row iii) of Table 4-1/G.708.

4.2.3 *Different types of TUG-2s*

For the interconnection of different types of TUG-2s, the TU-1s are transferred from the TUG-22 to the TUG-21. The TUG-21 is used as the interconnection unit. In the absence of bilateral agreement on an AU-3 type, the TUG-21s are directly assembled into a VC-4. This arrangement is shown in row iv) of Table 4-1/G.708.

The method of interconnection between an AU-31 containing TUG-21s and an AU-31 containing TUG-22s is for further study.

5 Overhead functions

5.1 *Types of overhead*

Several types of overhead have been identified for application in the synchronous digital hierarchy. The types of overhead described below and their applications are shown in Figure 5-1/G.708.

5.1.1 *Section overhead (SOH)*

Section overhead capacity is added to either an AU-4 or an assembly of AU-3s to create an STM-1. The content always includes STM-1 framing. Content representing section performance monitoring and other maintenance and operational functions can be added or modified without disassembly of the STM-1, as appropriate, for various configurations of elements (e.g. intermediate regenerator monitoring, protection switching control).

TABLE 4-1/G.708

Interconnection of STM-1s

	STM-1 structure A	Conversion steps	Interconnection: STM-1 structure if needed	Interconnection: Intercon-nection unit	Conversion steps	STM-1 structure B	Parameters
i)	AU-x/C-x or TUG-2p	AU-x $\rightarrow$ VC-x	AU-x	VC-x	VC-x $\leftarrow$ AU-x	AU-x/C-x or TUG-2p	x = 4, 32 or 31 p = 1 or 2
ii)	AU-3x/C-3x	AU-3x $\rightarrow$ VC-3x $\rightarrow$ TU-3x $\rightarrow$ $\rightarrow$ VC 4	AU-4	VC-4	VC-4 $\leftarrow$ AU-4	AU-4/TU-3x/C-3x	x = 1 or 2
iii)	AU-x/TUG-2p	AU-x $\rightarrow$ VC-x $\rightarrow$ TUG-2p	AU-y [a)]	TUG-2p	TUG-2p $\leftarrow$ VC-z $\leftarrow$ AU-z	AU-z/TUG-2p	x = 4, 32 or 31 y = 4, 32 or 31 z = 4, 32 or 31; $z \neq x$ p = 1 or 2
iv)	AU-x/TUG-22/TU-1p	AU-x $\rightarrow$ VC-x $\rightarrow$ TUG-21	AU-y [a)]	TUG-21	TUG-21 $\leftarrow$ TU-1p $\leftarrow$ TUG-22 $\leftarrow$ $\leftarrow$ VC-z $\leftarrow$ AU-z	AU-z/TUG-22/TU-1p	x = 4, 32 or 31 y = 4, 32 or 31 z = 4 or 31; $z \neq x$ p = 1 or 2 (see note)

/ Item to the left is carrying item to the right.

$\rightarrow$ Conversion "From $\rightarrow$ To" (to arrive at the interconnection unit).

a) In the absence of a bilateral agreement on an AU-3, an AU-4 should be used.

Note – The case where x = 31 and z = 31 is for further study.

5.1.2 *Virtual container path overhead (POH)*

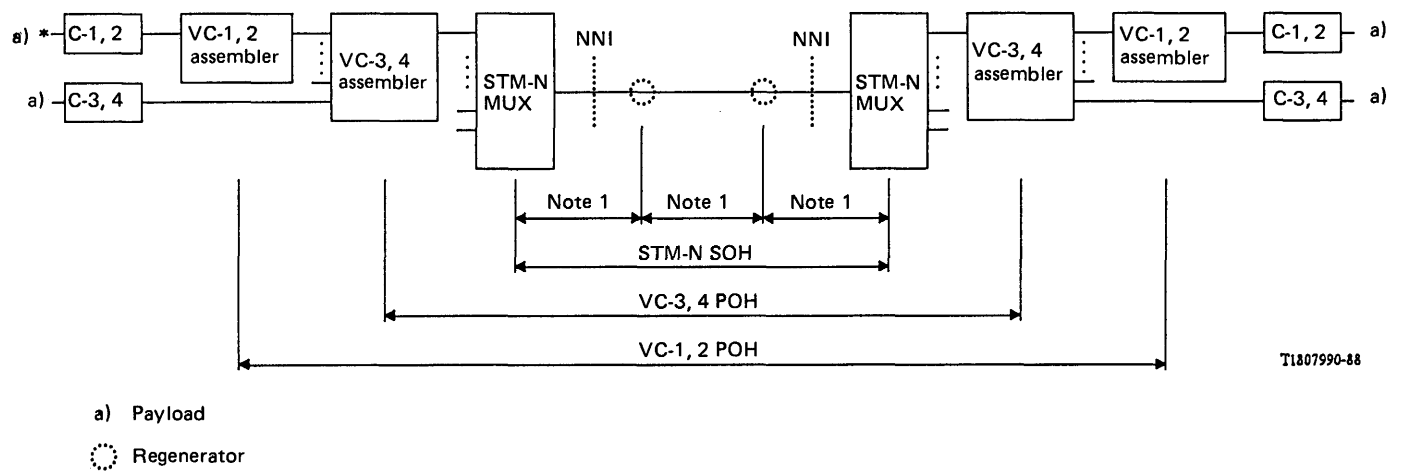
Virtual container path overhead provides for communication between the point of assembly of a virtual container and its point of disassembly. Two categories of virtual container path overhead have been identified:

– *Basic virtual container path overhead (VC-1, 2 POH)*

  Basic virtual container POH is added to the container (C-1, 2) when the VC-1, 2 is created. Among the functions included in this overhead are virtual container path performance monitoring, signals for maintenance purposes and alarm status indications.

– *Higher order virtual container path overhead (VC-3, 4 POH)*

  VC-3 POH is added to either an assembly of TUG-2s or a C-3 to form a VC-3. VC-4 POH is added to either an assembly of TU-3s or a C-4 to form a VC-4. Among the functions included within this overhead are virtual container path performance monitoring, alarm status indications, signals for maintenance purposes and multiplex structure indications (VC-3,4 composition).



Note 1 – The need to dedicate some of the section overhead to monitoring of intermediate network elements (i.e. regenerators, or radio or satellite links) is for further study.

Note 2 – This figure shows a functional grouping associated with the proper termination of the signal. Note that the specific function outlined may be performed with one or more pieces of equipment.

Note 3 – POH may be connected through cross-connects or other MUX equipment.

FIGURE 5-1/G.708

Overhead entities – an example

5.2 *Overhead descriptions*

The location of the various section and VC-3, 4 path overhead bytes in the STM-1 frame is illustrated in Figure 3-4/G.708.

5.2.1 *SOH byte descriptions*

5.2.1.1 *Framing: A1, A2*

Six bytes are dedicated to each STM-1. The pattern shall be A1A1A1A2A2A2 (A1 = 11110110, A2 = 00101000). These bytes shall be provided in all STM-1 signals within an STM-N.

5.2.1.2 *Data communication channel: D1-D12*

Twelve bytes are allocated for section data communication. These bytes are defined only for STM-1 No. 1 of an STM-N signal.

5.2.1.3 *STM identifier: C1*

This is a unique number assigned to an STM-1 prior to it being multiplexed to a higher STM-N level. Upon demultiplexing, this byte may be used to identify the position of any particular STM-1 within the incoming STM-N signal.

5.2.1.4 *Orderwire: E1, E2*

These two bytes provide orderwire channels for voice communication. These bytes are defined only for STM-1 No. 1 of an STM-N signal.

5.2.1.5 *User channel: F1*

This byte is reserved for user purposes (e.g. network operators). This byte is defined only for STM-1 No. 1 of an STM-N signal.

5.2.1.6 *BIP-8: B1*

One byte is allocated in each STM-1 for a bit error monitoring function of an elementary regenerator section. This function shall be a Bit Interleaved Parity 8 (BIP-8) code using even parity. The BIP-8 is computed over all bits of the previous STM-N frame after scrambling and is placed in byte B1 before scrambling. (For details of the scrambling process, see Recommendation G.709.) The B1 byte shall be monitored and recomputed at every regenerator.

Note – Bit Interleaved Parity-N (BIP-N) code is defined as a method of error monitoring. With even parity, an N bit code is generated by the transmitting equipment over a specified portion of the signal in such a manner that the first bit of the code provides even parity over the first bit of all N-bit sequences in the covered portion of the signal, the second bit provides even parity over the second bit of all N-bit sequences within the specified portion, etc. Even parity is generated by setting the BIP-N bits so that there are an even number of 1s in each of all the N-bit sequences including the BIP-N.

5.2.1.7 *BIP-24: B2* x *3*

Three bytes are allocated in each STM-1 for a bit error monitoring function of a section. This function shall be a Bit Interleaved Parity 24 (BIP-24) code using even parity. The BIP-24 is computed over all bits of the previous STM-1 frame except for the first three rows of section overhead (A1 through D3) and is placed in bytes B2 before scrambling. This parity code is not recomputed at regenerators. These bytes shall be provided in all STM-1 signals within an STM-N signal.

5.2.1.8 *APS channel: K1, K2*

Two bytes are allocated for Automatic Protection Switching (APS) signalling. These bytes are defined only for STM-1 No. 1 of an STM-N signal.

5.2.1.9 *Spare: Z1, Z2*

Six bytes are allocated for functions not yet defined. These bytes have no defined value. These bytes are reserved in all STM-1s of an STM-N.

5.2.2 *AU pointer descriptions*

5.2.2.1 *Pointer value*

Two bytes are allocated for a pointer which indicates the offset in bytes between the pointer and the first byte of the associated virtual container POH. For a complete specification and location of these bytes, see Recommendation G.709.

5.2.2.2 *Pointer action*

Three pointer action bytes are allocated in an AU-4 for frequency justification purposes. One pointer action byte is allocated for AU-3s and TU-*n*s. For a complete specification of these bytes, refer to Recommendation G.709.

In the event of a negative justification, they carry valid information.

5.2.3 *VC-n (n = 3, 4) POH byte descriptions*

5.2.3.1 *Path BIP-8: B3*

One byte is allocated in each virtual container for a path bit error monitoring function. This function shall be a BIP-8 code using even parity. The BIP-8 is computed over all bits of the previous container and is placed in the B3 byte.

5.2.3.2 *Path status: G1*

One byte is allocated to return the VC-*n* path terminating status performance information to the VC-*n* path originating point.

5.2.3.3 *Signal label: C2*

One byte is allocated to indicate the composition of the VC-*n* payload.

5.2.3.4 *VC-*n *path user channel: F2*

One byte is allocated for user communication purposes.

5.2.3.5 *VC-*n *path trace*: *J1*

This byte is used at the VC-*n* termination point to verify the VC-*n* path connection.

5.2.3.6 *Spare: Z3-Z5*

Three bytes are allocated for as yet undefined purposes.

5.2.3.7 *Multiframe indicator: H4*

This byte is allocated to provide a multiframe indication, when required.

6 Physical specification of the NNI

Specification for physical, electrical or optical characteristics of the NNI will be contained in another Recommendation which is under study.

Recommendation G.709

SYNCHRONOUS MULTIPLEXING STRUCTURE

(Melbourne, 1988)

The CCITT,

considering

(a) that Recommendation G.707 describes the advantages offered by a synchronous digital hierarchy and multiplexing method and specifies a set of synchronous digital hierarchy bit rates;

(b) that Recommendation G.708 specifies

- the general principles and frame structure of the network node interface (NNI) for the synchronous digital hierarchy;
- the overall frame size of 9 rows × 270 columns and section overhead (SOH) definition and its byte allocation;
- arrangements for international synchronous interconnection of STM-1s;

(c) that Recommendations G.707, G.708 and G.709 form a coherent set of specifications for the synchronous digital hierarchy and NNI, *recommends*

that the formats for mapping multiplexing elements into the STM-1 at the Network Node Interface (NNI) and the method of multiplexing to STM-N shall be as described in this Recommendation.

1 Basic multiplexing structure

Descriptions of the various multiplexing elements are given in Recommendation G.708.

The relationships between the various multiplexing elements are shown in Figure 1-1/G.709. The detailed multiplexing structure is described in the following sections.

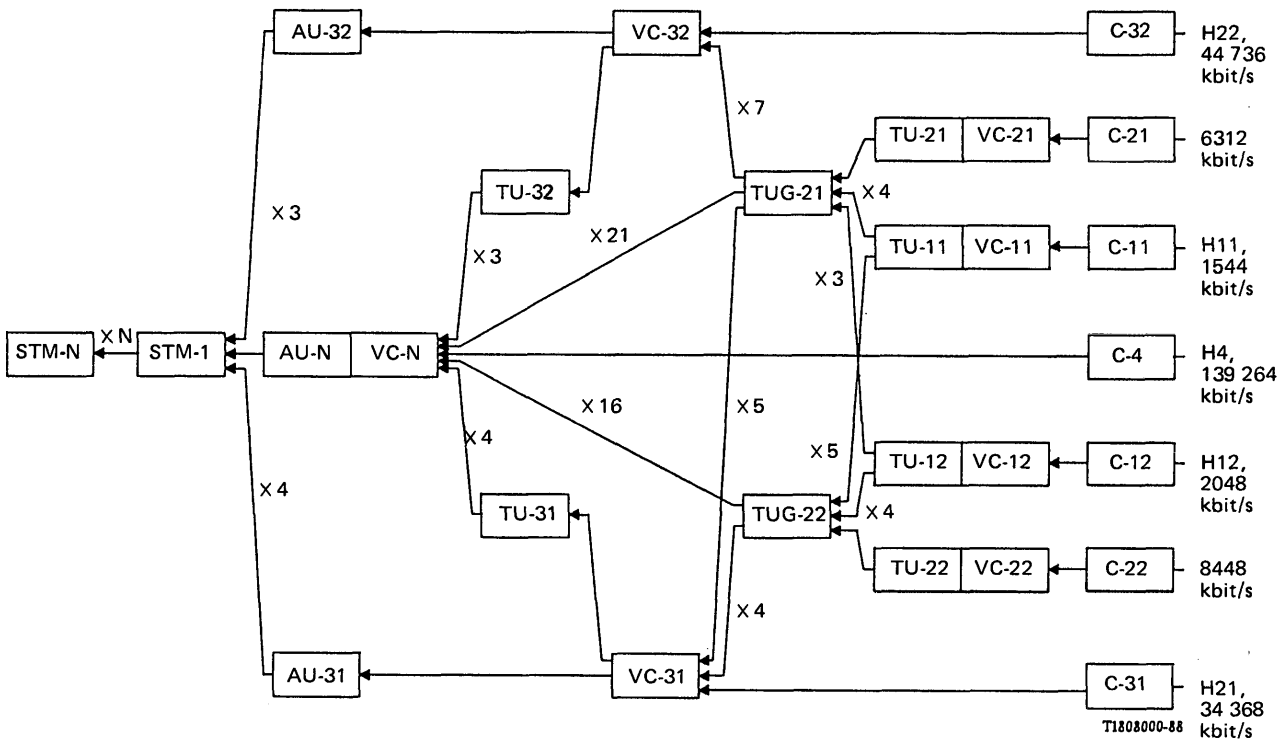


FIGURE 1-1/G.709

Multiplexing structure

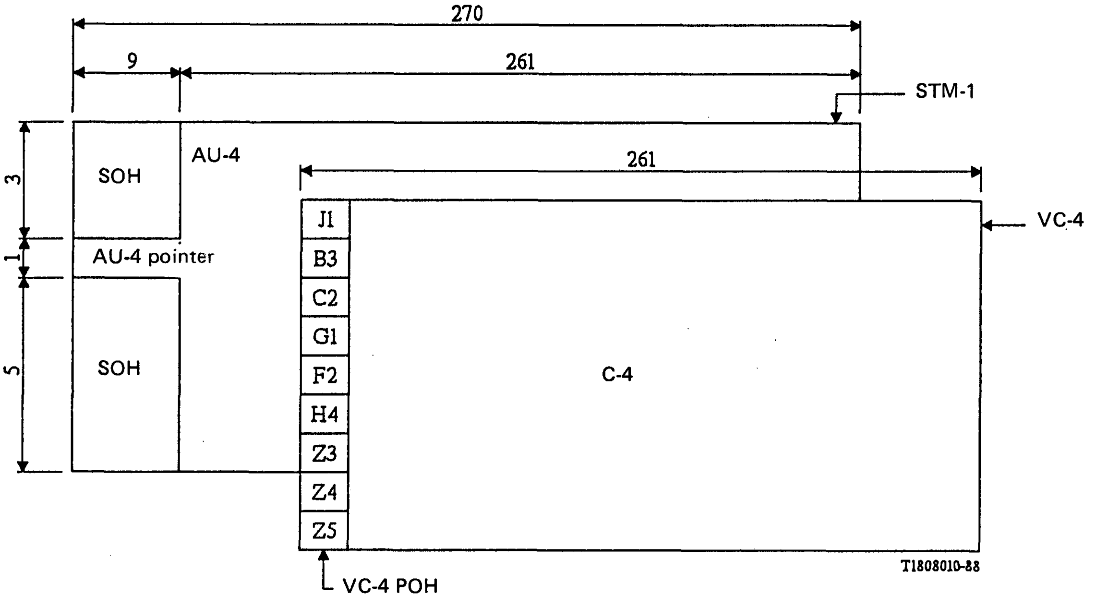
2 Mapping formats and multiplexing method

2.1 *Mapping and multiplexing up to STM-1*

2.1.1 *Mapping of VC-4 into AU-4*

The STM-1 mapping format for transporting one VC-4 in an AU-4 is shown in Figure 2-1/G.709. The VC-4 consists of a 9-row by 261-column payload structure; the first column of the VC-4 is devoted to path overhead (POH). The payload of the VC-4 shown in Figure 2-1/G.709 is a single C-4. Other possible VC-4 payloads include a single 139 264 kbit/s signal in a C-4, four VC-31s (shown in Figure 2-2/G.709 and carried in four TU-31s), three VC-32s (shown in Figure 2-3/G.709 and carried in three TU-32s), and a group of either 21 TUG-21s or 16 TUG-22s (shown in Figure 2-4/G.709).

The STM-1 format shown in Figure 2-1/G.709 consists of an AU-4 plus section overhead (SOH). The VC-4 does not have a fixed phase with respect to the AU-4 (and the STM-1); therefore, the location of the first byte of the VC-4 with respect to the AU-4 frame is given by the AU-4 pointer. Note that the AU-4, including the AU-4 pointer, has a fixed location in the STM-1 frame.



Note – See Figures 5-4/G.709 and 5-5/G.709 for detailed mapping structure.

FIGURE 2-1/G.709

Mapping of VC-4 into an STM-1

2.1.2 *Mapping of four VC-31s into AU-4*

The STM-1 mapping format for transporting four VC-31s in an AU-4 is shown in Figure 2-2/G.709. Each TU-31 consists of a 9-row by 64-column payload structure plus six bytes of POH plus a three-byte TU-31 pointer. The payload of the VC-31 shown in Figure 2-22/G.709 is a single C-31. Other possible VC-31 payloads include a single 34 368 kbit/s signal in a C-31 (shown in Figure 5-10/G.709) or a group of either five TUG-21s or four TUG-22s (shown in Figure 2-5/G.709).

The four VC-31s are carried independently in the 261-column VC-4. Each of the VC-31s does not have a fixed phase with respect to the start of the VC-4. Therefore, the location of the first byte of each VC-31 with respect to the VC-4 POH is given by a 3-byte TU-31 pointer (H1, H2, H3). These four TU-31 pointers reside in a fixed location in the VC-4 as shown in Figure 2-2/G.709.

As described in § 2.1.1, the phase of the VC-4 with respect to the AU-4 is given by the AU-4 pointer.

2.1.3 *Mapping of three VC-32s into AU-4*

The STM-1 mapping format for transporting three VC-32s in an AU-4 is shown in Figure 2-3/G.709. Each TU-32 consists of a 9-row by 84-column payload structure plus one column of POH and one 3-byte TU-32 pointer. The payload of the VC-32 shown in Figure 2-3/G.709 is a single C-32. Other possible VC-32 payloads include a single 44 736 kbit/s signal in a C-32 or a group of seven TUG-21s (shown in Figure 2-5/G.709).

The three VC-32s are carried independently in the 261-column VC-4. Each of the VC-32s does not have a fixed phase with respect to the start of the VC-4. Therefore, the location of the first byte of each VC-32 with respect to the VC-4 POH is given by a 3-byte TU-32 pointer (H1, H2, H3). These three TU-32 pointers reside in a fixed location in the VC-4 as shown in Figure 2-3/G.709; 36 fixed stuff bytes are also required in the VC-4.

As described in § 2.1.1, the phase of the VC-4 with respect to the AU-4 is given by the AU-4 pointer.

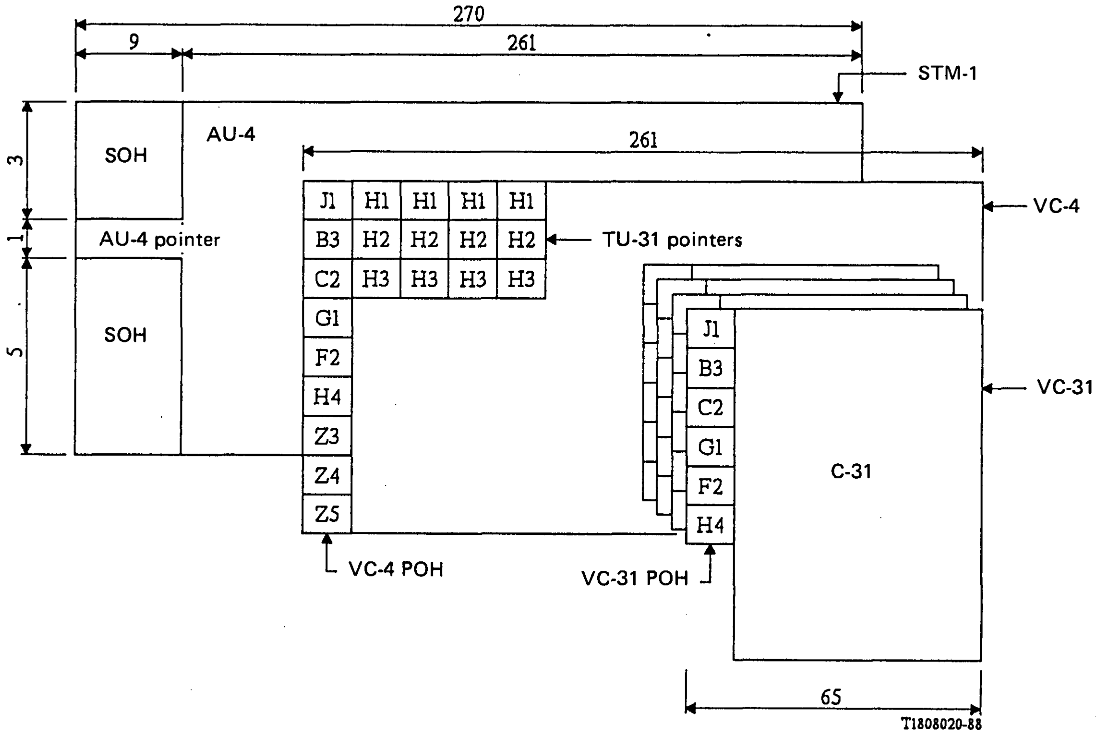


FIGURE 2-2/G.709

Mapping of four VC-31s into an AU-4

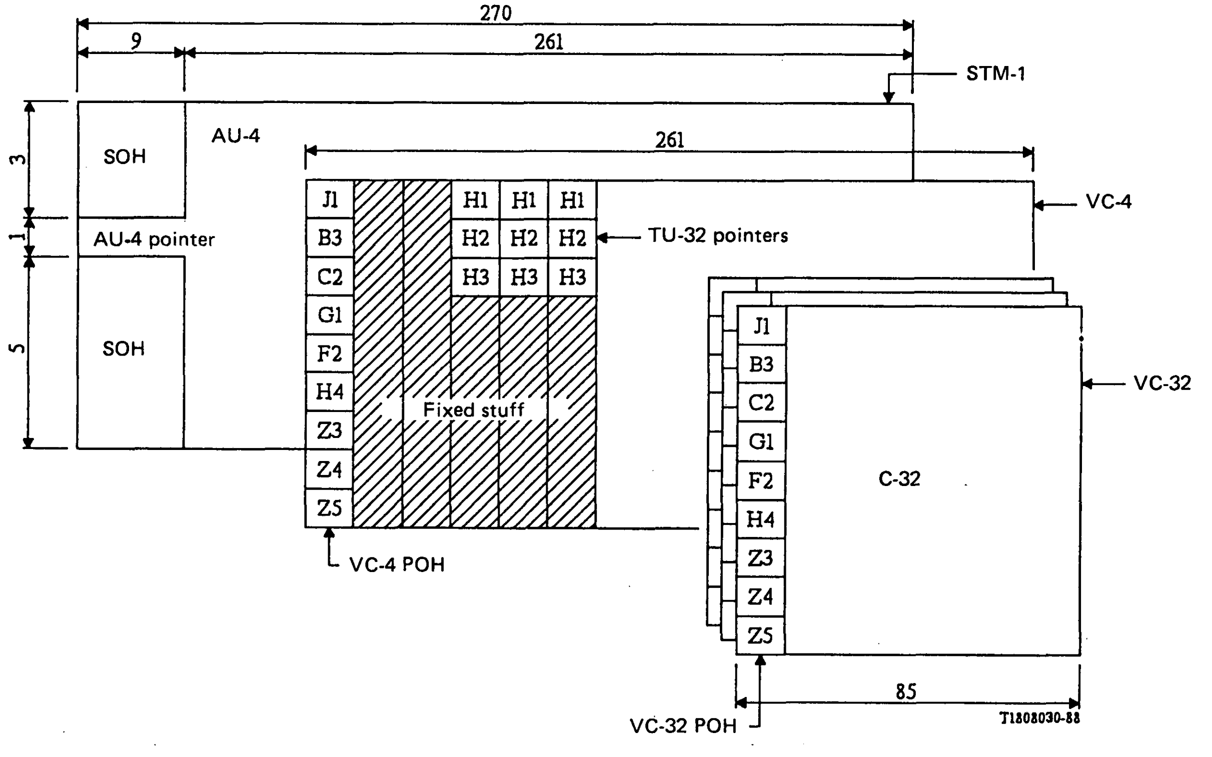


FIGURE 2-3/G.709

Mapping of three VC-32s into an AU-4

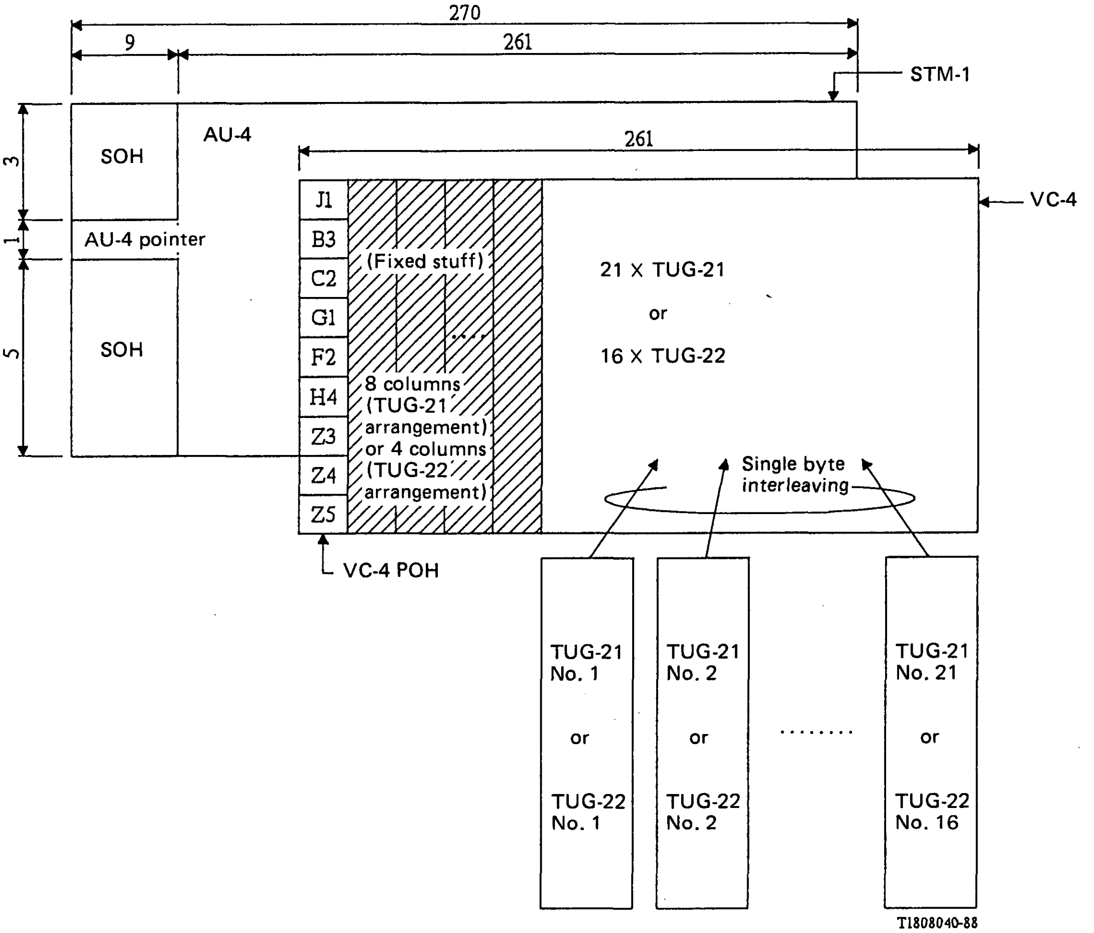
2.1.4 *Mapping of TUG-2s into AU-4*

The STM-1 mapping format transporting TUG-21s and TUG-22s into an AU-4 is shown in Figure 2-4/G.709. The AU-4 can carry a group of either 21 TUG-21s or 16 TUG-22s.

The TUG-21 payload structure has 9 rows and 12 columns. When used to transport TUG-21s, the VC-4 consists of one column of VC-4 POH, eight columns of fixed stuff, and a remaining 252-column payload structure. The 21 TUG-21s are mapped into this 9-row by 252-column structure using a fixed phase with respect to the VC-4. The TUG-21s are single byte interleaved as shown in Figure 2-4/G.709.

The TUG-22 payload structure has 9 rows and 16 columns. The VC-4 consists of one column of VC-4 POH, four columns of fixed stuff and 256 payload columns when used to carry the 16 TUG-22s. The TUG-22s are single byte interleaved into the 9-row by 256-column structure.

As described in § 2.1.1, the phase of the VC-4 with respect to the AU-4 is given by the AU-4 pointer.



Note – See Figures 5-4/G.709 and 5-5/G.709 for detailed mapping structure.

FIGURE 2-4/G.709

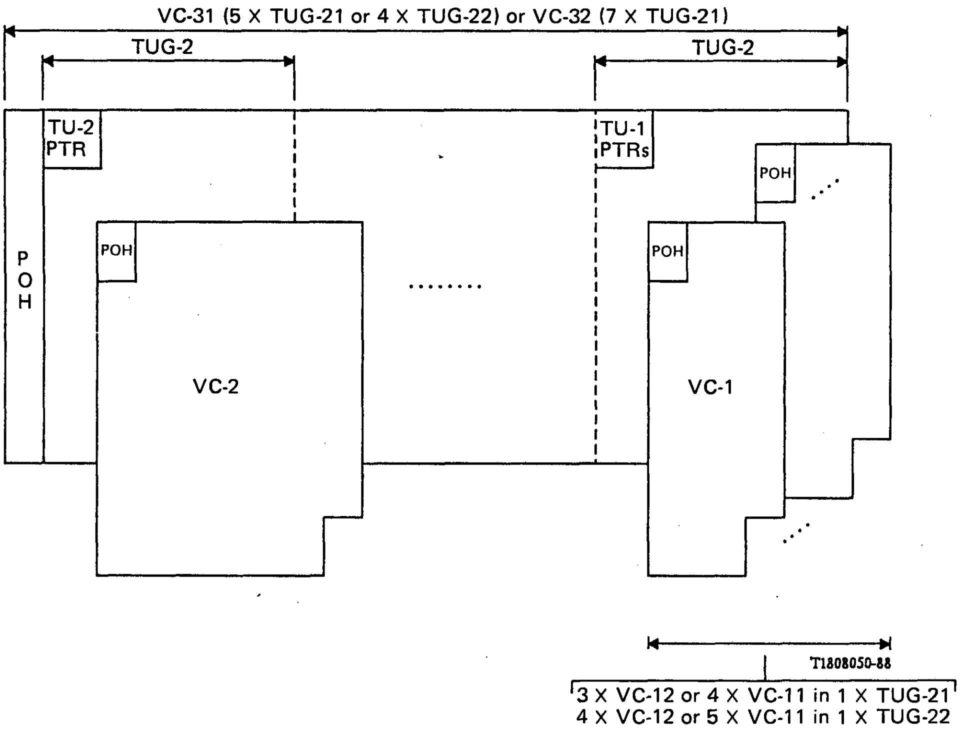
Schematic structure of TUG-2s into an AU-4

2.1.5 *Mapping of four AU-31s into STM-1*

The STM-1 mapping format for transporting four VC-31s within four AU-31s is shown in Figure 2-6/G.709. A VC-31 is defined to be a 9-row by 64-column payload structure, plus six bytes of POH, located in row 1 to 6 of the first column, according to the figure.

Each AU-31 pointer has a fixed phase with respect to the STM-1 frame. As shown in Figure 2-6/G.709, the four AU-31 pointers are located in columns 11 to 14, rows 1 to 3 of the STM-1, one pointer in each column. Columns 11 to 270 of the STM-1 are divided between each of the AU-31s; thus, each AU-31 occupies alternately every fourth column.

The phase of each VC-31 is not fixed with respect to its AU-31. Therefore, the location of the first byte of each VC-31 with respect to the AU-31 frame is given by AU-31 pointer (H1, H2, H3). The payload of the VC-31 shown in Figure 2-6/G.709 is a single C-31. Other possible VC-31 payloads include a single 34 368 kbit/s signal in a C-31 and a group of five TUG-21s or four TUG-22s (shown in Figure 2-5/G.709).



Note – See Figures 5-9/G.709, 5-11/G.709 and 5-12/G.709 for detailed mapping structure.

FIGURE 2-5/G.709

Schematic structure of VC-1s and VC-2s into VC-3s via TUG-2s

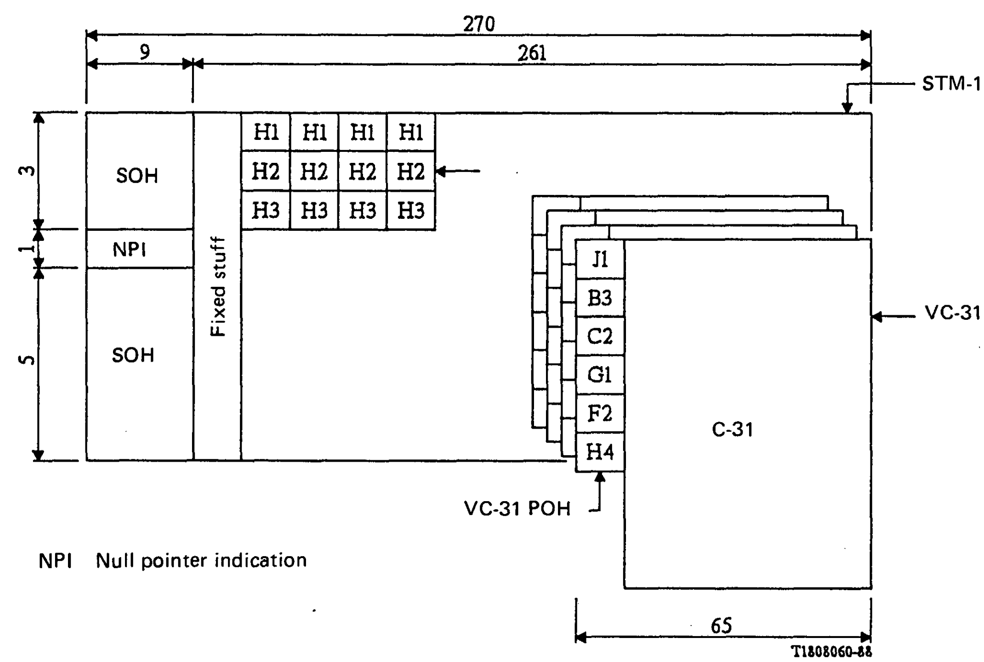


FIGURE 2-6/G.709

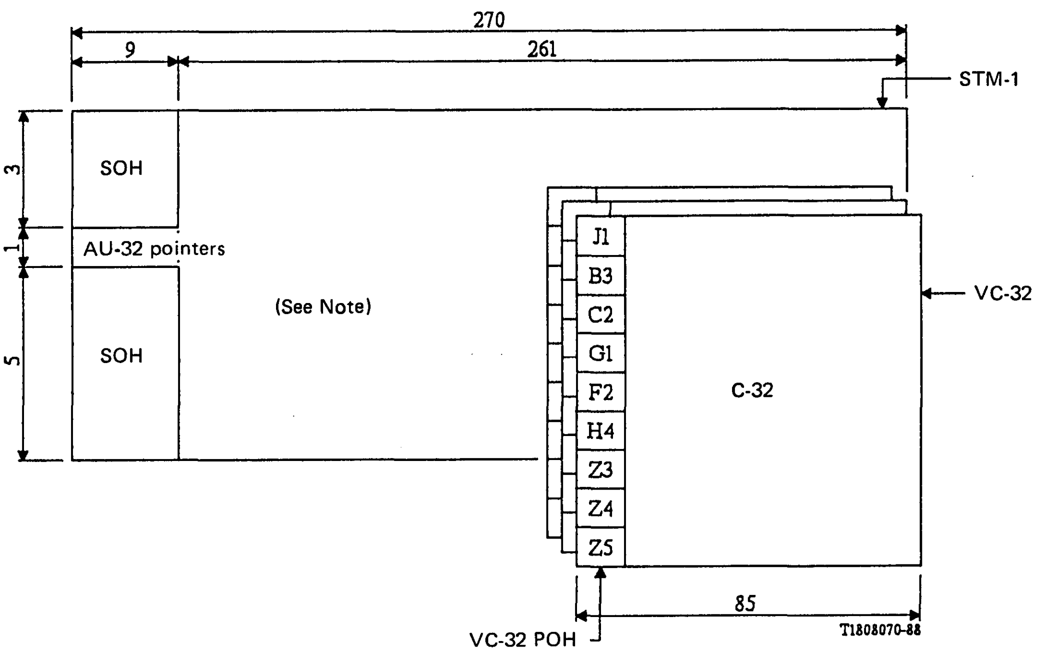
Mapping of four AU-31s into STM-1

2.1.6 *Mapping of three AU-32s into STM-1*

The STM-1 mapping format for transporting three VC-32s within three AU-32s is shown in Figure 2-7/G.709. A VC-32 is defined to be a 9-row by 85-column payload structure, with the first column consisting of VC-32 POH. When mapped into its AU-32, two columns of fixed stuff are added to each VC-32 payload to make it equal the AU-32 payload capacity. These two fixed stuff columns are fixed with respect to the VC-32 POH and are inserted between columns 29 and 30, and between columns 57 and 58 of the VC-32.

Each AU-32 pointer has a fixed phase with respect to the STM-1 frame. As shown in Figure 2-7/G.709, the three AU-32 pointers are located in the fourth row of the first nine columns of the STM-1 frame, between the bytes of the SOH. The remaining 261 columns of the STM-1 are divided between each of the AU-32s; thus, each AU-32 occupies alternately every third column of the 261. AU-32 number one consists of three bytes of AU-32 pointer, plus STM-1 columns 10, 13, 16,... where columns 1 through 9 contain the SOH and the AU-32 pointers.

The phase of each VC-32 (plus fixed stuff columns) is not fixed with respect to its AU-32. Therefore, the locations of the first byte of each VC-32 with respect to the AU-32 frame is given by the AU-32 pointer (H1, H2, H3). The payload of the VC-32 shown in Figure 2-7/G.709 is a single C-32. Other possible VC-32 payloads include a single 44 736 kbit/s signal into a C-32 (shown in Figure 5-8/G.709) and a group of seven TUG-21s (shown in Figure 2-5/G.709).



Note – Two columns of fixed stuff are added to each VC-32 when it is mapped into AU-32 (see § 2.1.6).

FIGURE 2-7/G.709

Mapping of three AU-32s into STM-1

2.1.7 *Mapping of TUGs into a VC*

Figure 2-5/G.709 shows the schematic mapping of TUG-2s into a VC-3. The details of these mappings are given in § 5; this section presents the general multiplexing principles involved.

The VC-31 consists of six bytes of VC-31 POH plus a 9-row by 64-column payload structure. This payload structure can be used to carry five TUG-21s or four TUG-22s. The individual TUG-2 has a fixed location in the VC-31 frame; this is shown schematically in Figure 2-5/G.709.

The VC-32 consists of nine bytes of VC-32 POH plus a 9-row by 84-column payload structure. This payload structure can be used to carry seven TUG-21s. Again, the individual TUG-21 has a fixed location in the VC-32 frame.

Each TUG-21 can carry a single VC-21 or four VC-11s or three VC-12s. Each TUG-22 can carry a single VC-22 or four VC-12s or five VC-11s. The VCs do not have a fixed phase with respect to the VC-3 POH; TU pointers are used to indicate the position of the VCs in the TUG frame.

2.2 *STM-N multiplexing*

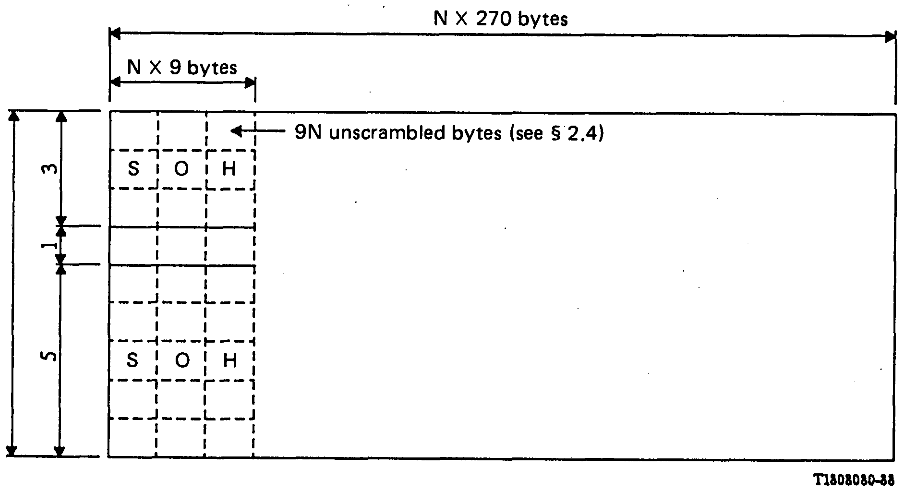
2.2.1 *STM-N frame format*

The STM-N signal is formed by single byte interleaving N STM-1 signals. The STM-N frame structure is depicted in Figure 2-8/G.709.

The first byte of the STM-N signal shall be the first A1 framing byte from STM-1 No. 1 followed sequentially by the first A1 byte from STM-1 No. 2 through No. N. The first bit to be transmitted shall be the most significant bit of the first A1 framing byte from STM-1 No. 1.

Before byte interleaving STM-1 signals to form an STM-N signal, all of the SOH and the AU-*n* (n = 3 or 4) pointers in the signals to be interleaved must be 125 µs frame aligned. The alignment is accomplished by adjusting the values of the AU-*n* pointers to reflect the new relative positions of the VC-*n*s.

Note that is is permitted to mix STM-1s containing AU-3s and STM-1s containing AU-4s in the same STM-N.



Note – Refer to Figure 3-4/G.708 for SOH byte allocations.

FIGURE 2-8/G.709

STM-N frame

2.2.2 *STM-N interleaving*

If an STM-N level signal is input to a byte interleaver with STM-M level output (M > N), N bytes of each STM-N are consecutively placed on the output STM-M signal. This method of interleaving is illustrated in Figure 2-9/G.709 where STM-X, STM-Y and STM-Z (X + Y + Z = M) inputs are sequentially interleaved to form an STM-M output.

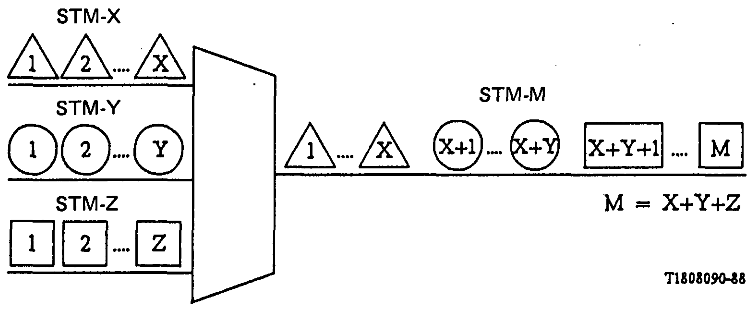


FIGURE 2-9/G.709

STM-N byte interleaving (N = X, Y, Z)

2.2.3 *Concatenated STM-1s*

STM-1 signals can be concatenated together to form an STM-Nc which can transport payloads requiring greater than one C-4 capacity. A concatenation indication, used to show that this multi-C-4 payload carried in a single VC-4-Nc should be kept together, is contained in the AU-4 pointer. See § 3.4 for details.

2.3 *Maintenance signals*

2.3.1 *Section maintenance signals*

The section alarm indication signal (AIS) is detected as an all 1s in bits 6, 7, 8 of byte K2 after descrambling.

Far end receive failure (FERF) is to return an indication to the transmitting STM-N MUX that the receiving STM-N MUX has detected an incoming section failure or is receiving section AIS.

FERF is detected by a 110 code in bit positions 6, 7 and 8 of the K2 APS byte after descrambling.

2.3.2 *Path maintenance signals*

The VC-*n* (n = 3, 4) unequipped indication is an all 0s VC-*n* path signal label after descrambling. This code indicates to VC-*n* terminating equipment that the VC-n is intentionally unoccupied so that alarms can be inhibited. This code is generated as an all 0s VC-*n* path signal label and a valid VC-n path BIP-8 (byte B3); the VC-*n* payload is unspecified.

An alarm indication signal (AIS) is a signal sent downstream as an indication that an upstream failure has been detected and an alarm generated. The TU-*n* (n = 1, 2, 3) path AIS is specified as all 1s in the entire TU-*n*, including the TU-*n* pointer. Similarly, the AU-*n* (n = 3, 4) path AIS is specified as all 1s in the entire AU-*n*, including the AU-*n* pointer. All path AISs are carried within STM-N signals having valid SOH.

The path status byte (G1) is used to convey the terminating path status and performance to the originator of a VC-*n* (n = 3 or 4). Bits 1 through 4 convey the count of errors detected using the path BIP-8 code. This code has nine legal values, 0-8. The remaining seven possible values should be interpreted as zero errors.

2.4 *Timing recovery*

The STM-N (N ⩾ 1) signal must have sufficient bit timing content at the NNI. A suitable bit pattern, which prevents a long sequence of 1s and 0s, is provided by using a scrambler. Its operation shall be functionally identical to that of a frame synchronous scrambler of sequence length 127 operating at the line rate.

The generating polynomial shall be $1 + x^6 + x^7$. Figure 2-10/G.709 gives a functional diagram of the frame synchronous scrambler.

The scrambler shall be reset to 1111111 on the most significant bit of the byte following the last byte of the first row of the STM-N SOH. (This is the most significant bit of the $9 \times N + 1$ transmitted byte of the STM-N; see Figure 2-8/G.709.) This bit, and all subsequent bits to be scrambled, shall be added modulo 2 to the output from the x^7 position of the scrambler. The scrambler shall run continuously throughout the complete STM-N frame.

The first row of the STM-N SOH ($9 \times N$ bytes, including the A1 and A2 framing bytes) shall not be scrambled.

Note – Care should be taken in selecting the binary content of the bytes reserved for national use and which are excluded from the scrambling process of the STM-N signal, to ensure that long sequences of 1s or 0s do not occur.

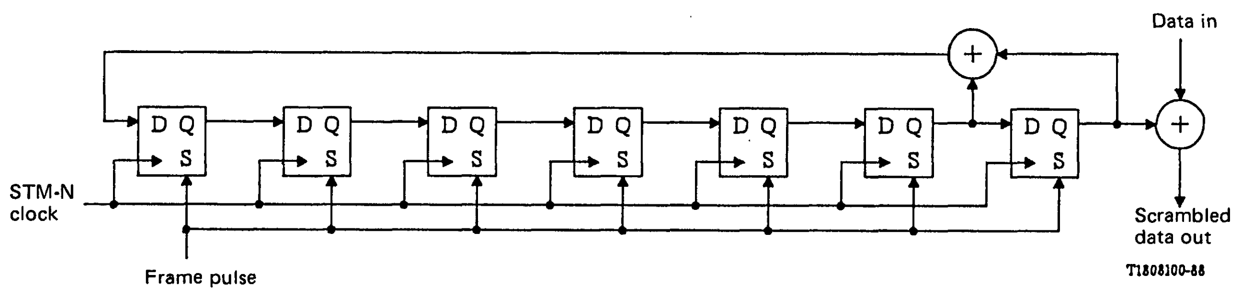


FIGURE 2-10/G.709

Frame synchronous scrambler (functional diagram)

2.5 *Conceptual steps for STM-N assembly*

For a better understanding of the detailed structure of the STM-N frame shown in Figure 2-8/G.709, the conceptual steps required to assemble the STM-N frames in the direct (non-nested) arrangement are listed:

1) Each VC-*n* (*n* = 3 or 4) has either six or nine bytes devoted to path overhead (POH) functions. Of these, the BIP-8 error check byte (B3) is calculated over the entire contents of the VC-*n* and the result is placed in the B3 byte of the following frame.

   If it is appropriate, the VC-*n* unequipped signal consisting of an all 0s pattern for the VC-*n* is inserted. (See § 2.3.)

2) After all of the required VC-*n*s have been assembled, AU-*n* pointer values are calculated so as to frame align all of the AU-*n*s within a single STM-N frame.

   If the contents of the VC-*n* are lost due to an equipment or other failure, the AU-*n* path AIS signal is inserted into the AU-*n*. The AU-*n* path AIS is defined in § 2.3.

3) The SOH bytes are then added to the STM-N frame. It is convenient to consider the last five rows of the SOH first. Of the N × 45 such SOH bytes, N × 9 are allocated to the N × 3 B2, N × 3 Z1 and N × 3 Z2 bytes. Thus, each STM-1 has a full complement (3) of these bytes in the STM-N. The remaining STM-N SOH bytes in the last five rows (K1 and K2, D4-D12 and E2) are limited to the first STM-1 in any STM-N signal. The content of the unused SOH bytes of STM-1 No. 2 through No. N are for national use.

4) The N × 3 B2 bytes of an STM-N contain a bit interleaved parity N × 24 (BIP-N × 24) code using even parity which is calculated across the entire previous STM-N frame excluding the first three rows of SOH.

5) A line signal failure would result in the insertion of a section AIS at this point in the assembly of an STM-N (see § 2.3).

6) The remaining bytes of SOH contained in the first three rows (27 × N bytes) of the STM-N are added next. Of these, the B1, E1, F1, D1-D3 bytes are present only in STM-1 No. 1 of any STM-N signal. The content of the unused SOH bytes of STM-1 No. 2 through No. N are for national use.

7) The STM-1s are then byte interleaved to form an STM-N, as described in § 2.2.2, and subsequently serialized and scrambled as described in § 2.4.

8) The final operation is the calculation of a BIP-8 code over the entire STM-N bit stream on a frame-by-frame basis. The result is loaded into byte B1 of STM-1 No. 1 in the following frame when the SOH is loaded.

3 Pointer

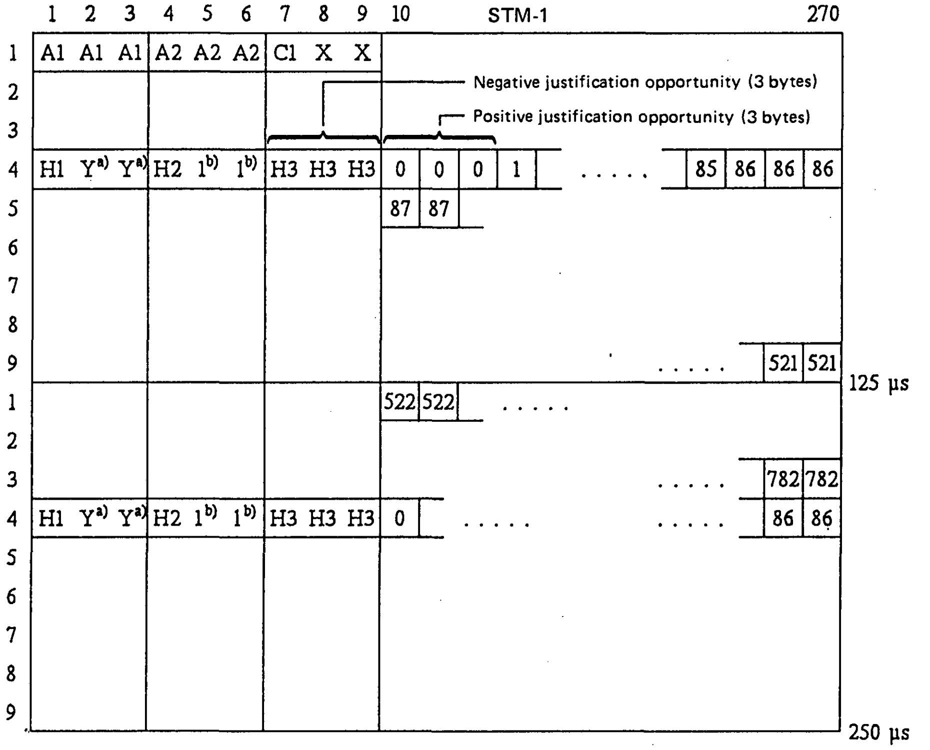
3.1 *AU pointer*

The AU pointer provides a method of allowing flexible and dynamic alignment of the VC within the AU frame.

Dynamic alignment means that the VC is allowed to "float" within the AU frame. Thus the pointer is able to accommodate differences not only in the phases of the VC and SOH, but in the frame rates as well.

3.1.1 *AU pointer location*

The AU-4 pointer is contained in bytes H1, H2 and H3 as shown in Figure 3-1/G.709. The three individual AU-32 pointers are contained in three separate H1, H2 and H3 bytes as shown in Figure 3-2/G.709. Likewise the four individual AU-31 pointers are contained in four separate H1, H2 and H3 bytes as shown in Figure 3-3/G.709.



a) Y byte = 1001SS11 (S bits are unspecified).

b) All 1s byte.

FIGURE 3-1/G.709

AU-4 pointer offset numbering

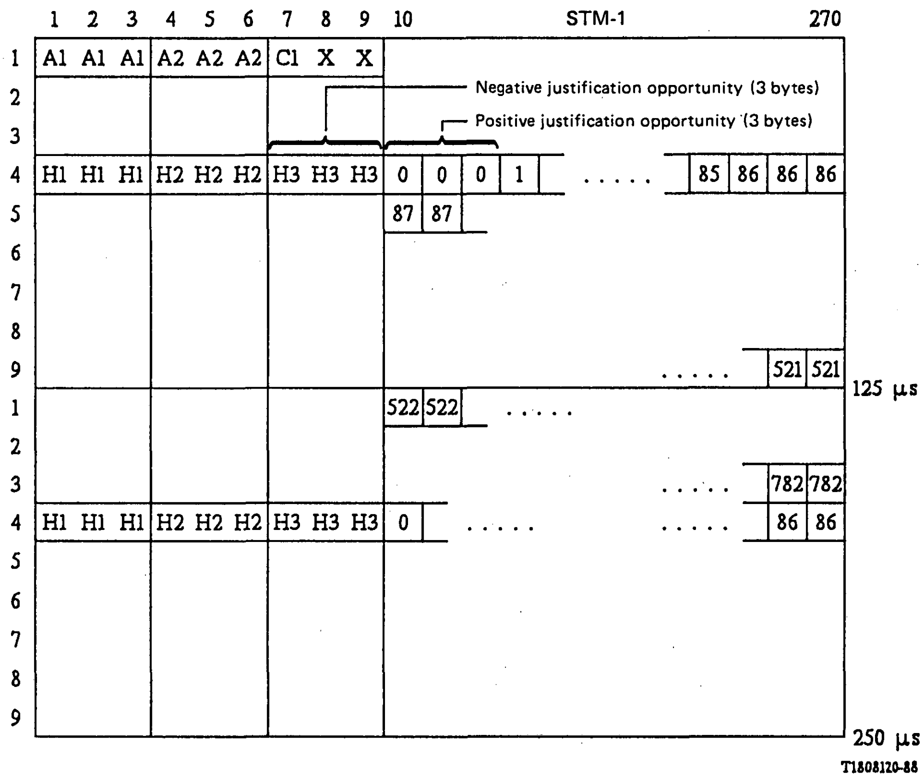
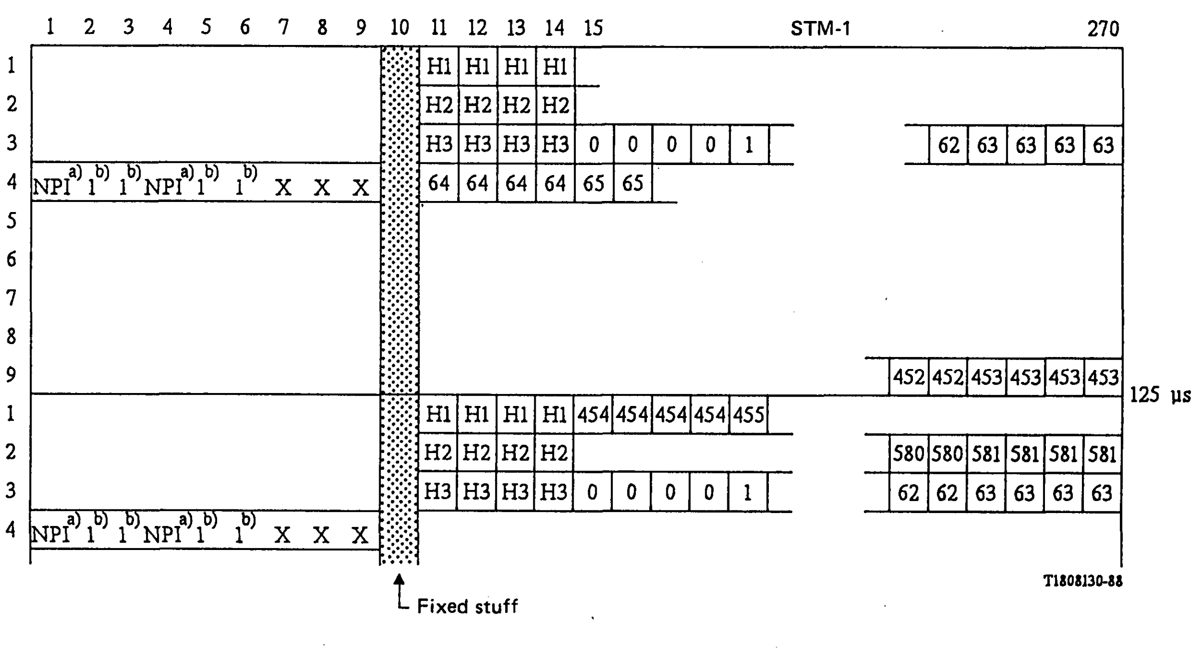


FIGURE 3-2/G.709

AU-32 pointer offset numbering



a) Two NPI bytes form a 16 bit sequence 1001SS1111100000 (S bits are unspecified).

b) All 1s byte.

FIGURE 3-3/G.709

AU-31 pointer offset numbering

3.1.2 *AU pointer value*

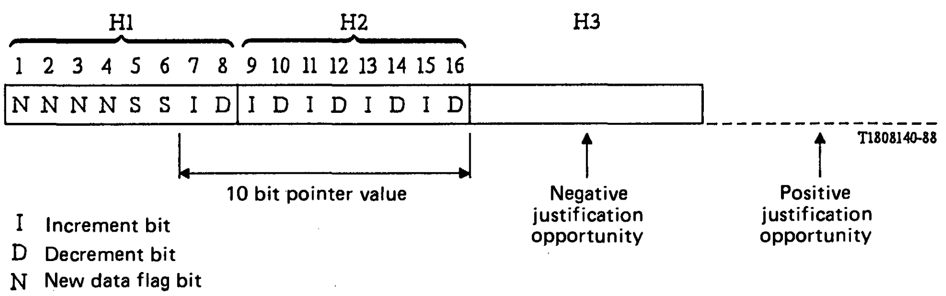
The pointer contained in H1 and H2 designates the location of the bytes where the VC begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Figure 3-4/G.709. The last 10 bits (bits 7-16) of the pointer word carry the pointer value. The two S bits (bits 5 and 6) indicate the AU type.

As illustrated in Figure 3-4/G.709, the AU-4 pointer value is a binary number with a range of 0 to 782 which indicates the offset between the pointer and the first byte of the VC. As shown in Figure 3-1/G.709, the H1 and H2 bytes contain the pointer value while the position which the pointer indicates is the very first byte of the consecutive three bytes. Figure 3-4/G.709 also indicates two additional valid pointers: the concatenation indication (CI) and the null pointer indication (NPI). The CI is indicated by 1001 in bits 1-4, with bits 5-6 unspecified, and ten 1s in bits 7-16. The NPI is indicated by 1001 in bits 1-4, with bits 5-6 unspecified, and five 1s in bits 7-11 followed by five 0s in bits 12-16.

As illustrated in Figure 3-4/G.709, the AU-32 pointer value is also a binary number with a range of 0 to 782. Since there are three AU-32s in the STM-1, each AU-32 has its own associated H1, H2 and H3 bytes. In Figure 3-2/G.709, the H bytes are shown in sequence. The first H1, H2, H3 set refers to the first AU-32, and the second set to the second AU-32, and so on. The same is true for the information bytes. For the AU-32s, each pointer operates independently.

Likewise, as illustrated in Figure 3-4/G.709, the AU-31 pointer value is a binary number with a range of 0 to 581. Since there are four AU-31s in the STM-1, each AU-31 has its own associated H1, H2 and H3 bytes. In Figure 3-3/G.709, the H bytes are shown in sequence. The first H1, H2, H3 set refers to the first AU-31, the second set to the second AU-31, and so on. The same is true for the information bytes. For the AU-31s, each pointer operates independently.

In all cases, the STM-1 SOH and AU pointer bytes are not counted in the offset. For example, in an AU-4, the pointer value of 0 indicates that the VC starts in the byte location that immediately follows the last H3 byte, whereas an offset of 87 indicates that the VC starts three bytes after the K2 byte.



New data flag

Enabled: 1001
Disabled: 0110

Negative justification

Invert 5 D-bits
Accept majority vote

SS values	AU/TU type
10	AU-4, AU-32, TU-32
01	AU-31, TU-31

Pointer value (normal range) (bits 7-16)

AU-4 : 0 - 782 decimal
AU-31 : 0 - 581 decimal
AU-32 : 0 - 782 decimal
TU-32 : 0 - 764 decimal
TU-31 : 0 - 581 decimal

Concatenation indication (CI)

1001SS1111111111 (S bits are unspecified)

Null pointer indication (NPI)

1001SS1111100000 (S bits are unspecified)

Positive justification

Invert 5 I-bits
Accept majority vote

FIGURE 3-4/G.709

AU/TU-3 pointer (H1, H2, H3) coding

3.1.3 *Frequency justification*

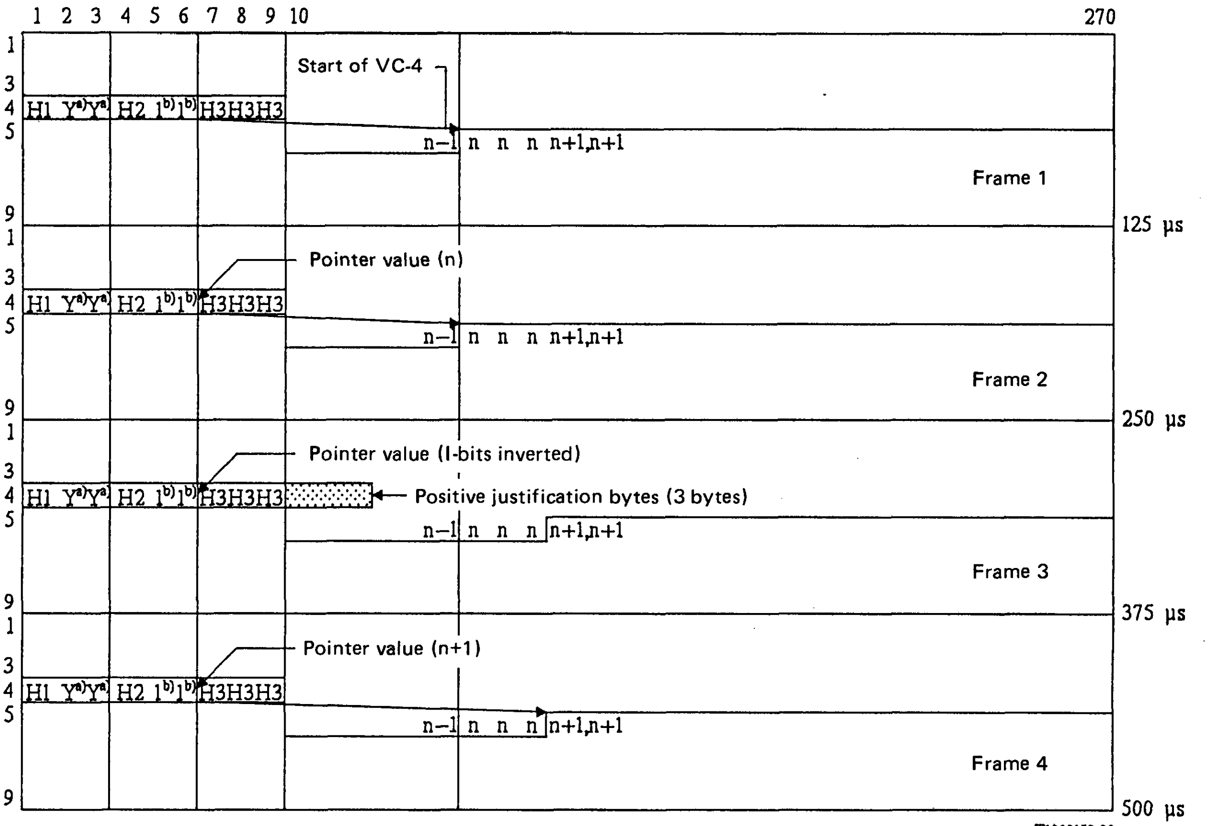
If there is a frequency offset between the frame rate of the SOH and that of the VC, then the pointer value will be incremented or decremented as needed, accompanied by a corresponding positive or negative justification byte or bytes. Consecutive pointer operations must be separated by at least three frames (i.e. every fourth frame) in which the pointer value remains constant.

If the frame rate of the VC is too slow with respect to that of the SOH, then the alignment of the VC must periodically slip back in time and the pointer value must be incremented by one. This operation is indicated by inverting bits 7, 9, 11, 13 and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. Three positive justification bytes appear immediately after the last H3 byte in the AU-4 frame containing inverted I-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 3-5/G.709.

For AU-32 frames, a positive justification byte appears immediately after the associated H3 byte of the individual AU-32 frame containing inverted I-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 3-6/G.709. The same is true for AU-31 as shown in Figure 3-7/G.709.

If the frame rate of the VC is too fast with respect to that of the SOH, then the alignment of the VC must periodically be advanced in time and the pointer value must be decremented by one. This operation is indicated by inverting bits 8, 10, 12, 14 and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. Three negative justification bytes appear in the H3 bytes in the AU-4 frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 3-8/G.709.

For AU-32 frames, a negative justification byte appears in the H3 byte of the individual AU-32 frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 3-9/G.709. The same is true for AU-31 as shown in Figure 3-10/G.709.



a) Y byte = 1001SS11 (S bits are unspecified).

b) All 1s byte.

FIGURE 3-5/G.709

AU-4 pointer adjustment operation – positive justification

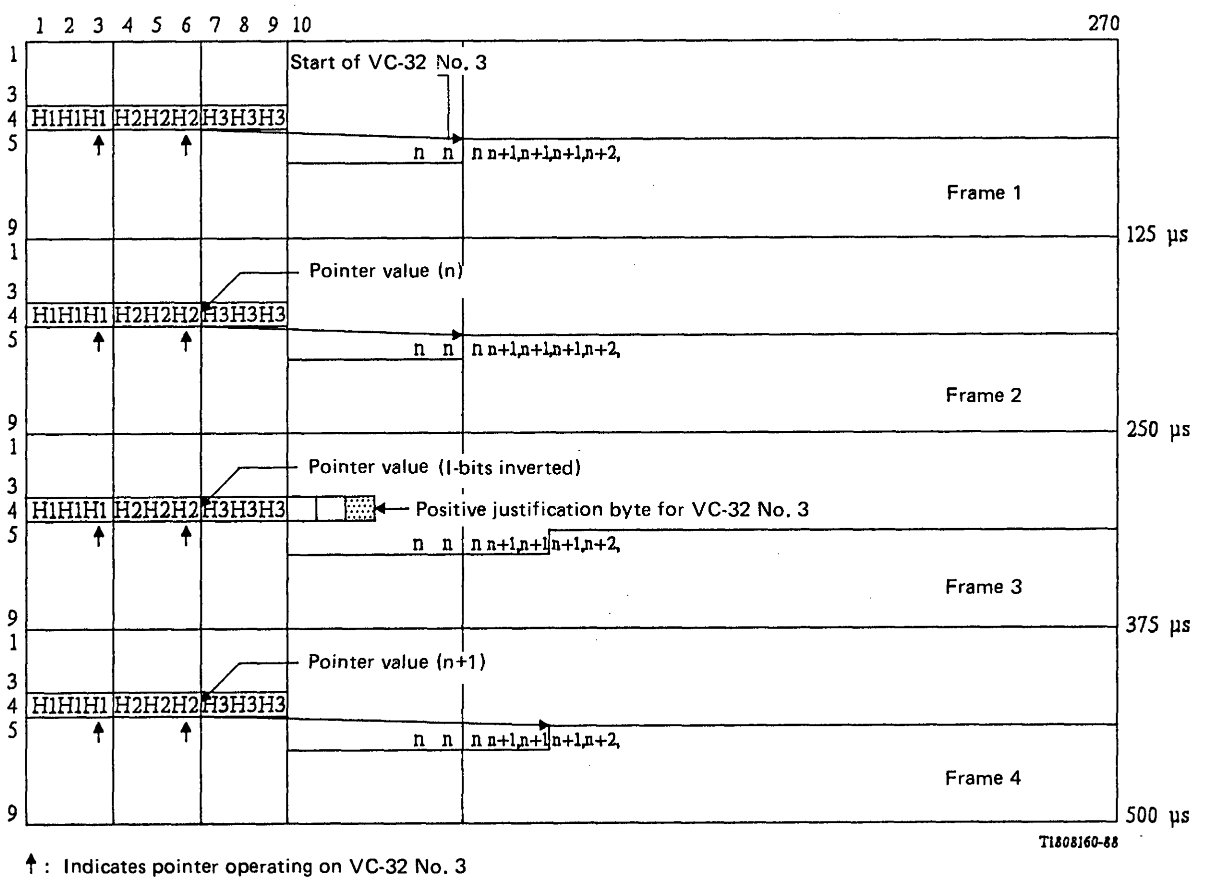
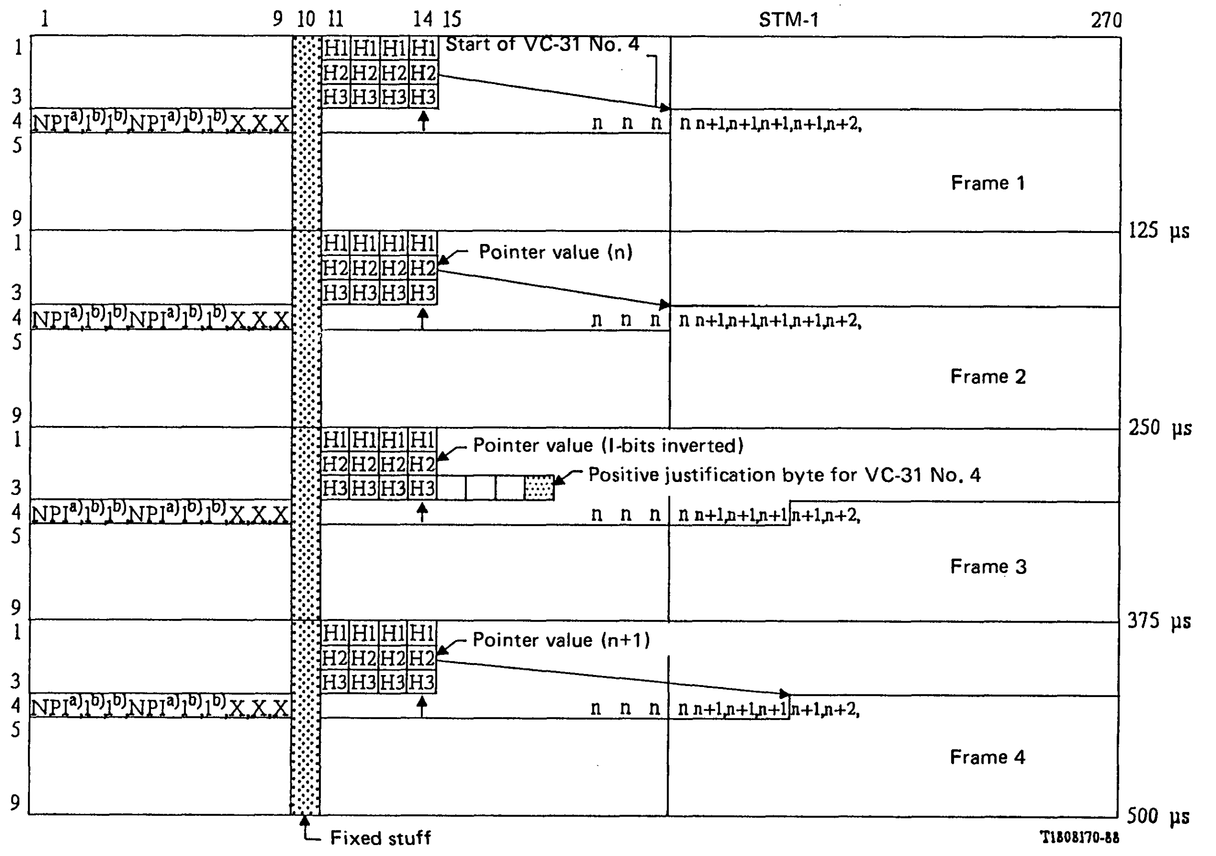


FIGURE 3-6/G.709

AU-32 pointer adjustment operation – positive justification



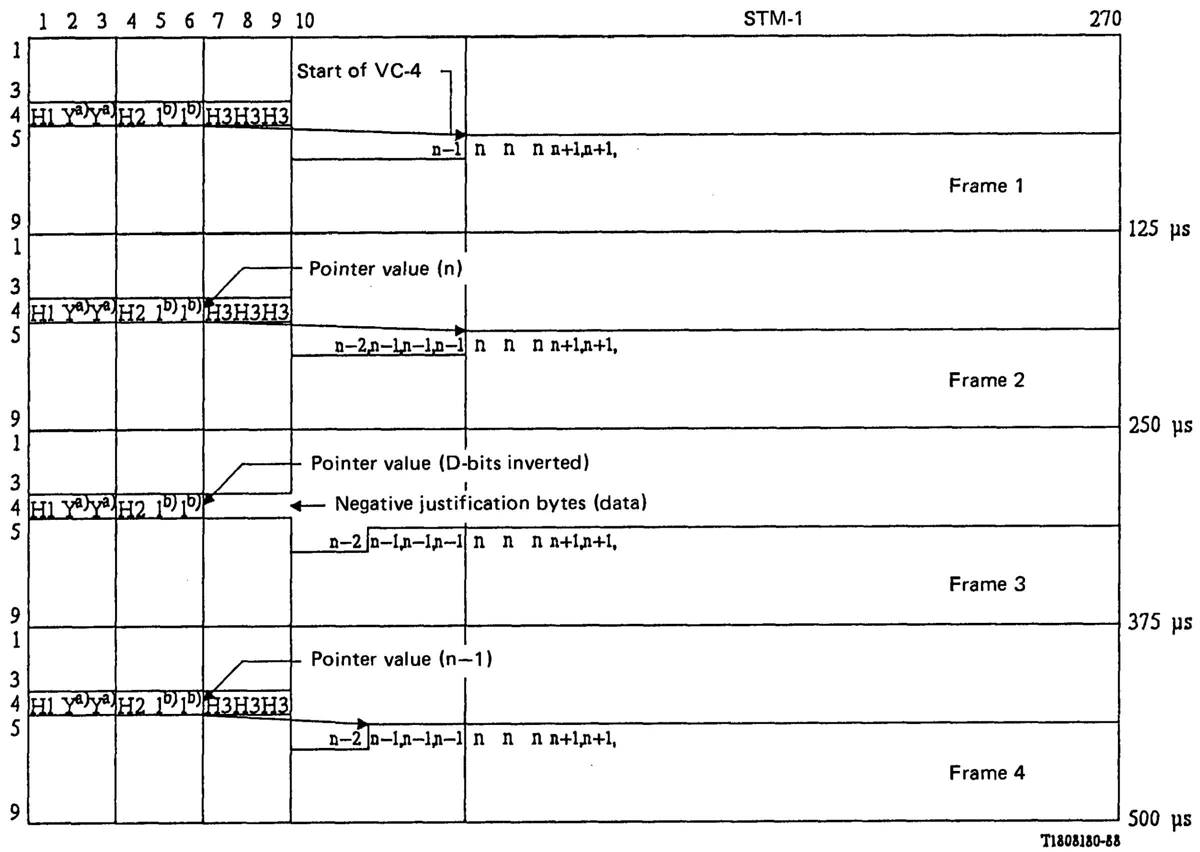
a) Two NPI bytes form a 16 bit sequence 1001SS1111100000 (S bits are unspecified).

b) All 1s byte.

↑: Indicates pointer operating on VC-31 No. 4

FIGURE 3-7/G.709

AU-32 pointer adjustment operation – positive justification

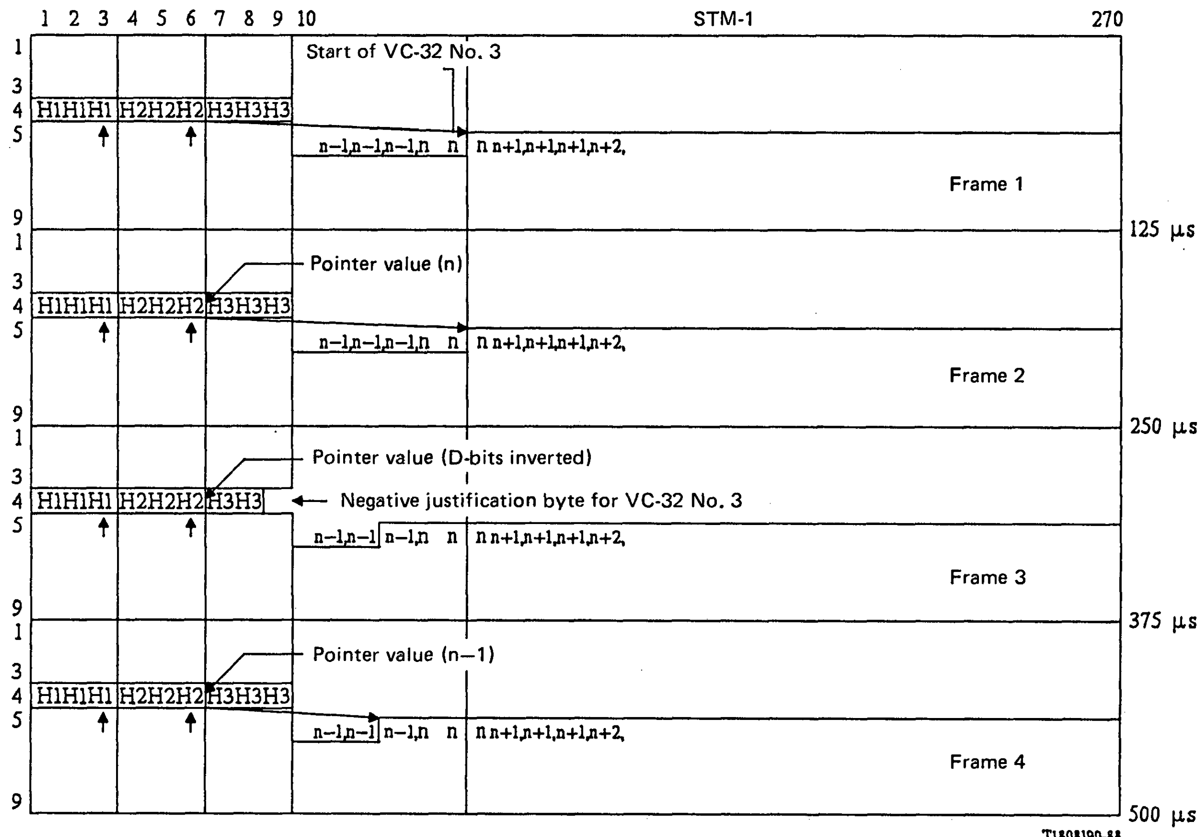


a) Y byte = 1001SS11 (S bits are unspecified).

b) All 1s byte.

FIGURE 3-8/G.709

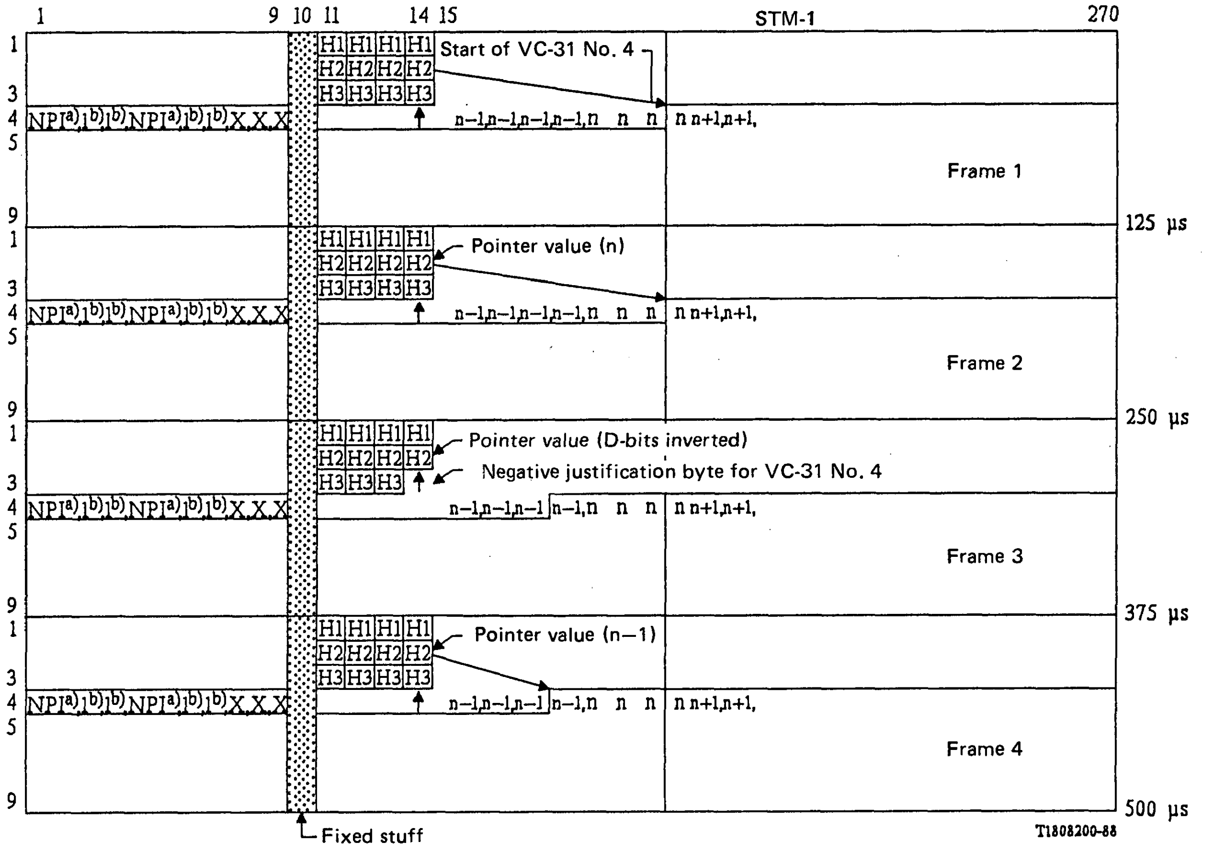
AU-4 pointer adjustment operation – negative justification



↑: Indicates pointer operating on the VC-32 No. 3.

FIGURE 3-9/G.709

AU-32 pointer adjustment operation – negative justification



a) Two NPI bytes form a 16 bit sequence 1001SS1111100000 (S bits are unspecified).

b) All 1s byte.

↑ : Indicates pointer operating on VC-31 No. 4.

FIGURE 3-10/G.709

AU-31 pointer adjustment operation – negative justification

3.1.4 *New data flag*

Bits 1-4 (N-bits) of the pointer word carry a new data flag (NDF) which allows an arbitrary change of the pointer value if that change is due to a change in the payload.

Four bits are allocated to the flag to allow error correction. The decoding may be performed by accepting NDF enabled if at least three bits match. Normal operation is indicated by a 0110 code in the N-bits. NDF is indicated by inversion of the N-bits to 1001. The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated. NDF should be enabled when the pointer value transits between its normal value and the CI or NPI.

3.1.5 *Pointer generation*

The following summarizes the rules for generating the AU pointers.

1) During normal operation, the pointer locates the start of the VC within the AU frame. The NDF is set to 0110.
2) The pointer value can only be changed by rules 3, 4 or 5.
3) If a positive justification is required, the current pointer value is sent with the I-bits inverted and the subsequent positive justification opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. No subsequent increment or decrement operation is allowed for at least three frames following this operation.
4) If a negative justification is required, the current pointer value is sent with the D-bits inverted and the subsequent negative justification opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. No subsequent increment or decrement operation is allowed for at least three frames following this operation.
5) If the alignment of the VC changes for any reason other than rules 3 or 4, the new pointer value shall be sent accompanied by NDF set to 1001. The NDF only appears in the first frame that contains the new values. The new location of the VC begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

3.1.6 *Pointer interpretation*

The following summarizes the rules for interpreting the AU pointers.

1) During normal operation, the pointer locates the start of the VC within the AU frame.
2) Any variation from the current pointer value is ignored unless a consistent new value is received three times consecutively or it is preceded by one of rules 3, 4 or 5.
3) If the majority of the I-bits of the pointer word are inverted, a positive justification operation is indicated. Subsequent pointer values shall be incremented by one.
4) If the majority of the D-bits of the pointer word are inverted, a negative justification operation is indicated. Subsequent pointer values shall be decremented by one.
5) If the NDF is set to 1001, then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value regardless of the state of the receiver.

3.2 *TU-3 pointers*

There are two types of TU-3 pointers: TU-31 and TU-32. The TU-3 pointer provides a method of allowing flexible and dynamic alignment of VC-3 within the TU-3 frame, independent of the actual contents of the VC. Dynamic alignment means that the VC-3 is allowed to "float" within the TU-3 frame.

3.2.1 *TU-3 pointer location*

Three individual TU-32 pointers are contained in the three separate H1, H2 and H3 bytes as shown in Figure 3-11/G.709. Four individual TU-31 pointers are contained in the four separate H1, H2 and H3 bytes as shown in Figure 3-12/G.709.

3.2.2 *TU-3 pointer value*

The TU-3 pointer value contained in H1 and H2 designates the location of the byte where the VC-3 begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Figure 3-4/G.709. The last ten bits (bits 7-16) of the pointer word carry the pointer value. The two S bits (bits 5 and 6) indicate the TU type.

The TU-32 pointer value is a binary number with a range of 0-764 which indicates the offset between the pointer and the first byte of the VC-32 as shown in Figure 3-11/G.709.

The TU-31 pointer value is a binary number with a range of 0-581 which indicates the offset between the pointer and the first byte of the VC-31 as shown in Figure 3-12/G.709.

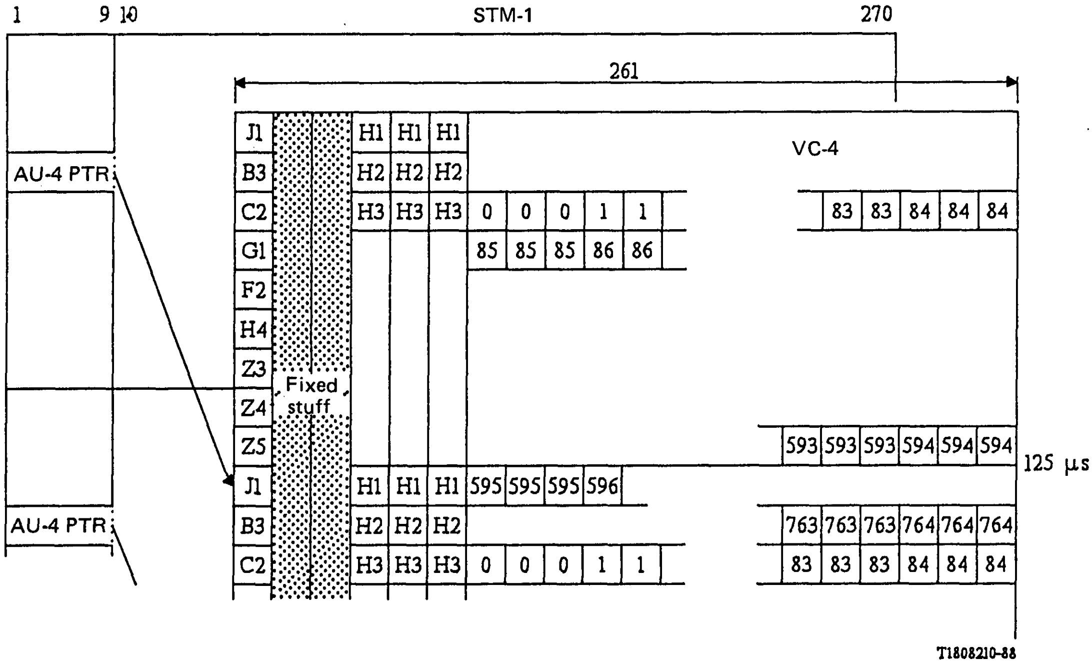


FIGURE 3-11/G.709

TU-32 pointer offset numbering

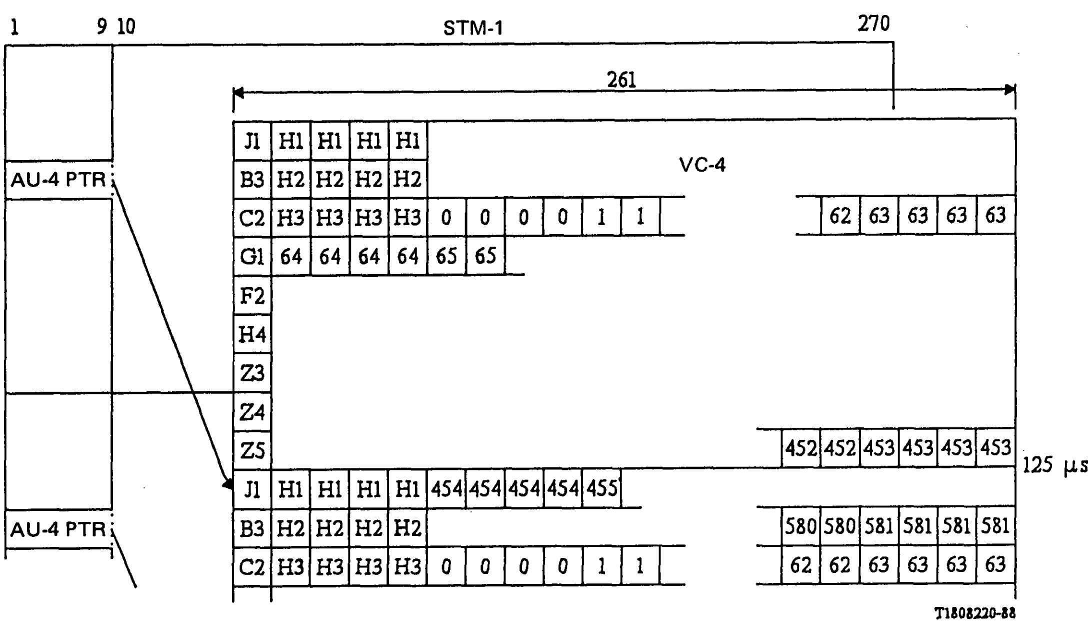


FIGURE 3-12/G.709

TU-31 pointer offset numbering

3.2.3 *Frequency justification*

If there is a frequency offset between the TU-3 frame rate and that of the VC-3, then the pointer value will be incremented or decremented as needed accompanied by a corresponding positive or negative justification byte. Consecutive pointer operations must be separated by at least three frames in which the pointer value remains constant.

If the frame rate of the VC-3 is too slow with respect to that of the TU-3 frame rate, then the alignment of the VC must periodically slip back in time and the pointer must be incremented by one. This operation is indicated by inverting bits 7, 9, 11, 13 and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. A positive justification byte appears immediately after the individual H3 byte in the TU-3 frame containing inverted I-bits. Subsequent TU-3 pointers will contain the new offset.

If the frame rate of the VC-3 is too fast with respect to that of the TU-3 frame rate, then the alignment of the VC must be periodically advanced in time and the pointer must be decremented by one. This operation is indicated by inverting bits 8, 10, 12, 14 and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. A negative justification byte appears in the individual H3 byte in the TU-3 frame containing inverted D-bits. Subsequent TU-3 pointers will contain the new offset.

3.2.4 *New data flag*

Bits 1-4 (N-bits) of the pointer word carry a NDF which allows an arbitrary change of the value of the pointer if that change is due to a change in the VC-3.

Four bits are allocated to the flag to allow for error correction. The decoding may be performed by accepting NDF enabled if at least three bits match. Normal operation is indicted by a 0110 code in the N-bits; NDF is indicated by inversion of the N-bits to 1001. The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated.

3.2.5 *Pointer generation*

The following summarizes the rules for generating the TU-3 pointers.

1) During normal operation, the pointer locates the start of the VC-3 within the TU-3 frame. The NDF is set to 0110.
2) The pointer value can only be changed by rules 3, 4 or 5.
3) If a positive justification is required, the current pointer value is sent with the I-bits inverted and the subsequent positive justification opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. No subsequent increment or decrement operation is allowed for at least three frames following this operation.
4) If a negative justification is required, the current pointer value is sent with the D-bits inverted and the subsequent negative justification opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. No subsequent increment or decrement operation is allowed for at least three frames following this operation.
5) If the alignment of the VC changes for any reason other than rules 3 or 4, the new pointer value shall be sent accompanied by the NDF set to 1001. The NDF only appears in the first frame that contains the new value. The new VC location begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

3.2.6 *Pointer interpretation*

The following summarizes the rules for interpreting the TU-3 pointers.

1) During normal operation the pointer locates the start of the VC-3 within the TU-3 frame.
2) Any variation from the current pointer value is ignored unless a consistent new value is received three times consecutively or it is preceded by one of rules 3, 4 or 5.
3) If the majority of the I-bits of the pointer word are inverted, a positive justification is indicated. Subsequent pointer values shall be incremented by one.

4) If the majority of the D-bits of the pointer word are inverted, a negative justification is indicated. Subsequent pointer values shall be decremented by one.

5) If the NDF is set to 1001, then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value regardless of the state of the receiver.

3.3 *TU-1/TU-2 pointers*

The TU-1 pointer is only used with floating mapping. Floating and locked modes of operation are described in § 5.2.

The TU-1 and TU-2 pointers provide a method of allowing flexible and dynamic alignment of the VC-1/VC-2 within the TU-1 and TU-2 multiframes, independent of the actual contents of the VC.

3.3.1 *TU-1/TU-2 pointer location*

The TU-1/TU-2 pointers are contained in the V1 and V2 bytes as illustrated in Figure 3-13/G.709.

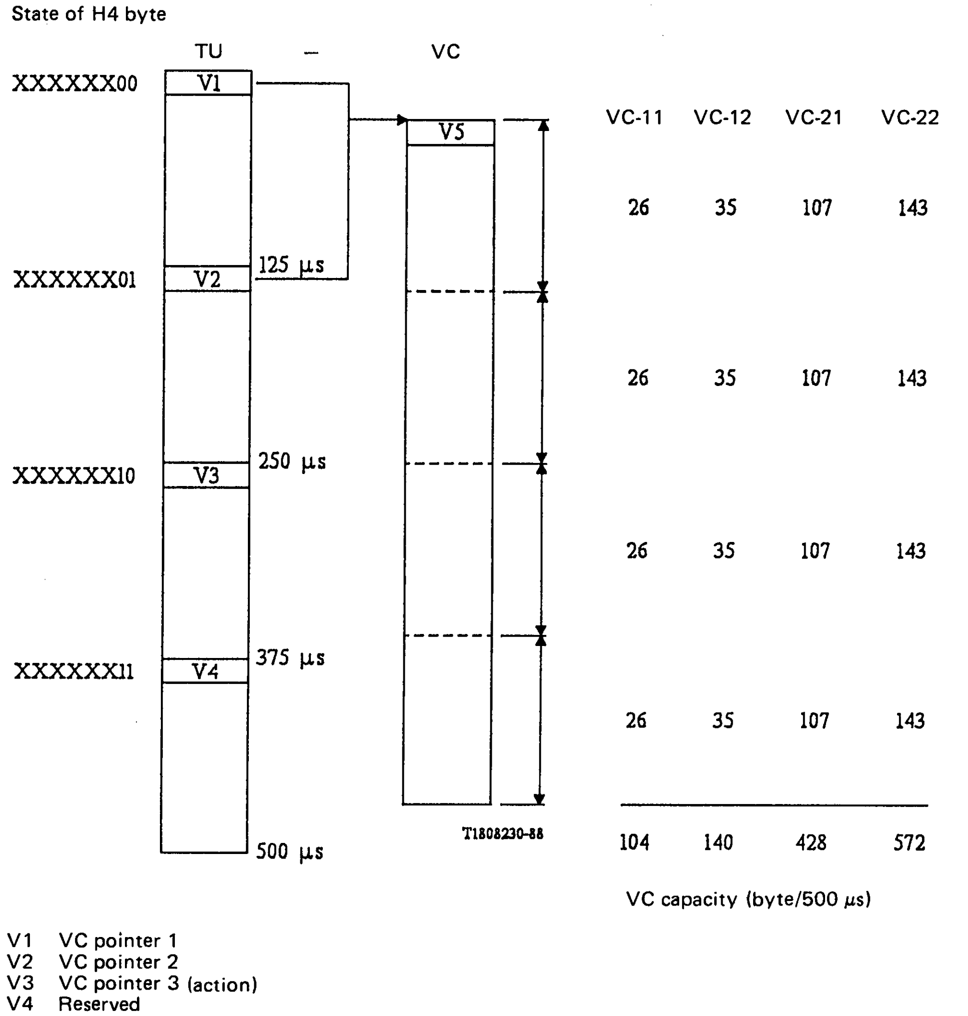


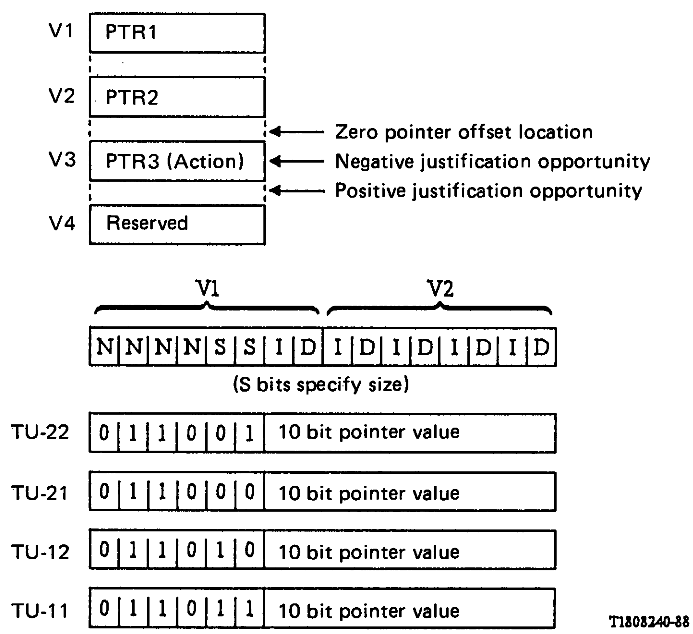
FIGURE 3-13/G.709

VC mapping in multiframed TU

3.3.2 *TU-1/TU-2 pointer value*

The TU pointer word is shown in Figure 3-14/G.709.

The pointer value (bits 7-16) is a binary number which indicates the offset from V2 to the first byte of the VC-1/VC-2. The range of the offset is different for each of the TU sizes as illustrated in Figure-3-15/G.709. Note that the pointer bytes are not counted in the offset calculation.



New Data Flag

– Invert 4 N-bits
– Accept only exact match

Negative justification

– Invert 5 D-bits
– Accept majority vote

Positive justification

– Invert 5 I-bits
– Accept majority vote

Pointer value (normal range)

TU-22: 0-571 decimal
TU-21: 0-427 decimal
TU-12: 0-139 decimal
TU-11: 0-103 decimal

Concatenation indication (CI)

1001SS1111111111 (5 bits are unspecified)

FIGURE 3-14/G.709

TU-1/TU-2 pointer coding

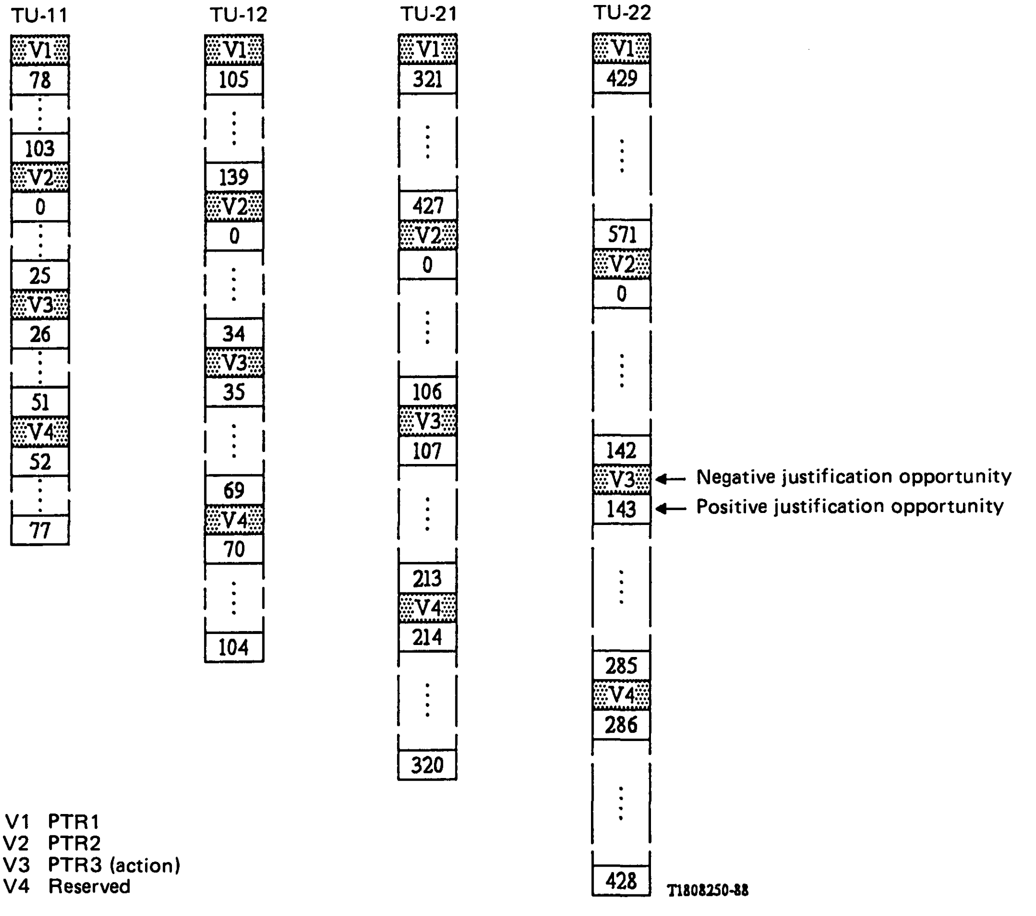


FIGURE 3-15/G.709

TU pointer offsets

3.3.3 *TU-1/TU-2 multiframe indication byte*

TU-1/TU-2 multiframe indication byte (H4) relates to the lowest level of multiplexing structure and indicates a variety of different multiframes for use by certain payloads. Specifically it provides:

- 500 μs (4-frame) multiframe identifying frames containing TU-1/TU-2 pointers in the floating TU-1/TU-2 mode, and reserved byte locations in the locked TU-1 mode;
- 2 ms (16-frame) multiframe for byte synchronous out-slot-signalling for 2048 kbit/s payloads in the locked TU-1 mode;
- 3 ms (24-frame) multiframe for byte synchronous out-slot-signalling for 1544 kbit/s payloads in the locked TU-1 mode.

The coding of the H4 byte is illustrated in Figures 3-16/G.709 to 3-18/G.709.

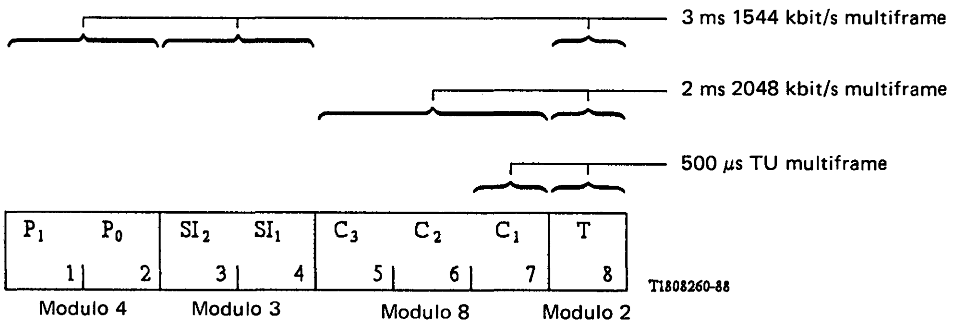


FIGURE 3-16/G.709

TU multiframe indicator byte (H4)

Bit 1 2	3 4	5 6 7	8	Frame	Time
					0
0 0	0 0	0 0 0	0	0	
0 0	0 0	0 0 0	1	1	
0 0	0 1	0 0 1	0	2	
0 0	0 1	0 0 1	1	3	500 µs TU multiframe
0 0	1 0	0 1 0	0	4	
0 0	1 0	0 1 0	1	5	
0 1	0 0	0 1 1	0	6	
0 1	0 0	0 1 1	1	7	
0 1	0 1	1 0 0	0	8	
0 1	0 1	1 0 0	1	9	
0 1	1 0	1 0 1	0	10	
0 1	1 0	1 0 1	1	11	
1 0	0 0	1 1 0	0	12	
1 0	0 0	1 1 0	1	13	
1 0	0 1	1 1 1	0	14	
1 0	0 1	1 1 1	1	15	2 ms 2048 kbit/s signalling cycle
1 0	1 0	0 0 0	0	16	
1 0	1 0	0 0 0	1	17	
1 1	0 0	0 0 1	0	18	
1 1	0 0	0 0 1	1	19	
1 1	0 1	0 1 0	0	20	
1 1	0 1	0 1 0	1	21	
1 1	1 0	0 1 1	0	22	
1 1	1 0	0 1 1	1	23	3 ms 1544 kbit/s signalling cycle
0 0	0 0	1 0 0	0	24	
0 0	0 0	1 0 0	1	25	
0 0	0 1	1 0 1	0	26	
0 0	0 1	1 0 1	1	27	
0 0	1 0	1 1 0	0	28	
0 0	1 0	1 1 0	1	29	
0 1	0 0	1 1 1	0	30	
0 1	0 0	1 1 1	1	31	
0 1	0 1	0 0 0	0	32	
0 1	0 1	0 0 0	1	33	
0 1	1 0	0 0 1	0	34	
0 1	1 0	0 0 1	1	35	
1 0	0 0	0 1 0	0	36	
1 0	0 0	0 1 0	1	37	
1 0	0 1	0 1 1	0	38	
1 0	0 1	0 1 1	1	39	
1 0	1 0	1 0 0	0	40	
1 0	1 0	1 0 0	1	41	
1 1	0 0	1 0 1	0	42	
1 1	0 0	1 0 1	1	43	
1 1	0 1	1 1 0	0	44	
1 1	0 1	1 1 0	1	45	
1 1	1 0	1 1 1	0	46	
1 1	1 0	1 1 1	1	47	6 ms = cycle repeat time

Note – The full H4 coding sequence is mandatory in locked TU mode, and optional in floating TU mode.

FIGURE 3-17/G.709

TU multiframe indicator byte (H4) full coding sequence

Bit				Frame	Time
1 2	3 4	5 6 7	8		
					0
1 1	1 1	1 1 0	0	0	
1 1	1 1	1 1 0	1	1	
1 1	1 1	1 1 1	0	2	
1 1	1 1	1 1 1	1	3	500 µs TU multiframe

Note 1 – The use of reduced mode can be detected by bits 3 and 4 being equal to binary 1.

Note 2 – The reduced H4 coding sequence is optional in floating TU mode.

FIGURE 3-18/G.709

TU multiframe indicator byte (H4) reduced coding sequence

For network elements that operate only in the floating TU-1/TU-2 mode, a simplified multiframe alignment byte may be used. The simplified version provides only the 500 µs multiframe. The 2 or 3 ms multiframe of any signalling within floating TU-1s is indicated by per-TU multiframe indicators carried within the TU-1. Figure 3-13/G.709 shows the VC-1/VC-2 mapping in the multiframed TU-1/TU-2.

A converter from locked to floating TUs is permitted to pass H4 through transparently. A converter from floating to locked TUs must recover and align the multiframes from all of the floating TUs, and thus can transmit any convenient full multiframe on the locked TU side.

3.3.4 *TU-1/TU-2 frequency justification*

The TU-1/TU-2 pointer is used to frequency justify the VC-1/VC-2 exactly the same way that the TU-3 pointer is used to frequency justify the VC-3. A positive justification opportunity immediately follows the V3 byte. Additionally, V3 serves as the negative justification opportunity such that when the opportunity is taken, V3 is overwritten by data. This is also shown in Figure 3-15/G.709. The indication of whether or not a justification opportunity has been taken is provided by the I- and D-bits of the pointer in the current TU multiframe. The value contained in V3 when not being used for a negative justification is not defined. The receiver is required to ignore the value contained in V3 whenever it is not used as negative justification.

3.3.5 *TU-1/TU-2 sizes*

Bits 5 and 6 of TU-1/TU-2 pointer indicate the size of the TU. Four sizes are currently provided as shown in Table 3-1/G.709.

TABLE 3-1/G.709

Size (binary)	Designation	TU pointer range (in 500 µs)
01	TU-22	0 à 571
00	TU-21	0 à 427
10	TU-12	0 à 139
11	TU-11	0 à 103

Note that this technique is only used at the TU-1/TU-2 levels.

3.3.6 *New data flag (NDF)*

Bits 1-4 (N-bits) of the pointer word carry an NDF. It is the mechanism which allows an arbitrary change of the value of a pointer, and possibly also the size of the TU, if that change is due to a change in the payload. If the change includes a change in size then, implicitly, there must be a simultaneous new data transition in all of the TUs in the TUG-21.

As with the TU-3 pointer NDF, the normal value is 0110 (transmitted), and the value 1001 (received exactly) indicates a new alignment for the VC, and possibly a new size. If a new size is indicated, then all TU pointers (1 to 4) in the TUG-21 must simultaneously indicate NDF with the same new size. The new alignment, and possibly size, is indicated by the pointer value and size value accompanying the NDF and takes effect at the offset indicated. The NDF should be enabled when the pointer value transits between its normal value and the concatenation indication (CI).

3.3.7 *TU concatenation*

TU-2s may be concatenated to form a TU-2-mc (concatenated m × TU-2s) to carry payloads requiring a capacity of more than a C-21 (for the TU-21 case) or C-22 (for the TU-22 case). A CI (1001 in bits 1-4, bits 5-6 unspecified, and all 1s in bits 7-16 of the TU-2 pointer) is used to show that this multi-C-2 payload, carried in a single VC-2-mc (concatenated m × VC-2), must be kept together.

Note that the TU-2 is carried in a TUG-2 as shown in Figure 5-4/G.709 and Figure 5-5/G.709.

If a TU-2 pointer contains the concatenation indication, then the pointer processor determines that this TU-2 is concatenated to the previous TU-2, and all operations indicated by the previous TU-2 pointer are to be performed on this TU-2 as well.

3.3.8 *TU pointer generation and interpretation*

The rules for generating and interpreting the TU-1/TU-2 pointer for the VC-1/VC-2 are an extension to the rules provided in §§ 3.2.5 and 3.2.6 for the TU-3 pointer with the following modifications:

1) The term TU-3 is replaced with TU-1/TU-2 and the term VC-3 is replaced with VC-1/VC-2.
2) Additional pointer generation rule 6: If the size of the TU within a TUG-21 is to change, then an NDF, as described in rule 5, is to be sent in all TUs of the new size in the group simultaneously.
3) Additional pointer interpretation rule 6: If an NDF of 1001 and an arbitrary new size of TU are received simultaneously in all of the TUs within a TUG-21, then the coincident pointers and sizes shall replace the current ones immediately.

3.4 *Pointer operation for STM-1 concatenation*

A concatenation indication contained in the AU-4 pointer is used to show that the STM-1 is part of an STM-Nc.

The AU-4 within the first STM-1 of an STM-Nc shall have a normal range of pointer values. All subsequent AU-4s within the grouped STM-Nc shall have their pointer values set to 1001 in bits 1-4, bits 5-6 unspecified, and all 1s in bits 7-16. Since this value does not indicate a valid offset, the pointer processors shall interpret this value to mean that they shall perform the same operations as performed on the first AU-4 of the grouped STM-Nc. The NDF must be set when changing a pointer to/from the concatenation value.

3.4.1 *Pointer generation*

The following additional pointer generation rule shall apply for AU-4 pointers:

If an STM-Nc signal is being transmitted, a pointer is generated for the AU-4 within the first STM-1 only. The concatenation indication is generated in place of the other pointers; all operations indicated by the AU-4 pointer in the first STM-1 apply to each STM-1 in the STM-Nc.

3.4.2 *Pointer interpretation*

The following additional pointer interpretation rule shall apply for AU-4 pointers:

If the pointer contains the concatenation indication, then the operations performed on the STM-1 are identical to those performed on the first STM-1 within the STM-Nc. Rules 3 and 4 of § 3.1.6 do not apply to this pointer.

4 Path overhead

4.1 *VC-1/VC-2 path overhead*

The first byte in the VC-1/VC-2 pointed to by the TU-1/TU-2 pointer is the VC-1/VC-2 path overhead byte. This byte is designated as V5.

This byte provides the functions of error checking, signal, label and path status of the VC-1/VC-2 paths. The bit assignments of the VC-1/VC-2 POH are specified in the following paragraphs and are illustrated in Figure 4-1/G.709.

V5 is used only in floating mode VC-1/VC-2s and is designated as an R-byte in locked mode VC-1/VC-2s. Floating mode and locked mode operation is described in § 5.8.

Bits 1 and 2 are used for error performance monitoring. A bit interleaved parity (BIP) scheme is specified. Bit 1 is set such that parity of all odd number bits (1, 3, 5 and 7) in all bytes in the previous VC-1/VC-2 is even and bit 2 is set similarly for the even number bits (2, 4, 6 and 8). Note that the calculation of the BIP-2 includes the VC-1/VC-2 POH bytes but excludes the TU-1/TU-2 pointers.

Bit 3 is a VC-1/VC-2 path far-end-block-error (FEBE) indication that is set to 1 and sent back towards a VC-1/VC-2 path originator if one or more errors were detected by the BIP-2, and is otherwise set to 0.

Bit 4 is unused (X). The receiver is required to ignore the value of this bit.

Bits 5 through 7 provide a VC-1/VC-2 signal label. Eight binary values are possible in these three bits. Value 0 indicates "VC-1/VC-2 path unequipped", and value 1 indicates "VC-1/VC-2 path equipped – non-specific payload". The remaining six values are reserved to be defined as required in specific VC-1/VC-2 mappings. Any value received, other than 0, indicates an equipped VC-1/VC-2 path.

Bit 8 is a VC-1/VC-2 path remote alarm indication. This bit is set to a 1 if either a TU-1/TU-2 path alarm indication signal (AIS) or a signal failure condition is being received, otherwise it is set to 0. The VC-1/VC-2 path remote alarm indication is sent back by the VC-1/VC-2 assembler.

BIP-2		FEBE	Unused	L1 Signal label	L2	L3	Remote alarm
1	2	3	4	5	6	7	8

VC path signal label coding

0 0 0 Unequipped
0 0 1 Equipped, non-specific payload
0 1 0
⋮
1 1 0
1 1 1 } Equipped, unused

VC path FEBE coding

0 No errors
1 One or more errors

T1808290-88

Note – VC path overhead is defined only in VC-21 No. 1 of VC-21-mc.

FIGURE 4-1/G.709

VC-1/VC-2 path overhead (V5)

4.2 *VC-3/VC-4 path overhead*

The VC-3/VC-4 POH will be assigned to and remain with the payload until the payload is demultiplexed and will be used for functions that are necessary in transporting all VC-3/VC-4. Note that this does not preclude the allocation of other overhead in specific mappings (such as justification control for mapping asynchronous 44 736 kbit/s signals). That type of overhead is payload specific whereas the POH defined in this section is payload independent.

The VC-4/VC-32 POH consists of nine bytes denoted J1, B2, C2, G1, F2, H4, Z1-Z3. The VC-31 POH consists of six bytes denoted J1, B3, C2, G1, G2, H4.

4.2.1 *VC-3/VC-4 path trace (J1)*

This is the first byte in the VC; its location is indicated by the associated AU/TU pointer. This byte is used to repetitively transmit a 64 byte, fixed length string so that a path receiving terminal can verify its continued connection to the intended transmitter. The content of the message is not constrained by this standard since it is assumed to be user programmable at both transmit and receive ends.

4.2.2 *Path BIP-8 (B3)*

One byte is allocated in each VC-3 or VC-4 for a path error monitoring function. This function shall be a BIP-8 code using even parity. The path BIP-8 is calculated over all bits of the previous VC-3 or VC-4 before scrambling. The computed BIP-8 is placed in the B3 byte of the VC-3 or VC-4 before scrambling.

4.2.3 *Signal label (C2)*

One byte is allocated to indicate the composition of the VC-3/VC-4. Of the 256 possible binary values, two are defined here and the remaining 254 values are reserved to be defined as required in specific VC-3/VC-4 mappings.

- Value 0 indicates "VC-3/VC-4 path unequipped". This value shall be originated if the section is complete but there is no VC-3/VC-4 path originating equipment.
- Value 1 indicates "VC-3/VC-4 path equipped – non-specific payload". This value can be used for all payloads that need no further differentiation, or that achieve differentiation by other means such as messages from an operations system.

Note that any value received, other than value 0, constitutes an "equipped" condition.

4.2.4 *Path status (G1)*

One byte is allocated to convey back to a VC-3/VC-4 path originator the path terminating status and performance. This feature permits the status and performance of the complete duplex path to be monitored at either end, or at any point along that path. As illustrated in Figure 4-2/G.709, bits 1 through 4 convey the count of interleaved-bit blocks that have been detected in error by the path BIP-8 code (B3). This count has nine legal values, namely 0-8 errors. The remaining seven possible values represented by these four bits can only result from some unrelated condition and shall be interpreted as zero errors. VC-3/VC-4 path remote alarm indication is sent back by the VC-3/VC-4 assembler whenever the VC-3/VC-4 assembler is not receiving a valid signal. The VC-3/VC-4 path remote alarm indication is bit 5, which is set to one to indicate VC-3/VC-4 path remote alarm and is otherwise set to zero. The specific received conditions under which VC-3/VC-4 path remote alarm is initiated are path AIS, signal failure conditions or path tracer mismatch. Bits 6, 7 and 8 are not used.

4.2.5 *Path user channel (F2)*

One byte is allocated for user communication purposes between path elements.

4.2.6 *Multiframe indicator (H4)*

This byte provides a generalized multiframe indicator for payloads. Currently, this indicator is only used for TUG-structured payloads as described in § 3.3.3.

4.2.7 *Spare (Z3-Z5)*

Three bytes are allocated for future, as yet undefined, purposes. These bytes have no defined value. The receiver is required to ignore the value contained in these bytes.

FEBE				Remote alarm	Unused		
1	2	3	4	5	6	7	8

VC path FEBE coding

T1808300-88

0 0 0 0 No errors
0 0 0 1 One error
⋮
0 1 1 1 Seven errors
1 0 0 0
1 0 0 1 ⎫
⋮ ⎬ No errors
1 1 1 1 ⎭

FIGURE 4-2/G.709

VC-3/VC-4 path status (G1)

5 Mapping of tributaries into VCs

Accommodation of asynchronous and synchronous tributaries presently defined in Recommendation G.702 shall be possible. At the TU-1/TU-2 level, asynchronous accommodation utilizes only the floating mode, whereas synchronous accommodation utilizes both the locked and the floating mode.

Figure 5-1/G.709 shows TU-1 and TU-2 sizes and formats.

5.1 *Mapping of tributaries into VC-4*

5.1.1 *Asynchronous 139 264 kbit/s*

One 139 264 kbit/s signal can be mapped into a VC-4 container of an STM-1 frame as shown in Figures 5-2/G.709 and 5-3/G.709.

The VC-4 container consists of nine bytes (1 column) path overhead (POH) plus a 9 row by 260 column payload structure as shown in Figure 5-2/G.709.

This payload can be used to carry one 139 264 kbit/s signal:

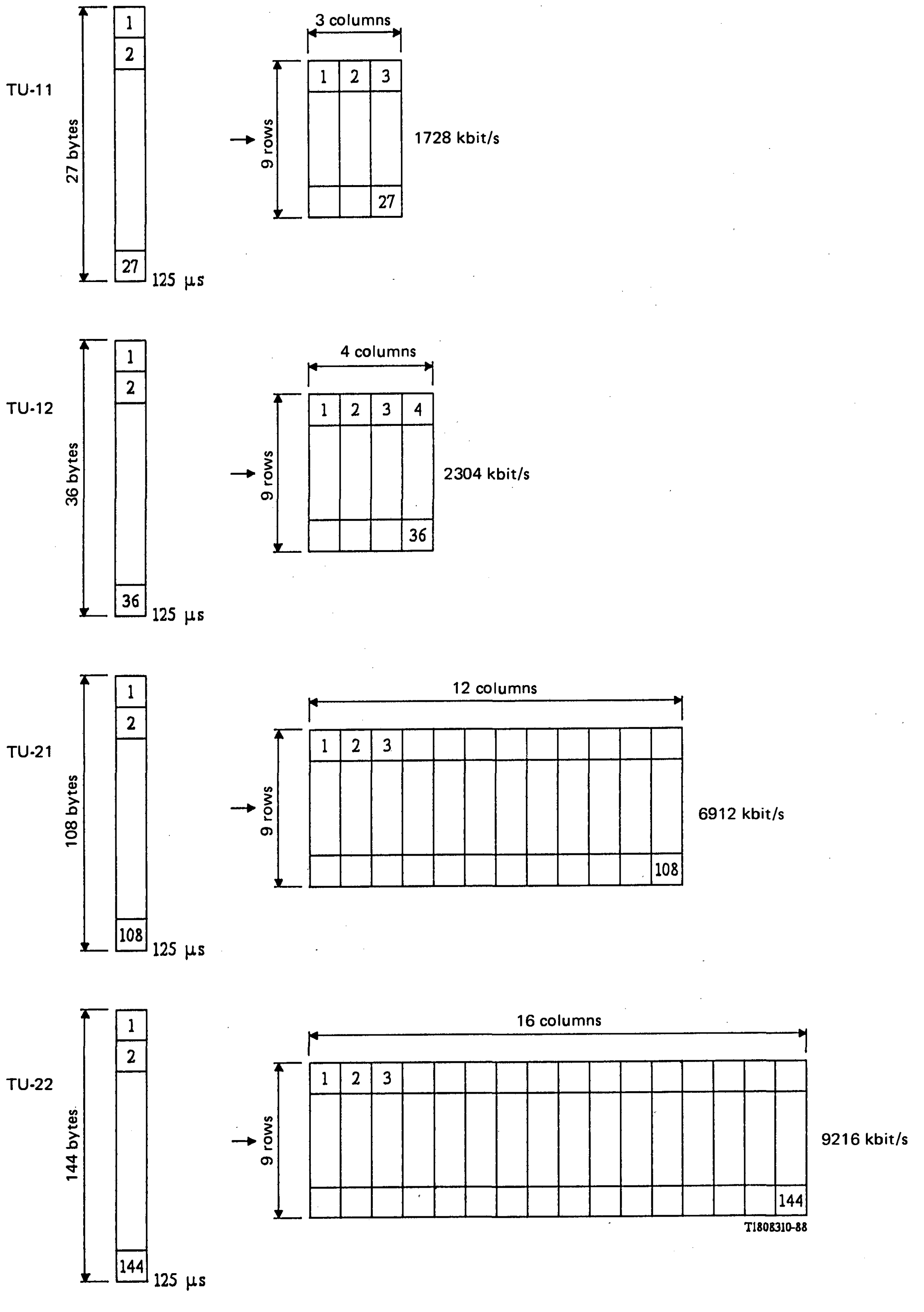
- Each of the nine rows is partitioned into 20 blocks, consisting of 13 bytes each (Figure 5-2/G.709).
- In each row one justification opportunity (S) bit and five justification control (C) bits are provided (Figure 5-3/G.709).
- The first byte of one block consists of:
  - i) eight information (I) bits (byte W), or
  - ii) eight fixed stuff (R) bits (byte Y), or
  - iii) one justification control (C) bits, plus five fixed fixed stuff (R) bits, plus two overhead (O) bits (byte X), or
  - iv) six information (I) bits, plus one justification opportunity (S) bit, plus one fixed stuff (R) bit, (byte Z).
- The last 12 bytes of one block consists of information bits (I).

The sequence of all these bytes is shown in Figure 5-3/G.709.

The overhead (O) bits are reserved for further overhead communication purposes.

The set of five justification control (C) bits in every row is used to control the corresponding justification opportunity (S) bit. C C C C C = 0 0 0 0 0 indicates that the S bit is an information bit, whereas C C C C C = 1 1 1 1 1 indicates that the S bit is a justification bit. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S bit when used as justification bit is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a justification bit.



Note – The TU pointer bytes (V1-V4) are located in byte 1 (using a four-frame multiframe).

FIGURE 5-1/G.709

TU-1 and TU-2 sizes and formats

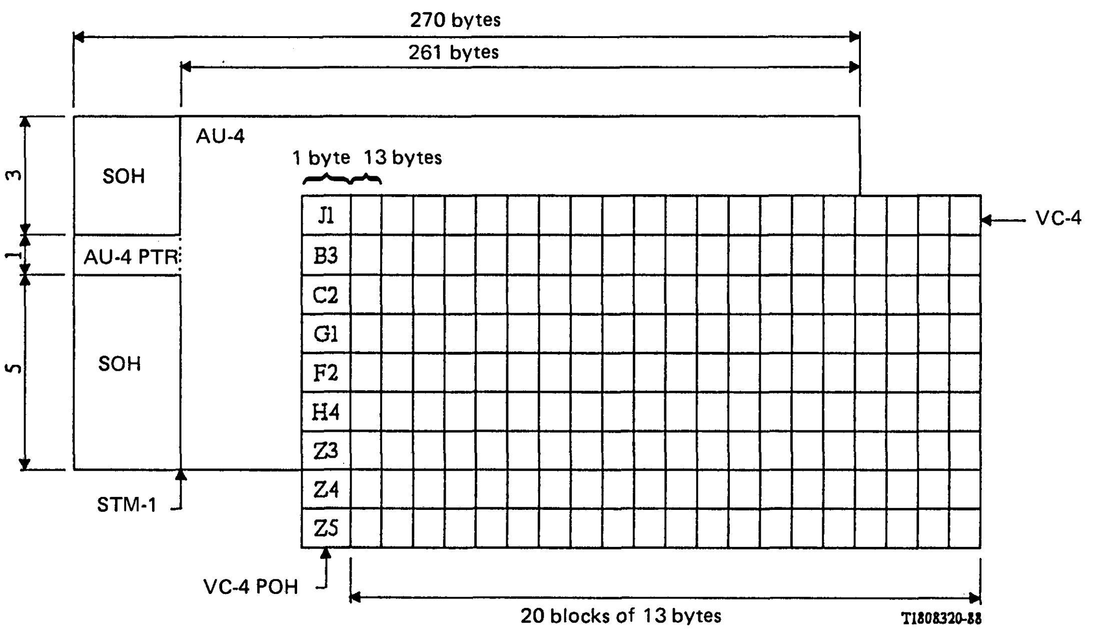
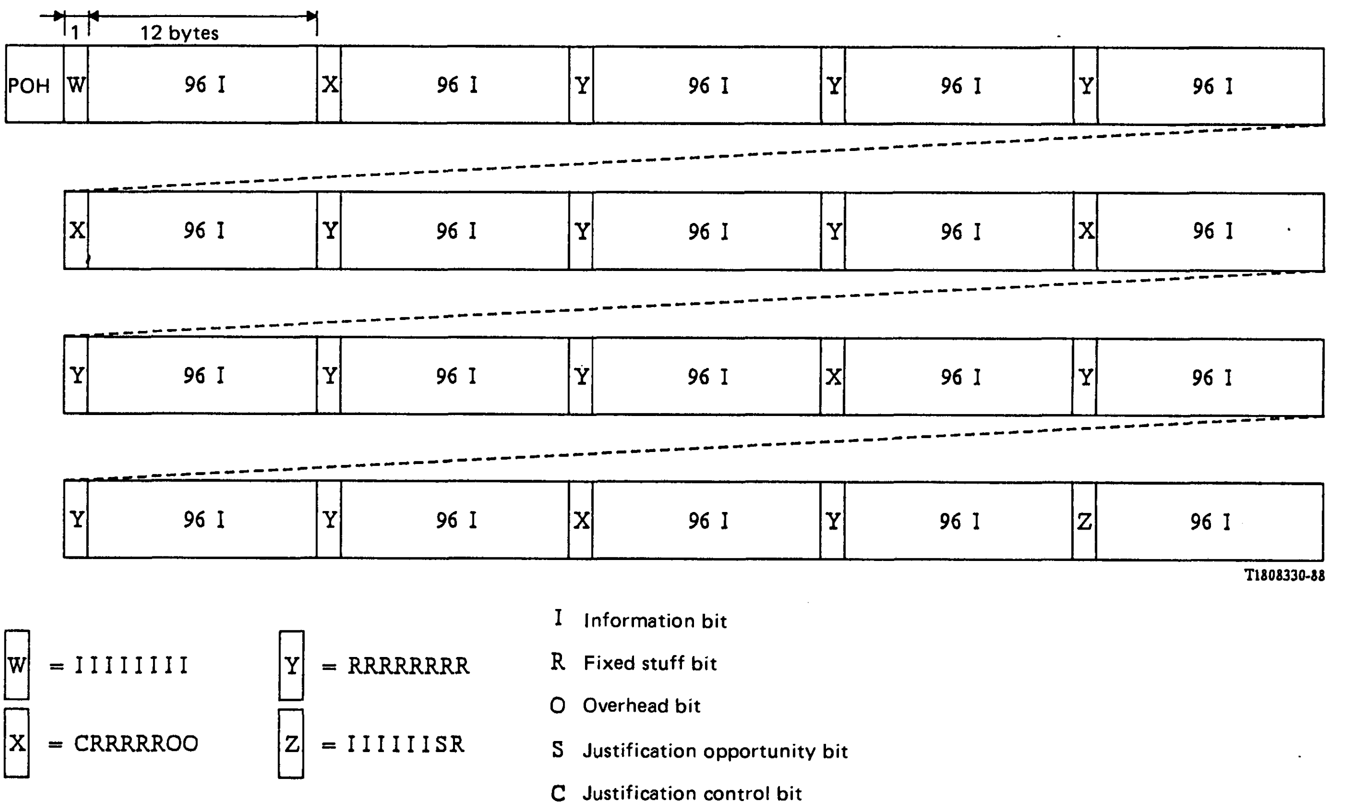


FIGURE 5-2/G.709

Mapping of VC-4 into STM-1 and block structure of VC-4 for asynchronous 139 264 kbit/s mapping



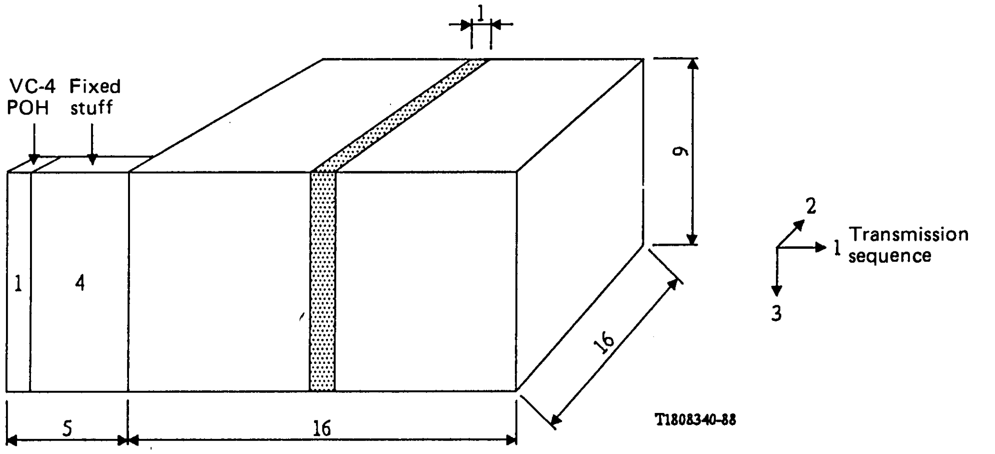
Note — This figure shows one row of the nine-row VC-4 container structure.

FIGURE 5-3/G.709

Mapping of asynchronous 139 264 kbit/s tributary into VC-4

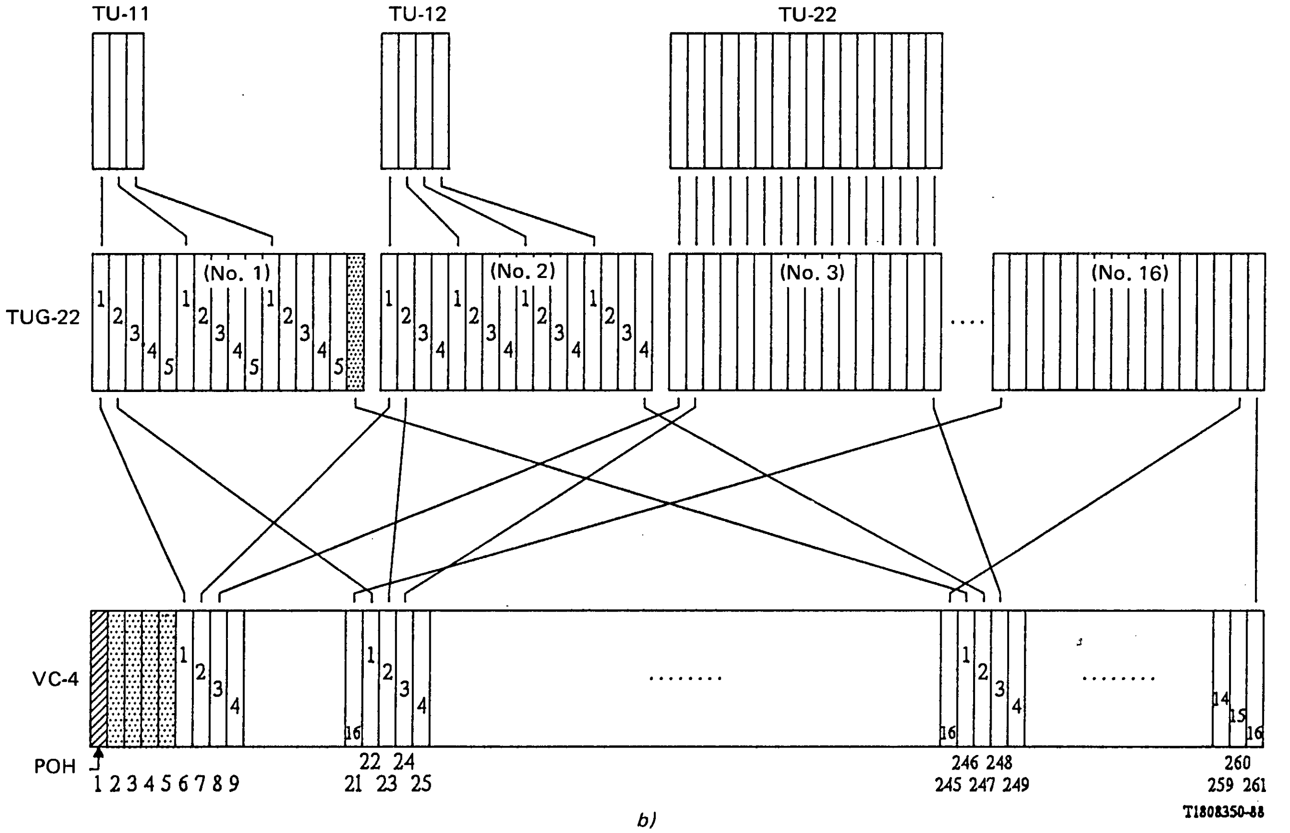
5.1.2 *TUG-22*

Sixteen TUG-22s can be mapped into a VC-4. This is illustrated in three-dimensional form in a) of Figure 5-4/G.709 and in linear form in b) of Figure 5-4/G.709.



Note – For clarity in the figure, only one TUG-22 has been shown (indicated by the shaded slice). The other TUG-22s are mapped into the VC-4 in the same way.

a)



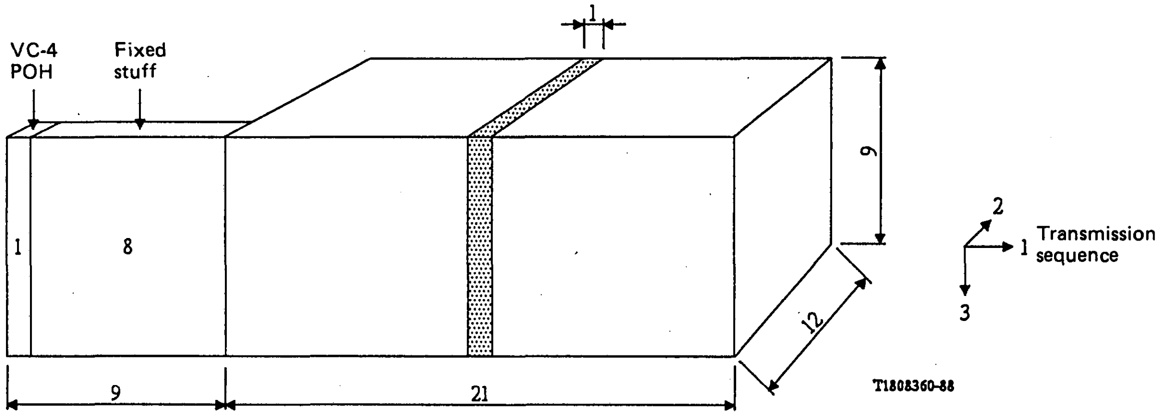
b)

FIGURE 5-4/G.709

Mapping of TUG-22 into VC-4

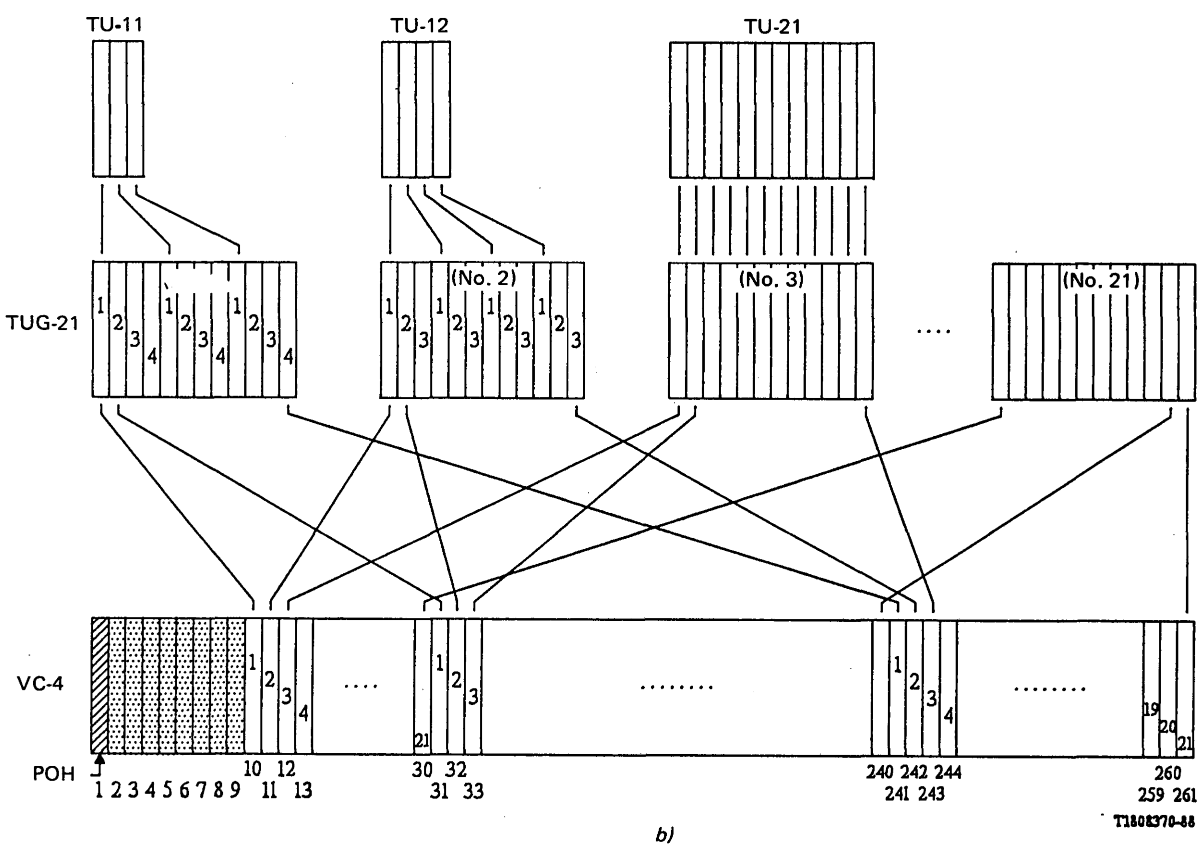
5.1.3 *TUG-21*

Twenty-one TUG-21s can be mapped into a VC-4. This is shown in three-dimensional form in a) of Figure 5-5/G.709 and in linear form in b) of Figure 5-5/G.709.



Note – For clarity in the figure, only one TUG-21 has been shown (indicated by the shaded slice). The other TUG-21s are mapped into the VC-4 in the same way.

a)



b)

FIGURE 5-5/G.709

Mapping of TUG-21 into VC-4

5.1.4 *TU-32*

Three TU-32s can be mapped into a VC-4. This is illustrated in Figure 5-6/G.709.

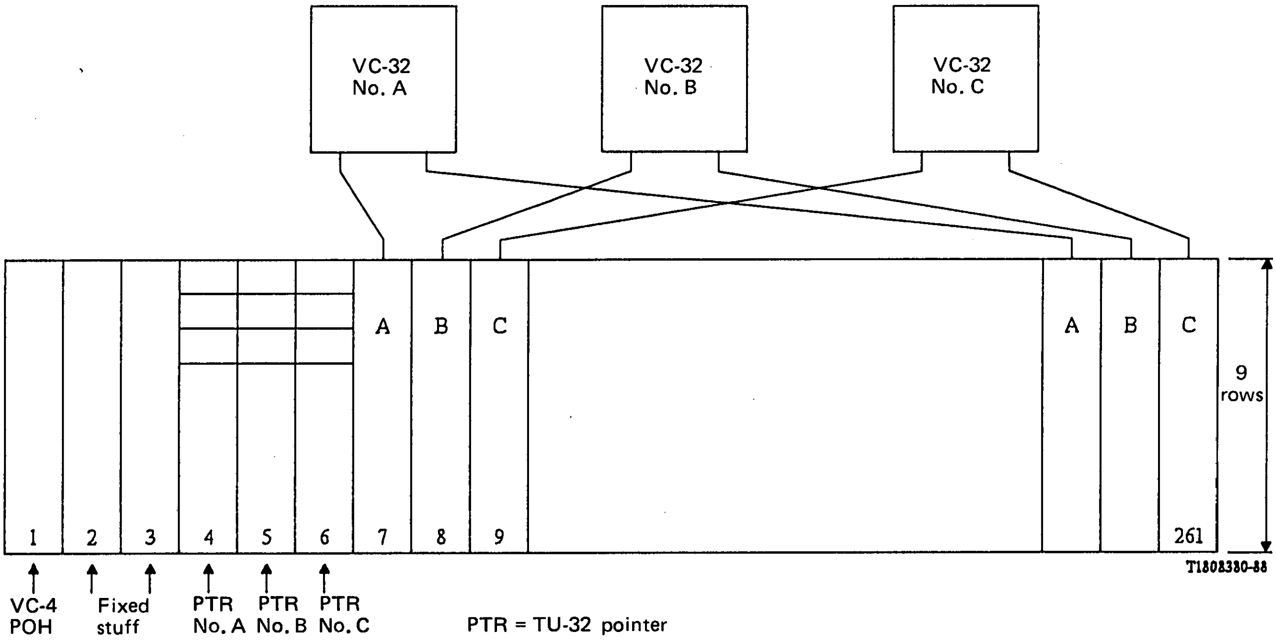


FIGURE 5-6/G.709

Mapping of TU-32 into VC-4

5.1.5 *TU-31*

Four TU-31s can be mapped into a VC-4. This is illustrated in Figure 5-7/G.709.

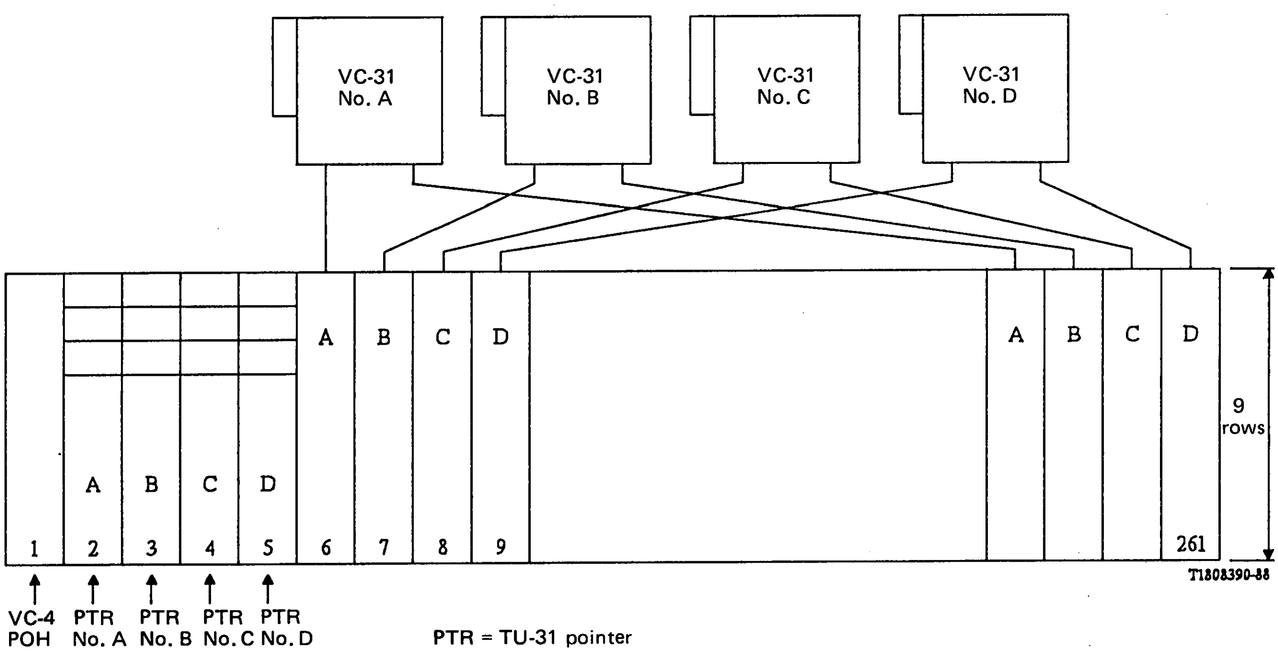


FIGURE 5-7/G.709

Mapping of TU-31 into VC-4

5.2 *Mapping of tributaries into VC-32*

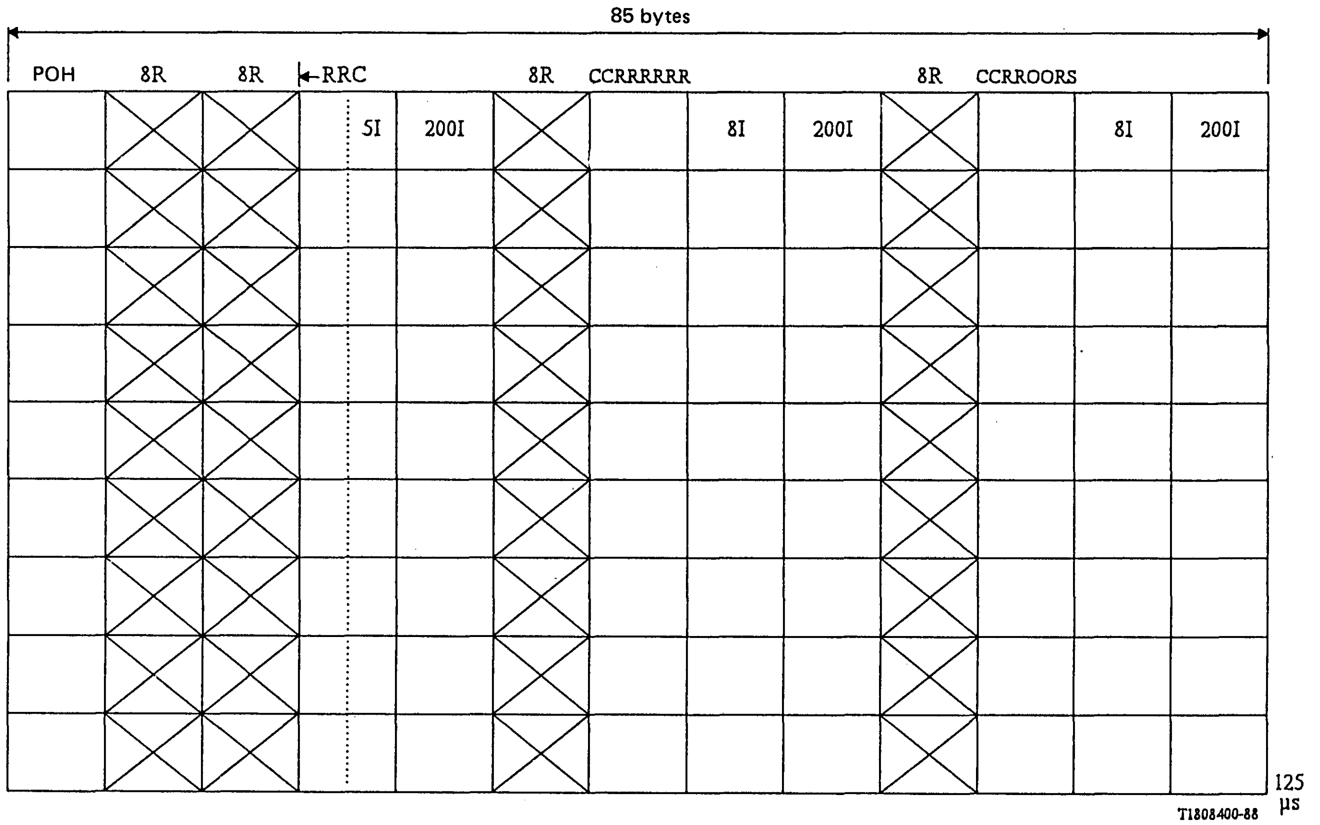
5.2.1 *Asynchronous 44 736 kbit/s*

One 44 736 kbit/s signal can be mapped into a VC-32, as shown in Figure 5-8/G.709.

The VC-32 consists of nine subframes every 125 µs. Each subframe consists of one byte of VC-3 POH, 621 data bits, a set of five justification control bits, one justification opportunity bit and two overhead communication channel bits. The remaining bits are fixed stuff (R) bits. The O bits are reserved for future overhead communication purposes.

The set of five justification control (C) bits is used to control the justification opportunity (S) bit. C C C C C = 0 0 0 0 0 indicates that the S bit is a data bit, whereas C C C C C = 1 1 1 1 1 indicates that S bit is a justification bit. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S bit when used as justification bits is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a justification bit.



R Fixed stuff bit
C Justification control bit
S Justification opportunity bit
I Information bit
O Overhead bit

FIGURE 5-8/G.709

Mapping of an asynchronous 44 736 kbit/s tributary into a VC-32

5.2.2 *TUG-21*

Seven TUG-21s can be mapped into a VC-32. This is illustrated in Figure 5-9/G.709. The figure also illustrates the formation of the TUG-21 from TU-11, TU-12 and TU-21.

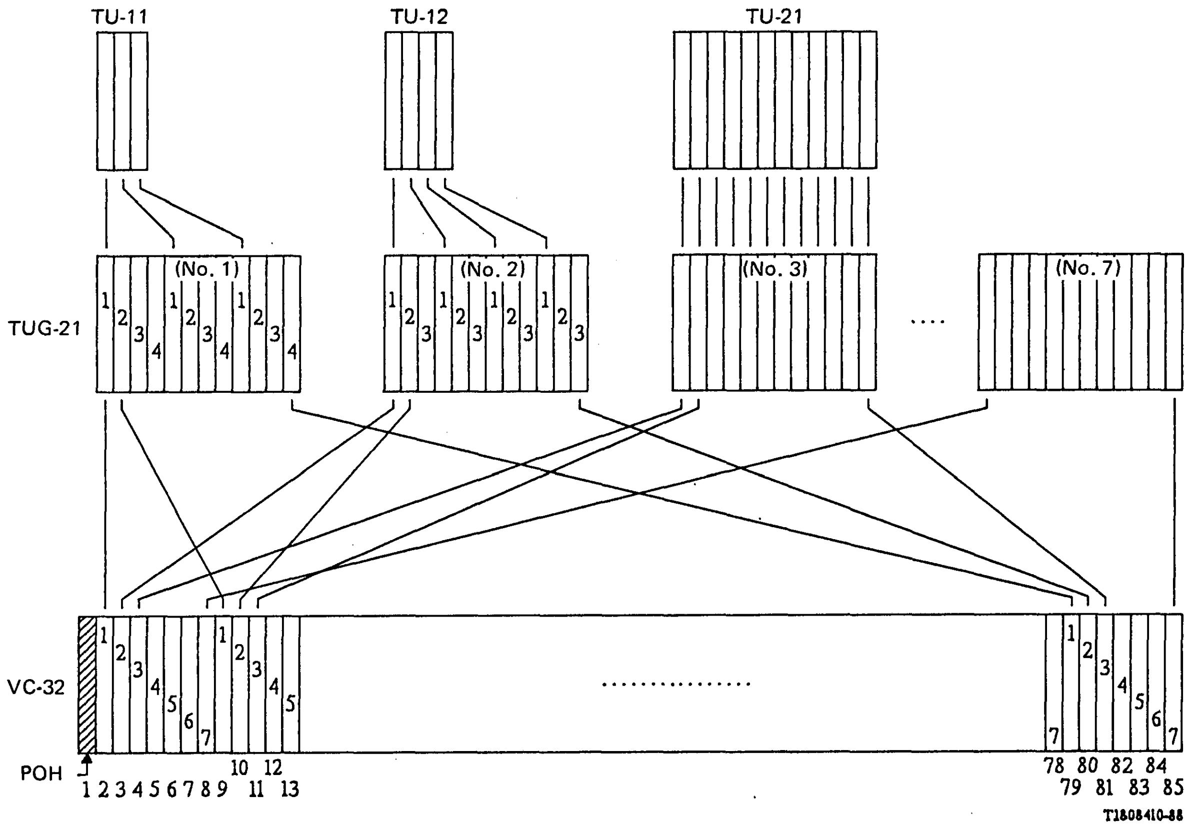


FIGURE 5-9/G.709

Mapping of TUG-21s into VC-32

5.3 *Mapping of tributaries into VC-31*

5.3.1 *Asynchronous 34 368 kbit/s*

One 34 368 kbit/s signal can be mapped into a VC-31 as shown in Figure 5-10/G.709.

In addition to the VC-31 POH, the VC-31 consists of a payload of 9 × 64 bytes every 125 µs. This payload is divided in three subframes, each subframe divided in 12 sectors and consisting of:

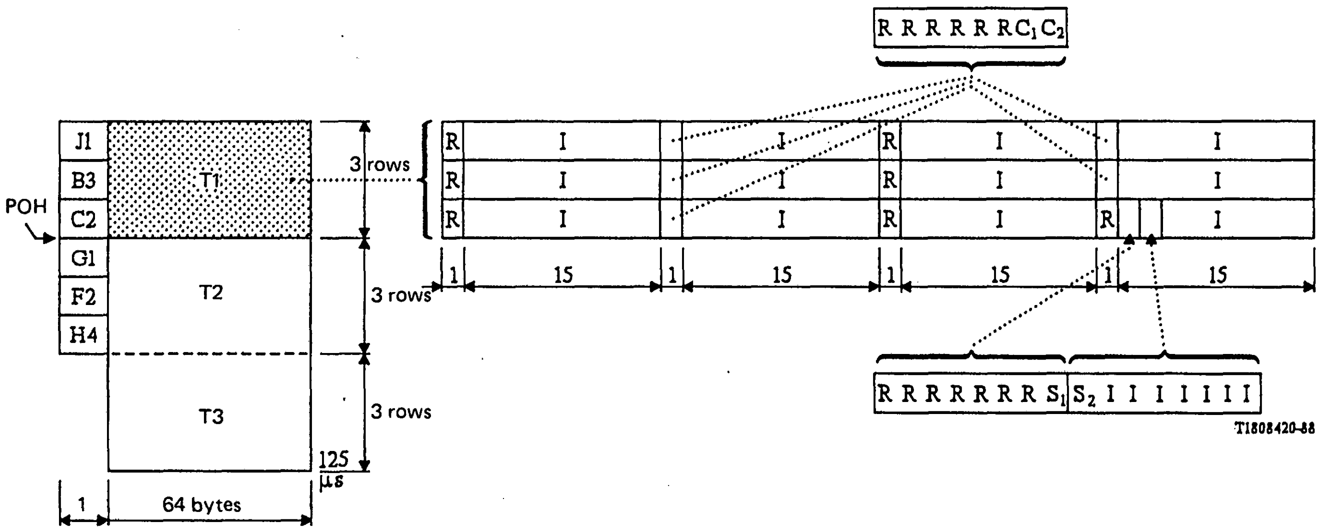
- 1431 information (I) bits.
- two sets of five justification control bits (C_1, C_2).
- two justification opportunity bits (S_1, S_2).
- 93 fixed stuff bits (R).

Two sets (C_1, C_2) of five justification control bits are used to control the two justification opportunity bits S_1 and S_2 respectively.

C_1 C_1 C_1 C_1 C_1 = 0 0 0 0 0 indicates that S_1 is a data bit while C_1 C_1 C_1 C_1 C_1 = 1 1 1 1 1 indicates that S_1 is a justification bit. C_2 bits control S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

Note – The same mapping could be used for bit or byte synchronous 34 368 kbit/s. In these cases, S_1 bit should be a fixed stuff and the S_2 bit an information bit. By setting the C_1 bits to 1 and the C_2 bits to 0, a common desynchronizer could be used for both asynchronous and synchronous 34 368 kbit/s.



R Fixed stuff bit
C1, C2 Justification control bit
S1, S2 Justification opportunities bit
I Information bit

FIGURE 5-10/G.709

Mapping of an asynchronous 34 368 kbit/s tributary into a VC-31

5.3.2 *TUG-22*

Four TUG-22s can be mapped into a VC-31. This is illustrated in Figure 5-11/G.709. The figure also illustrates the formation of the TUG-22 from TU-11, TU-12 and TU-22.

5.3.3 *TUG-21*

Five TUG-21s can be mapped into a VC-31. This is illustrated in Figure 5-12/G.709. The figure also illustrates the formation of the TUG-21 from TU-11, TU-12 and TU-21.

5.4 *Mapping of tributaries into VC-22*

5.4.1 *Asynchronous 8448 kbit/s*

One 8448 kbit/s signal can be mapped into a VC-22. Figure 5-13/G.709 shows this over a period of 500 µs.

In addition to the VC-22 POH, the VC-22 consists of:

- 4220 information (I) bits.
- 24 justification control bits (C_1, C_2).
- eight justification opportunity bits (S_1, S_2).
- 316 fixed stuff (R) bits.

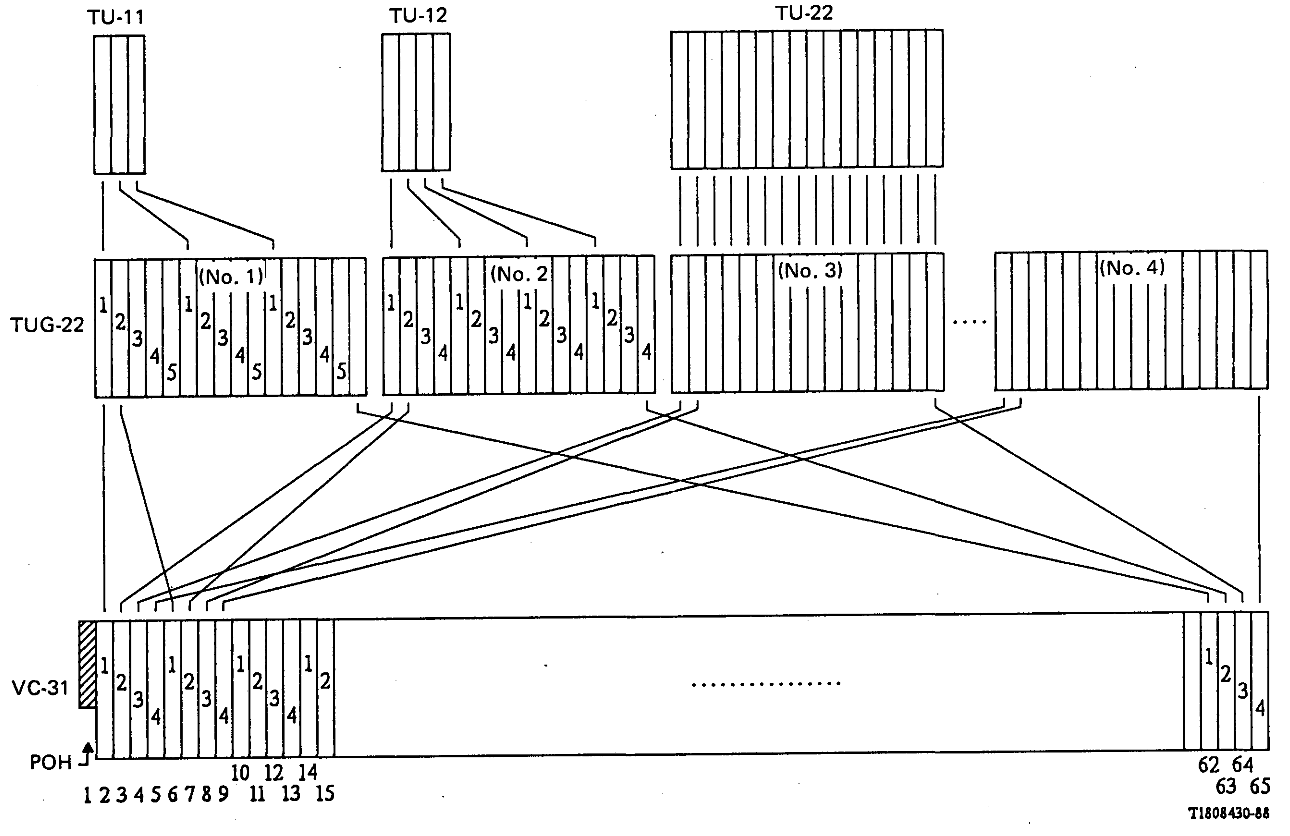
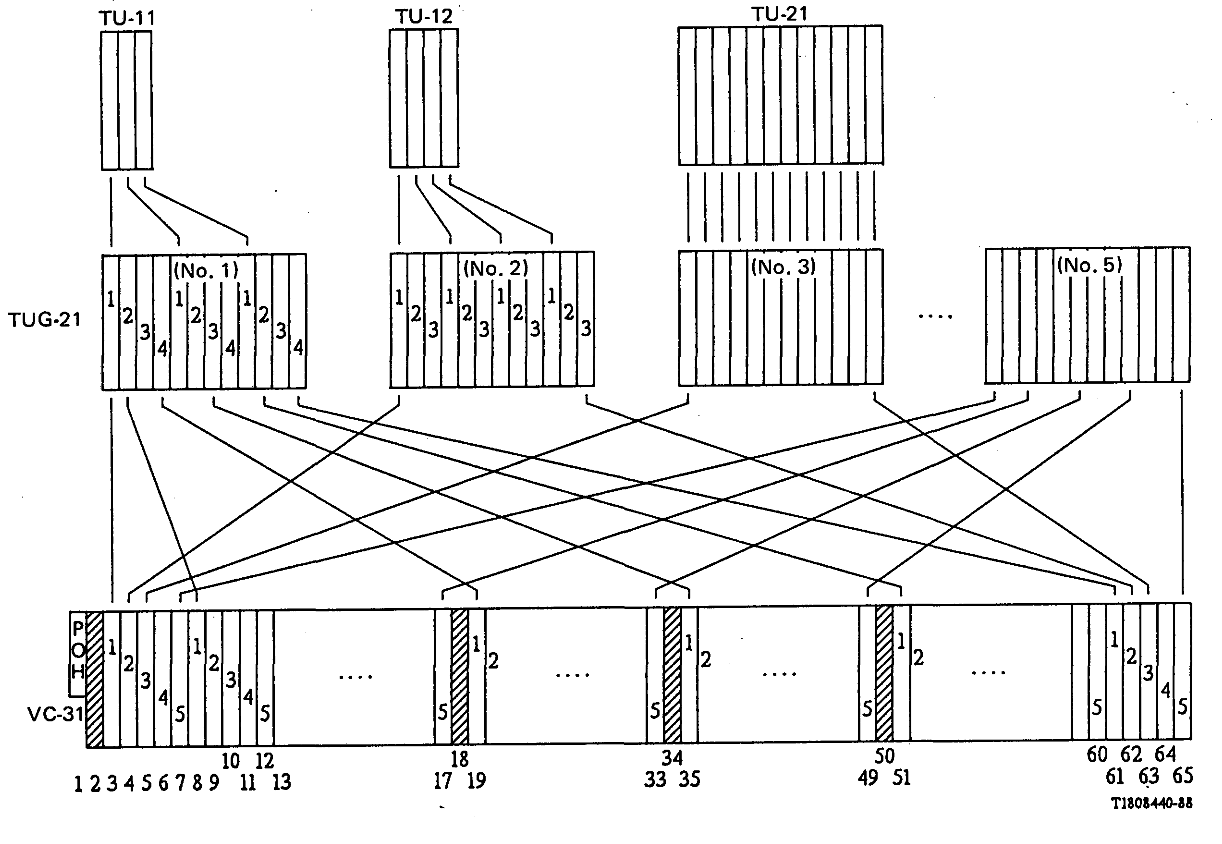


FIGURE 5-11/G.709

Mapping of TUG-22s into a VC-31



Note – Columns 2, 18, 34 and 50 are fixed stuff.

FIGURE 5-12/G.709

Mapping of TUG-21s into a VC-31

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunity bits S_1 and S_2 respectively.

C_1 C_1 C_1 = 0 0 0 indicates that S_1 is a data bit while C_1 C_1 C_1 = 1 1 1 indicates that S1 is a justification bit. C_2 bits control S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit error in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

V5	(11 × 8) I	R	(11 × 8) I	I I I I I I I I		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRR		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRR		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRS_1	S_2I I I I I I I	(9 × 8) I	125 µs
R	(11 × 8) I	R	(11 × 8) I	I I I I I I I I		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRR		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRR		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRS_1	S_2I I I I I I I	(9 × 8) I	250 µs
R	(11 × 8) I	R	(11 × 8) I	I I I I I I I I		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRR		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRR		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRS_1	S_2I I I I I I I	(9 × 8) I	375 µs
R	(11 × 8) I	R	(11 × 8) I	I I I I I I I I		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRR		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRR		(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	C_1C_2RRRRRS_1	S_2I I I I I I I	(9 × 8) I	500 µs

T1808450-88

R Fixed stuff bit
C Justification control bit
S Justification opportunity bit
I Information bit

FIGURE 5-13/G.709

Mapping of asynchronous 8448 kbit/s tributary into a VC-22

5.4.2 *Synchronous 8448 kbit/s*

One bit or byte synchronous 8448 kbit/s signal can be mapped into a VC-22. Figure 5-14/G.709 shows this over a period of 500 µs.

Note – A common desynchronizer can be used for both asynchronous and synchronous mappings.

VS	(11 × 8) I	R	(11 × 8) I	IIIIIIII	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(10 × 8) I	125 µs
R	(11 × 8) I	R	(11 × 8) I	IIIIIIII	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(10 × 8) I	250 µs
R	(11 × 8) I	R	(11 × 8) I	IIIIIIII	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(10 × 8) I	375 µs
R	(11 × 8) I	R	(11 × 8) I	IIIIIIII	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(11 × 8) I	
R	(11 × 8) I	R	(11 × 8) I	10RRRRRR	(10 × 8) I	500 µs

T1808460-88

R Fixed stuff bit
C Justification control bit
S Justification opportunity bit
I Information bit

FIGURE 5-14/G.709

Mapping of synchronous 8448 kbit/s tributary into a VC-22

5.5 *Mapping of tributaries into VC-21*

5.5.1 *Asynchronous 6312 kbit/s*

One 6312 kbit/s signal can be mapped into a VC-21. Figure 5-15/G.709 shows this over a period of 500 µs.

In addition to the VC-2 POH, the VC-21 consists of 3152 data bits, 24 justification control bits, eight justification opportunity bits and 32 overhead communication channel bits. The remaining bits are fixed stuff (R). The O bits are reserved for future overhead communication purposes.

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunities S_1 and S_2 respectively. C_1 C_1 C_1 = 0 0 0 indicates that S_1 is a data bit while C_1 C_1 C_1 = 1 1 1 indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit errors in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

5.5.2 *Bit synchronous 6312 kbit/s*

The bit synchronous mapping for 6312 kbit/s tributary is shown in Figure 5-16/G.709.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mapping.

V5	IIIIIIIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	C_1C_2OOOOIR	(24 × 8) I	RRRRRRRR	
IIIIIIII	C_1C_2OOOOIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	C_1C_2IIIS_1S_2R	(24 × 8) I		125 µs
RRRRRRRR	IIIIIIIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	C_1C_2OOOOIR	(24 × 8) I	RRRRRRRR	
IIIIIIII	C_1C_2OOOOIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	C_1C_2IIIS_1S_2R	(24 × 8) I		250 µs
RRRRRRRR	IIIIIIIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	C_1C_2OOOOIR	(24 × 8) I	RRRRRRRR	
IIIIIIII	C_1C_2OOOOIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	C_1C_2IIIS_1S_2R	(24 × 8) I		375 µs
RRRRRRRR	IIIIIIIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	C_1C_2OOOOIR	(24 × 8) I	RRRRRRRR	
IIIIIIII	C_1C_2OOOOIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	C_1C_2IIIS_1S_2R	(24 × 8) I		500 µs

T1808471-89

R Fixed stuff bit
C Justification control bit
S Justification opportunity bit
I Information bit
O Overhead bit

FIGURE 5-15/G.709

Mapping of asynchronous 6312 kbit/s tributary

V5	IIIIIIIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	10OOOOIR	(24 × 8) I	RRRRRRRR	
IIIIIIII	10OOOOIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	10IIIRIR	(24 × 8) I		125 µs
RRRRRRRR	IIIIIIIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	10OOOOIR	(24 × 8) I	RRRRRRRR	
IIIIIIII	10OOOOIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	10IIIRIR	(24 × 8) I		250 µs
RRRRRRRR	IIIIIIIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	10OOOOIR	(24 × 8) I	RRRRRRRR	
IIIIIIII	10OOOOIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	10IIIRIR	(24 × 8) I		375 µs
RRRRRRRR	IIIIIIIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	10OOOOIR	(24 × 8) I	RRRRRRRR	
IIIIIIII	10OOOOIR	(24 × 8) I	RRRRRRRR	
RRRRRRRR	10IIIRIR	(24 × 8) I		500 µs

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R Fixed stuff bit
I Information bit
O Overhead bit

FIGURE 5-16/G.709

Mapping of bit synchronous 6312 kbit/s tributary

5.5.3 *Byte synchronous 6312 kbit/s*

Under study.

5.6 *Mapping of tributaries into VC-12*

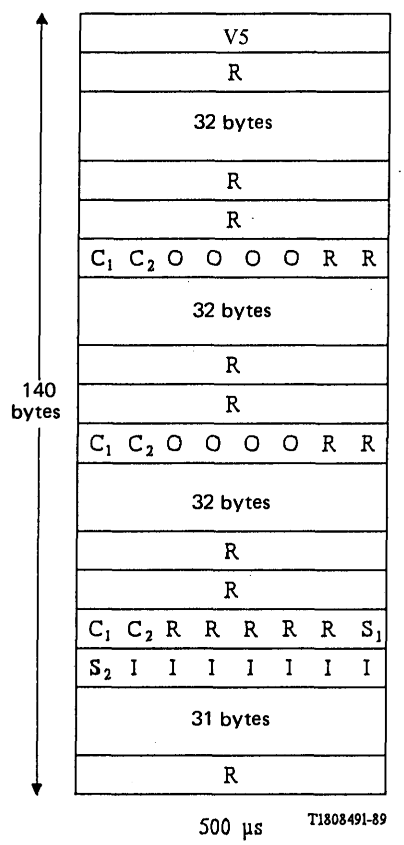
5.6.1 *Asynchronous 2048 kbit/s*

One 2048 kbit/s signal can be mapped into a VC-12. Figure 5-17/G.709 shows this over a period of 500 µs.

In addition to the VC-1 POH, the VC-12 consists of 1023 data bits, six justification control bits, two justification bits and eight overhead communication channel bits. The remaining bits are fixed stuff (R) bits. The O bits are reserved for future overhead communication purposes.

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunities S_1 and S_2 respectively. C_1 C_1 C_1 = 0 0 0 indicates that S_1 is a data bit while C_1 C_1 C_1 = 1 1 1 indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit errors in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.



I Information bit
O Overhead bit
C Justification control bit
S Justification opportunity bit
R Fixed stuff bit(s)

FIGURE 5-17/G.709

Mapping of asynchronous 2048 kbit/s tributary

5.6.2 *Bit synchronous 2048 kbit/s*

The bit synchronous mapping for 2048 kbit/s tributaries is shown in Figure 5-18/G.709.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mappings.

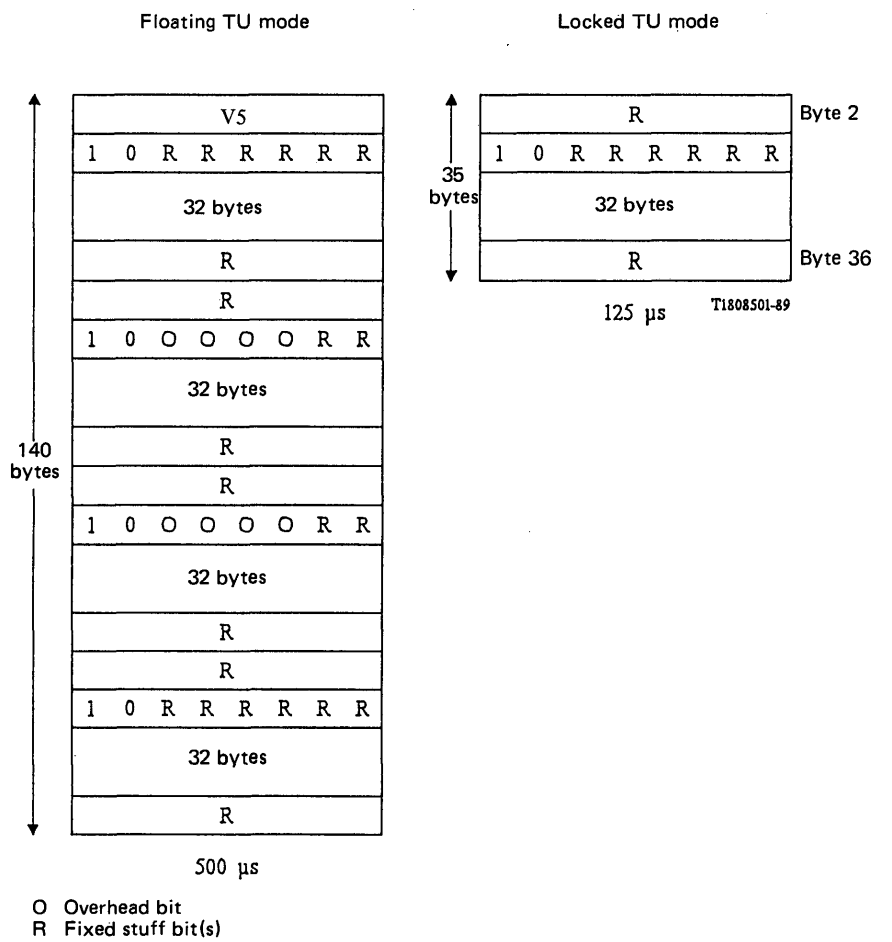


FIGURE 5-18/G.709

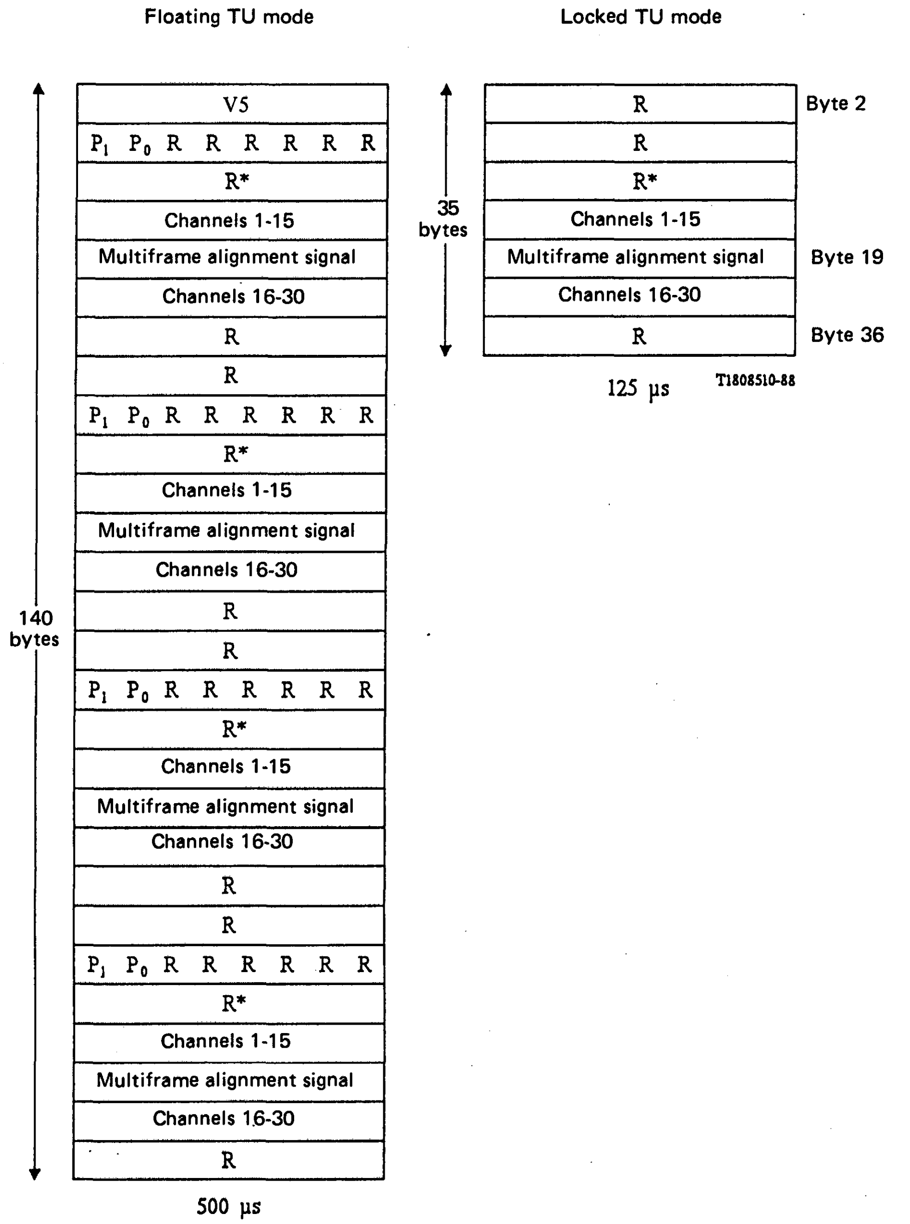
Bit synchronous mapping for 2048 kbit/s tributary

5.6.3 *Byte synchronous mapping for 2048 kbit/s*

Figure 5-19/G.709 shows byte synchronous mapping for 30-channel 2048 kbit/s tributaries employing Channel Associated Signalling (CAS). Signalling is carried in byte 19. The signalling assignments are shown in Figure 5-20/G.709.

The S_1, S_2, S_3 and S_4 bits contain the signalling for the 30 × 64 kbit/s channels. The phase of the signalling bits is indicated in the P_1 and P_0 bits in floating TU mode, and in the multiframe indicator byte (H4) in locked TU mode. This is illustrated in Figure 5-20/G.709.

Byte synchronous mapping of 31 channel tributaries is shown in Figure 5-21/G.709. Byte 19 carries tributary channel 16.



R Fixed stuff bit(s)
R* May be used for timeslot 0 if required
P_1P_0 00 at the start of the signalling frame on the first byte of the signalling frame

FIGURE 5-19/G.709

Byte synchronous mapping for 2048 kbit/s tributary (30 channel with channel associated signalling)

Locked														
				Floating										
H4 value				CAS format								Channel		
C_3	C_2	C_1	T	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4		P_1	P_0
0	0	0	0	0	0	0	0	x	y	x	x	None	0	0
0	0	0	1	a	b	c	d	a	b	c	d	1/16	0	0
0	0	1	0	a	b	c	d	a	b	c	d	2/17	0	0
1	1	1	1	a	b	c	d	a	b	c	d	15/30	1	1

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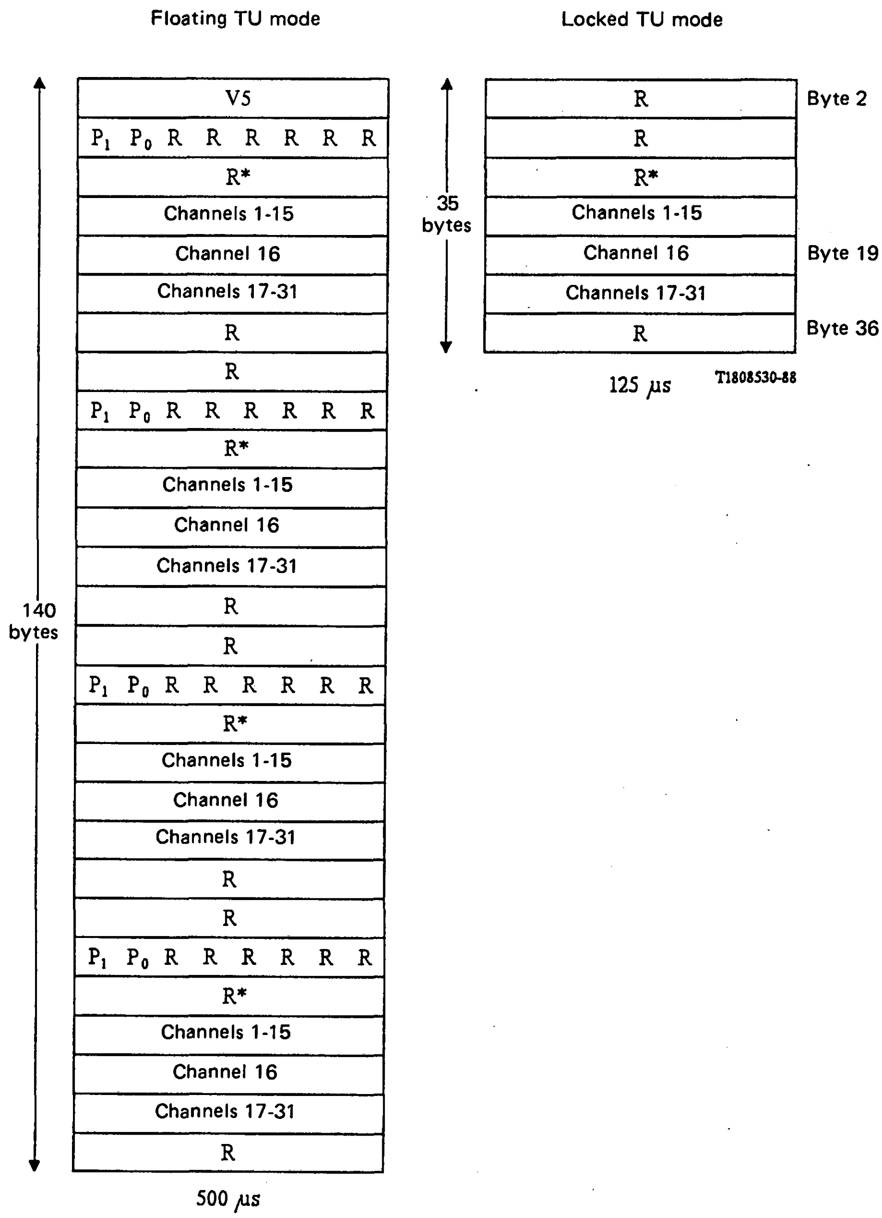
FIGURE 5-20/G.709

Out-slot signalling assignments (30-channel signalling operations)



R Fixed stuff bit(s)
R* May be used for timeslot 0 if required
P_1P_0 00 at the start of the signalling frame on the first byte of the signalling frame

FIGURE 5-21/G.709

Byte synchronous mapping for 2048 kbit/s tributary (31 channel with common channel signalling)

5.7 *Mapping of tributaries into VC-11*

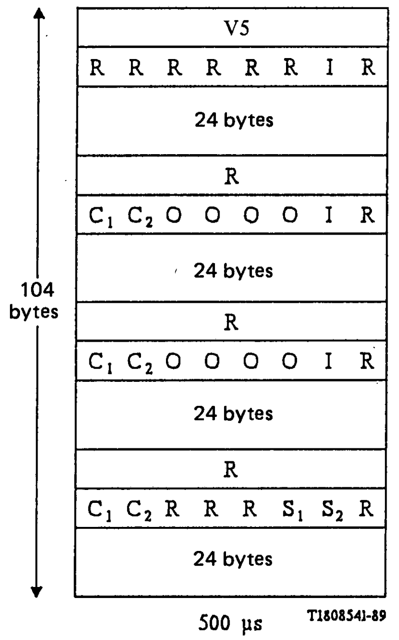
5.7.1 *Asynchronous 1544 kbit/s*

One 1544 kbit/s signal can be mapped into a VC-11. Figure 5-22/G.709 shows this over a period of 500 µs.

In addition to the VC-1 POH, the VC-11 consists of 771 data bits, six justification control bits, two justification opportunity bits and eight overhead communication channel bits. The remaining bits are fixed stuff (R) bits. The eight O bits are reserved for future communication purposes.

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunities, S_1 and S_2 respectively. C_1 C_1 C_1 = 0 0 0 indicates that S_1 is a data bit while C_1 C_1 C_1 = 1 1 1 indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit errors in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.



I Information bit
O Overhead bit
C Justification control bit
S Justification opportunity bit
R Fixed stuff bit(s)

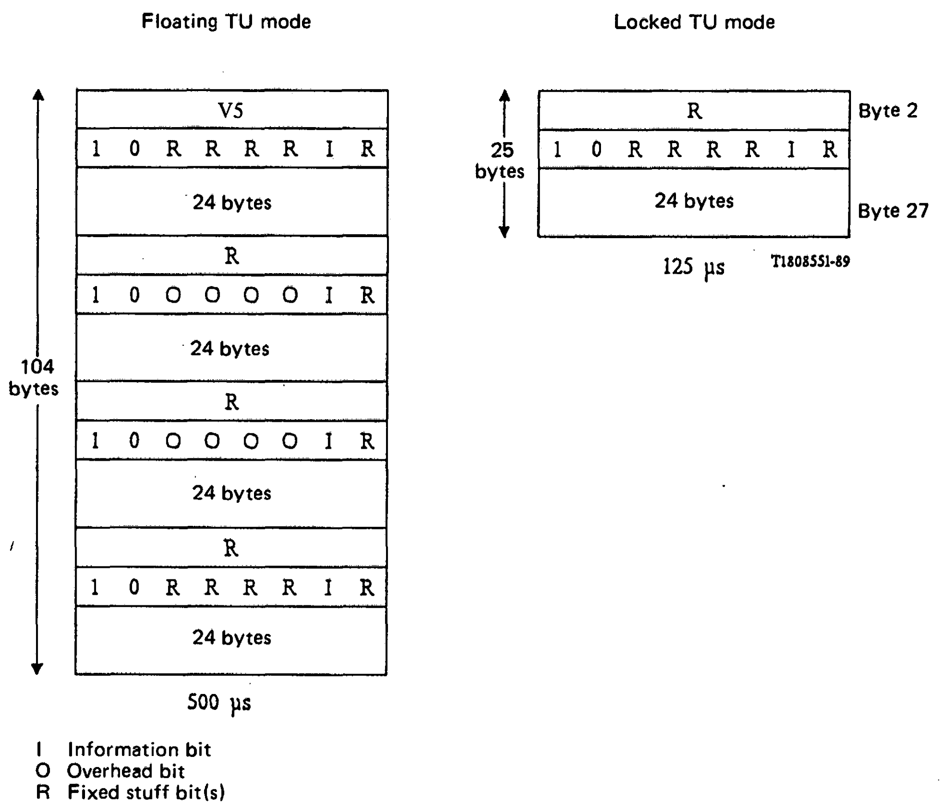
FIGURE 5-22/G.709

Mapping of asynchronous 1544 kbit/s tributary

5.7.2 *Bit synchronous 1544 kbit/s*

The bit synchronous mapping for 1544 kbit/s tributaries is shown in Figure 5-23/G.709.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mappings.



Note – O bits are currently not defined in the locked TU mode.

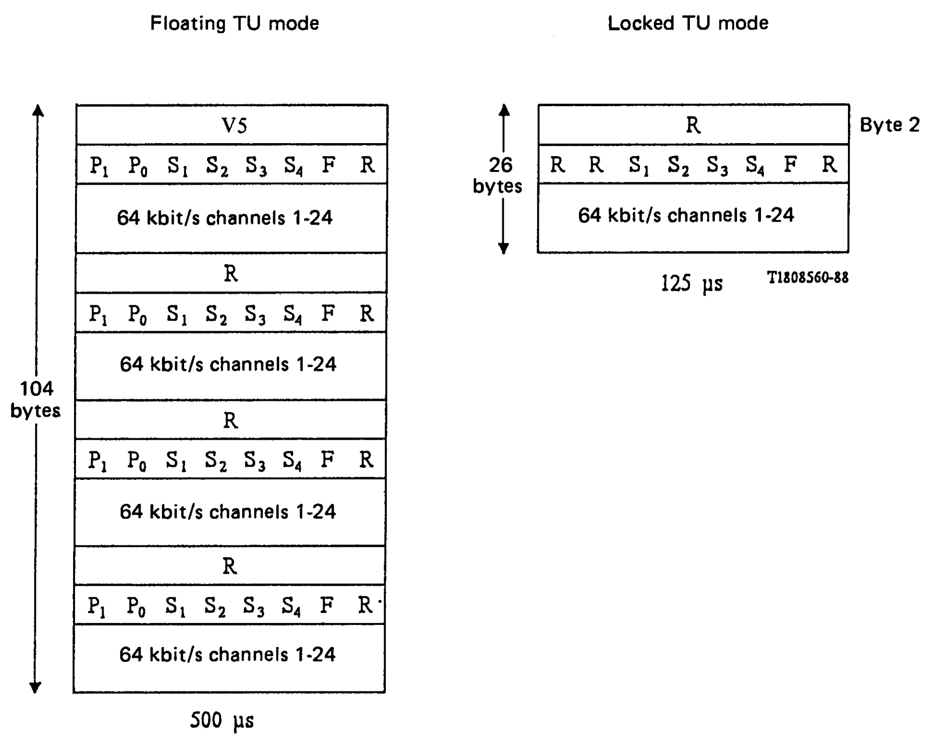
FIGURE 5-23/G.709

Bit synchronous mapping for 1544 kbit/s tributary

5.7.3 *Byte synchronous mapping for 1544 kbit/s*

The byte synchronous mapping for 1544 kbit/s is depicted in Figure 5-24/G.709.

The S_1, S_2, S_3 and S_4 bits contain the signalling for the 24 × 64 kbit/s channels. The phase of the signalling bits can be indicated in the P_1 and P_O bits in floating TU mode, and in the multiframe indicator byte (H4) in locked mode. This is illustrated in Figure 5-25/G.709. The usage of the PP bits has options, because the common signalling method and another channel associated signalling method (e.g. Recommendation G.704, §§ 3.1.3 and 3.2.3) do not need the PP bits. The operations of the alternative channel associated signalling method is shown in Figure 5-26/G.709.



F 1544 kbit/s tributary frame bit
P_1P_0 Signalling phase indicator
S Signalling bit
R Fixed stuff bit(s)
P_1P_0 00 on the first signalling byte of the multiframe

FIGURE 5-24/G.709

Byte synchronous mapping for 1544 kbit/s tributary

Locked																		
					Floating													
					Signalling													
H4 value					2 state				4 state				16 state					
P_1	P_0	S_2	S_1	T	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	P_1	P_0
0	0	0	0	0	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	0	0
0	0	0	0	1	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	0	0
0	0	0	1	0	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	0	0
0	0	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	0	0
0	0	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	0	0
0	0	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	0	0
0	1	0	0	0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	B_1	B_2	B_3	B_4	0	1
0	1	0	0	1	A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	0	1
0	1	0	1	0	A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	B_9	B_{10}	B_{11}	B_{12}	0	1
0	1	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	B_{13}	B_{14}	B_{15}	B_{16}	0	1
0	1	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	B_{17}	B_{18}	B_{19}	B_{20}	0	1
0	1	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	B_{21}	B_{22}	B_{23}	B_{24}	0	1
1	0	0	0	0	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	C_1	C_2	C_3	C_4	1	0
1	0	0	0	1	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	C_5	C_6	C_7	C_8	1	0
1	0	0	1	0	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	C_9	C_{10}	C_{11}	C_{12}	1	0
1	0	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	C_{13}	C_{14}	C_{15}	C_{16}	1	0
1	0	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	C_{17}	C_{18}	C_{19}	C_{20}	1	0
1	0	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	C_{21}	C_{22}	C_{23}	C_{24}	1	0
1	1	0	0	0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	D_1	D_2	D_3	D_4	1	1
1	1	0	0	1	A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	D_5	D_6	D_7	D_8	1	1
1	1	0	1	0	A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	D_9	D_{10}	D_{11}	D_{12}	1	1
1	1	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	D_{13}	D_{14}	D_{15}	D_{16}	1	1
1	1	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	D_{17}	D_{18}	D_{19}	D_{20}	1	1
1	1	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	D_{21}	D_{22}	D_{23}	D_{24}	1	1

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FIGURE 5-25/G.709

Out-slot signalling assignments (24-channel signalling operations)

Frame number	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
Use of S_i bit (i = 1, 2, 3, 4) (See Note 1)	Fs	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	X
	(See Note 2)	(See Note 3)						(See Note 5)

Note 1 – Each S_i (i = 1, 2, 3, 4) constitutes an independant signalling multiframe over eight frames. S_i includes the phase indicator in itself, so that the PP bits can not be used for the phase indicator.

Note 2 – The Fs bit is either alternate 0, 1 or the following 48 bit digital pattern:

A101011011 0000011001 1010100111 0011110110 10000101

For the 48-bit digital pattern, the A bit is usually fixed to state 1 and is reserved for optional use. The pattern is generated according to the following primitive polynomial (refer to Recommendation X.50):

$$x^7 + x^4 + 1$$

Note 3 – Y_j bit (j = 1 to 6) carries channel associated signalling or maintenance information. When the 48 bit pattern is adopted as Fs frame alignment signal, each Y_j bit (j = 1 to 6) can be multiframed, as follows:

$$Y_{j1}, Y_{j2}, \ldots, Y_{j12}.$$

Y_{j1} bit carries the following 16-bit frame alignment pattern generated according to the same primitive polynomial as for the 48-bit pattern:

A011101011011000

The A bit is usually fixed to 1 and is reserved for optional use. Each Y_{ji} (i = 2 to 12) bit carries channel associated signalling for sub-rate circuits and/or maintenance information.

Note 4 – S_i bits (Fs, $Y_1, \ldots, Y_6$ and X) all at state 1 indicate Alarm Indication Signal (AIS) for six 64 kbit/s channels.

Note 5 – The X bit is usually fixed to state 1. When backward AIS for six 64 kbit/s channels is required to be sent, the X bit is set to state 0.

FIGURE 5-26/G.709

Out-slot signalling assignments (24-channel signalling operations)

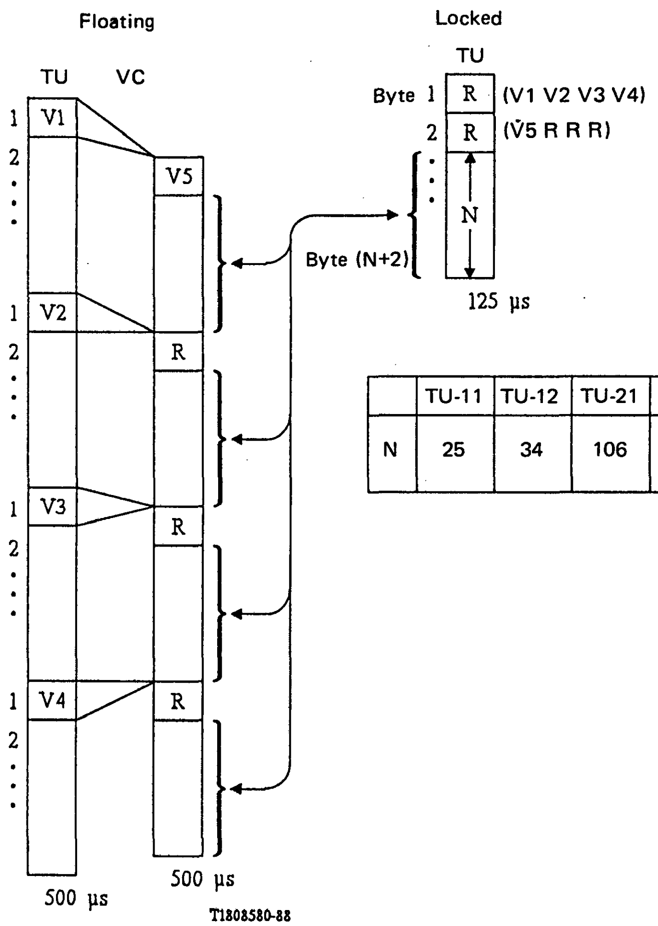
5.8 *Floating and locked mode conversion*

There are two possible multiplexing modes of the TU structures: floating and locked.

In the floating TU mode four consecutive 125 µs VC-n frames are organized into a 500 µs multiframe, the phase of which is indicated by the multiframe indicator byte (H4) in the VC-*n* POH. This 500 µs TU multiframe is shown in Figure 3-13/G.709.

Locked TU mode of transport is a fixed mapping of synchronous structured payloads into a VC-*n*. This provides a direct correspondence between subtending tributary information and the location of that information within the VC-*n*. Since the tributary information is fixed and immediately identifiable with respect to the TU-*n* or AU-*n* pointer associated with the VC-*n*, no TU pointers are available for payload usage.

Figure 5-27/G.709 illustrates the conversion between floating and locked TU modes for each of the four TU sizes. Note that certain bytes (R) in the current set of mapping are not used in the floating mode in order that those mappings can be used in both floating and locked modes. Since the V1-V4 and V5 bytes are reserved, the 500 µs TU multiframe is unnecessary. Therefore the role of the multiframe indicator byte (H4) in locked mode is to define 2 and 3 ms signalling frames for byte synchronous mappings.



	TU-11	TU-12	TU-21	TU-22
N	25	34	106	142

V1 PTR-1
V2 PTR-2
V3 PTR-3 (action)
V4 Reserved
V5 VC-1/VC-2 POH

FIGURE 5-27/G.709

Conversion between floating and locked TU modes

7.1 Coding of analogue signals by pulse code modulation

Recommendation G.711

PULSE CODE MODULATION (PCM) OF VOICE FREQUENCIES

(Geneva, 1972; further amended)

1 General

The characteristics given below are recommended for encoding voice-frequency signals.

2 Sampling rate

The nominal value recommended for the sampling rate is 8000 samples per second. The tolerance on that rate should be ± 50 parts per million (ppm).

3 Encoding law

3.1 Eight binary digits per sample should be used for international circuits.

3.2 Two encoding laws are recommended and these are commonly referred to as the A-law and the μ-law. The definition of these laws is given in Tables 1a/G.711 and 1b/G.711 and Tables 2a/G.711 and 2b/G.711 respectively.

When using the μ-law in networks where suppression of the all 0 character signal is required, the character signal corresponding to negative input values between decision values numbers 127 and 128 should be 00000010 and the value at the decoder output is −7519. The corresponding decoder output value number is 125.

3.3 The number of quantized values results from the encoding law.

3.4 Digital paths between countries which have adopted different encoding laws should carry signals encoded in accordance with the A-law. Where both countries have adopted the same law, that law should be used on digital paths between them. Any necessary conversion will be done by the countries using the μ-law.

3.5 The rules for conversion are given in Tables 3/G.711 and 4/G.711.

3.6 *Conversion to and from uniform PCM*

Every "decision value" and " quantized value" of the A (resp. μ) law should be associated with a "uniform PCM value". (For a definition of "decision value" and "quantized value", see Recommendation G.701 and in particular Figure 2/G.701). This requires the application of a 13 (14) bit uniform PCM code. The mapping from A-law PCM, and μ-law PCM, respectively, to the uniform code is given in Tables 1/G.711 and 2/G.711. The conversion to A-law or μ-law values from uniform PCM values corresponding to the decision values, is left to the individual equipment specification. One option is described in Recommendation G.721, § 4.2.8 subblock COMPRESS.

4 Transmission of character signals

When character signals are transmitted serially, i.e. consecutively on one physical medium, bit No. 1 (polarity bit) is transmitted first and No. 8 (the least significant bit) last.

5 Relationship between the encoding laws and the audio level

The relationship between the encoding laws of Tables 1/G.711 and 2/G.711 and the audio signal level is defined as follows:

A sine-wave signal of 1 kHz at a nominal level of 0 dBm0 should be present at any voice frequency output of the PCM multiplex when the periodic sequence of character signals of Table 5/G.711 for the A-law and of Table 6/G.711 for the μ-law is applied to the decoder input.

The resulting theoretical load capacity (T_{max}) is +3.14 dBm0 for the A-law, and +3.17 dBm0 for the μ-law.

Note – The use of another digital periodic sequence representing a nominal reference frequency of 1020 Hz at a nominal level of −10 dBm0 (preferred value, see Recommendation O.6) or 0 dBm0 is acceptable, provided that the theoretical accuracy of that sequence does not differ by more than ± 0.03 dB from a level of −10 dBm0 or 0 dBm0 respectively. In accordance with Recommendation O.6, the specified frequency tolerance should be 1020 Hz + 2 Hz, − 7 Hz.

If a sequence representing −10 dBm0 is used, the nominal value at the voice frequency outputs should be −10 dBm0.

TABLE 1a/G.711

A-law, positive input values

1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note 1)	Character signal before inversion of the even bits Bit number 1 2 3 4 5 6 7 8	Quantized value (value at decoder output) y_n	Decoder output value number
		4096	(128)	(4096)			
					1 1 1 1 1 1 1 1	4032	128
			127	3968			
7	16 × 128				(see Note 2)		
			113	2176			
					1 1 1 1 0 0 0 0	2112	113
		2048	112	2048			
6	16 × 64				(see Note 2)		
			97	1088			
					1 1 1 0 0 0 0 0	1056	97
		1024	96	1024			
5	16 × 32				(see Note 2)		
			81	544			
					1 1 0 1 0 0 0 0	528	81
		512	80	512			
4	16 × 16				(see Note 2)		
			65	272			
					1 1 0 0 0 0 0 0	264	65
		256	64	256			
3	16 × 8				(see Note 2)		
			49	136			
					1 0 1 1 0 0 0 0	132	49
		128	48	128			
2	16 × 4				(see Note 2)		
			33	68			
					1 0 1 0 0 0 0 0	66	33
		64	32	64			
1 ↓	32 × 2				(see Note 2)		
			1	2			
					1 0 0 0 0 0 0 0	1	1
			0	0			

Note 1 – 4096 normalized value units correspond to T_{max} = 3.14 dBm0.

Note 2 – The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to positive input values between two successive decision values numbered n and $n + 1$ (see column 4) is $(128 + n)$ expressed as a binary number

Note 3 – The value at the decoder output is $y_n = \frac{x_{n-1} + x_n}{2}$ for $n = 1, ..., 127, 128$.

Note 4 – x_{128} is a virtual decision value.

Note 5 – **In Tables 1/G.711 and 2/G.711 the values of the uniform code are given in columns 3, 5 and 7.**

TABLE 1b / G.711

A-law, negative input values

1	2	3	4	5	6	7	8
Segment Number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note 1)	Character signal before inversion of the even bits Bit number 1 2 3 4 5 6 7 8	**Quantized value (value at decoder output) y_n**	Decoder output value number
1	32 × 2		0	0			
					0 0 0 0 0 0 0 0	–1	1
			1	–2			
					(see Note 2)		
		–64	32	–64			
2	16 × 4				0 0 1 0 0 0 0 0	–66	33
			33	–68			
					(see Note 2)		
		–128	48	–128			
3	16 × 8				0 0 1 1 0 0 0 0	–132	49
			49	–136			
					(see Note 2)		
		–256	64	–256			
4	16 × 16				0 1 0 0 0 0 0 0	–264	65
			65	–272			
					(see Note 2)		
		–512	80	–512			
5	16 × 32				0 1 0 1 0 0 0 0	–528	81
			81	–544			
					(see Note 2)		
		–1024	96	–1024			
6	16 × 64				0 1 1 0 0 0 0 0	–1056	97
			97	–1088			
					(see Note 2)		
		–2048	112	–2048			
7	16 × 128				0 1 1 1 0 0 0 0	–2112	113
			113	–2176			
					(see Note 2)		
			127	–3968			
		–4096	(128)	(–4096)	0 1 1 1 1 1 1 1	–4032	128

Note 1 – 4096 normalized value units correspond to T_{max} = 3.14 dBm0.

Note 2 – The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to negative input values between two successive decision values numbered n and n + 1 (see column 4) is n expressed as a binary number.

Note 3 – The value at the decoder output is $y_n = \frac{x_{n-1} + x_n}{2}$ for n = 1, ..., 127, 128.

Note 4 – x_{128} is a virtual decision value.

Note 5 – **In Tables 1/G.711 and 2/G.711 the values of the uniform code are given in columns 3, 5 and 7.**

TABLEAU 2a / G.711

μ-law, positive input values

1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note 1)	Character signal Bit number 1 2 3 4 5 6 7 8	Quantized value (value at decoder output) y_n	Decoder output value number
		8159	(128)	(8159)			
8	16 × 256				1 0 0 0 0 0 0 0	8031	127
			127	7903	(see Note 2)		
			113	4319			
					1 0 0 0 1 1 1 1	4191	112
7	16 × 128	4063	112	4063	(see Note 2)		
			97	2143			
					1 0 0 1 1 1 1 1	2079	96
6	16 × 64	2015	96	2015	(see Note 2)		
			81	1055			
					1 0 1 0 1 1 1 1	1023	80
5	16 × 32	991	80	991	(see Note 2)		
			65	511			
					1 0 1 1 1 1 1 1	495	64
4	16 × 16	479	64	479	(see Note 2)		
			49	239			
					1 1 0 0 1 1 1 1	231	48
3	16 × 8	223	48	223	(see Note 2)		
			33	103			
					1 1 0 1 1 1 1 1	99	32
2	16 × 4	95	32	95	(see Note 2)		
			17	35			
					1 1 1 0 1 1 1 1	33	16
1 ↓	15 × 2	31	16	31	(see Note 2)		
			2	3			
					1 1 1 1 1 1 1 0	2	1
			1	1			
	1 × 1				1 1 1 1 1 1 1 1	0	0
			0	0			

Note 1 – 8159 normalized value units correspond to $T_{max} = 3.17$ dBm0.

Note 2 – The character signal corresponding to positive input values between two successive decision values numbered n and $n + 1$ (see column 4) is $(255 - n)$ expressed as a binary number.

Note 3 – The value at the decoder output is $y_0 = x_0 = 0$ for $n = 0$, and $y_n = \frac{x_n + x_{n+1}}{2}$ for $n = 1, 2, \ldots, 127$.

Note 4 – x_{128} is a virtual decision value.

Note 5 **– In Tables 1/G.711 and 2/G.711 the values of the uniform code are given in columns 3, 5 and 7.**

TABLE 2b / G.711

μ-law, negative input values

1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note 1)	Character signal Bit number 1 2 3 4 5 6 7 8	Quantized value (value at decoder output) y_n	Decoder output value number
1	1 × 1		0	0			
					0 1 1 1 1 1 1 1	0	0
			1	−1			
	15 × 2				0 1 1 1 1 1 1 0	−2	1
			2	−3			
					(see Note 2)		
		−31	16	−31			
					0 1 1 0 1 1 1 1	−33	16
2	16 × 4		17	−35			
					(see Note 2)		
		−95	32	−95			
					0 1 0 1 1 1 1 1	−99	32
3	16 × 8		33	−103			
					(see Note 2)		
		−223	48	−223			
					0 1 0 0 1 1 1 1	−231	48
4	16 × 16		49	−239			
					(see Note 2)		
		−479	64	−479			
					0 0 1 1 1 1 1 1	−495	64
5	16 × 32		65	−511			
					(see Note 2)		
		−991	80	−991			
					0 0 1 0 1 1 1 1	−1023	80
6	16 × 64		81	−1055			
					(see Note 2)		
		−2015	96	−2015			
					0 0 0 1 1 1 1 1	−2079	96
7	16 × 128		97	−2143			
					(see Note 2)		
		−4063	112	−4063			
					0 0 0 0 1 1 1 1	−4191	112
8	16 × 256		113	−4319			
					(see Note 2)		
			126	−7647			
					0 0 0 0 0 0 0 1	−7775	126
			127	−7903			
					0 0 0 0 0 0 0 0	−8031	127
		−8159	(128)	(−8159)			

Note 1 – 8159 normalized value units correspond to T_{max} = 3.17 dBm0.

Note 2 – The character signal corresponding to negative input values between two successive decision values numbered n and $n + 1$ (see column 4) is $(127 - n)$ expressed as a binary number for $n = 0, 1, ..., 127$.

Note 3 – The value at the decoder output is $y_0 = x_0 = 0$ for $n = 0$, and $y_n = \frac{x_n + x_{n+1}}{2}$ for $n = 1, 2, ..., 127$.

Note 4 – x_{128} is a virtual decision value.

Note 5 – **In Tables 1/G.711 and 2/G.711 the values of the uniform code are given in columns 3, 5 and 7.**

TABLE 3/G.711

μ-A conversion

μ-law Decoder output value number	*A-law* Decoder output value number	*μ-law* Decoder output value number	*A-law* Decoder output value number
0	1	44	41
1	1	45	42
2	2	46	43
3	2	47	44
4	3	48	46
5	3	49	48
6	4	50	49
7	4	51	50
8	5	52	51
9	5	53	52
10	6	54	53
11	6	55	54
12	7	56	55
13	7	57	56
14	8	58	57
15	8	59	58
16	9	60	59
17	10	61	60
18	11	62	61
19	12	63	62
20	13	64	64
21	14	65	65
22	15	66	66
23	16	67	67
24	17	68	68
25	18	69	69
26	19	70	70
27	20	71	71
28	21	72	72
29	22	73	73
30	23	74	74
31	24	75	75
32	25	76	76
33	27	77	77
34	29	78	78
35	31	79	79
36	33	80	81
37	34	81	82
38	35	82	83
39	36	83	84
40	37	84	85
41	38	85	86
42	39	86	87
43	40	87	88
		.	.
		.	.
		.	.
		127	128

Notes relative to Table 3/G.711

Note 1 – The input signals to an A-law decoder will normally include even bit inversion as applied in accordance with Note 2 of Table 1a/G.711. Consequently the output signals from a μ-A converter should have even bit inversion embodied within the converter output.

Note 2 – If a μ-A conversion is followed by an A-μ conversion, most of the octets are restored to their original values. Only those octets which correspond to μ-law decoder output value numbers 0, 2, 4, 6, 8, 10, 12, 14 are changed (the numbers being increased by 1). Moreover, in these octets, only bit No. 8 (least significant bit in PCM) is changed. Accordingly, the double conversion μ-A-μ is transparent to bits Nos. 1-7.

Similarly, if an A-μ conversion is followed by a μ-A conversion, only the octets corresponding to A-law decoder output value numbers 26, 28, 30, 32, 45, 47, 63 and 80 are changed. Again, only bit No. 8 is changed, i.e. the double conversion A-μ-A, too, is transparent to bits No. 1-7.

A consequence of this property is that in most of the analogue voice frequency signal range the additional quantizing distortion caused by μ-A-μ or A-μ-A conversion is considerably lower than that caused by either μ-A or A-μ conversion (see Recommendation G.113).

The A-μ-A transparency for bits 1 to 7 was achieved by modifying the table slightly from the optimum conversion in that μ-80 is converted to A-81 instead of A-80, and A-80 is converted to μ-79 instead of μ-80. This has an insignificant effect on quantizing distortion.

TABLE 4/G.711

μ-A conversion

A-law Decoder output value number	*μ-law* Decoder output value number	*A-law* Decoder output value number	*μ-law* Decoder output value number
1	1	51	52
2	3	52	53
3	5	53	54
4	7	54	55
5	9	55	56
6	11	56	57
7	13	57	58
8	15	58	59
9	16	59	60
10	17	60	61
11	18	61	62
12	19	62	63
13	20	63	64
14	21	64	64
15	22	65	65
16	23	66	66
17	24	67	67
18	25	68	68
19	26	69	69
20	27	70	70
21	28	71	71
22	29	72	72
23	30	73	73
24	31	74	74
25	32	75	75
26	32	76	76
27	33	77	77
28	33	78	78
29	34	79	79
30	34	80	79
31	35	81	80
32	35	82	81
33	36	83	82
34	37	84	83
35	38	85	84
36	39	86	85
37	40	87	86
38	41	88	87
39	42	89	88
40	43	90	89
41	44	91	90
42	45	92	91
43	46	93	92
44	47	94	93
45	48	95	94
46	48	96	95
47	49	97	96
48	49	98	97
49	50	.	.
50	51	.	.
		.	.
		128	127

Notes relative to Table 4/G.711

Note 1 – The output signals of an A-law decoder will have even bit inversion as applied within the encoder in accordance with Note 2 of Table 1a/G.711. Consequently the input signals to an A-μ converter will already be in this state, so that removal of even bit inversion should be embodied within the converter.

Note 2 – If a μ-A conversion is followed by an A-μ conversion, most of the octets are restored to their original values. Only those octets which correspond to μ-law decoder output value numbers 0, 2, 4, 6, 8, 10, 12, 14 are changed (the numbers being increased by 1). Moreover, in these octets, only bit 8 (least significant bit in PCM) is changed. Accordingly, the double conversion μ-A-μ is transparent to bits 1 to 7.

Similarly, if an A-μ conversion is followed by a μ-A conversion, only the octets corresponding to A-law decoder output value numbers 26, 28, 30, 32, 45, 47, 63 and 80 are changed. Again, only bit 8 is changed, i.e. the double conversion A-μ-A, too, is transparent to bits 1 to 7.

A consequence of this property is that in most of the analogue voice frequency signal range the additional quantizing distortion caused by μ-A-μ or A-μ-A conversion is considerably lower than that caused by either μ-A or A-μ conversion (see Recommendation G.113).

The A-μ-A transparency for bits 1 to 7 was achieved by modifying the table slightly from the optimum conversion in that μ-80 is converted to A-81 instead of A-80, and A-80 is converted to μ-79 instead of μ-80. This has an insignificant effect on quantizing distortion.

TABLE 5/G.711

A-law							
1	*2*	*3*	*4*	*5*	*6*	*7*	*8*
0	0	1	1	0	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	0

TABLE 6/G.711

μ-law							
1	*2*	*3*	*4*	*5*	*6*	*7*	*8*
0	0	0	1	1	1	1	0
0	0	0	0	1	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	1	1	1	0

PERFORMANCE CHARACTERISTICS OF PCM CHANNELS BETWEEN 4-WIRE INTERFACES AT VOICE FREQUENCIES

(Geneva, 1972, further amended)

The CCITT

recommends

that the performance characteristics which follow should be met between the voice-frequency ports of PCM channels coded in accordance with Recommendation G.711.

The performance limits quoted are to be considered as Recommendations to be met in all cases.

Except where indicated otherwise, the values and limits specified are those which should be obtained in 4-wire measurements using two PCM multiplex terminal equipments connected back-to-back and with the input and output ports of the channels terminated with their nominal impedance (except where specified in § 3.3 below).

To avoid level errors produced as a result of the use of test frequencies which are sub-multiples of the PCM sampling rate, the use of integer sub-multiples 8 kHz should also be avoided.

Where a nominal reference frequency of 1020 Hz is indicated, the actual frequency should be 1020 Hz + 2 Hz − 7 Hz in accordance with Recommendation O.6.

For an interim period Administrations may, for practical reasons, need to use a reference frequency of nominally 800 Hz, but slightly offset from this value to avoid sub-multiples of sampling frequency.

1 Attenuation/frequency distortion

The variations with frequency of the attenuation of any channel should lie within the limits shown in the mask of Figure 1/G.712.

The nominal reference frequency is 1020 Hz.

The preferred input power level is −10 dBm0. As an alternative, a level of 0 dBm0 may be used.

The distortion contributed by the separate encoding and decoding sides of the equipment should be nominally equal.

2 Group delay

2.1 *Absolute group delay*

The absolute group delay at the frequency of minimum group delay should not exceed 600 microseconds.

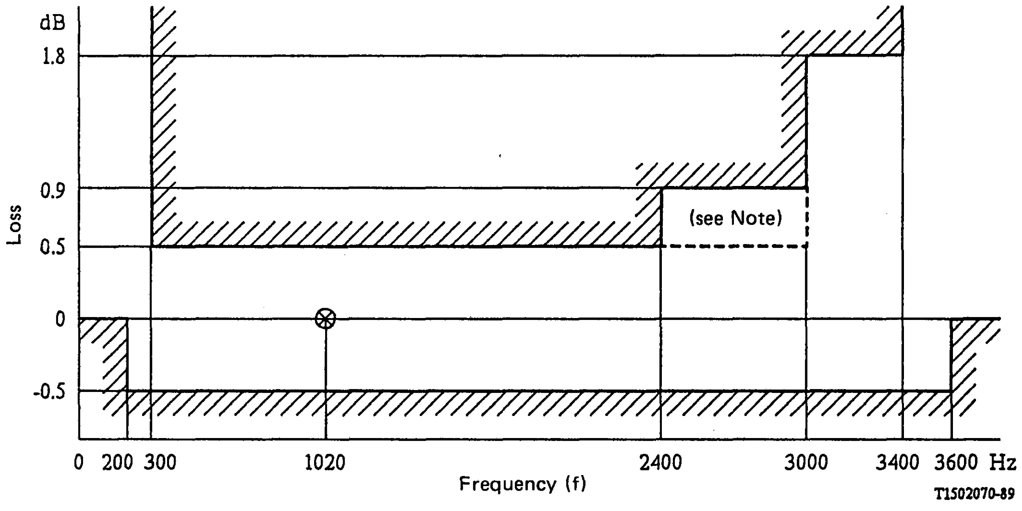
The minimum value of group delay is taken as the reference for the group delay distortion.

2.2 *Group delay distortion with frequency*

The group delay distortion should lie within the limits shown in the template of Figure 2/G.712.

2.3 *Input level*

The requirements of §§ 2.1 and 2.2 above should be met at an input power level of −10 dBm0 (preferred value). As an alternative, a level of 0 dBm0 may be used.



Note — In some applications in which several PCM channels may be connected in tandem, it may be necessary to extend the +0.5 dB limit from 2400 Hz to 3000 Hz.

FIGURE 1/G.712

Attenuation/frequency distortion

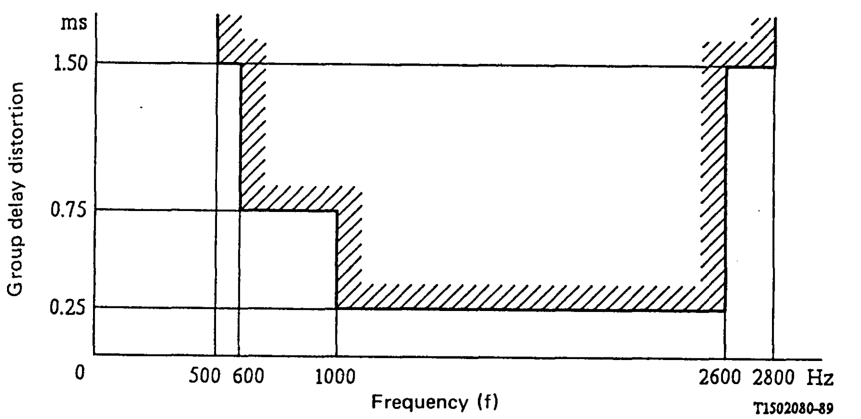


FIGURE 2/G.712

Group delay distortion with frequency

3 Impedance of voice frequency ports

3.1 *Nominal impedance*

The nominal impedance at the 4-wire voice-frequency input and output ports should be 600 ohms, balanced.

3.2 *Return loss*

The return loss, measured against the nominal impedance, should not be less than 20 dB over the frequency range 300 to 3400 Hz.

Note – The return loss limit should be met when the adjusting pads are set to 0 dB [1].

3.3 *Longitudinal balance*

The measurement arrangements for longitudinal balance parameters referred to below are defined in Recommendation O.9 which also gives some information about the requirements of test circuits (Note 1). The value of Z in the driving test circuit should be 600 ohm ± 20% and the termination at the other port should be the nominal characteristic impedance.

a) The longitudinal conversion loss (see Recommendation O.9, § 2.1) as measured at the input port should not be less than the limits shown in Figure 3/G.712.

b) The longitudinal conversion loss (see Recommendation O.9, § 2.1) as measured at the output port should not be less than the limits shown in Figure 3/G.712.

c) The difference between the longitudinal conversion transfer loss (see Recommendation O.9, § 2.3) at the specified frequencies and the insertion loss at the same frequencies should not be less than the limits shown in Figure 3/G.712. The requirement is only applicable to the configuration where the driving test circuit is applied to the input port and a measurement made at the output port. The measurement should be made with the switch *S*, shown in Figure 3/O.9, closed.

Note 1 – Attention is drawn to Recommendation O.9, § 3, which shows the equivalence between a number of different test driving circuits and also includes information concerning the inherent balance requirements of the test bridge.

Note 2 – Attention is drawn to the fact that these values represent minimum requirements. The magnitude of potential longitudinal signal voltages depends, for example, on system use, the system environment, the location of hybrid transformers and attenuators, and may therefore vary for different Administrations. Some Administrations have found it necessary to specify higher values for longitudinal conversion loss and longitudinal conversion transfer loss to ensure that transverse voltages caused by possible longitudinal signal voltages are sufficiently small.

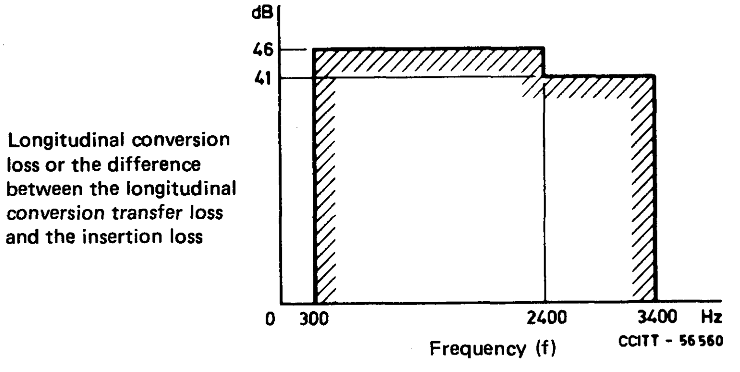


FIGURE 3/G.712

Longitudinal balance

4 Idle channel noise

4.1 *Weighted noise*

With the input and output ports of the channel terminated in the nominal impedance, the idle channel noise should not exceed −65 dBm0p.

4.2 *Single frequency noise*

The level of any single frequency (in particular the sampling frequency and its multiples), measured selectively, should not exceed −50 dBm0.

4.3 *Receiving equipment noise*

Noise contributed by the receiving equipment alone should be less than −75 dBm0p when its input is driven by a PCM signal corresponding to the decoder output value number 0 for the μ-law or decoder output value number 1 for the A-law.

5 Discrimination against out-of-band input signals

5.1 With any sine-wave signal in the range from 4.6 kHz to X kHz applied to the input port of the channel at a suitable level, the level of any image frequency produced at the output port of the channel should, as a minimum requirement, be at least 25 dB below the level of the test signal.

Note – It has been found that a suitable test level is −25 dBm0. The value of X is under study, but it should be at least 150 kHz.

5.2 Under the most adverse conditions encountered in a national network, the PCM channel should not contribute more than 100 pW0p of additional noise in the band 10 Hz-4 kHz at the channel output, as a result of the presence of out-of-band signals at the channel input.

Note 1 – The discrimination required depends on the performance of FDM channel equipments and telephone instruments in national networks and individual Administrations should carefully consider the requirements they should specify, taking into account the comments above and the requirement of § 5.2 above. In all cases at least the minimum requirement of § 5.1 above should be met.

Note 2 – Attention is drawn to the importance of the attenuation characteristic in the range 3400 to 4600 Hz. Although other attenuation characteristics can satisfy the requirements §§ 5.1 and 5.2 above, the filter template of Figure 4/G.712 gives adequate protection against the out-of-band signals.

6 Spurious out-of-band signals at the channel output

6.1 With any sine-wave signal in the range 300-3400 Hz at a level of 0 dBm0 applied to the input port of a channel, the level of spurious out-of-band image signals measured selectively at the output port should be lower than −25 dBm0.

6.2 The spurious out-of-band signals should not give rise to unacceptable interference in equipment connected to the PCM channel. In particular, the intelligible or unintelligible crosstalk in a connected FDM channel should not exceed a level of −65 dBm0 as a consequence of the spurious out-of-band signals at the PCM channel output.

Note 1 – The discrimination required depends on the performance of FDM channel equipment and telephone instruments in national networks and individual Administrations should carefully consider the requirements they should specify, taking into account the comments above and the requirement of § 6.2 above. In all cases at least the minimum requirement of § 6.1 above should be met.

Note 2 – Attention is drawn to the importance of the attenuation characteristic in the range 3400 to 4600 Hz. Although other attenuation characteristics can satisfy the requirements §§ 6.1 and 6.2 above, the filter template of Figure 4/G.712 gives adequate protection against the out-of-band signals.

7 Intermodulation

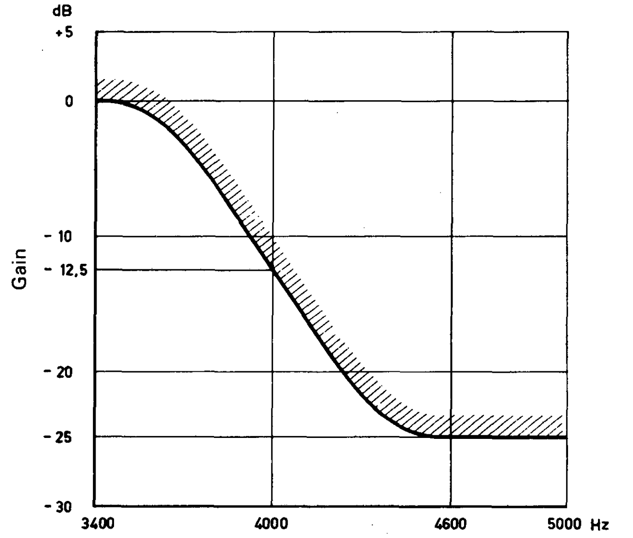
7.1 Two sine-wave signals of different frequencies f_1 and f_2 not harmonically related, in the range 300-3400 Hz and of equal levels in the range -4 to -21 dBm0, applied simultaneously to the input port of a channel should not produce any $2f_1 - f_2$ intermodulation product having a level greater than -35 dB relative to the level of one of the two input signals.

7.2 A signal having a level of -9 dBm0 at any frequency in the range 300-3400 Hz and a signal of 50 Hz at a level of -23 dBm0 applied simultaneously to the input port should not produce any intermodulation product of a level exceeding -49 dBm0.

Note – These requirements are in practice always met if the requirements according to §§ 8 and 10 are met.

8 Total distortion, including quantizing distortion

Two alternative methods are recommended. It should be noted that the two test methods are not exactly equivalent. The noise test method (Method 1) gives fairly smooth curves, not very dependent upon input signal level. The sine-wave method (Method 2) can be more sensitive in identifying possible localized codec imperfections. Thus the two methods respond to practical codec impairments in slightly different ways.



Note – The curved portion of the graph conforms to the equation $G = 12.5 \left[\sin \frac{\pi(4000 - f)}{1200} - 1\right]$ dB for the range $3400 \leqslant f \leqslant 4600$.

FIGURE 4/G.712

Gain relative to gain at 1000 Hz

Note – Some Administrations have taken the position that the requirements of both test methods should be met. Other Administrations are of the opinion that meeting the requirements of either test method is sufficient to meet network performance requirements. In practice Administrations may choose to use only one method in production testing and operational situations.

Method 1

With a noise signal corresponding to Recommendation O.131 [2] applied to the input port of a channel, the ratio of signal-to-total distortion power should lie above the limits shown in Figure 5/G.712.

Note – The derivation of the limits, based on a signal having a Gaussian distribution of its instantaneous values, is given in Annex A.

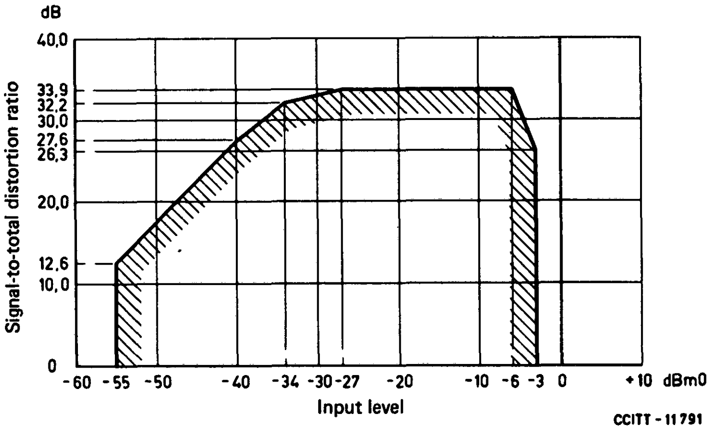


FIGURE 5/G.712

Signal-to-total distortion ratio as a function of input level (Method 1)

Method 2

With a sine-wave signal at a nominal frequency of 1020 Hz (preferred value) or 820 Hz (see Recommendation O.132 [6]) applied to the input port of a channel, the ratio of signal-to-total distortion power measured with the proper noise weighting (see the Recommendation cited in [3]), should lie above the limits shown in Figure 6/G.712.

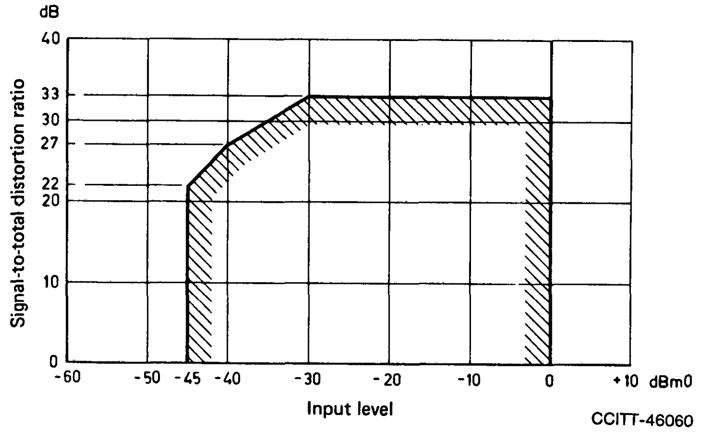


FIGURE 6/G.712

Signal-to-total distortion ratio as a function of input level (Method 2)

9 Spurious in-band signals at the channel output port

With a sine-wave signal in the frequency range 700-1100 Hz and at a level of 0 dBm0 applied to the input port of a channel, the output level at any frequency other than the frequency of the applied signal, measured selectively in the frequency band 300-3400 Hz, should be less than −40 dBm0.

10 Variation of gain with input level

Two alternative methods are recommended. (See comments in § 8.)

Method 1

With a band limited noise signal, as defined in Recommendation O.131, applied to the input of any channel at a level between −55 dBm0 and −10 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits of the mask of Figure 7a/G.712. The measurement should be limited to the frequency band 350-550 Hz in accordance with the filter characteristic defined in Recommendation O.131, § 3.2.1.

Furthermore, with a sine-wave signal in the frequency range 700-1100 Hz applied to the input port of any channel at a level between −10 dBm0 and +3 dBm0, the gain variation of that channel relative to the gain at an input level of −10 dBm0 should lie within the limits of the mask of Figure 7b/G.712. The measurement should be made selectively.

Method 2

With a sine-wave signal in the frequency range 700-1100 Hz applied to the input port of any channel at a level between −55 dBm0 and +3 dBm0, the gain variation of that channel relative to the gain at an input level of −10 dBm0, should lie within the limits of the mask of Figure 7c/G.712. The measurement should be made selectively.

11 Interchannel crosstalk

11.1 The crosstalk between individual channels of a multiplex should be such that with a sine-wave signal in the frequency range 700-1100 Hz and at a level of 0 dBm0 applied to an input port, the crosstalk level received in any other channel should not exceed −65 dBm0.

Note – In order to overcome fundamental gain enhancement effects, associated with PCM encoders, which can mask the true crosstalk, an activating signal may be injected into the disturbed channel when implementing crosstalk measurements with sine-wave signals. Suitable activating signals are band limited noise (see Recommendation O.131) at a level in the range −50 to −60 dBm0 or a sine-wave at a level in the range −33 to −40 dBm0. Care must be taken in the choice of frequency and the filtering characteristics of the measuring apparatus in order that the activating signal does not significantly affect the accuracy of the crosstalk measurement.

11.2 When a white noise signal shaped in accordance with Recommendation G.227 [4] at a level of 0 dBm0 is applied to the input port of up to four channels, the level of the crosstalk received in any other channel should not exceed −60 dBm0p. Uncorrelated noise should be used when more than one input channel is energized.

12 Go-to-return crosstalk

The crosstalk between a channel and its associated return channel should be such that with a sine-wave signal at any frequency in the range 300-3400 Hz and at a level of 0 dBm0 applied to an input port, the crosstalk level measured at the output of the corresponding return channel should not exceed −60 dBm0.

13 Interference from signalling

The maximum level of any interference into a channel should not exceed −60 dBm0p when signalling (10 Hz signal with a 50/50 duty ratio) is active simultaneously on all channels.

14 Relative levels at voice-frequency ports

The specifications should conform to the Recommendation cited in [5].

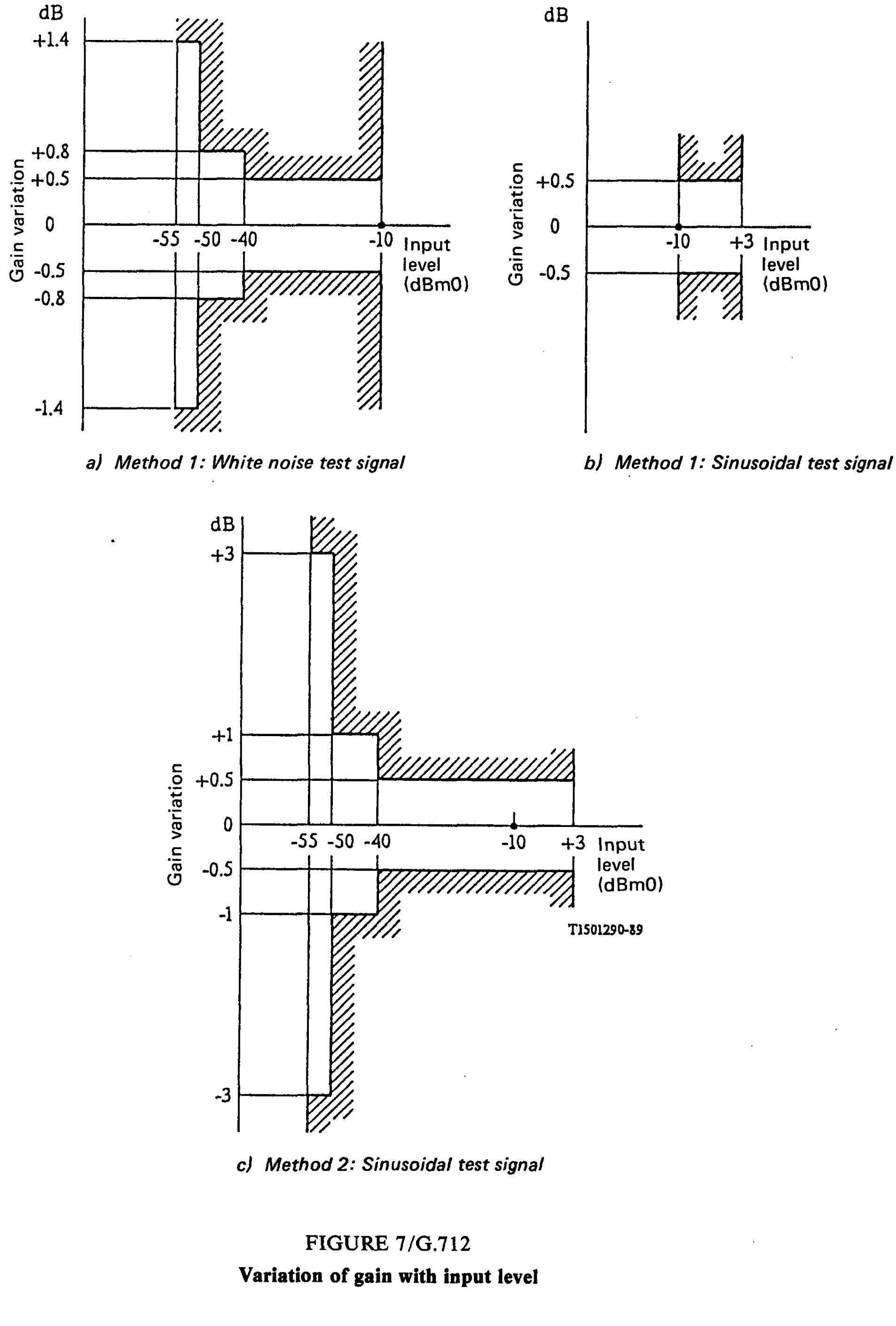


FIGURE 7/G.712

Variation of gain with input level

15 Adjustment of relative levels

Adjustment (especially initial adjustment) of the relative levels, and hence of the gain of the separate encoding and decoding sides of PCM channels, should be made at typical values of environmental conditions. The adjustments should lead to a deviation of the actual values against the nominal values not exceeding ± 0.3 dB, and should be made as follows:

15.1 The decoding side should be adjusted to conform with § 4 of Recommendation G.711 within a tolerance of ± 0.3 dB in practice.

15.2 The encoding side should be adjusted by connecting its output to a standard digital analyzer which has been adjusted to have precisely nominal gain, and applying a sine-wave signal at a nominal frequency of 1020 Hz at a level of 0 dBm0 to the voice-frequency input of the encoding side. The encoding side should then be adjusted so that the resulting sine-wave signal at the voice-frequency output of the decoding side is at a level of 0 dBm0. In practice the adjustment should be made with a tolerance of ± 0.3 dB.

Alternatively, a decoding side with a known error, within the limits defined in § 15.1, may be used provided that account is taken of this known error in adjusting the encoding side.

15.3 The load capacity of the encoding side may be checked by applying a sine-wave signal at a nominal frequency of 1020 Hz at its voice-frequency input. The level of this signal should be initially well below T_{max} and should then be slowly increased. The input level should be measured at which the first occurrence is observed of the character signal corresponding to the extreme quantizing interval for both positive and negative values. T_{max} is taken as being 0.3 dB greater than the measured input level.

This method allows T_{max} to be checked for both positive and negative amplitudes and the values thus obtained should be within ± 0.3 dB of the theoretical load capacity (i.e. +3.14 dBm0 for the A-law or +3.17 dBm0 for the μ-law). As an alternative, the occurrence of the largest pulse amplitude at the decoder output may be used as a means of identifying T_{max}.

16 Short-term and long-term variation of loss with time

When a sine-wave signal at a nominal frequency of 1020 Hz and at a level of −10 dBm0 (preferred value; 0 dBm0 may be used) is applied to any voice-frequency input, the level measured at the corresponding voice-frequency output should not vary by more than ± 0.2 dB during any 10-minute interval of typical operation, nor by more than ± 0.5 dB during any one year under the permitted variations in the power supply voltage and temperature.

ANNEX A

(to Recommendation G.712)

Method of derivation of the signal-to-total distortion ratio for the A-law

The signal-to-quantizing distortion ratio produced by PCM systems can be obtained analytically in a number of different ways. The method adopted here is a special case of a more general analysis which enables the calculated results to be compared directly with those obtained by practical measurements of the systems.

The compression characteristic of the system is assumed to be "ideal" – i.e. to meet precisely the theoretical segmented law, with the system a.c. zero coincident with the centre decision amplitude. The input signal is assumed to be symmetrical about a.c. zero, and to have a Gaussian distribution of instantaneous amplitudes. For a given input, of variance σ_v^2, the total output variance may be determined as σ_u^2, and the variance of the signal content in the output, by linear regression, as $m^2 \sigma_v^2$ where m is the slope of the regression line of output on input.

The variance of the distortion components is then $\sigma_\varepsilon^2 = \sigma_u^2 - m^2 \sigma_v^2$, and the signal-to-quantizing distortion ratio in dB is:

$$10 \log_{10} \frac{m^2 \sigma_v^2}{\sigma_\varepsilon^2}$$

The limits of Figure 5/G.712, which refer to *total* distortion, have been derived from the theoretical values of signal-to-*quantizing* distortion for A-law coding by subtracting 4.5 dB. In this way, practical imperfections of codecs as well as a certain amount of noise are taken into account. (Actually, the subtraction of 4.5 dB was applied to the break-points of the tolerance scheme in Figure 5/G.712.)

References

[1] CCITT Recommendation *12-channel terminal equipments*, Vol. III, Rec. G.232, Figure 5/G.232.

[2] CCITT Recommendation *Specification for a quantizing distortion measuring apparatus using a pseudo-random noise stimulus*, Vol. IV, Rec. O.131.

[3] CCITT Recommendation *Assumptions for the calculation of noise on hypothetical reference circuits for telephony*, Vol. III, Rec. G.223, Table 4/G.223.

[4] CCITT Recommendation *Conventional telephone signal*, Vol. III, Rec. G.227.

[5] CCITT Recommendation *12-channel terminal equipments*, Vol. III, Rec. G.232, § 11.

[6] CCITT Recommendation *Specification for a quantizing distortion measuring equipment using sinusoidal test signal*, Vol. IV, Rec. O.132.

Recommendation G.713

PERFORMANCE CHARACTERISTICS OF PCM CHANNELS BETWEEN 2-WIRE INTERFACES AT VOICE FREQUENCIES

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

The CCITT,

considering

that Recommendation G.712 defines the performance of back-to-back PCM terminals between analogue 4-wire interfaces;

that in some operational situations PCM channels will be utilized on a 2-wire basis in association with 2-wire/4-wire terminating units;

that, depending on equipment realization, sometimes the 2-wire/4-wire terminating units, including signalling functions, will form an integral part of the PCM multiplex terminal and in other realizations they will be located remotely;

that there is a variety of signalling schemes employed nationally by different Administrations and these signalling systems have a varying degree of impact on the transmission performance characteristics;

that, in some cases, PCM multiplex terminals are also used to terminate analogue circuits onto digital exchanges,

recommends

that the performance characteristics which follow should be met between voice-frequency ports of PCM channels coded in accordance with Recommendation G.711.

The parameters and values specified in this Recommendation apply to the use of PCM equipment connected to analogue trunks or to analogue exchanges.

When PCM equipment is connected directly to analogue subscriber lines, different values for some of the parameters may be required. Recommendation Q.552 contains those values. They may also be applied if the PCM equipment is directly connected to an analogue local exchange that is virtually transparent with regard to the impedances connected to its ports and the subscriber lines are short (e.g. less than 500 meters).

Except where indicated otherwise, the design objectives given below should be met when measured between the 2-wire audio input and output ports of two PCM terminal equipments connected back-to-back and with input and output ports terminated with their nominal impedances (except where specified in §§ 3.3 and 11).

The limits should be considered to apply to the combination of the 2-wire to 4-wire terminating units and the PCM multiplex equipment regardless of whether the two functions are integrated into a single equipment or realized separately. In the latter case, an allowance has not been included for the effect of the interconnecting cable.

Unless stated otherwise, measurements should be made with the 4-wire loop opened in such a way that the impedances presented to the 4-wire ports of the 2-wire/4-wire terminating unit are representative of those that will occur in normal operation. This condition may be achieved by interrupting the digital signal in the opposite direction to the direction of measurement and injecting an idle character signal into the appropriate channel (decoder output value number 0 for μ-law or decoder output value number 1 for A-law with the sign bit in a fixed state). It should be noted that the opening of the 4-wire loop is considered necessary to determine the intrinsic performance of the equipment. In normal operation, where the loop is not opened, account needs to be taken of the impact on overall performance of the terminating impedances connected to the 2-wire interfaces.

In deriving the limits, an allowance has been included for the effect of possible signalling functions and/or line current feeding on the transmission performance. The limits should be met when any signalling function is in the normal speaking condition, but excluding any dynamic signalling conditions, e.g. metering.

The limits do not, in general, have any allowance for the effects of line current noise. The permissible amount of line current noise and the need for allowances are under study.

To avoid level errors produced as a result of the use of test frequencies which are sub-multiples of the PCM sampling rate, the use of integer sub-multiples of 8 kHz should also be avoided.

Where a nominal reference frequency of 1020 Hz is indicated, the actual frequency should be 1020 Hz + 2 Hz − 7 Hz in accordance with Recommendaton O.6.

For an interim period Administrations may, for pratical reasons, need to use a reference frequency of nominally 800 Hz, but slightly offset from this value to avoid sub-multiples of sampling frequencies.

1 Attenuation/frequency distortion

The variations with frequency of the attenuation of any channel should be within the limits shown in the mask of Figure 1/G.713.

The nominal reference frequency is 1020 Hz.

The preferred input power level is −10 dBm0. As an alternative, a level of 0 dBm0 may be used.

The distortion contributed by the separate encoding and decoding sides should be nominally equal.

2 Group delay

2.1 *Absolute group delay*

The absolute group delay at the frequency of minimum group delay should not exceed 750 microseconds.

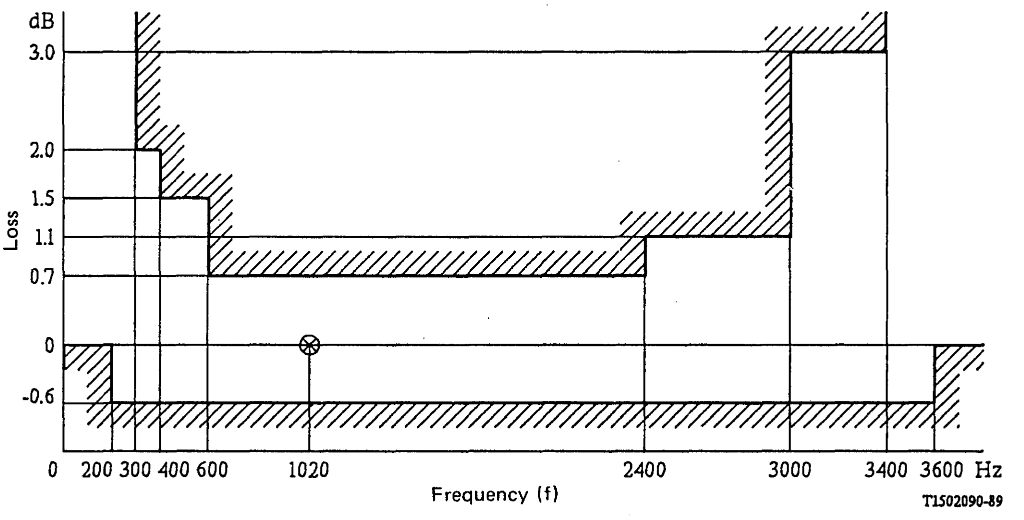
The minimum value of group delay is taken as the reference for the group delay distortion.

2.2 *Group delay distortion with frequency*

The group delay distortion should lie within the limits shown in the template of Figure 2/G.713.

2.3 *Input level*

The requirements of §§ 2.1 and 2.2 should be met at an input power level of −10 dBm0 (preferred value). As an alternative, a level of 0 dBm0 may be used.



Note – Some Administration apply a limit of 1 dB maximum loss for the frequency range 300 to 3000 Hz.

FIGURE 1/G.713

Attenuation/frequency distortion

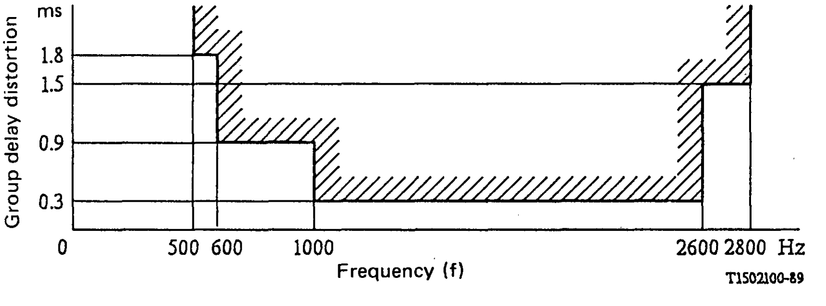


FIGURE 2/G.713

Group delay distortion with frequency

3 Impedance of voice-frequency ports

3.1 *Nominal impedance*

No single value of impedance is recommended.

The most widely used value of nominal impedance at 2-wire audio input and output ports is 600 ohms resistive (balanced). Some Administrations adopt values of 600 ohms + 2.16 μF or 900 ohms + 2.16μF, and one Administration uses 900 ohms resistive, the latter representing a compromise value suitable for loaded and unloaded cables.

Note – Some examples of complex impedances used in connection with subscriber lines can be found in Recommendation Q.552, § 2.2.1.

3.2 *Return loss*

The return loss, measured against the nominal impedance, should meet the limits given below:

Frequency range (Hz)	Return loss (dB)
300 to 600	> 12
600 to 3400	> 15

3.3 *Longitudinal balance*

The measurements arrangements for longitudinal balance parameters referred to below are defined in Recommendation O.9 which also gives some information about the requirements of test circuits (Note 1). The value of Z in the driving test circuit should be 600 ohms ± 20% and the termination at the other port shall be the nominal characteristic impedance.

a) The longitudinal conversion loss (see Recommendation O.9, § 2.1) as measured at the 2-wire voice-frequency interfaces should not be less than the limits shown in Figure 3/G.713.

b) The difference between the longitudinal conversion transfer loss (see Recommendation O.9, § 2.3) at the specified frequencies and the insertion loss at the same frequencies should not be less than the limits shown in Figure 3/G.713. The requirement is only applicable to the configuration where the driving test circuit is applied to one of the 2-wire voice-frequency interfaces and a measurement made at the other 2-wire voice-frequency interface. The measurement should be made with the Switch S, shown in Figure 3/O.9, closed.

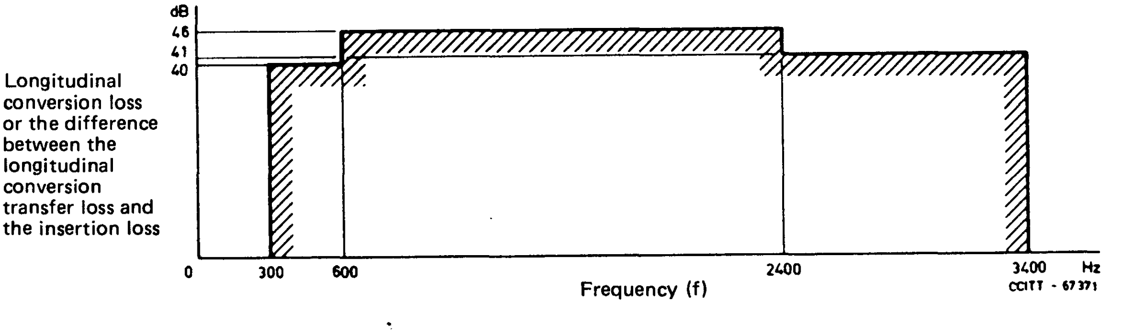


FIGURE 3/G.713

Longitudinal balance

Note 1 – Attention is drawn to Recommendation O.9, § 3, which shows the equivalence between a number of different test driving circuits and also includes information concerning the inherent balance requirements of the test bridge.

Note 2 – Attention is drawn to the fact that these values represent minimum requirements. The magnitude of potential longitudinal signal voltages depends, for example, on system use, the system environment, the location of hybrid transformers and attenuators, and may therefore vary for different Administrations. Some Administrations have found it necessary to specify higher values for longitudinal conversion loss and longitudinal conversion transfer loss to ensure that transverse voltages caused by possible longitudinal signal voltages are sufficiently small.

Note 3 – The possible need to introduce limits for frequencies below 300 Hz, in particular at 50 or 60 Hz, is under study. Overall rejection of longitudinal interference can be achieved by a combination of good longitudinal balancing and high pass filtering (see § 5.2).

Note 4 – The measurements should be made selectively.

4 Idle channel noise

4.1 *Weighted noise*

With the input and output ports of the channel terminated in the nominal impedance, the idle channel noise should not exceed −65 dBm0p.

Note – This limit does not include any allowance for additional noise which might be present when signalling takes place on the two wires. The derivation of limits for this case, taking account of the philosophy adopted in Recommendation Q.507, is under study. Due to the effects of quantization, it is not necessarily the case that the noise powers can be added.

4.2 *Single frequency noise*

The level of any single frequency (in particular the sampling frequency and its multiples), measured selectively, should not exceed −50 dBm0.

4.3 *Receiving equipment noise*

Noise contributed by the receiving equipment alone should be less than −75 dBm0p when its input is driven by a PCM signal corresponding to the decoder output value number 0 for the μ-law or decoder output value number 1 for the A-law.

5 Discrimination against out-of-band input signals

5.1 *Input signals above 4.6 kHz*

With any sine-wave signal in the range from 4.6 kHz to X kHz applied to the input port of the channel at a suitable level, the level of any image frequency produced at the output port of the channel should, as a minimum requirement, be at least 25 dB below the level of the test signal.

Note – It has been found that a suitable test level is −25 dBm0. The value of X is under study, but it should be at least 150 kHz.

5.2 *Signals below 300 Hz*

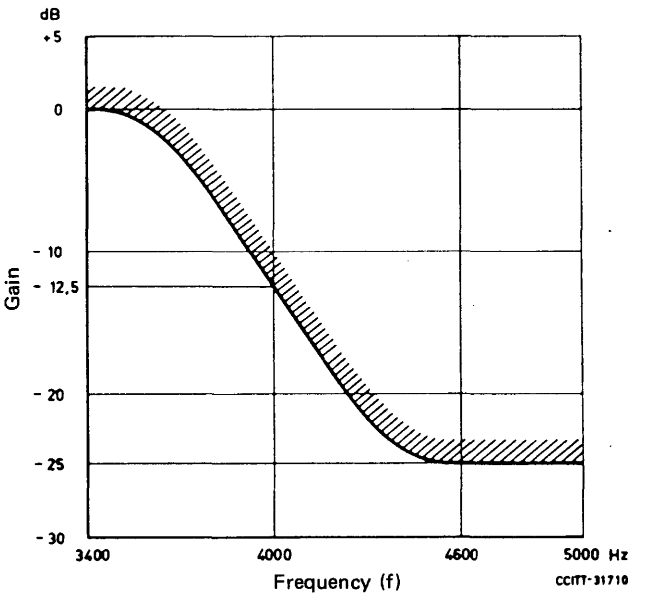
No particular value is recommended.

Note 1 – While some Administrations have no particular requirement in this respect some other Administrations have found it necessary to provide at least 20 to 26 dB rejection in the send side at frequencies across the band 15-60 Hz.

Note 2 – Overall rejection of longitudinal interference can be achieved by a combination of good longitudinal balancing (see § 3.3) and high pass filtering.

5.3 *Overall requirement*

Attention is drawn to the importance of the attenuation characteristic in the range 3400 to 4600 Hz. Although other attenuation characteristics can satisfy the above requirements, the filter template of Figure 4/G.713 gives adequate protection against the out-of-band signals above 3.4 kHz.



Note – The curved portion of the graph conforms to the equation $G = 12.5 \left[\sin \frac{\pi(4000-f)}{1200} - 1\right]$ dB for the range $3400 \leq f \leq 4600$.

FIGURE 4/G.713

Gain relative to gain at 1000 Hz

6 Spurious out-of-band signals at the channel output

With a digitally simulated sine-wave signal in the frequency range 300-3400 Hz and at a level of 0 dBm0 applied to a channel time slot at the decoder input, the level of spurious out-of-band image signals measured selectively at the output port should as minimum requirement be lower than −25 dBm0.

Attention is drawn to the importance of the attenuation characteristic in the range 3400 to 4600 Hz. Although other attenuation characteristics can satisfy the above requirement, the filter template of Figure 4/G.713 gives adequate protection against the out-of-band signals.

7 Total distortion, including quantizing distortion

Two alternative methods are recommended. It should be noted that the two test methods are not exactly equivalent. The noise test method (Method 1) gives fairly smooth curves, not very dependent upon input signal level. The sine-wave method (Method 2) can be more sensitive in identifying possible localized codec imperfections. Thus the two methods respond to practical codec impairments in slightly different ways.

Note 1 – Some Administrations have taken the position that the requirements of both test methods should be met. Other Administrations are of the opinion that meeting the requirements of either test method is sufficient to meet network performance requirements. In practice Administrations may choose to use only one method in production testing and operational situations.

Note 2 – The limits for Methods 1 and 2 do not include any allowance for additional noise which might be present when signalling takes place on the two wires. The derivation of limits for this case, taking account of the philosophy adopted in Recommendation Q.507, is under study.

Method 1

With a noise signal corresponding to Recommendation O.131 applied to the input port of a channel, the ratio of signal-to-total distortion power measured at the output port should lie above the limits shown in Figure 5/G.713.

Note 1 – These limits are based on a noise signal having a Gaussian distribution of amplitudes and the derivation of the limits is given in Annex A of Recommendation G.712.

Note 2 – The limits take into account the attenuation-frequency distortion in the frequency range of the noise stimulus.

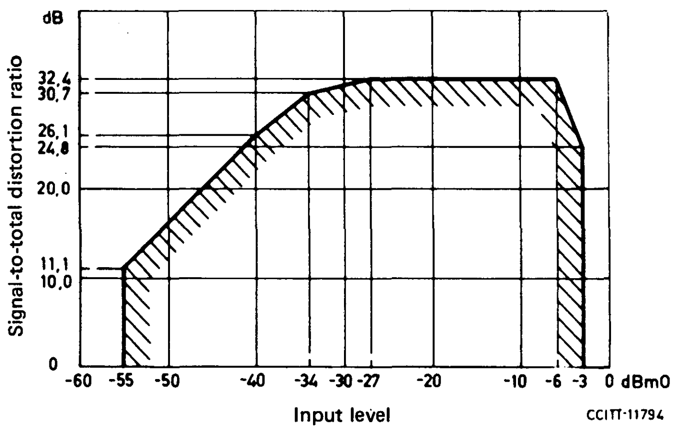


FIGURE 5/G.713

Signal-to-total distortion ratio as a function of input level (Method 1)

Method 2

With a sine-wave signal at a nominal frequency of 1020 Hz (preferred value) or 820 Hz (see Recommendation O.132) applied to the input port of a channel, the ratio of signal-to-total distortion power measured with the proper noise weighting (see Table 4/G.223), should lie above the limits shown in Figure 6/G.713.

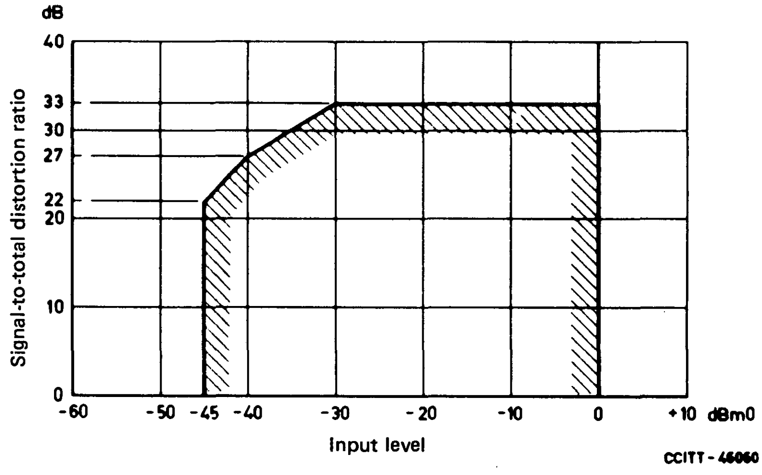


FIGURE 6/G.713

Signal-to-total distortion ratio as a function of input level (Method 2)

8 Spurious in-band signals at the channel output port

With a sine-wave signal in the frequency range 700-1100 Hz and at a level of 0 dBm0 applied to the input port of a channel, the output level at any frequency other than the frequency of the applied signal, measured selectively in the frequency band 300-3400 Hz, should be less than −40 dBm0.

9 Variation of gain with input level

Two alternative methods are recommended (see comments in § 7).

Method 1

With a band limited noise signal, as defined in Recommendation O.131, applied to the input of any channel at a level between −55 dBm0 and −10 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits of the mask of Figure 7a/G.713. The measurement should be limited to the frequency band 350-550 Hz in accordance with the filter characteristic defined in Recommendation O.131, § 3.2.1.

Furthermore, with a sine-wave signal in the frequency range 700-1100 Hz applied to the input of any channel at a level between −10 dBm0 and +3 dBm0, the gain variation of that channel relative to the gain at an input level of −10 dBm0, should lie within the limits of the mask of Figure 7b/G.713. The measurement should be made selectively.

Method 2

With a sine-wave signal in the frequency range 700-1100 Hz applied to the input port of any channel at a level between −55 dBm0 and +3 dBm0, the gain variation of that channel relative to the gain at an input level of −10 dBm0 should lie within the limits of the mask of Figure 7c/G.713. The measurement should be made selectively.

10 Interchannel crosstalk

10.1 The crosstalk between individual channels of a multiplex should be such that with the sine-wave signal in the frequency range 700-1100 Hz and at a level of 0 dBm0 applied to an input port, the crosstalk level received in any other channel should not exceed −65 dBm0.

Note – In order to overcome fundamental gain enhancement effects, associated with PCM encoders, which can mask the true crosstalk, an activating signal may be injected into the disturbed channel when implementing crosstalk measurements with sine-wave signals. Suitable activating signals are band limited noise (see Recommendation O.131) at a level in the range −50 to −60 dBm0 or a sine-wave at a level in the range −33 to −40 dBm0. Care must be taken in the choice of frequency and the filtering characteristics of the measuring apparatus in order that the activating signal does not significantly affect the accuracy of the crosstalk measurement.

10.2 When a white noise signal shaped in accordance with Recommendation G.227 at a level of 0 dBm0 is applied to the input port of up to four channels, the level of the crosstalk received in any other channel should not exceed −60 dBm0p. Uncorrelated noise should be used when more than one input channel is energized.

11 Echo and stability

11.1 *Terminal balance return loss (TBRL)*

This quantity characterizes the equipment performance required to comply with the network performance objective of Recommendation G.122 in respect of echo. The TBRL is defined as the balance return loss (see definition in Recommendation Q.552, § 3.1.8.1) measured against a balance test network. It is related to the "Half-Loop Loss" HLL i.e. the loss between the digital test input point, T_i, and the digital test output point, T_o (see Figure 8/G.713) as follows:

$$\text{HLL} = T_i \text{ to } T_o \text{ loss} = P_i + P_o + \text{TBRL} \qquad \text{(dB)}$$

where P_i and P_o are the measured values of loss in the equivalent circuit of Figure 8/G.713 which represent all the loss between the digital test point and the 2-wire point, or conversely, at the measurement frequency.

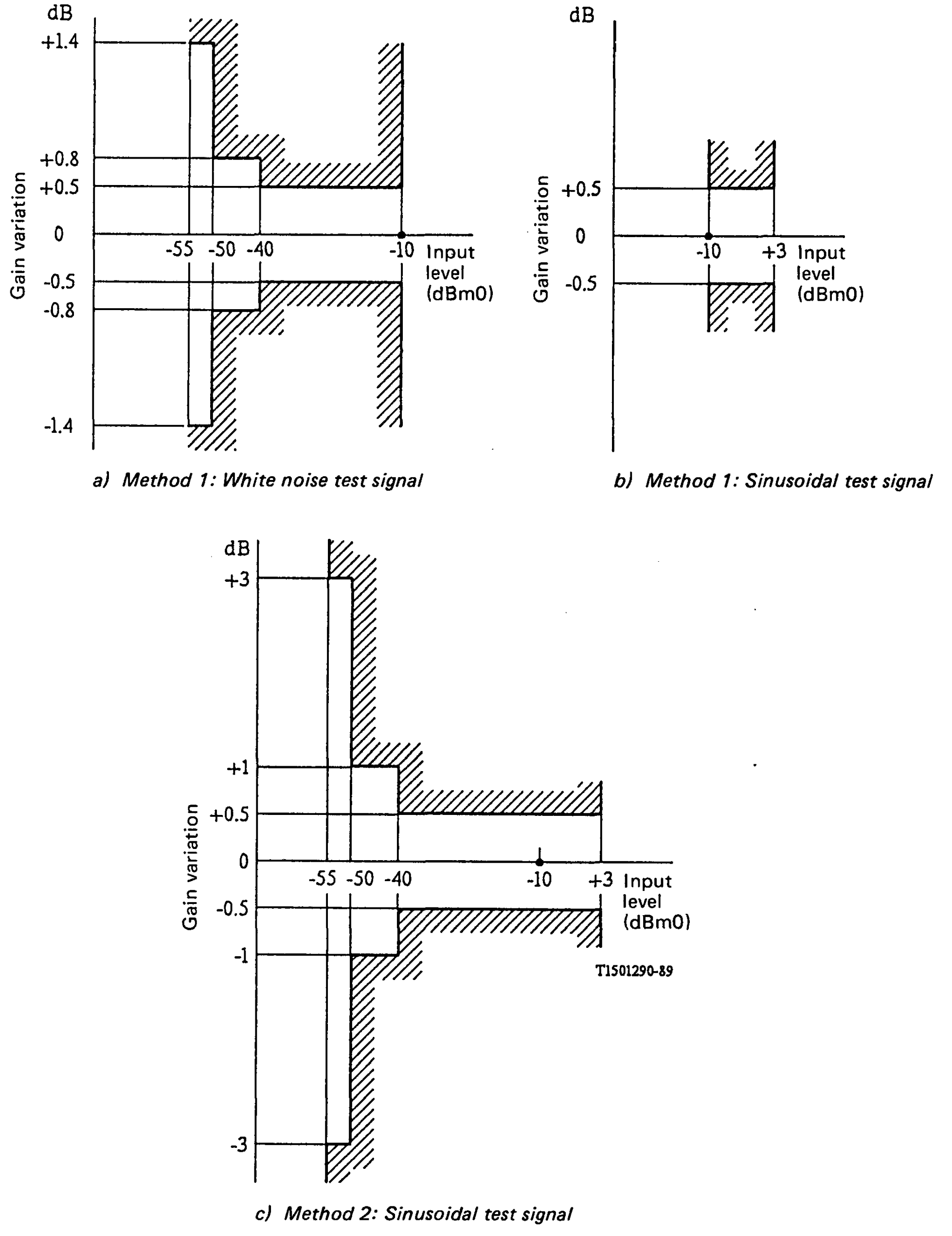


FIGURE 7/G.713

Variation of gain with input level

The TBRL should be measured in the arrangement of Figure 8/G.713 with a sinusoidal test signal at frequencies across the telephone band covering the bandwidth 300 to 3400 Hz.

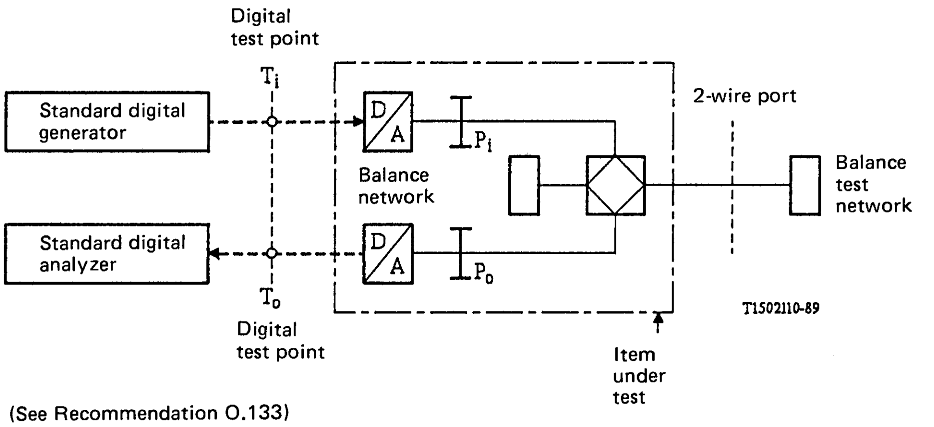


FIGURE 8/G.713

Arrangement for measuring half-loop loss

Values for the nominal balance impedance and for the maximum deviation of this impedance from the nominal value, differ from one Administration to another. The range of impedances presented at the 2-wire port during normal operation also varies considerably. Administrations will need to establish their own requirements for TBRL taking account of national or international transmission plans. As a minimum requirement, the TBRL limits shown in Figure 9/G.713 should be met when the 2-wire port is terminated with a balance test network which is representative of the impedance conditions expected in the speaking condition from a population of 2-wire trunks connected to the PCM muldex. The limits are provisional.

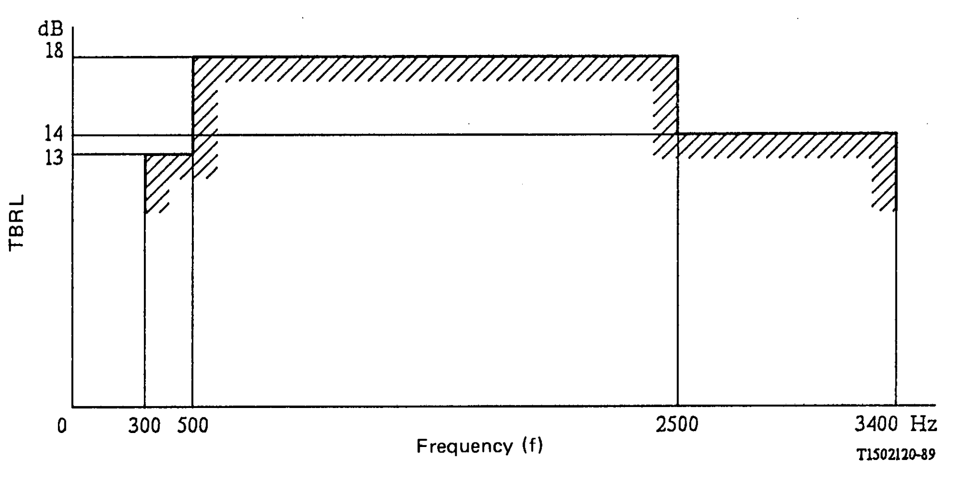


FIGURE 9/G.713

Minimum values of terminal balance return loss (provisional)

11.2 *Stability loss (SL)*

The stability loss is defined as the minimum value of the half-loop loss measured in the arrangement of Figure 8/G.713. The stability loss should be measured between T_i and T_o by terminating the 2-wire port with stability test networks representing the worst case terminating condition encountered in normal operation. Some Administrations may find that open circuit and short circuit terminations are sufficiently representative of worst case conditions. Other Administrations may need to specify, for example, an inductive termination to represent that worst case condition.

The stability loss at any frequency can be expressed as follows:

$$\mathrm{SL} \geqslant P_i + P_o - X \qquad \mathrm{dB}$$

where P_i and P_o are measured values of loss, at the measurement frequency, under normal terminating conditions at the 2-wire port. X is a factor dependent on the interaction between the 2-wire input impedance, the 2-wire balance impedance and the impedance actually applied at the 2-wire port. X can be computed or measured by the method described in Recommendation Q.552.

The 2-wire input and balance impedances at a 2-wire/4-wire interface usually have to be optimized by Administrations with regard to echo and sidetone. The worst case terminations depend on the actual network conditions. Thus, the value of X is fully determined by network conditions and the impedance strategy. Values between 0 and 3 dB have been observed in practice.

Administrations should choose the nominal values of P_i and P_o taking account of the value of X for their particular operating conditions and of national and international transmission plans for overall network stability (see Recommendation G.122).

12 Interference from signalling

The maximum level of any interference into a channel should not exceed −50 dBm0p, when signalling (10 Hz signal with 50/50 duty ratio) is active on all the channels except the channel under test.

13 Relative levels at voice frequence ports

On account of differences in network transmission plans and equipment utilization, Administrations have differing requirements for the range of relative levels to be provided. It would appear that the following ranges would encompass the requirements of a large number of Administrations:

- input level (encoding side): 0 to −5 dBr in 0.5 dB steps;
- output level (decoding side): −2 to −7.5 dBr in 0.5 dB steps.

It has been recognized that it is not necessarily appropriate for a particular design of equipment to be capable of operating over the entire range.

14 Adjustment of actual relative levels

Adjustment (especially initial adjustment) of the relative levels, and hence of the gain of the separate encoding and decoding sides of PCM channels, should be made at typical values of environmental conditions. The adjustments should lead to a deviation of the actual values against the nominal values not exceeding ± 0.4 dB, and should be made as follows:

14.1 The decoding side should be adjusted to conform with § 4 of Recommendation G.711 within a tolerance of ± 0.4 dB in practice.

14.2 The encoding side should be adjusted by connecting its output to a standard digital analyzer which has been adjusted to have precisely nominal gain, and applying a sine-wave signal at a nominal frequency of 1020 Hz at a level of 0 dBm0 to the voice-frequency input of the encoding side. The encoding side should then be adjusted so that the resulting sine-wave signal at the voice-frequency output of the decoding side is at a level of 0 dBm0. In practice the adjustment should be made with a tolerance of ± 0.4 dB.

Alternatively a decoding side with a known error, within the limits defined in § 14.1, may be used provided that account is taken of this known error in adjusting the encoding side.

14.3 The load capacity of the encoding side may be checked by applying a sine-wave signal at a nominal frequency of 1020 Hz at its voice-frequency input. The level of this signal should be initially well below T_{max} and should then be slowly increased. The input level should be measured at which the first occurrence is observed of the character signal corresponding to the extreme quantizing interval for both positive and negative values. T_{max} is taken as being 0.3 dB greater than the measured input level.

This method allows T_{max} to be checked for both positive and negative amplitudes and the values thus obtained should be within ± 0.4 dB of the theoretical load capacity (i.e. +3.14 dBm0 for the A-law or +3.17 dBm0 for the μ-law). As an alternative, the occurrence of the largest pulse amplitude at the decoder output may be used as a means of identifying T_{max}.

15 Short-term and long-term variations of loss with time

When a sine-wave signal at a nominal frequency of 1020 Hz and at a level of −10 dBm0 (preferred value; 0 dBm0 may be used) is applied to any voice-frequency input, the level measured at the corresponding voice-frequency output should not vary by more than ± 0.2 dB during any 10-minute interval of typical operation, nor by more than ± 0.6 dB during any one year under the permitted variations in the power supply voltage and temperature.

Recommendation G.714

SEPARATE PERFORMANCE CHARACTERISTICS FOR THE ENCODING AND DECODING SIDES OF PCM CHANNELS APPLICABLE TO 4-WIRE VOICE-FREQUENCY INTERFACES

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

1 General

The CCITT,

considering

(a) that Recommendation G.712 defines the performance of point-to-point PCM systems between 4-wire voice-frequency ports;

(b) that with the introduction of digital switching into telecommunication networks, many PCM systems will not be operated on a point-to-point basis. In these instances a particular PCM send side will be associated no longer with a particular distant PCM receive side. Furthermore, the combination is likely to vary on a call by call basis;

(c) that for digital signals crossing an international border, the send and receive sides of PCM systems are likely to be of different origin;

(d) that it is necessary to achieve compatibility between send and receive side interconnections as can arise in the situations outlined above,

recommends

that for those PCM systems for which there is a need for separate specification, the requirements given below should be met for the separate send and receive sides when measured at the voice-frequency ports. These specifications should ensure that, if not stated otherwise, any combination of PCM multiplexes corresponding to the specifications meets also those of Recommendation G.712.

Note – In the following sections, the concepts of a "standard digital generator" and a "standard digital analyzer" should be assumed and these are defined as follows:

A **standard digital generator** is a hypothetical device which is absolutely ideal, i.e. a perfect analogue-to-digital converter preceded by an ideal low pass filter (assumed to have no attenuation frequency distortion and no envelope delay distortion), and which may be simulated by a digital processor.

A **standard digital analyzer** is a hypothetical device which is absolutely ideal, i.e. a perfect digital-to-analogue converter followed by an ideal low pass filter (assumed to have no attenuation frequency distortion and no envelope delay distortion), and which may be simulated by a digital processor.

Recommendation O.133 contains information about test equipment based on these concepts. Account should be taken of the measurement accuracy provided by test equipment designed in accordance with that Recommendation.

The following specifications are based on ideal measuring equipment. Therefore, they do not include any margin for measurement errors.

To avoid level errors produced as a result of the use of test frequencies which are sub-multiples of the PCM sampling rate, the use of integer sub-multiples of 8 kHz should be avoided.

Where a nominal reference frequency of 1020 Hz is indicated (measurement of attenuation/frequency distortion and adjustment of relative levels), the actual frequency should be 1020 Hz, +2 Hz, −7 Hz in accordance with Recommendation O.6.

For an interim period Administrations may, for practical reasons, need to use a reference frequency of nominally 800 Hz.

2 Relative levels at voice-frequency ports

The specification should conform to Recommendation G.232, § 11.

3 Adjustment of actual relative levels

3.1 The gain of the encoding side should be adjusted by connecting its output to a standard digital analyzer and applying a sine-wave signal at a nominal frequency of 1020 Hz at a level of 0 dBm0 to the voice-frequency input. The adjustment should result in an output level of 0 dBm0 ± 0.3 dB at the audio output of the receive side and should be made under typical conditions of power supply voltage, humidity and temperature.

The load capacity of the encoding side may be checked by applying a sine-wave signal at nominal frequency of 1020 Hz at its voice-frequency input. The level of this signal should be initially well below T_{max} and should then be slowly increased. The input level should be measured at which the first occurrence is observed of the character signal corresponding to the extreme quantizing interval for both positive and negative values. T_{max} is taken as being 0.3 dB greater than the measured input level.

This method allows T_{max} to be checked for both positive and negative amplitudes and the values thus obtained should be within ± 0.3 dB of the theoretical load capacity (i.e. +3.14 dBm0 for the A-law or +3.17 dBm0 for the μ-law).

3.2 The decoding side should be adjusted to conform with § 4 of Recommendation G.711 within a tolerance of ± 0.3 dB.

4 Short-term and long-term variations of loss with time

4.1 When a sine-wave signal at a nominal frequency of 1020 Hz and at a level of −10 dBm0 (preferred value; 0 dBm0 may be used) is applied to any voice-frequency input, the level measured at the corresponding voice-frequency output of a decoding side having nominal gain should not vary by more than ± 0.3 dB during any one year under the permitted variations in the power supply voltage and temperature.

4.2 When a digitally simulated sine-wave signal at a level of −10 dBm0 (preferred value; however, 0 dBm0 sequence of Recommendation G.711, Tables 5/G.711 and 6/G.711, may be used) is applied to any channel time slot at the decoder input, the level measured at the corresponding voice-frequency output should not vary by more than ± 0.1 dB during any 10-minute interval of typical operation, nor by more than ± 0.3 dB during any one year under the permitted variations in the power supply voltage and temperature.

5 Nominal impedance and return loss of voice-frequency ports

The nominal impedance at the 4-wire voice-frequency input and output ports should be 600 ohms, balanced.

The return loss, measured against the nominal impedance, should not be less than 20 dB over the frequency range 300 Hz to 3400 Hz.

Note – The return loss limit should be met when the adjusting pads are set to 0 dB (see Recommendation G.232, Figure 5/G.232).

6 Longitudinal balance

The longitudinal balance parameters referred to below are defined in Recommendation O.9 which also gives some information about the requirements of test circuits (Note 1). The value of Z in the driving test circuit should be 600 ohms ± 20%.

a) The longitudinal conversion loss (see Recommendation O.9, § 2.1) as measured at the input port of the encoding side should not be less than the limits shown in Figure 1/G.714.

b) The longitudinal conversion loss (see Recommendation O.9, § 2.1) as measured at the output port of the decoding side should not be less than the limits shown in Figure 1/G.714.

Note 1 – Attention is drawn to Recommendation O.9, § 3, which shows the equivalence between a number of different test driving circuits and also includes information concerning the inherent balance requirements of the test bridge.

Note 2 – Attention is drawn to the fact that these values represent minimum requirements. The magnitude of potential longitudinal signal voltages depends, for example, on system use, the system environment, the location of hybrid transformers and attenuators, and may therefore vary for different Administrations. Some Administrations have found it necessary to specify higher values for longitudinal conversion loss to ensure that transverse voltages caused by possible longitudinal signal voltages are sufficiently small.

Note 3 – The need to include other balance parameters is under study.

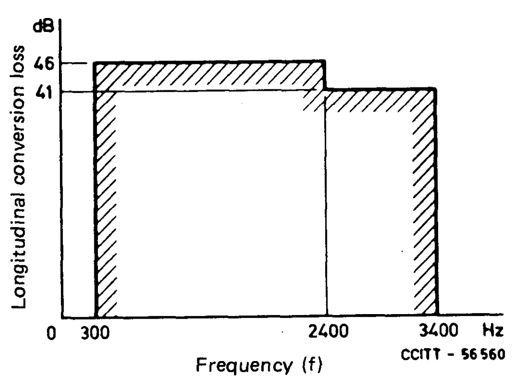


FIGURE 1/G.714

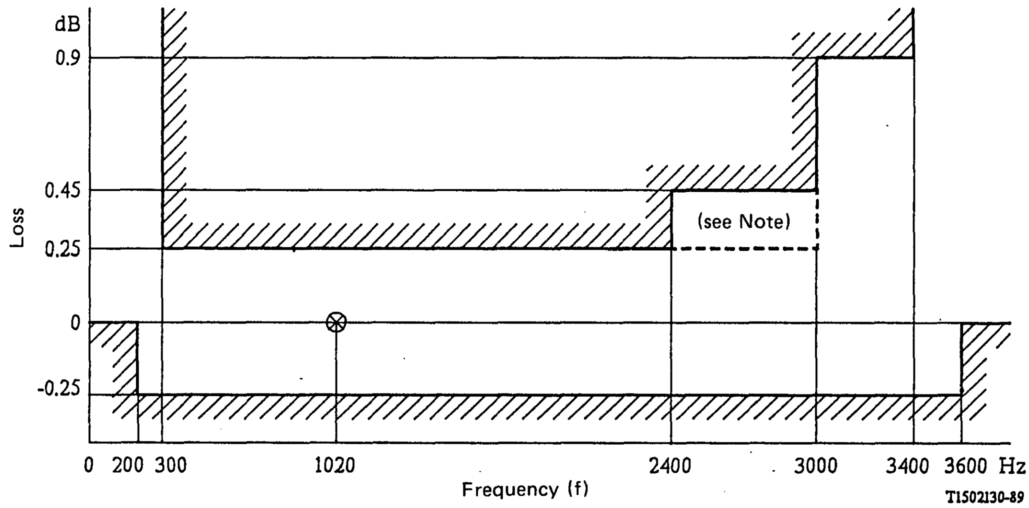
Longitudinal balance

7 Attenuation/frequency distortion of the encoding or the decoding side

The variations with frequency of the attenuation of any channel should lie within the limits shown in the mask of Figure 2/G.714.

The nominal reference frequency is 1020 Hz.

The preferred input power level is –10 dBm0. As an alternative, a level of 0 dBm0 may be used.



Note – In some applications in wich several PCM channels may be connected in tandem, it may be necessary to extend the + 0.25 dB limit from 2400 Hz to 3000 Hz.

FIGURE 2/G.714

Attenuation/frequency distortion

8 Group delay

Note – The following are design objectives only. It does not seem necessary to define special test equipment to make these measurements between the voice-frequency input and the digital output and between the digital input and the voice-frequency output.

8.1 *Absolute group delay*

8.1.1 The absolute group delay of the encoding side at the frequency of minimum group delay should not exceed 360 microseconds.

8.1.2 The absolute group delay of the decoding side at the frequency of minimum group delay should not exceed 240 microseconds.

8.2 *Group-delay distortion with frequency of the encoding or decoding side*

The group delay distortion should lie within the limits shown in the mask of Figure 3/G.714.

The minimum value of group delay for each side is taken as the reference for the group delay distortion.

8.3 *Input level*

The requirements of §§ 8.1 and 8.2 above should be met at an input power level of – 10 dBm0 (preferred value). As an alternative, a level of 0 dBm0 may be used.

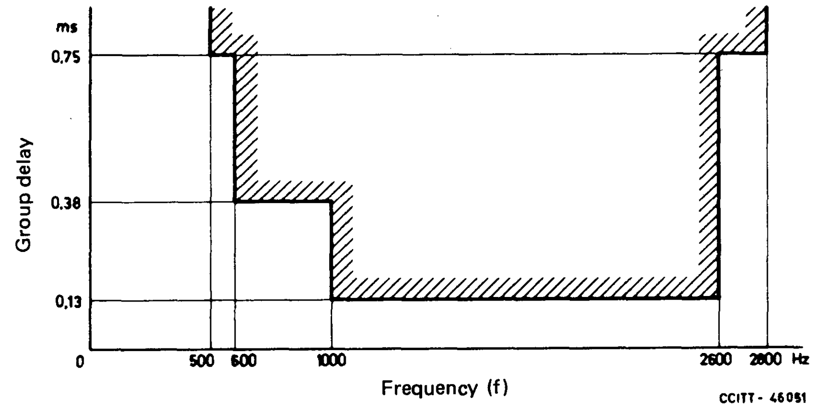


FIGURE 3/G.714

Group delay distortion with frequency

9 Weighted noise measured at the encoding side

With the input ports of the channel terminated in the nominal impedance, the idle channel noise should not exceed −66 dBm0p.

10 Receiving equipment noise

Noise contributed by the receiving equipment alone should be less than −75 dBm0p when its input is driven by a PCM signal corresponding to the decoder output value number 0 for the μ-law or decoder output value number 1 for the A-law.

11 Discrimination against out-of-band input signals (only applicable to encoding side)

11.1 *Input signals above 4.6 kHz*

With any sine-wave signal in the range from 4.6 kHz to X kHz applied to the input port of the channel at a suitable level, the level of any image frequency produced in the time slot corresponding to the channel should, as a minimum requirement, be at least 25 dB below the level of the test signal.

Note – It has been found that a suitable test level is −25 dBm0. The value of X is under study, but it should be at least 150 kHz.

11.2 *Overall requirement*

Under the most adverse conditions encountered in a national network the PCM channel should not contribute more than 100 pW0p of additional noise in the band 10 Hz-4 kHz at the channel output, as a result of the presence of out-of-band signals at the channel input.

Note 1 – The discrimination required depends on the performance of FDM channel equipments and telephone instruments in national networks, and individual Administrations should carefully consider the requirements they should specify taking into account the comments above and the requirement of § 11.2 above. In all cases at least the minimum requirement of § 11.1 above should be met.

Note 2 – Attention is drawn to the importance of the attenuation characteristic in the range 3400 to 4600 Hz. Although other attenuation characteristics can satisfy the requirements of §§ 11.1 and 11.2 above, the filter template of Figure 4/G.712 gives adequate protection against the out-of-band signals.

12 **Spurious out-of-band signals at channel output** (only applicable to decoding side)

12.1 *Level of individual components*

With a digitally simulated sine-wave signal in the frequency range 300-3400 Hz and at a level of 0 dBm0 applied to a channel time slot at the decoder input, the level of spurious out-of-band image signals measured selectively at the output port should be lower than −25 dBm0.

12.2 *Overall requirement*

The spurious out-of-band signals should not give rise to unacceptable interference in the equipment connected to the PCM channel. In particular, the intelligible or unintelligible crosstalk, in a connected FDM channel should not exceed a level of −65 dBm0 as a consequence of the spurious out-of-band signals at the PCM channel output.

Note 1 – The discrimination required depends on the performance of FDM channel equipment and telephone instruments in national networks and individual Administrations should carefully consider the requirements they should specify, taking into account the comments above and the requirement of § 12.2 above, in all cases at least the minimum requirement of § 12.1 above should be met.

Note 2 – Attention is drawn to the importance of the attenuation characteristic in the range 3400 to 4600 Hz. Although other attenuation characteristics can satisfy the requirements of §§ 12.1 and 12.2 above, the filter template of Figure 4/G.712 gives adequate protection against the out-of-band signals.

13 **Single frequency noise from the encoding or decoding side**

The level of any single frequency (in particular for the decoding side, at the sampling frequency and its multiples), measured selectively, should not exceed −50 dBm0.

14 **Total distortion, including quantizing distortion**

Two alternative methods are recommended. It should be noted that the two test methods are not exactly equivalent. The noise test method (Methd 1) gives fairly smooth curves, not very dependent upon input signal level. The sine-wave method (Method 2) can be more sensitive in identifying possible localized codec imperfections. Thus the two methods respond to practical codec impairments in slightly different ways.

Note 1 – Some Administrations have taken the position that the requirements of both test methods should be met. Other Administrations are of the opinion that meeting the requirements of either test method is sufficient to meet network performance requirements. In practice, Administrations may choose to use only one method in production testing and operational situations.

Note 2 – There is a slight possibility that an adverse combination of encoding and decoding sides might not meet the overall requirements of Recommendation G.712. To minimize this possibility some Administrations suggest that encoding and decoding sides of the same design should always meet the overall requirements of Recommendation G.712.

14.1 *Method 1* (encoding side)

With a noise signal corresponding to Recommendation O.131 applied to the input port of a channel, the ratio of signal-to-total distortion power should lie above the limits shown in Figure 4a/G.714.

14.2 *Method 1* (decoding side)

With a digitally simulated noise signal corresponding to Recommendation O.131 applied to the time slot of any telephone channel, the ratio of signal-to-total distortion power should lie above the limits shown in Figure 4b/G.714.

The values in the mask include the distortion power of an ideal encoder.

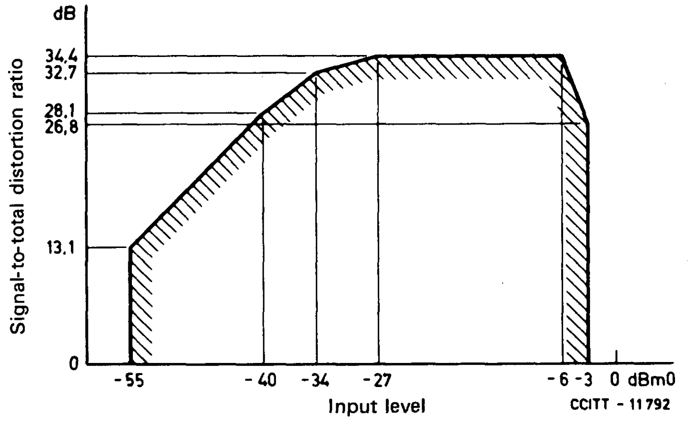


FIGURE 4a/G.714

Signal-to-total distortion ratio as function of input level (Method 1), encoding side

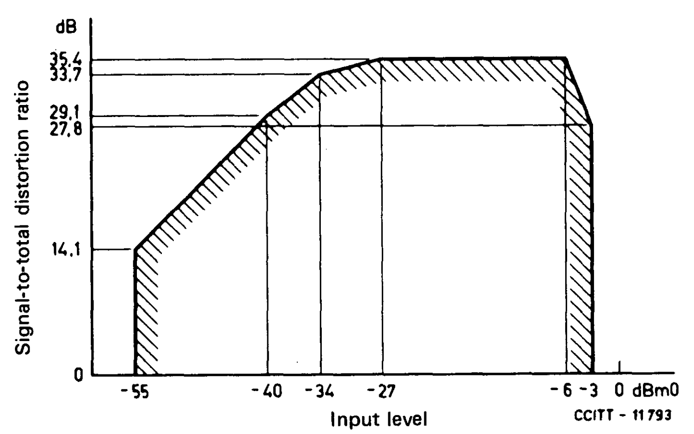


FIGURE 4b/G.714

Signal-to-total distortion ratio as a function of the input level (Method 1), decoding side

14.3 *Method 2* (encoding side)

With a sine-wave signal at a nominal frequency of 1020 Hz (preferred value) or 820 Hz (see Recommendation O.132) applied to the input port of a channel, the ratio of signal-to-total distortion power measured with the proper noise weighting (see Table 4/G.223) should lie above the limits shown in Figure 5/G.714.

14.4 *Method 2* (decoding side)

With a digitally simulated sine-wave signal at a nominal frequency of 1020 Hz (preferred value) or 820 Hz (see Recommendation O.132) applied to the timeslot of any channel, the ratio of signal-to-total distortion power measured with the proper noise weighting (see Table 4/G.223) should lie above the limits shown in Figure 5/G.714.

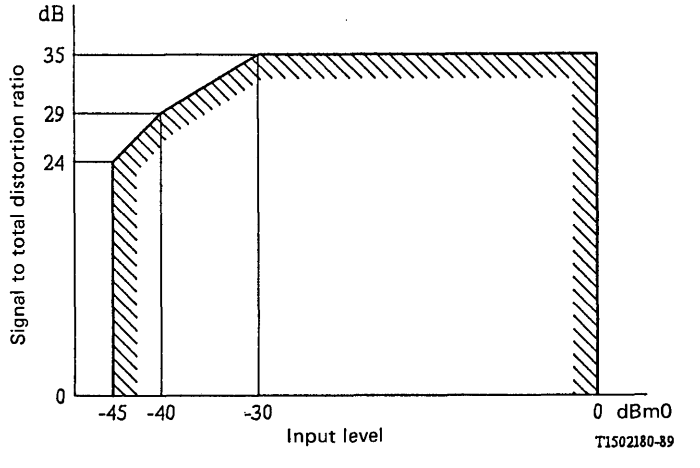


FIGURE 5/G.714

Signal-to-total distortion ratio as a function of the input level (Method 2), send and receive side

15 Variation of gain with input level

Two alternative methods are recommended (see comments in § 14).

15.1 *Method 1* (encoding side)

With a band limited noise signal as defined in Recommendation O.131, applied to the input port of any channel at a level between −55 dBm0 and −10 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits of Figure 6a/G.714. The measurement should be limited to the frequency band 350-550 Hz in accordance with the filter characteristics defined in Recommendation O.131, § 3.2.1.

Furthermore, with a sine-wave signal in the frequency range 700 to 1100 Hz applied to the input port of any channel at a level between −10 dBm0 and +3 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0 should lie within the limits of Figure 6b/G.714. The measurement should be made selectively.

15.2 *Method 1* (decoding side)

With a digitally simulated band limited noise signal, corresponding to Recommendation O.131, applied to the time slot of any telephone channel at a level between −55 and −10 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits of Figure 6a/G.714. The measurements should be limited to the frequency band 350 to 550 Hz in accordance with the filter characteristic defined in Recommendation O.131, § 3.2.1.

Furthermore, with a digitally simulated sine-wave signal in the frequency range 700 to 1100 Hz applied to the time slot of any telephone channel at a level between −10 dBm0 and +3 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits of Figure 6b/G.714. The measurement should be made selectively.

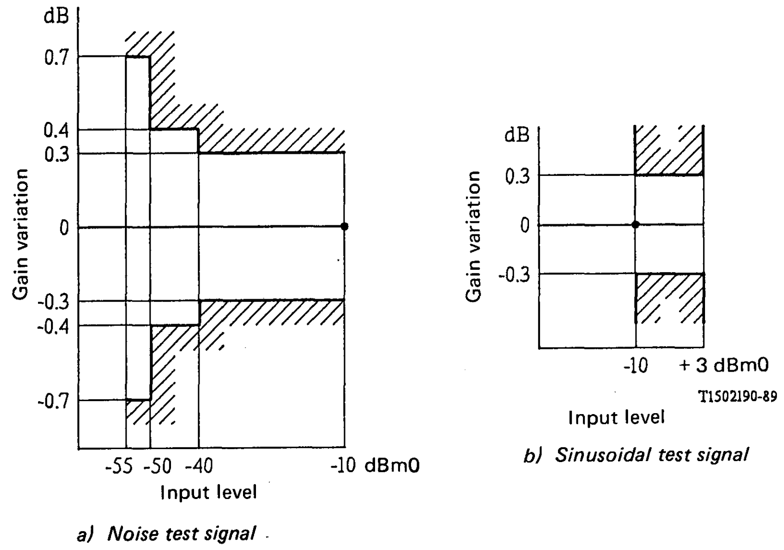


FIGURE 6/G.714

Variation of gain with input level (Method 1)

15.3 *Method 2* (encoding side)

With a sine-wave signal in the frequency range 700 to 1100 Hz applied to the input port of any channel at a level between −55 dBm0 and +3 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits given in Figure 7/G.714. The measurement should be made selectively.

15.4 *Method 2* (decoding side)

With a digitally simulated sine-wave signal in the frequency range 700 to 1100 Hz applied to the time slot of any telephone channel at a level between −55 dBm0 and +3 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits given in Figure 7/G.714. The measurement should be made selectively.

16 Crosstalk measurements with sine-wave signals

16.1 *General*

For the crosstalk measurements, auxiliary signals are injected as indicated in Figures 8/G.174 to 11/G.714. These signals are:

- the quiet code, i.e. a PCM signal corresponding to decoder output value number 0 (μ-law) or output value number 1 (A-law) (with the sign bit in a fixed state);
- a low level activating signal. Suitable activating signals are, for example, a band-limited noise signal (see Recommendation O.131), at a level in the range −50 to −60 dBm0 or a sine-wave signal at a level in the range from −33 to −40 dBm0. Care must be taken in the choice of frequency and the filtering characteristics of the measuring apparatus in order that the activating signal does not significantly affect the accuracy of the crosstalk measurement.

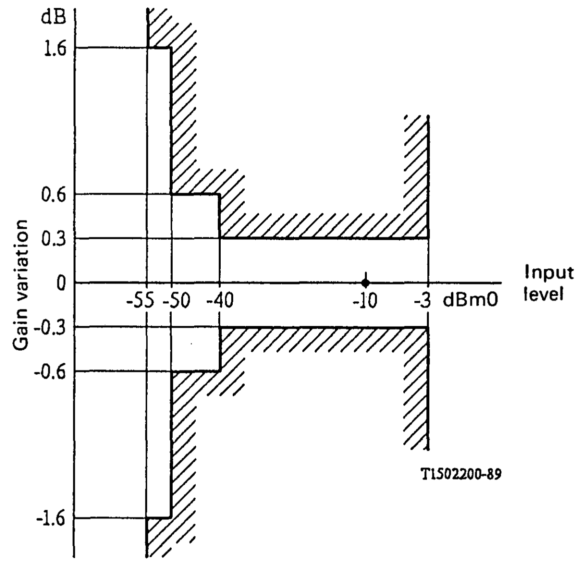


FIGURE 7/G.714

Variation of gain with input level (Method 2)

16.2 *Far-end and near-end crosstalk measured with analogue test signal*

The crosstalk between individual channels of a multiplex should be such that with a sine-wave signal in the frequency range 700 to 1100 Hz and at a level of 0 dBm0 applied to a voice-frequency input port, the crosstalk level produced in any other channel should not exceed -73 dBm0 for NEXT and -70 dBm0 for FEXT (see Figure 8/G.714).

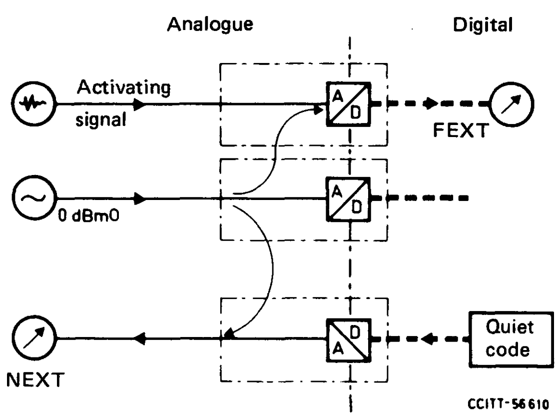


FIGURE 8/G.714

Measurements with analogue test signal between different channels

16.3 *Go-to-return crosstalk measured with analogue test signal*

The crosstalk between a channel and its associated return channel should be such that with a sine-wave signal at any frequency in the range 300-3400 Hz and at a level of 0 dBm0 applied to an input port, the crosstalk level measured at the output of the corresponding return channel should not exceed −66 dBm0. See Figure 9/G.714.

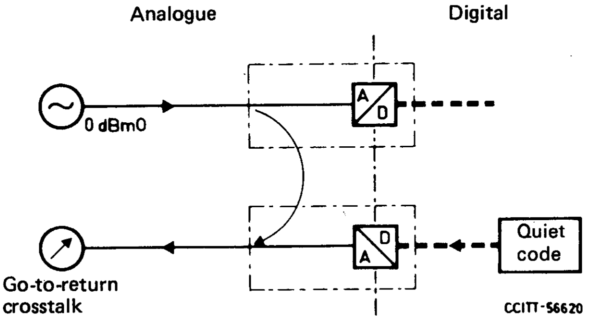


FIGURE 9/G.714

Measurements with analogue test signal between go and return directions of the same channel

16.4 *Far-end and near-end crosstalk measured with digital test signal*

The crosstalk between individual channels of a multiplex should be such that with a digitally simulated sine-wave signal in the frequency range 700 to 1100 Hz and at a level of 0 dBm0 applied to the digital input, the crosstalk level received in any other channel should not exceed −70 dBm0 for NEXT and −73 dBm0 for FEXT (see Figure 10/G.714).

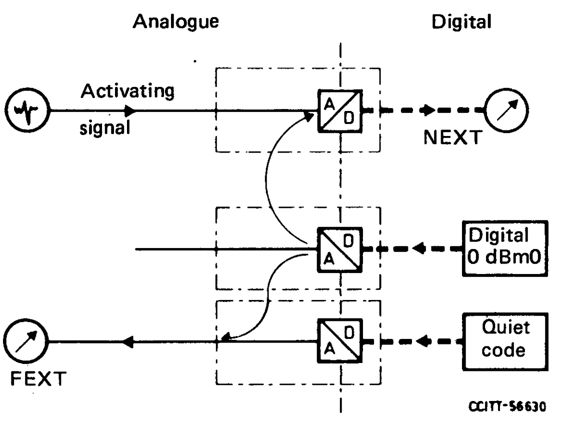


FIGURE 10/G.714

Measurements with digital test signal between different channels

16.5 *Go-to-return crosstalk measured with digital test signal*

The crosstalk between a channel and its associated return channel should be such that with a digitally simulated sine-wave signal at any frequency in the range 300-3400 Hz and at a level of 0 dBm0 applied to the digital input port, the crosstalk level measured at the digital output of the corresponding return channel should not exceed −66 dBm0. See Figure 11/G.714.

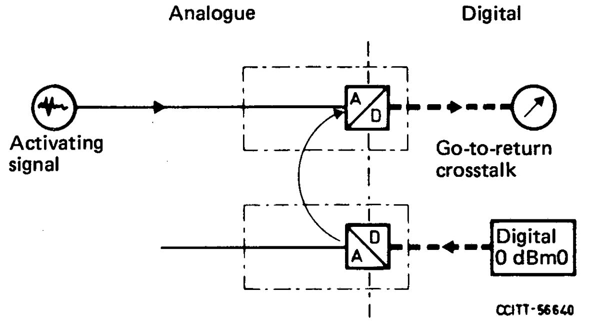


FIGURE 11/G.714

Measurements with digital test signal between go and return directions of the same channel

17 Crosstalk caused by conventional telephone signals (according to Recommendation G.227)

Under study.

18 Interference from signalling

The characterization of such interference by separate measurements requires four different types of measurement (see Figure 12/G.714), for crosstalk. In each case the maximum level of interference in one channel should not exceed −63 dBm0p when signalling (10 Hz signal with 50/50 duty ratio) is active simultaneously on all channels.

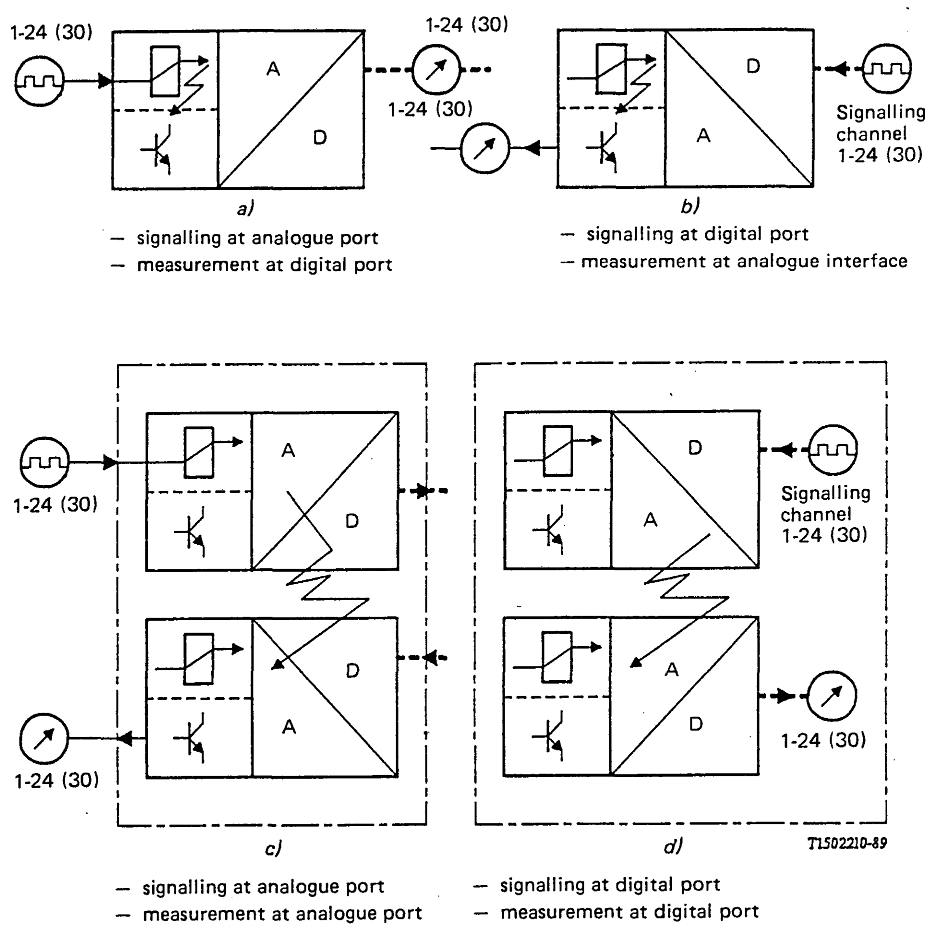


FIGURE 12/G.714

Measurement of signalling interference contributions

Recommendation G.715

SEPARATE PERFORMANCE CHARACTERISTICS FOR THE ENCODING AND DECODING SIDE OF PCM CHANNELS APPLICABLE TO 2-WIRE INTERFACES

(Melbourne, 1988)

1 General

The CCITT,

considering

(a) that Recommendation G.712 defines the performance of point-to-point PCM systems between 4-wire voice-frequency ports;

(b) that with the introduction of digital switching into telecommunication networks, many PCM systems will not be operated on a point-to-point basis. In these instances a particular PCM encoding side will be associated no longer with a particular distant PCM decoding side. Furthermore, the combination is likely to vary on a call-by-call basis;

(c) that for digital signals crossing an international border, the encoding and decoding sides of PCM systems are likely to be of different origin;

(d) that it is necessary to achieve compatibility between encoding and decoding side interconnections as can arise in the situations outlined above,

recommends

that for those PCM systems for which there is a need for separate specification, the requirements given below should be met for the separate encoding and decoding sides when measured at the 2-wire voice-frequency ports. These specifications should ensure that, if not stated otherwise, any combination of PCM multiplexes corresponding to the specifications meets also those of Recommendation G.713.

The parameters and values specified in this Recommendation apply to the use of PCM equipment connected to analogue trunks or to analogue exchanges. When PCM equipment is connected directly to analogue subscriber lines, different values for some of the parameters may be required. Recommendation Q.552 contains those values. They may also be applied if the PCM equipment is directly connected to an analogue local exchange that is virtually transparent with regard to the impedances connected to its ports and the subscriber lines are short (e.g. less than 500 meters).

In deriving the limits, an allowance has been included for the effect of possible signalling functions and/or line current feeding on the transmission performance. The limits should be met when any signalling function is in the normal speaking condition, but excluding any dynamic signalling conditions, e.g. metering.

The limits do not, in general, have any allowance for the effects of line current noise. The permissible amount of line current noise and the need for allowances are under study.

Note – In the following section, the concepts of a "standard digital generator" and "a standard digital analyzer" should be assumed and these are defined as follows:

A **standard digital generator** is a hypothetical device which is absolutely ideal, i.e. a perfect analogue-to-digital converter followed by an ideal low pass filter (assumed to have no attenuation/frequency distortion and no envelope delay distortion), and which may be simulated by a digital processor.

A **standard digital analyzer** is a hypothetical device which is absolutely ideal, i.e. a perfect digital-to-analogue converter followed by an ideal low pass filter (assumed to have no attenuation/frequency distortion and no envelope delay distortion), and which may be simulated by a digital processor.

Recommendation O.133 contains information about test equipment based on these concepts. Account should be taken of the measurement accuracy provided by test equipment designed in accordance with that Recommendation.

The following specifications are based on ideal measuring equipment. Therefore, they do not include any margin for measurement errors.

To avoid level errors produced as a result of the use of test frequencies which are sub-multiples of the PCM sampling rate, the use of integer sub-multiples of 8 kHz should be avoided.

Where a nominal reference frequency of 1020 Hz is indicated (measurement of attenuation/frequency distortion and adjustment of relative levels), the actual frequency should be 1020 Hz, +2 Hz, −7 Hz in accordance with Recommendation O.6.

For an interim period Administrations may, for practical reasons, need to use a reference frequency of nominally 800 kHz.

2 Adjustment of actual relative levels

2.1 The gain of the encoding side should be adjusted by connecting its output to a standard digital analyzer and applying a sine-wave signal at a nominal frequency of 1020 Hz at a level of 0 dBm0 to the voice-frequency input. The adjustment should result in an output level of 0 dBm0 ± 0.4 dB and should be made under typical conditions of power supply voltage, humidity and temperature.

The load capacity of the encoding side may be checked by applying a sine-wave signal at a frequency of 1020 Hz at its voice-frequency input. The level of this signal should be initially well below T_{max} and should then be slowly increased. The input level should be measured at which the first occurence is observed of the character signal corresponding to the extreme quantizing interval for both positive and negative values. T_{max} is taken as being 0.3 dB greater than the measured input level.

This method allows T_{max} to be checked for both positive and negative amplitudes and the values thus obtained should be within 0.4 dB of the theoretical load capacity (i.e. +3.14 dBm0 for the A-law or +3.17 dBm0 for the μ-law).

2.2 The decoding side should be adjusted to conform with § 4 of Recommendation G.711 within a tolerance of ± 0.4 dB.

3 Short-term and long-term variation of loss with time

3.1 When a sine-wave signal at a nominal frequency of 1020 Hz and at a level of −10 dBm0 (preferred value; however, a level of 0 dBm0 may be used) is applied to any voice-frequency input, the level measured at the corresponding time slot output of a standard digital analyzer should not vary by more than ± 0.1 dB during any 10-minute interval of typical operation nor by more than ± 0.3 dB during any one year under the permitted variations in the power supply voltage and temperature.

3.2 When a digitally simulated sine-wave signal at a frequency of 1020 Hz and at a level of -10 dBm0 (preferred value; however the 0 dBm0 sequence of Recommendation G.711, Tables 5/G.711 and 6/G.711 may be used) is applied to any channel time slot at the decoder input, the level measured at the corresponding voice-frequency output should not vary by more than ±0.1 dB during any 10-minute interval of typical operation, nor by more than ±0.3 dB during any one year under the permitted variations in the power supply voltage and temperature.

4 Impedance of voice-frequency ports

4.1 *Nominal impedance*

No single value of impedance is recommended.

The most widely used value of nominal impedance at 2-wire audio input and outputs ports is 600 ohms resistive (balanced). Some Administrations adopt values of 600 ohms + 2.16 μF or 900 ohms + 2.16 μF, and one Administration uses 900 ohms resistive, the latter representing a compromise value suitable for loaded and unloaded cables.

Note – Some examples of complex impedances used in connection with subscriber lines can be found in Recommendation Q.552, § 2.2.1.

4.2 *Return loss*

The return loss, measured against the nominal impedance, should meet the limits given in Table 1/G.715.

TABLE 1/G.715

Frequency range (Hz)	Return loss (dB)
300 to 600	> 12
600 to 3400	> 15

Note – Reflections due to impedance and balance impedance mismatches at 2-wire/4-wire interfaces may cause severe sidetone and echo problems in the network. Administrations need to adopt a suitable impedance strategy, including tolerances, to ensure an adequate transmission quality. (For further information, see Recommendation G.121 § 5, and Supplement 10 of Volume VI.)

5 Longitudinal balance

The longitudinal balance parameters referred to below are defined in Recommendation O.9 which also gives some information about the requirements of test circuits (Note 1). The value of Z in the driving test circuit should be 750 ohms ± 20%.

a) The longitudinal conversion loss (see RecommendationO.9, § 2.1) as measured at the input port of the encoding side should not be less than the limits shown in Figure 1/G.715.

b) The longitudinal conversion loss (see Recommendation O.9, § 2.1) as measured at the output port of the decoding side should not be less than the limits shown in Figure 1/G.715.

Note 1 – Attention is drawn to Recommendation 0.9, § 3, which shows the equivalence between a number of different test driving circuits and also includes information concerning the inherent balance requirements of the test bridge.

Note 2 – Attention is drawn to the fact that these values represent minimum requirements. The magnitude of potential longitudinal signal voltages depends, for example, on system use, the system environment, the location of hybrid transformers and attenuators, and may therefore vary for different Administrations. Some Administrations have found it necessary to specify higher values for longitudinal conversion loss to ensure that transverse voltages caused by possible longitudinal signal voltages are sufficiently small.

Note 3 – The possible need to introduce limits for frequencies below 300 Hz, in particular at 50 or 60 Hz, is under study. Overall rejection of longitudinal interference can be achieved by a combination of good longitudinal balancing and high filtering (see § 11.2).

Note 4 – The measurements should be made selectively.

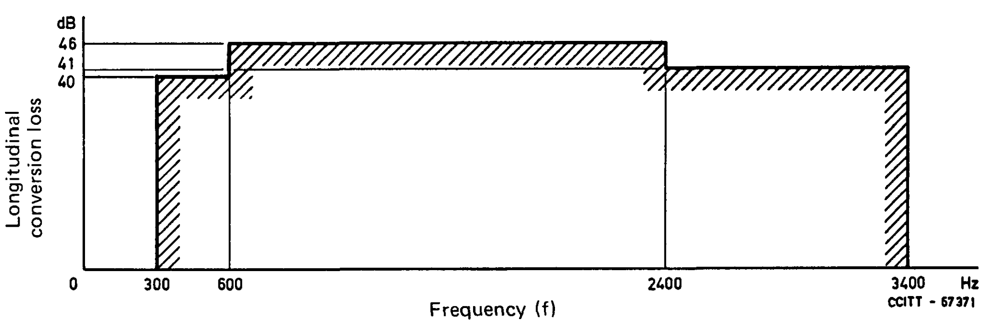


FIGURE 1/G.715

Longitudinal balance

6 Relative levels at voice-frequency ports

Due to differences in network transmission plans and equipment utilization, Administrations have differing requirements for the range of relative levels to be provided. It would appear that the following ranges would encompass the requirements of a large number of Administrations:

– input level (encoding side) 0 to –5 dBr in 0.5 dB steps;

– output level (decoding side) –2 to –7.5 dBr in 0.5 dB steps.

It has been recognized that it is not necessarily appropriate for a particular design of equipment to be capable of operating over the entire range.

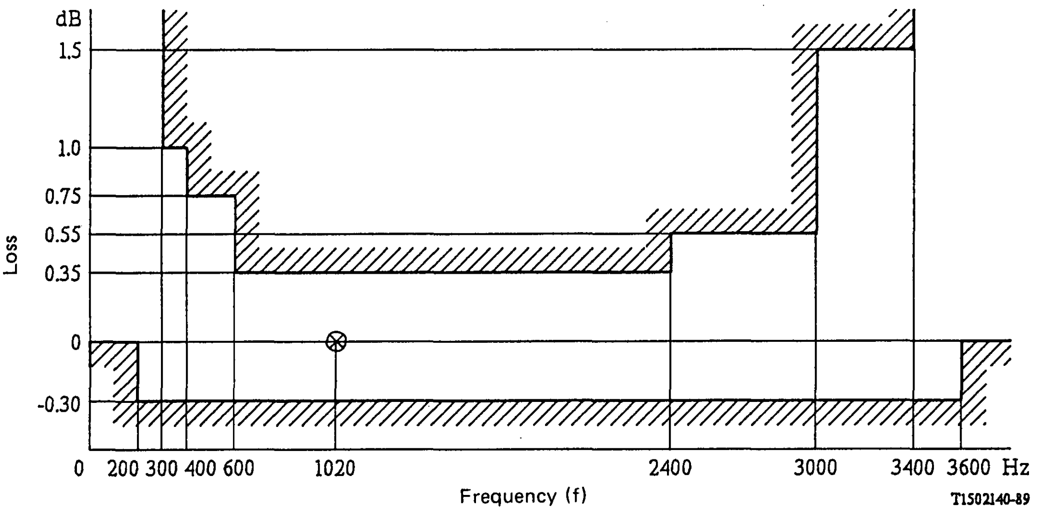
Note – The requirements in this section are different from the requirements in Recommendation Q.552, § 2.1.4.

7 Attenuation/frequency distortion of the encoding or the decoding side

The variations with frequency of the attenuation of any channel should be within the limits shown in the mask of Figure 2/G.715.

The nominal reference frequency is 1020 Hz.

The preferred input power level is −10 dBm0, in accordance with Recommendation O.6. As an alternative, a level of 0 dBm0 may be used if complex nominal impedances are used. The measuring method to be applied is described in Recommendation Q.551, § 1.2.5 and in Annex A to Recommendation G.121.



Note — Some Administrations apply a limit of 0.5 dB maximum loss for the frequency range 300 to 3000 Hz.

FIGURE 2/G.715

Attenuation/frequency distortion

8 Group delay

Note – The following are design objectives only. It does not seem necessary to define special test equipment to make these measurements between the voice-frequency input and the digital output and between the digital input and the voice-frequency output.

8.1 *Absolute group delay*

8.1.1 Absolute group delay of the encoding side at the frequency of minimum group delay should not exceed 450 microseconds.

8.1.2 The absolute group delay of the decoding side at the frequency of minimum group delay should not exceed 300 microseconds.

8.2 *Group delay distortion with frequency of the encoding or decoding side*

The group delay distortion should lie within the limits shown in the mask of Figure 3/G.715.

The minimum value of group delay for each side is taken as the reference for the group delay distortion.

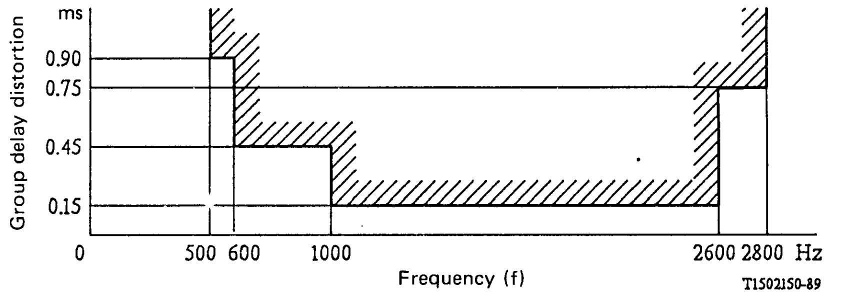


FIGURE 3/G.715

Group delay distortion with frequency

8.3 *Input level*

The requirements of § 8.1 and § 8.2 above should be met at an input power level of −10 dBm0 (preferred value; however, 0 dBm0 may be used) in accordance with Recommendation O.6.

9 Weighted noise measured at the encoding side

With the input ports of the channel terminated in the nominal impedance, the idle channel noise should not exceed −66 dBm0p.

10 Weighted noise measured at the decoding side

Noise contributed by the decoding equipment alone should be less than −75 dBm0p when its input is driven by a PCM signal (quiet code) corresponding to the decoder output value number 0 for the μ-law or decoder output value number 1 for the A-law.

11 Discrimination against out-of-band input signals (only applicable to encoding side)

11.1 *Input signal above 4.6 kHz*

With any sine-wave signal in the range from 4.6 kHz to X kHz applied to the input port of the channel at a suitable level, the level of any image frequency produced in the time slot corresponding to the channel should, as a minimum requirement, be at least 25 dB below the level of the test signal.

Note – It has been found that a suitable test level is −25 dBm0. The value X is under study, but it should be at least 150 kHz.

11.2 *Signal below 300 Hz*

No particular value is recommended.

Note 1 – While some Administrations have no particular requirement in this respect, some other Administrations have found it necessary to provide at least 20 to 26 dB rejection at the encoding side at frequencies across the band 15-60 Hz.

Note 2 – Overall rejection of longitudinal interference can be achieved by a combination of good longitudinal balancing (see § 5) and high pass filtering.

12 Spurious out-of-band signals at channel output (only applicable to decoding side)

With a digitally simulated sine-wave signal in the frequency range 300-3400 Hz and at a level of 0 dBm0 applied to a channel time slot at the decoder input, the level of spurious out-of-band image signals measured selectively at the output port should as a minimum requirement be lower than −25 dBm0.

Note – Attention is drawn to the importance of the attenuation characteristic in the range 3400 to 4600 Hz. Although other attenuation characteristics can satisfy the above requirement, the filter template of Figure 4/G.713 gives adequate protection against out-of-band signals.

13 Single frequency noise from the encoding or decoding side

The level of any single frequency (in particular for the decoding side at the sampling frequency and its multiples) measured selectively, should not exceed −50 dBm0.

14 Total distortion, including quantizing distortion

Two alternative methods are recommended. It should be noted that the two test methods are not exactly equivalent. The noise test method (Method 1) gives fairly smooth curves. The sine-wave method (Method 2) can be more sensitive in identifying possible localized codec imperfections. Thus the two methods respond to practical codec impairments in slightly different ways.

Note 1 – Some Administrations have taken the position that the requirements of both test methods should be met. Other Administrations are of the opinion that meeting the requirements of either test method is sufficient to meet network performance requirements. In practice, Administrations may choose to use only one method in production testing and operational situations.

Note 2 – There is a slight possibility that an adverse combination of encoding and decoding sides might not meet the overall requirements of Recommendation G.713. To minimize this possibility some Administrations suggested that encoding and decoding sides of the same design should always meet the overall requirements of Recommendation G.713.

Note 3 – The limits for Methods 1 and 2 do not include any allowance for additional noise which might be present when signalling takes place on the two wires. The derivation of limits for this case, taking account of the philosophy adopted in Recommendation Q.551, is under study.

14.1 *Method 1* (encoding side)

With a noise signal corresponding to Recommendation O.131 applied to the input port of a channel, the ratio of signal-to-total distortion power should lie above the limits shown in Figure 4a/G.715.

14.2 *Method 1* (decoding side)

With a digitally simulated noise signal corresponding to Recommendation O.131 applied to the time slot of any telephone channel, the ratio of signal-to-total distortion power should lie above the limits shown in Figure 4b/G.715.

The value in the mask includes the distortion power of an ideal encoder.

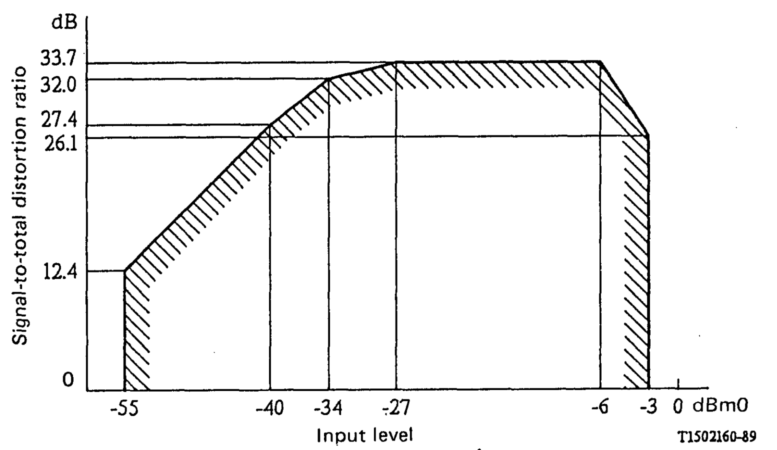


FIGURE 4a/G.715

Signal-to-total distortion ratio as function of input level (Method 1), encoding side

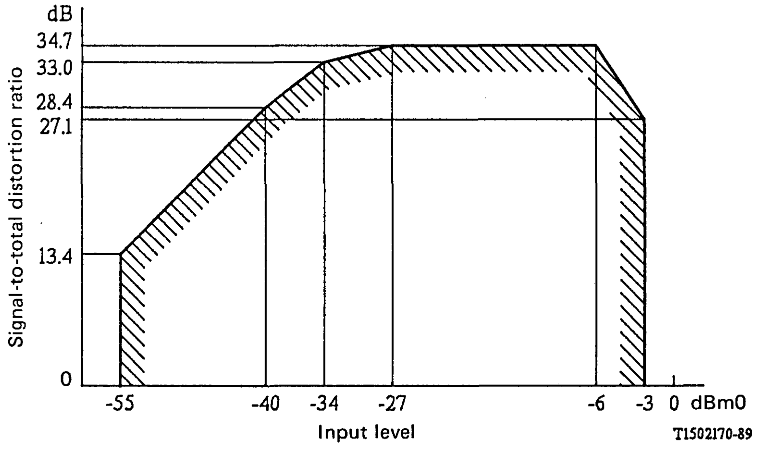


FIGURE 4b/G.715

Signal-to-total distortion ratio as a function of the input level (Method 1), decoding side

14.3 *Method 2* (encoding side)

With a sine-wave signal at a nominal frequency of 1020 Hz (preferred value) or 820 Hz (see Recommendation O.132) applied to the input port of a channel, the ratio of signal-to-total distortion power measured with the proper noise weighting (see Table 4/G.223) should lie above the limits shown in Figure 5/G.715.

14.4 *Method 2* (decoding side)

With a digitally simulated sine-wave signal at a nominal frequency of 1020 Hz (preferred value) or 820 Hz (see Recommendation O.132) applied to the time slot of any channel, the ratio of signal-to-total distortion power measured with the proper noise weighting (see Table 4/G.223) should lie above the limits shown in Figure 5/G.715.

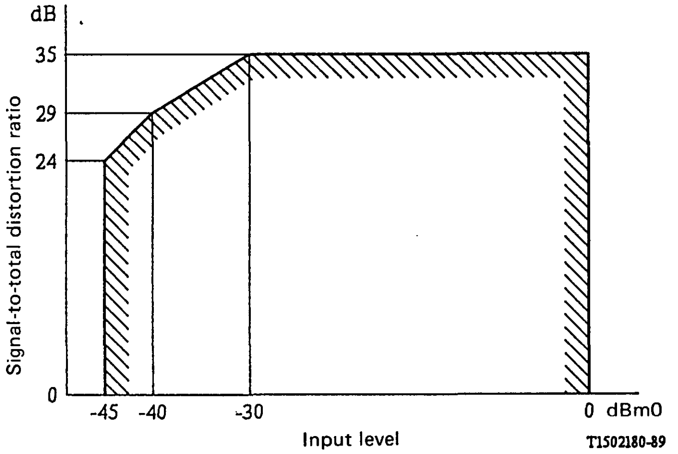


FIGURE 5/G.715

Signal-to-total distortion ratio as a function of the input level (Method 2)

15 Variation of gain with input level

Two alternative methods are recommended (see comments in § 14).

Note – There is a slight possibility that an adverse combination of encoding and decoding sides might not meet the overall requirements of Recommendation G.713. To minimize this possibility encoding and decoding sides of the same design should always meet the overall requirements of Recommendation G.713.

15.1 *Method 1* (encoding side)

With a band limited noise signal as defined in Recommendation O.131, applied to the input port of any channel at a level between –55 dBm0 and –10 dBm0, the gain variation of that channel, relative to the gain at an input level of –10 dBm0, should lie within the limits of Figure 6a/G.715. The measurement should be limited to the frequency band 350 to 550 Hz in accordance with the filter characteristics defined in Recommendation O.131, § 3.2.1.

Furthermore, with a sine-wave signal in the frequency range 700 to 1100 Hz applied to the input port of any channel at a level between –10 dBm0 and +3 dBm0, the gain variation of that channel, relative to the gain at an input level of –10 dBm0 should lie within the limits of Figure 6b/G.715. The measurement should be made selectively.

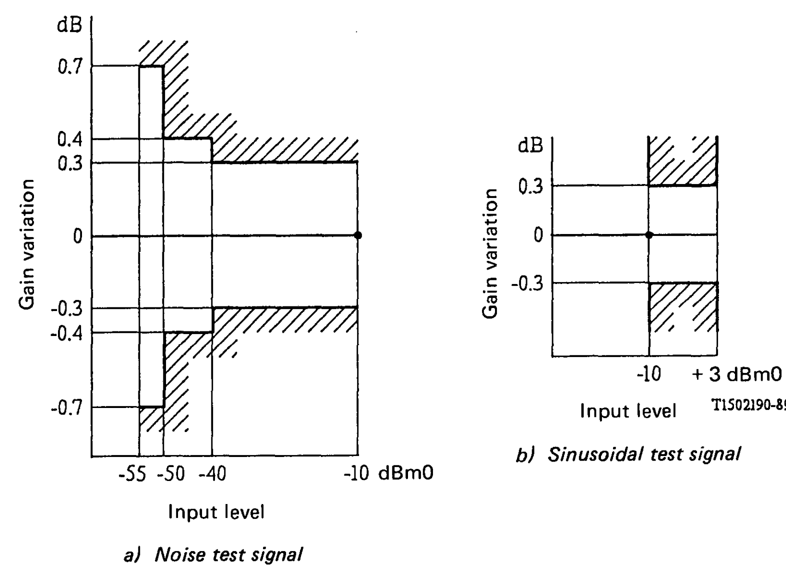


FIGURE 6/G.715

Variation of gain with input level (Method 1)

15.2 *Method 1* (decoding side)

With a digitally simulated band limited noise signal, corresponding to Recommendation O.131, applied to the time slot of any telephone channel at a level between –55 and –10 dBm0, the gain variation of that channel, relative to the gain at an input level of –10 dBm0, should lie within the limits of Figure 6a/G.715. The measurements should be limited to the frequency band 350 to 550 Hz in accordance with the filter characteristics defined in Recommendation O.131, § 3.2.1.

Furthermore, with a digitally simulated sine-wave signal in the frequency range 700 to 1100 Hz applied to the time slot of any telephone channel at a level between –10 dBm0 and +3 dBm0, the gain variation of that channel, relative to the gain at an input level of –10 dBm0, should lie within the limits of Figure 6b/G.715. The measurement should be made selectively.

15.3 *Method 2* (encoding side)

With a sine-wave signal in the frequency range 700 to 1100 Hz applied to the input port of any channel at a level between −55 dBm0 and +3 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits given in Figure 7/G.715. The measurement should be made selectively.

15.4 *Method 2* (decoding side)

With a digitally simulated sine-wave signal in the frequency range 700 to 1100 Hz applied to the time slot of any telephone channel at a level between −55 dBm0 and +3 dBm0, the gain variation of that channel, relative to the gain at an input level of −10 dBm0, should lie within the limits given in Figure 7/G.715. The measurement should be made selectively.

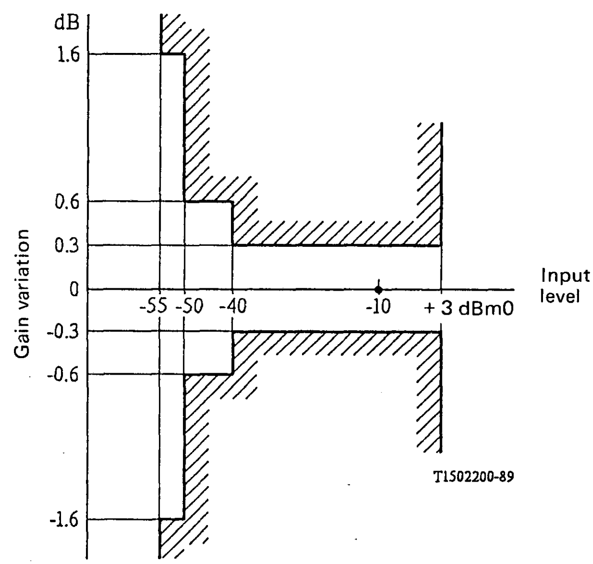


FIGURE 7/G.715

Variation of gain with input level (Method 2)

16 Crosstalk measurements with sine-wave signals

16.1 *General*

For the crosstalk measurements, auxillary signals are injected as indicated in Figures 8/G.715 and 9/G.715. These signals are:

- the quiet code, i.e. a PCM signal corresponding to decoder output value number 0 (μ-law) or output value number 1 (A-law) (with the sign bit in a fixed state);
- a low level activating signal. Suitable activating signals are, for example, a band-limited noise signal (see Recommendation O.131), at a level in the range −50 to −60 dBm0 or a sine-wave signal at a level in the range from −33 to −40 dBm0. Care must be taken in the choice of frequency and the filtering characteristics of the measuring apparatus in order that the activating signal does not significantly affect the accuracy of the crosstalk measurement.

16.2 *Far-end and near-end crosstalk measured with analogue test signal*

The crosstalk between individual channels of a multiplex should be such that with a sine-wave signal in the frequency range 700 to 1100 Hz and at a level of 0 dBm0 applied to a voice-frequency input port, the crosstalk level produced in any other channel should not exceed −73 dBm0 for NEXT (near end crosstalk) and −70 dBm0 for FEXT (far-end crosstalk) (see Figure 8/G.715).

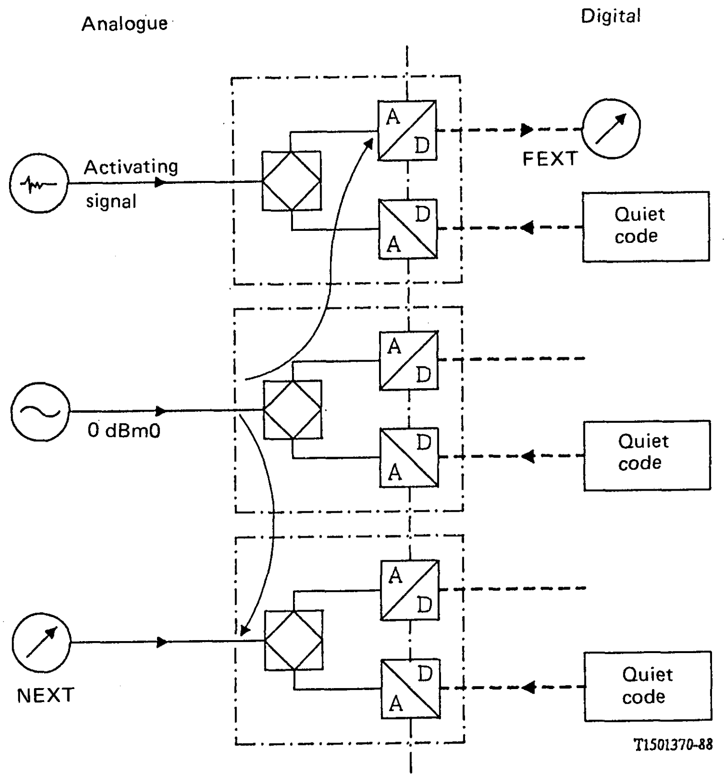


FIGURE 8/G.715

Measurements with analogue test signal between different channels

16.3 *Far-end and near-end crosstalk measured with digital test signal*

The crosstalk between individual channels of a multiplex should be such that with a digitally simulated sine-wave signal in the frequency range 700 to 1100 Hz and at a level of 0 dBm0 applied to the digital input, the crosstalk level received in any other channel should not exceed −70 dBm0 for NEXT and −73 dBm0 for FEXT (see Figure 9/G.715).

17 Echo and stability

17.1 *Terminal balance return loss (TBRL)*

This quantity characterizes the equipment performance required to comply with the network performance objective of Recommendation G.122 in respect of echo. The TBRL is defined as the balance return loss (see definition in Recommendation Q.552, § 3.1.8.1) measured against a balance test network. It is related to the half-loop loss (HLL), i.e., the loss between the digital test input point, T_i and the digital test output point, T_o (see Figure 10/G.715) as follows:

$$\text{HLL} = T_i \text{ to } T_o \text{ loss} = P_i + P_o + \text{TBRL (dB)}$$

where P_i and P_o are the measured values of loss in the equivalent circuit of Figure 10/G.715 which represent all the loss between the digital test point and the 2-wire port, or conversely at the measurement frequency.

The TBRL should be measured in the arrangement of Figure 10/G.715 with a sinusoidal test signal at frequencies across the telephone band covering the bandwidth 300 to 3400 Hz.

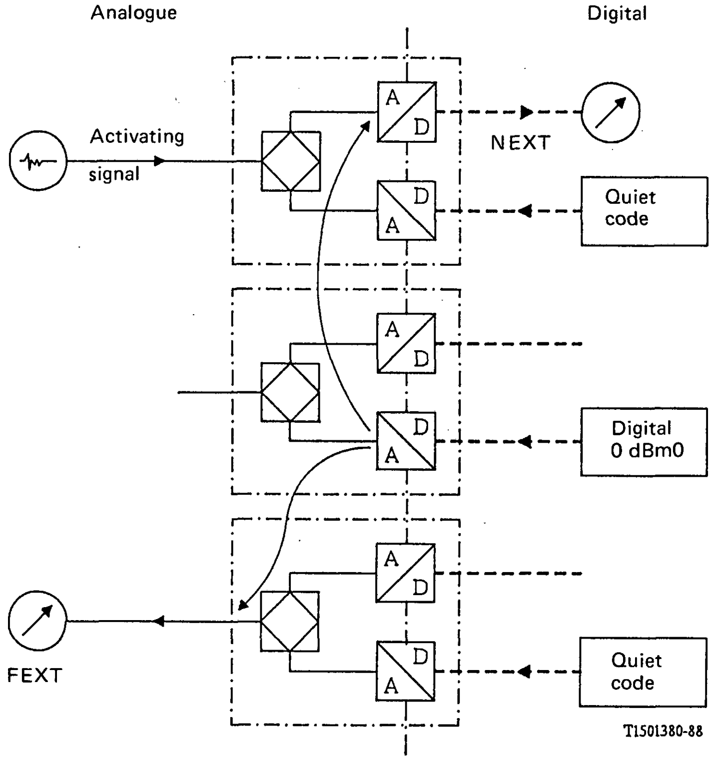


FIGURE 9/G.715

Measurements with digital test signal between different channels

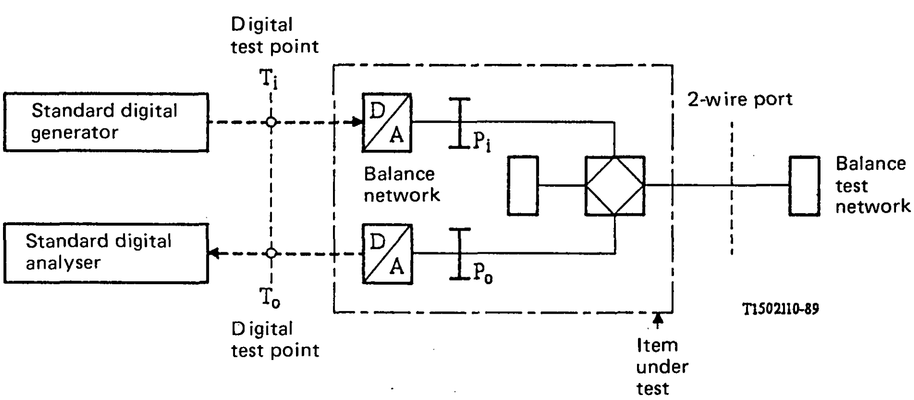


FIGURE 10/G.715

Arrangement for measuring half-loop loss

Values for the nominal balance impedance and for the maximum deviation of this impedance from the nominal value, differ from one Administration to another. The range of impedances presented at the 2-wire port during normal operation also varies considerably. Administrations will need to establish their own requirements for TBRL taking account of national or international transmission plans. As a minimum requirement, the TBRL limits shown in Figure 11/G.715 should be met when the 2-wire port is terminated with a balance test network which is representative of the impedance conditions expected in the speaking condition from a population of 2-wire trunks connected to the PCM muldex. The limits are provisional.

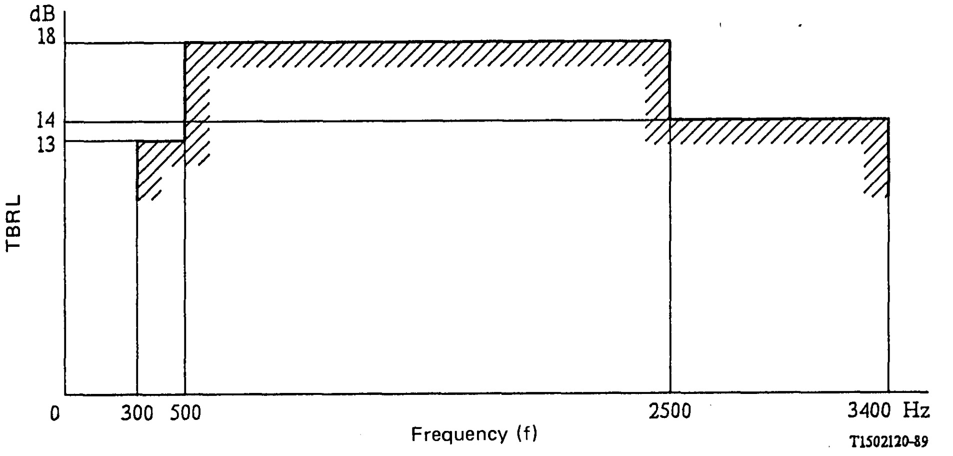


FIGURE 11/G.715

Minimum values of terminal balance return loss (provisional)

17.2 *Stability loss (SL)*

The stability loss is defined as the minimum value of the half-loop loss measured in the arrangement of Figure 10/G.715. The stability loss should be measured between T_i and T_o by terminating the 2-wire port with stability test networks representing the worst-case terminating condition encountered in normal operation. Some Administrations may find that open circuit and short circuit terminations are sufficiently representative of worst-case conditions. Other Administrations may need to specify, for example, an inductive termination to represent that worst-case condition.

The stability loss at any frequency can be expressed as follows:

$$\mathrm{SL} \geqslant P_i + P_o - X \, \mathrm{dB}$$

where P_i and P_o are measured values of loss, at the measurement frequency, under normal terminating conditions at the 2-wire port. X is a factor dependent on the interaction between the 2-wire input impedance, the 2-wire balance impedance and the impedance actually applied at the 2-wire port. X can be computed or measured by the methods described in Recommendation Q.552.

The 2-wire input and balance impedances at a 2-wire/4-wire interface usually have to be optimized by Administrations with regard to echo and sidetone. The worst case terminations depend on the actual network conditions. Thus, the value of X is fully determined by network conditions and the impedance strategy. Values between 0 and 3 dB have been observed in practice.

Administrations should choose the nominal values of P_i and P_o taking account of the value of X for their particular operating conditions and of national and international transmission plans for overall network stability (see Recommendation G.122).

18 Interference from signalling

The characterization of such interference by separate measurements requires four different types of measurements, for crosstalk (see Figure 12/G.715). In each case the maximum level of interference in one channel should not exceed X dBm0p when signalling (10 Hz signal with a 50/50 duty ratio) is active simultaneously on all channels.

Note – The value of X is under study.

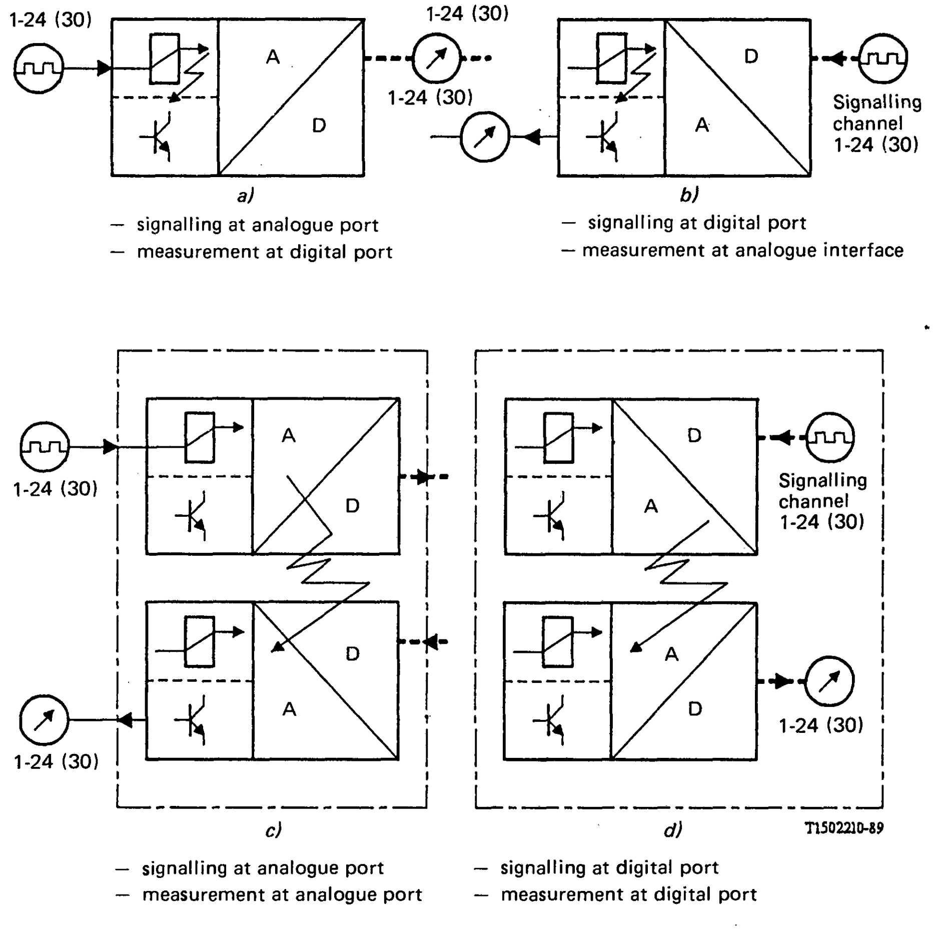


FIGURE 12/G.715

Measurement of signalling interference contributions

7.2 Coding of analogue signals by methods other than PCM

Recommendation G.721

32 kbit/s ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION (ADPCM)[1]

(Melbourne, 1988)

1 General

The characteristics below are recommended for the conversion of a 64 kbit/s A-law or μ-law PCM channel to and from a 32 kbit/s channel. The conversion is applied to the PCM bit stream using an ADPCM transcoding technique. The relationship between the voice frequency signals and the PCM encoding/decoding laws is fully specified in Recommendation G.711.

Paragraphs 1.1 and 1.2 of this Recommendation provide an outline description of the ADPCM transcoding algorithm, §§ 2 and 3 provide the principles and functional descriptions of the ADPCM encoding and decoding algorithms respectively, whilst § 4 is the precise specification for the algorithm computations. Networking aspects and digital test sequences are addressed in Apendices I and II respectively to this Recommendation.

Simplified block diagrams of both the ADPCM encoder and decoder are shown in Figure 1/G.721.

In § 4, each sub-block in the encoder and decoder is precisely defined using one particular logical sequence. If other methods of computation are used, extreme care should be taken to ensure that they yield *exactly* the same value for the output processing variables. Any further departures from the processes detailed in § 4 will incur performance penalties which may be severe.

Note 1 – For the time being, the 32 kbit/s ADPCM algorithm defined in this Recommendation is intended for transmission purposes since switching applications at this bit rate are a subject for further study by the CCITT.

Note 2 – Prior to the definition of this Recommendation, other 32 kbit/s ADPCM algorithms of similar performance have been incorporated in equipment designs and used in national telecommunications networks.

Note 3 – In the short term, due to the limited availability of 32 kbit/s ADPCM equipment, the use of 32 kbit/s ADPCM in the international network, when requested by one of the Administrations concerned, will require bilateral and/or multilateral agreement.

Note 4 – Signalling and multiplexing considerations are beyond the scope of this Recommendation (see for example Recommendation G.761).

1.1 *ADPCM encoder*

Subsequent to the conversion of the A-law or μ-law PCM input signal to uniform PCM, a difference signal is obtained, by subtracting an estimate of the input signal from the input signal itself. An adaptative 15-level quantizer is used to assign four binary digits to the value of the difference signal for transmission to the decoder. An inverse quantizer produces a quantized difference signal from these same four binary digits. The signal estimate is added to this quantized difference signal to produce the reconstructed version of the input signal. Both the reconstructed signal and the quantized difference signal are operated upon by an adaptive predictor which produces the estimate of the input signal, thereby completing the feedback loop.

[1] This Recommendation G.721 completely replaces the text of Recommendation G.721 published in Fascicle III.3 of the *Red Book*. It should be noted that systems designed in accordance with the present Recommendation will not be compatible with systems designed in accordance with the *Red Book* version.

1.2 *ADPCM decoder*

The decoder includes a structure identical to the feedback portion of the encoder, together with a uniform PCM to A-law or μ-law conversion and a synchronous coding adjustment.

The synchronous coding adjustment prevents cumulative distortion occurring on synchronous tandem codings (ADPCM-PCM-ADPCM, etc. digital connections) under certain conditions (see § 3.7). The synchronous coding adjustment is achieved by adjusting the PCM output codes in a manner which attempts to eliminate quantizing distortion in the next ADPCM encoding stage.

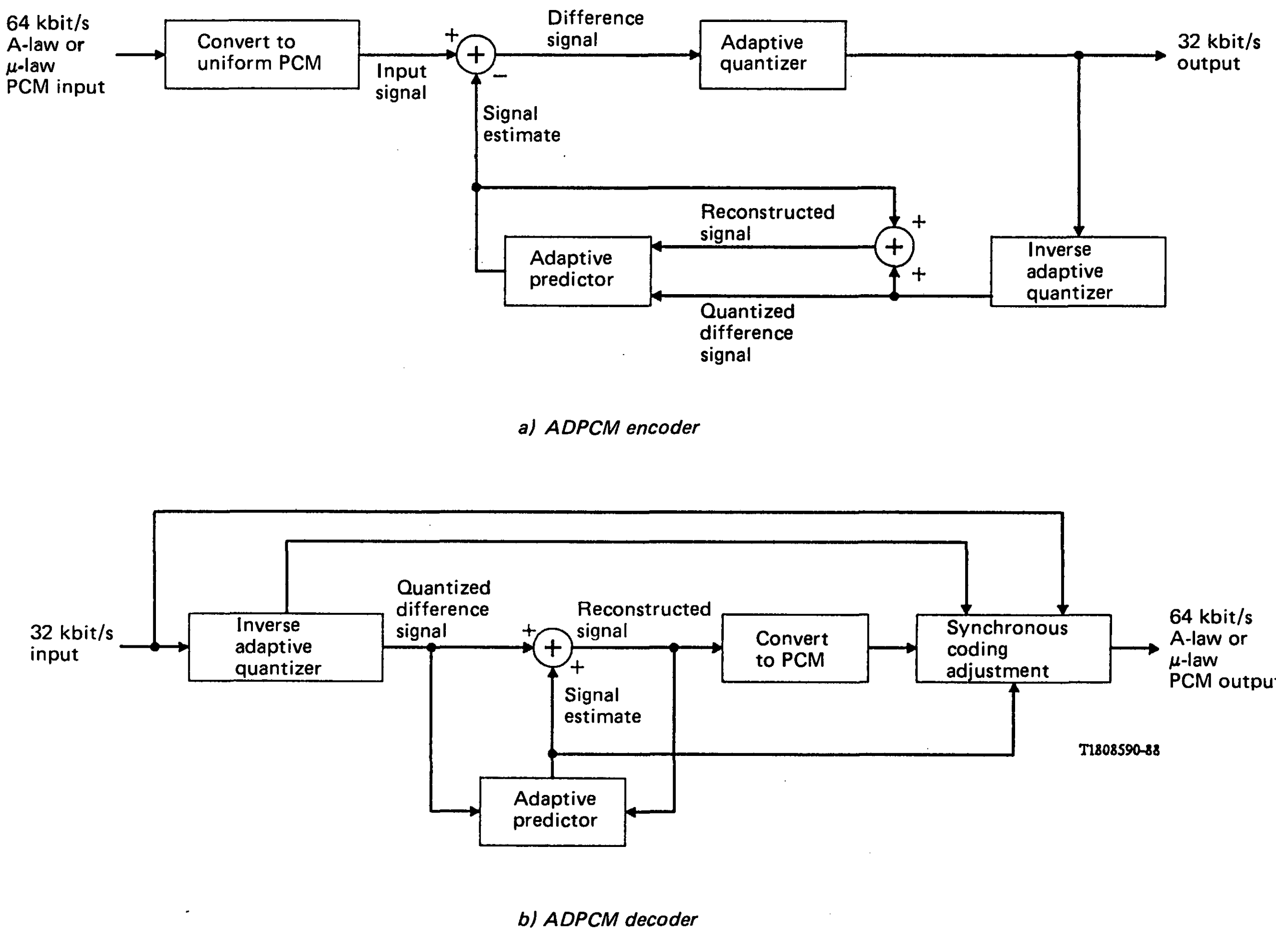


FIGURE 1/G.721

Simplified block diagrams

2 ADPCM encoder principles

Figure 2/G.721 is a block schematic of the encoder. For each variable to be described, k is the sampling index and samples are taken at 125 μs intervals. A fundamental description of each block is given below in §§ 2.1 to 2.8.

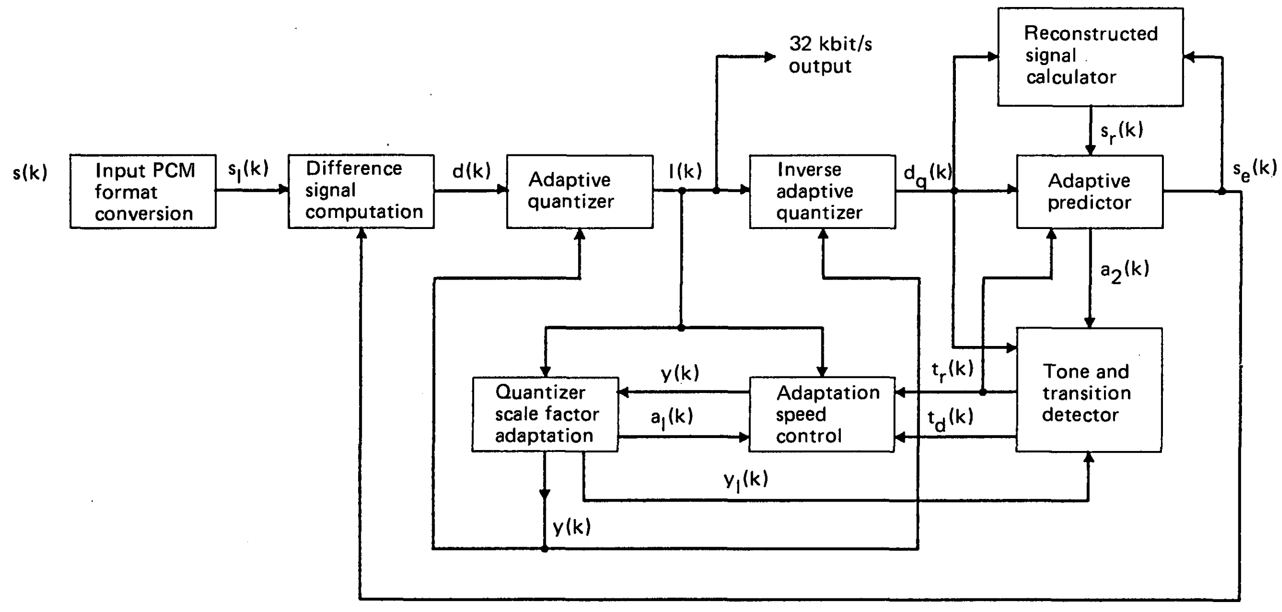


FIGURE 2/G.721

Encoder block schematic

2.1 *Input PCM format conversion*

This block converts the input signal $s(k)$ from A-law or μ-law PCM to a uniform PCM signal $s_l(k)$.

2.2 *Difference signal computation*

This block calculates the difference signal $d(k)$ from the uniform PCM signal $s_l(k)$ and the signal estimate $s_e(k)$:

$$d(k) = s_l(k) - s_e(k) \tag{2-1}$$

2.3 *Adaptive quantizer*

A 15-level non-uniform adaptive quantizer is used to quantize the difference signal $d(k)$. Prior to quantization, $d(k)$ is converted to a base 2 logarithmic representation and scaled by $y(k)$ which is computed by the scale factor adaptation block. The normalized input/output characteristic (infinite precision values) of the quantizer is given in Table 1/G.721. Four binary digits are used to specify the quantized level representing $d(k)$ (three for the magnitude and one for the sign). The 4-bit quantizer output $I(k)$ forms the 32 kbit/s output signal; it is also fed to the inverse adaptive quantizer, the adaptation speed control and the quantizer scale factor adaptation blocks.

2.4 *Inverse adaptive quantizer*

A quantized version $d_q(k)$ of the difference signal is produced by scaling, using $y(k)$, specific values selected from the normalized quantizing characteristic given in Table 1/G.721 and then transforming the result from the logarithmic domain.

TABLE 1/G.721

Quantizer normalized input/output characteristic

Normalized quantizer input range $\log_2\lvert d(k)\rvert - y(k)$	$\lvert I(k)\rvert$	Normalized quantizer output $\log_2\lvert d_q(k)\rvert - y(k)$
[3.12, $+\infty$)	7	3.32
[2.72, 3.12)	6	2.91
[2.34, 2.72)	5	2.52
[1.91, 2.34)	4	2.13
[1.38, 1.91)	3	1.66
[0.62, 1.38)	2	1.05
[-0.98, 0.62)	1	0.031
($-\infty$, -0.98)	0	$-\infty$

Note – The convention used here is that "[" indicates that the endpoint value is included in the range, ")" indicates that the endpoint value is excluded from the range.

2.5 *Quantizer scale factor adaptation*

This block computes $y(k)$, the scaling factor for the quantizer and the inverse quantizer. The inputs are the 4-bit quantizer output $I(k)$ and the adaptation speed control parameter $a_l(k)$.

The basic principle used in scaling the quantizer is bimodal adaptation:

– fast for signals (e.g. speech) that produce difference signals with large fluctuations;

– slow for signals (e.g. voiceband data, tones) that produce difference signals with small fluctuations.

The speed of adaptation is controlled by a combination of fast and slow scale factors.

The fast (unlocked) scale factor $y_u(k)$ is recursively computed in the base 2 logarithmic domain from the resultant logarithmic scale factor $y(k)$:

$$y_u(k) = (1 - 2^{-5})y(k) + 2^{-5}W[I(k)], \qquad (2\text{-}2)$$

where $y_u(k)$ is limited by $1.06 \leqslant y_u(k) \leqslant 10.00$.

The discrete function $W(I)$ is defined as follows (infinite precision values):

|I(k)|	7	6	5	4	3	2	1	0
W(I)	70.13	22.19	12.38	7.00	4.00	2.56	1.13	−0.75

The factor $(1 - 2^{-5})$ introduces finite memory into the adaptive process so that the states of the encoder and decoder converge following transmission errors.

The slow (locked) scale factor $y_l(k)$ is derived from $y_u(k)$ with a low pass filter operation:

$$y_l(k) = (1 - 2^{-6})y_l(k - 1) + 2^{-6}y_u(k) \tag{2-3}$$

The fast and slow scale factors are then combined to form the resultant scale factor:

$$y(k) = a_l(k)y_u(k - 1) + [1 - a_l(k)]y_l(k - 1), \tag{2-4}$$

where $0 \leqslant a_l(k) \leqslant 1$ (see § 2.6).

2.6 *Adaptation speed control*

The controlling parameter $a_l(k)$ can assume values in the range [0, 1]. It tends towards unity for speech signals and towards zero for voiceband data signals and tones. It is derived from a measure of the rate-of-change of the difference signal values.

Two measures of the average magnitude of $I(k)$ are computed:

$$d_{ms}(k) = (1 - 2^{-5})d_{ms}(k - 1) + 2^{-5}F[I(k)], \tag{2-5}$$

and

$$d_{ml}(k) = (1 - 2^{-7})d_{ml}(k - 1) + 2^{-7}F[I(k)], \tag{2-6}$$

where $F[I(k)]$ is defined by

|I(k)|	7	6	5	4	3	2	1	0
F[I(k)]	7	3	1	1	1	0	0	0

$d_{ms}(k)$ is thus a relatively short term average of $F[I(k)]$ and $d_{ml}(k)$ is a relatively long term average of $F[I(k)]$.

Using these two averages, the variable $a_p(k)$ is defined:

$$a_p(k) = \begin{cases} (1 - 2^{-4})a_p(k - 1) + 2^{-3}, & \text{if } \left|d_{ms}(k) - d_{ml}(k)\right| \geqslant 2^{-3}d_{ml}(k) \\ (1 - 2^{-4})a_p(k - 1) + 2^{-3}, & \text{if } y(k) < 3 \\ (1 - 2^{-4})a_p(k - 1) + 2^{-3}, & \text{if } t_d(k) = 1 \\ 1, \text{ if } t_r(k) = 1 & \\ (1 - 2^{-4})a_p(k - 1), & \text{otherwise} \end{cases} \tag{2-7}$$

Thus, $a_p(k)$ tends towards the value 2 if the difference between $d_{ms}(k)$ and $d_{ml}(k)$ is large (average magnitude of $I(k)$ changing) and $a_p(k)$ tends towards the value 0 if the difference is small (average magnitude of $I(k)$ relatively constant). $a_p(k)$ also tends towards 2 for an idle channel (indicated by $y(k) < 3$) or partial band signals (indicated by $t_d(k) = 1$ as described in § 2.8). Note that $a_p(k)$ is set to 1 upon detection of a partial band signal transition (indicated by $t_r(k) = 1$, see § 2.8).

$a_p(k - 1)$ is then limited to yield $a_l(k)$ used in Equation (2-4) above:

$$a_l(k) = \begin{cases} 1, & a_p(k - 1) > 1 \\ a_p(k - 1), & a_p(k - 1) \leqslant 1 \end{cases} \tag{2-8}$$

This asymmetrical limiting has the effect of delaying the start of a fast to slow state transition until the absolute value of $I(k)$ remains constant for some time. This tends to eliminate premature transitions for pulsed input signals such as switched carrier voiceband data.

2.7 *Adaptive predictor and reconstructed signal calculator*

The primary function of the adaptive predictor is to compute the signal estimate $s_e(k)$ from the quantized difference signal $d_q(k)$. Two adaptive predictor structures are used, a sixth order section that models zeros and a second order section that models poles in the input signal. This dual structure effectively caters for the variety of input signals which might be encountered.

The signal estimate is computed by:

$$s_e(k) = \sum_{i=1}^{2} a_i(k-1)s_r(k-i) + s_{ez}(k), \tag{2-9}$$

where $s_{ez}(k) = \sum_{i=1}^{6} b_i(k-1)d_q(k-i)$,

and the reconstructed signal is defined as

$$s_r(k-i) = s_e(k-i) + d_q(k-i).$$

Both sets of predictor coefficients are updated using a simplified gradient algorithm:

for the second order predictor:

$$a_1(k) = (1-2^{-8})a_1(k-1) + (3 \cdot 2^{-8})\,\mathrm{sgn}\,[p(k)]\,\mathrm{sgn}\,[p(k-1)], \tag{2-10}$$

$$a_2(k) = (1-2^{-7})a_2(k-1) + 2^{-7}\{\mathrm{sgn}\,[p(k)]\,\mathrm{sgn}\,[p(k-2)] - f[a_1(k-1)]\,\mathrm{sgn}\,[p(k)]\,\mathrm{sgn}\,[p(k-1)]\}, \tag{2-11}$$

where $p(k) = d_q(k) + s_{ez}(k)$,

$$f(a_1) = \begin{cases} 4a_1, & |a_1| \leqslant 2^{-1} \\ 2\,\mathrm{sgn}\,(a_1), & |a_1| > 2^{-1}, \end{cases}$$

and sgn [0] $= 1$, except sgn $[p(k-i]$ is defined to be 0 only if $p(k-i) = 0$ and $i = 0$;

with the stability constraints:

$$|a_2(k)| \leqslant 0.75 \text{ and } |a_1(k)| \leqslant 1 - 2^{-4} - a_2(k).$$

If $t_r(k) = 1$ (see § 2.8), then $a_1(k) = a_2(k) = 0$.

For the sixth order predictor:

$$b_i(k) = (1-2^{-8})b_i(k-1) + 2^{-7}\,\mathrm{sgn}\,[d_q(k)]\,\mathrm{sgn}\,[d_q(k-i)], \tag{2-12}$$

for $i = 1, 2, \ldots, 6$.

If $t_r(k) = 1$ (see § 2.8), then $b_1(k) = b_2(k) = \ldots = b_6(k) = 0$.

As above, sgn [0] $= 1$, except sgn $[d_q(k-1)]$ is defined to be 0 only if $d_q(k-1) = 0$ and $i = 0$. Note that $b_i(k)$ is implicitly limited to $\pm$ 2.

2.8 *Tone and transition detector*

In order to improve performance for signals originating from FSK modems operationg in the character mode, a two-step detection process is defined. First, partial band signal (e.g. tone) detection is invoked so that the quantizer can be driven into the fast mode of adaptation:

$$t_d(k) = \begin{cases} 1, \; a_2(k) < -0.71875 \\ 0, \text{ otherwise.} \end{cases} \tag{2-13}$$

In addition, a transition from a partial band signal is defined so that the predictor coefficients can be set to zero and the quantizer can be forced into the fast mode of adaptation:

$$t_r(k) = \begin{cases} 1, \ a_2(k) < -0.71875 \text{ and } |d_q(k)| > 24 \cdot 2^{y_l(k)} \\ 0, \text{ otherwise.} \end{cases} \tag{2-14}$$

3 ADPCM decoder principles

Figure 3/G.721 is a block schematic of the decoder. A functional description of each block is given in §§ 3.1 to 3.7 below.

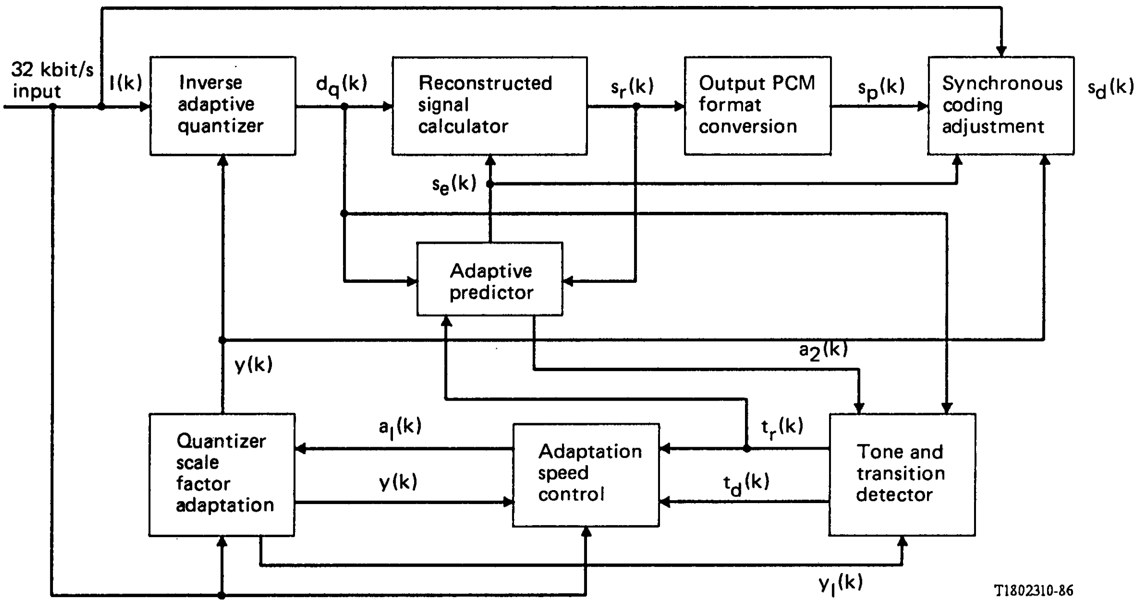


FIGURE 3/G.721

Decoder block schematic

3.1 *Inverse adaptive quantizer*

The function of this block is described in § 2.4.

3.2 *Quantizer scale factor adaptation*

The function of this block is described in § 2.5.

3.3 *Adaptation speed control*

The function of this block is described in § 2.6.

3.4 *Adaptive predictor and reconstructed signal calculator*

The functions of this block are described in § 2.7.

3.5 *Tone and transition detector*

The function of this block is described in § 2.8.

3.6 *Output PCM format conversion*

This block converts the reconstructed uniform PCM signal $s_r(k)$ into either an A-law or μ-law PCM signal $s_p(k)$ as required.

3.7 *Synchronous coding adjustment*

The synchronous coding adjustment prevents cumulative distortion occurring on synchronous tandem codings (ADPCM-PCM-ADPCM, etc. digital connections), when:

i) the transmission of the 32 kbit/s ADPCM and the intermediate 64 kbit/s PCM signals is error free, and,

ii) the 32 kbit/s ADPCM and intermediate 64 kbit/s PCM bit streams are not disturbed by digital signal processing devices.

If the coder and decoder have different initial conditions, as may occur after switching for example, then the synchronous tandeming property may take time to establish. Furthermore, if this property is disturbed or not acquired initially then it may be recovered for those signals of sufficient level with spectra that occupy the majority of the 200-3400 Hz band (e.g. speech, 4800 bit/s voiceband data).

When a decoder is synchronously connected to an encoder, the synchronous coding adjustment block estimates quantization in the encoder. If all state variables in both the decoder and the encoder have identical values and there are no transmission errors, the forced equivalence of both 4-bit quantizer output sequences for all values of k guarantees the property of non-accumulation of distortion.

This is accomplished by first converting the A-law or μ-law signal $s_p(k)$ to a uniform PCM signal $s_{lx}(k)$ and then computing a difference signal $d_x(k)$:

$$d_x(k) = s_{lx}(k) - s_e(k) \tag{3-1}$$

The difference signal $d_x(k)$ is then compared to the ADPCM quantizer decision interval determined by $I(k)$ and $y(k)$. The signal $s_d(k)$ is then defined as follows:

$$s_d(k) = \begin{cases} s_p^+(k), \ d_x(k) < \text{lower interval boundary} \\ s_p^-(k), \ d_x(k) \geqslant \text{upper interval boundary} \\ s_p(k), \ \text{otherwise} \end{cases} \tag{3-2}$$

where

$s_d(k)$: the output PCM code word of the decoder,

$s_p^+(k)$: the PCM code word that represents the next more positive PCM output level (when $s_p(k)$ represents the most positive output level, then $s_p^+(k)$ is constrained to be the value $s_p(k)$),

$s_p^-(k)$: the PCM code word that represents the next more negative PCM output level (when $s_p(k)$ represents the most negative output level, then $s_p^-(k)$ is constrained to be the value $s_p(k)$).

4 Computational details

Paragraphs 4.1 and 4.2 provide the computational details for each of the encoder and decoder elements.

Proper timing for the encoder and decoder is obtained by executing all of the delay blocks simulataneously and proceeding to calculate the signals which can be derived using this information. For example, SE of Figure 9/G.721 is calculated using delay values and then SE is used as shown in Figure 4/G.721.

Implementations of the algorithm may be confirmed with a reasonable level of confidence by using the digital test sequences described in Appendix II to this Recommendation. The sequences are given in terms of encoder PCM input words, ADPCM words and decoder PCM output words.

4.1 *Input and output signals*

Table 2/G.721 defines the input and output signals for the encoder and decoder.

An optional signal $R(k)$ represents a reset function that sets all internal memory elements to a specified condition so that an encoder or decoder can be forced into a known state, for applications which require an immediate reset function (e.g. digital circuit multiplication equipment, in which case the reset is mandatory, not optional).

TABLE 2/G.721

Input and output signals

ENCODER			
	Name	Number of bits	Description
Input	S	8	PCM input word
Input	LAW	1	PCM law select, 0 = μ-law, 1 = A-law
Input	R *(optional)*	1	Reset
Output	I	4	ADPCM word
DECODER			
	Name	Number of bits	Description
Input	I	4	ADPCM word
Input	LAW	1	PCM law select, 0 = μ-law, 1 = A-law
Input	R *(optional)*	1	Reset
Output	SD	8	Decoder PCM output word

4.2 *Description of variables and detailed specification of sub-blocks*

This section contains a detailed expansion of all blocks in Figures 2/G.721 and 3/G.721 described in Sections 2 and 3. The expansions are illustrated in Figures 4/G.721 to 11/G.721 with the internal processing variables as defined in Table 3/G.721. A brief functional description and full specification is given for each sub-block.

The notations used in the sub-block descriptions are as follows:

$\ll n$	denotes an *n*-bit shift left operation (zero fill),
$\gg n$	denotes an *n*-bit shift right operation (in the direction of the least significant bit, zero fill),
&	denotes the logical "and" operation,
+	denotes arithmetic addition,
–	denotes arithmetic subtraction,
*	denotes arithmetic multiplication,
**	denotes the logical "exclusive or" operation,
|	delineates comments to equations.

TABLE 3/G.721

Internal Processing Variables

Name	Bits (see note)	Binary representation	Optional reset values	Description
A1*, A2*	16 TC	S, 0,.., −14	0	Delayed predictor second order coefficients
A1P, A2P	16 TC	S, 0,.., −14		Second order predictor coefficients
A1R, A2R	16 TC	S, 0,.., −14		Triggered second order predictor coefficients
A1T	16 TC	S, 0,.., −14		Unlimited a_1 coefficient
A2T	16 TC	S, 0,.., −14		Unlimited a_2 coefficient
AL	7 SM	0,.., −6		Limited speed control parameter
AP*	10 SM	1,.., −8	0	Delayed unlimited speed control parameter
APP	10 SM	1,.., −8		Unlimited speed control parameter
APR	10 SM	1,.., −8		Triggered unlimited speed control parameter
AX	1 SM	1		Speed control parameter update
B1*,..., B6*	16 TC	S, 0,.., −14	0	Delayed sixth order predictor coefficients
B1P,..., B6P	16 TC	S, 0,.., −14		Sixth order predictor coefficients
B1R,..., B6R	16 TC	S, 0,.., −14		Triggered sixth order predictor coefficients
D	16 TC	S, 14,.., 0		Difference signal, only in encoder
DL	11 SM	3,.., −7		Log_2 (difference signal), only in encoder
DLN	12 TC	S, 3,.., −7		Log_2 (normalized difference), only in encoder
DLNX	12 TC	S, 3,.., −7		Log_2 (normalized difference), only in decoder
DLX	11 SM	3,.., −7		Log_2 (difference signal), only in decoder
DML*	14 SM	2,.., −11	0	Delayed long term average of F(I) sequence
DMLP	14 SM	2,.., −11		Long term average of F(I) sequence
DMS*	12 SM	2,.., −9	0	Delayed short term average of F(I) sequence
DMSP	12 SM	2,.., −9		Short term average of F(I) sequence
DQ	15 SM	S, 13,.., 0		Quantized difference signal
DQ0	11 FL	S, 4e, 6m		Quantified difference signal with delay 0
DQ1*,...,DQ6*	11 FL	S, 4e, 6m	32	Quantized difference signal with delays 1 to 6
DQL	12 TC	S, 3,.., −7		Log_2 (quantized difference signal)
DQLN	12 TC	S, 3,.., −7		Log_2 (normalized quantized difference)
DQS	1 TC	S		Sign bit of quantized difference signal
DS	1 TC	S		Sign bit of difference signal, only in encoder
DSX	1 TC	S		Sign bit of difference, signal, only in decoder
DX	16 TC	S, 14,.., 0		Difference signal, only in decoder
FI	3 SM	2,.., 0		Output of F(I)
PK0	1 TC	S		Sign of DQ+SEZ with delay 0
PK1*, PK2*	1 TC	S	0	Sign of DQ+SEZ with delays 1 and 2
SE	15 TC	S, 13,.., 0		Signal estimate
SEZ	15 TC	S, 13,.., 0		Sixth order predictor partial signal estimate
SIGPK	1 TC	0		Sgn [p(k)] flag
SL	14 TC	S, 12,.., 0		Linear input signal, only in encoder
SLX	14 TC	S, 12,.., 0		Quantized reconstructed, signal, only in decoder
SP	8			PCM reconstructed signal, only in decoder
SR	16 TC	S, 14,.., 0		Reconstructed signal
SR0	11 FL	S, 4e, 6m		Reconstructed signal with delay 0
SR1*, SR2*	11 FL	S, 4e, 6m	32	Reconstructed signal with delays 1 and 2
TD	1 TC	0	0	Delayed tone detect
TDP	1 TC	0		Tone detect
TDR	1 TC	0		Triggered tone detect
TR	1 TC	0		Transition detect
U1,..., U6	1 TC	S		Sixth order predictor coefficient update sign bit
WA1, WA2	16 TC	S, 13,.., −1		Partial product of signal estimate
WB1,..., WB6	16 TC	S, 13,.., −1		Partial product of signal etimate
WI	12 TC	S, 6,.., −4		Quantizer multiplier
Y	13 SM	3,.., −9		Quantizer scale factor
YL*	19 SM	3,.., −15	34 816	Delayed slow quantizer scale factor
YLP	19 SM	3,.., −15		Slow quantizer scale factor
YU*	13 SM	3,.., −9	544	Delayed fast quantizer scale factor
YUP	13 SM	3,.., −9		Fast quantizer scale factor
YUT	13 SM	3,.., −9		Unlimited fast quantizer scale factor

Note – TC denotes two's complement; SM denotes signed magnitude; FL denotes floating point; e denotes exponent bits; m denotes mantissa bits; S denotes sign bit

* Indicates variables that are set to specific values by the optional reset. When reset is invoked, the output of the DELAY sub-block (see § 4.2.4) is given in column 4.

4.2.1 *Input PCM format conversion and difference signal computation*

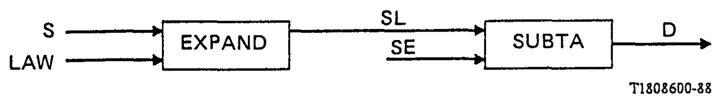


FIGURE 4/G.721

Input PCM format conversion and difference signal computation

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EXPAND

Inputs: S (SP in decoder), LAW

Output: SL (SLX in decoder)

Function: Convert either A-law or μ-law PCM to uniform PCM.

Decode PCM code word, S, according to Recommendation G.711 using character signals (column 6, before inversion of even bits for A-law) and values at decoder output (column 7). The values at decoder output, SS, must be represented in 13-bit signed magnitude form for A-law PCM and 14-bit signed magnitude form for μ-law PCM (the sign bit is equal to one for negative values).

Note – For A-law, S (and SP) includes even bit inversion (see Note 2 below Table 1/G.711).

when LAW = 0,	SSS = SS $\gg$ 13 SSQ = SS & 8191	μ-law
when LAW = 1,	SSS = SS $\gg$ 12 SSM = SS & 4095 SSQ = SSM $\ll$ 1	A-law

then

$$SL = \begin{cases} SSQ, & SSS = 0 \\ (16384 - SSQ)\ \&\ 16383, & SSS = 1 \end{cases}$$

Convert signed magnitude to two's complement

SUBTA

Inputs: SL (SLX in decoder), SE

Output: D (DX in decoder)

Function: Compute difference signal by subtracting signal estimate from input signal (or quantized reconstructed signal in decoder).

SLS = SL $\gg$ 13

$$SLI = \begin{cases} SL, & SLS = 0 \\ 49152 + SL, & SLS = 1 \end{cases}$$

Sign extension

SES = SE $\gg$ 14

$$SEI = \begin{cases} SE, & SES = 0 \\ 32768 + SE, & SES = 1 \end{cases}$$

Sign extension

D = (SLI + 65536 − SEI) & 65535

4.2.2 *Adaptive quantizer*

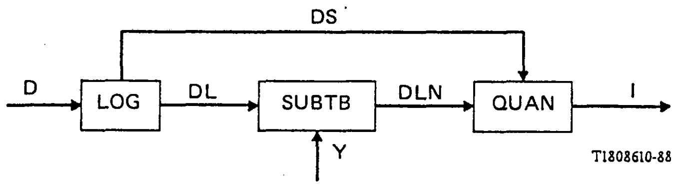

FIGURE 5/G.721

Adaptive quantizer

LOG

Input: D (DX in decoder)

Outputs: DL (DLX in decoder), DS (DSX in decoder)

Function: Convert difference signal from the linear to the logarithmic domain.

$DS = D \gg 15$

$$DQM = \begin{cases} D, & DS = 0 \\ (65536 - D)\ \&\ 32767, & DS = 1 \end{cases}$$

| Convert D from two's complement to signed magnitude

$$EXP = \begin{cases} 14, & 16384 \leqslant DQM \\ 13, & 8192 \leqslant DQM \leqslant 16383 \\ \cdot & \cdot \\ \cdot & \cdot \\ \cdot & \cdot \\ 1, & 2 \leqslant DQM \leqslant 3 \\ 0, & 0 \leqslant DQM \leqslant 1 \end{cases}$$

| Compute exponent

$MANT = ((DQM \ll 7) \gg EXP)\ \&\ 127$

| Compute approximation $\log_2 (1 + x) = x$

$DL = (EXP \ll 7) + MANT$

| Combine 7 mantissa bits and 4 exponent bits into one 11-bit word

---

QUAN (encoder only)

Inputs: DLN, DS

Output: I

Function: Quantize difference signal in logarithmic domain.

Quantizer decision levels and 4-bit outputs:

DS	DLN	I 1234	
0	400-2047	0111	
0	349- 399	0110	
0	300- 348	0101	
0	246- 299	0100	
0	178- 245	0011	
0	80- 177	0010	
0	0- 79	0001	– –| Positive portion of interval
0	3972-4095	0001	– –| Negative portion of interval
0	2048-3971	1111	
1	2048-3971	1111	
1	3972-4095	1110	– –| Negative portion of interval
1	0- 79	1110	– –| Positive portion of interval
1	80- 177	1101	
1	178- 245	1100	
1	246- 299	1011	
1	300- 348	1010	
1	349- 399	1001	
1	400-2047	1000	

Note – The I values are transmitted starting with bit 1.

SUBTB

Inputs: DL (DLX in decoder), Y

Output: DLN (DLNX in decoder)

Function: Scale logarithmic version of difference signal by subtracting scale factor.

DLN = (DL + 4096 – (Y $\gg$ 2)) & 4095

4.2.3 *Inverse adaptive quantizer*

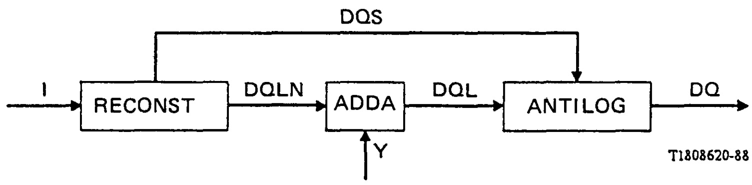

FIGURE 6/G.721

Inverse adaptive quantizer

ADDA

Inputs: DQLN, Y

Output: DQL

Function: Addition of scale factor to logarithmic version of quantized difference signal.

$DQL = (DQLN + (Y \gg 2))\ \&\ 4095$

ANTILOG

Inputs: DQL, DQS

Output: DQ

Function: Convert quantized difference signal from the logarithmic to the linear domain.

$DS = DQL \gg 11$ $DEX = (DQL \gg 7)\ \&\ 15$	Extract 4-bit exponent
$DMN = DQL\ \&\ 127$	Extract 7-bit mantissa
$DQT = (1 \ll 7) + DMN$ $DQMAG = \begin{cases} (DQT \ll 7) \gg (14 - DEX), & DS = 0 \\ (0, & DS = 1 \end{cases}$	Convert mantissa to linear using approximation $2^x = 1 + x$
$DQ = (DQS \ll 14) + DQMAG$	Attach sign bit to signed magnitude word

---

RECONST

Input: I

Outputs: DQLN, DQS

Function: Reconstruction of quantized difference signal in the logarithmic domain.

DQS = I ≫ 3

Quantizer output levels:

I 1234	DQS	DQLN
0111	0	425
0110	0	373
0101	0	323
0100	0	273
0011	0	213
0010	0	135
0001	0	4
0000	0	2048
1111	1	2048
1110	1	4
1101	1	135
1100	1	213
1011	1	273
1010	1	323
1001	1	373
1000	1	425

Note 1 – The I values are received starting with bit 1.

Note 2 – It is possible for the decoder to receive the code word 0000 because of transmission disturbances (e.g. line bit errors).

4.2.4 *Quantizer scale factor adaptation*

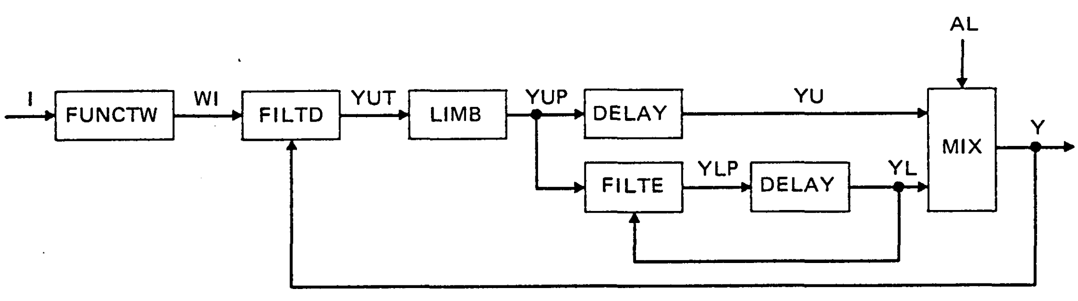

FIGURE 7/G.721

Quantizer scale factor adaptation

DELAY

Inputs: x, R (optional)

Output: y

Function: Memory block. For the input x, the output is given by:

$$y(k) = \begin{cases} x(k-1), & R = 0 \\ \text{optional reset value given in column 4 of Table 3/G.721,} & R = 1 \end{cases}$$ | Optional reset

---

FILTD

Inputs: WI, Y

Output: YUT

Function: Update of fast quantizer scale factor.

DIF = ((WI ≪ 5) + 131072 − Y) & 131071
DIFS = DIF ≫ 16 | Compute difference

$$\text{DIFSX} = \begin{cases} \text{DIF} \gg 5, & \text{DIFS} = 0 \\ (\text{DIF} \gg 5) + 4096, & \text{DIFS} = 1 \end{cases}$$ | Time constant is 1/32 | Sign extension

YUT = (Y + DIFSX) & 8191

FILTE

Inputs: YUP, YL

Output: YLP

Function: Update of slow quantizer scale factor.

DIF = (YUP + ((1048576 − YL) ≫ 6)) & 16383 | Compute difference
DIFS = DIF ≫ 13 | Time constant is 1/64

$$\text{DIFSX} = \begin{cases} \text{DIF}, & \text{DIFS} = 0 \\ \text{DIF} + 507904, & \text{DIFS} = 1 \end{cases}$$ | Sign extension

YLP = (YL + DIFSX) & 524287

FUNCTW

Input: I

Output: WI

Function: Map quantizer output into logarithmic version of scale factor multiplier.

$IS = I \gg 3$

$$IM = \begin{cases} I \,\&\, 7, & IS = 0 \\ (15 - I) \,\&\, 7, & IS = 1 \end{cases}$$

$$WI = \begin{cases} 1122, & IM = 7 \\ 355, & IM = 6 \\ 198, & IM = 5 \\ 112, & IM = 4 \\ 64, & IM = 3 \\ 41, & IM = 2 \\ 18, & IM = 1 \\ 4084, & IM = 0 \end{cases}$$ | Scale factor multipliers

---

LIMB

Input: YUT

Output: YUP

Function: Limit quantizer scale factor.

$GEUL = ((YUT + 11264) \,\&\, 16383) \gg 13$

$GELL = ((YUT + 15840) \,\&\, 16383) \gg 13$

$$YUP = \begin{cases} 544, & GELL = 1 \\ 5120, & GEUL = 0 \\ YUT, & \text{otherwise} \end{cases}$$ | Set lower limit to 1.06 | Set upper limit to 10.00

MIX

Inputs: AL, YU, YL

Output: Y

Function: Form linear combination of fast and slow quantizer scale factors.

$DIF = (YU + 16384 - (YL \gg 6)) \,\&\, 16383$
$DIFS = DIF \gg 13$ | Compute difference

$$DIFM = \begin{cases} DIF, & DIFS = 0 \\ (16384 - DIF) \,\&\, 8191, & DIFS = 1 \end{cases}$$ | Compute magnitude of difference

$PRODM = (DIFM * AL) \gg 6$ | Compute magnitude of product

$$PROD = \begin{cases} PRODM, & DIFS = 0 \\ (16384 - PRODM) \,\&\, 16383, & DIFS = 1 \end{cases}$$ | Convert magnitude to two's complement

$Y = ((YL \gg 6) + PROD) \,\&\, 8191$

4.2.5 *Adaptation speed control*

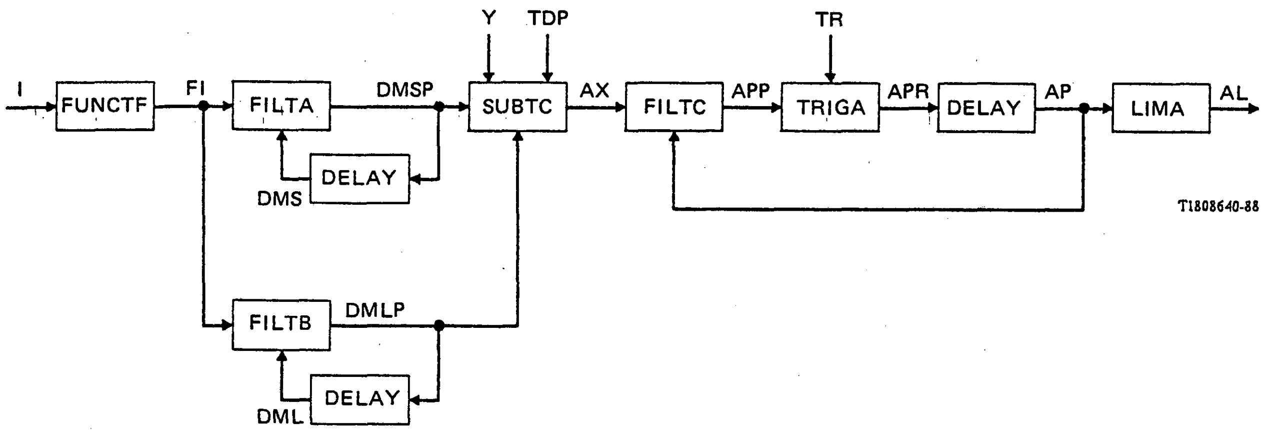

FIGURE 8/G.721

Adaptation speed control

DELAY

See § 4.2.4 for specification.

FILTA

Inputs: FI, DMS

Output: DMSP

Function: Update of short-term average of F(I)

$$\begin{array}{ll} \text{DIF} = ((\text{FI} \ll 9) + 8192 - \text{DMS}) \ \& \ 8191 & \\ \text{DIFS} = \text{DIF} \gg 12 & \text{Compute difference} \end{array}$$

$$\text{DIFSX} = \begin{cases} \text{DIF} \gg 5, & \text{DIFS} = 0 \\ (\text{DIF} \gg 5) + 3840, & \text{DIFS} = 1 \end{cases} \qquad \begin{array}{l} \text{Time constant is } 1/32 \\ \text{Sign extension} \end{array}$$

$$\text{DMSP} = (\text{DIFSX} + \text{DMS}) \ \& \ 4095$$

FILTB

Inputs: FI, DML

Output: DMLP

Function: Update of long-term average of F(I)

$$\begin{array}{ll} \text{DIF} = ((\text{FI} \ll 11) + 32768 - \text{DML}) \ \& \ 32767 & \\ \text{DIFS} = \text{DIF} \gg 14 & \text{Compute difference} \end{array}$$

$$\text{DIFSX} = \begin{cases} \text{DIF} \gg 7, & \text{DIFS} = 0 \\ (\text{DIF} \gg 7) + 16128, & \text{DIFS} = 1 \end{cases} \qquad \begin{array}{l} \text{Time constant is } 1/28 \\ \text{Sign extension} \end{array}$$

$$\text{DMLP} = (\text{DIFSX} + \text{DML}) \ \& \ 16383$$

FILTC

Inputs: AX, AP

Output: APP

Function: Low pass filter of speed control parameter.

$$\begin{array}{ll} \text{DIF} = ((\text{AX} \ll 9) + 2048 - \text{AP}) \ \& \ 2047 & \\ \text{DIFS} = \text{DIF} \gg 10 & \text{Compute difference} \end{array}$$

$$\text{DIFSX} = \begin{cases} \text{DIF} \gg 4, & \text{DIFS} = 0 \\ (\text{DIF} \gg 4) + 896, & \text{DIFS} = 1 \end{cases} \qquad \begin{array}{l} \text{Time constant is } 1/16 \\ \text{Sign extension} \end{array}$$

$$\text{APP} = (\text{DIFSX} + \text{AP}) \ \& \ 1023$$

FUNCTF

Input: I

Output: FI

Function: Map quantizer output into the F(I) function.

$IS = I \gg 3$

$$IM = \begin{cases} I \,\&\, 7, & IS = 0 \\ (15 - I) \,\&\, 7, & IS = 1 \end{cases}$$

$$FI = \begin{cases} 0, & 0 \leqslant IM \leqslant 2 \\ 1, & 3 \leqslant IM \leqslant 5 \\ 3, & IM = 6 \\ 7, & IM = 7 \end{cases}$$

LIMA

Input: AP

Output: AL

Function: Limit speed control parameter.

$$AL = \begin{cases} 64, & AP \geqslant 256 \\ AP \gg 2, & AP \leqslant 255 \end{cases}$$

SUBTC

Inputs: DMSP, DMLP, TDP, Y

Output: AX

Function: Compute magnitude of the difference of short- and long-term functions of quantizer output sequence and then perform threshold comparison for quantizing speed control parameter.

$DIF = ((DMSP \ll 2) + 32768 - DMLP) \,\&\, 32767$ | Compute difference

$DIFS = DIF \gg 14$

$$DIFM = \begin{cases} DIF, & DIFS = 0 \\ (32768 - DIF) \,\&\, 16383, & DIFS = 1 \end{cases}$$ | Compute magnitude of difference

$DTHR = DMLP \gg 3$

$$AX = \begin{cases} 0, & Y \geqslant 1536 \text{ and } DIFM < DTHR \text{ and } TDP = 0 \\ 1, & \text{otherwise} \end{cases}$$

TRIGA

Inputs: TR, APP

Output: APR

Function: Speed control trigger block

$$APR = \begin{cases} APP, & TR = 0 \\ 256, & TR = 1 \end{cases}$$

4.2.6 *Adaptive predictor and reconstructed signal calculator*

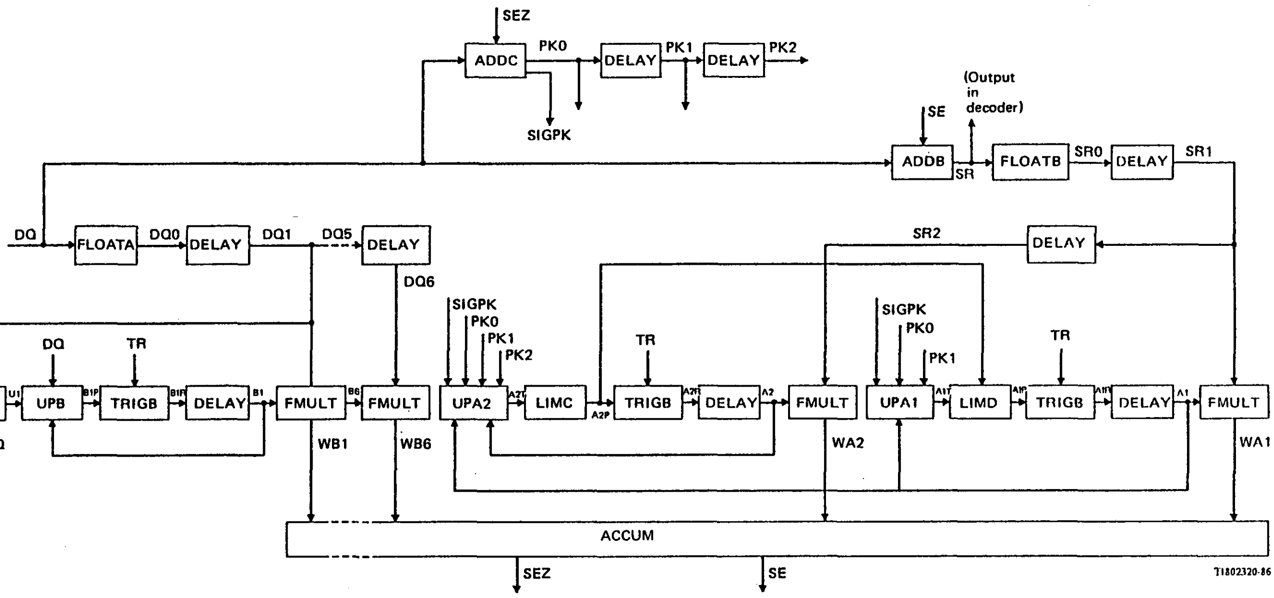

FIGURE 9/G.721

Adaptive predictor and reconstructed signal calculator

ACCUM

Inputs: WA1, WA2, WB1, WB2, WB3, WB4, WB5, WB6

Outputs: SE, SEZ

Function: Addition of predictor outputs to form the partial signal estimate (from the sixth order predictor) and the signal estimate.

SEZI = ((((((((WB1 + WB2) & 65535) + WB3) & 65535) + WB4) & 65535) + WB5) & 65535) + WB6) & 65535 | Sum for partial signal estimate

SEI = (((SEZI + WA2) & 65535) + WA1) & 65535 | Complete sum for signa estimate

SEZ = SEZI $\gg$ 1

SE = SEI $\gg$ 1

ADDB

Inputs: DQ, SE

Output: SR

Function: Addition of quantized difference signal and signal estimate to form reconstructed signal.

$$DQS = DQ \gg 14$$

$$DQI = \begin{cases} DQ, & DQS = 0 \\ (65536 - (DQ \,\&\, 16383)) \,\&\, 65535, & DQS = 1 \end{cases} \quad \Big| \text{ Convert signed magnitude to two's complement}$$

$$SES = SE \gg 14$$

$$SEI = \begin{cases} SE, & SES = 0 \\ (1 \ll 15) + SE, & SES = 1 \end{cases} \quad \Big| \text{ Sign extension}$$

$$SR = (DQI + SEI) \,\&\, 65535$$

ADDC

Inputs: DQ, SEZ

Output: PK0, SIGPK

Function: Obtain sign of addition of quantized difference signal and partial signal estimate.

$$DQS = DQ \gg 14$$

$$DQ1 = \begin{cases} DQ, & DQS = 0 \\ (65536 - (DQ \,\&\, 16383)) \,\&\, 65535, & DQS = 1 \end{cases} \quad \Big| \text{ Convert signed magnitude to two's complement}$$

$$SEZS = SEZ \gg 14$$

$$SEZI = \begin{cases} SEZ, & SEZS = 0 \\ (1 \ll 15) + SEZ, & SEZS = 1 \end{cases} \quad \Big| \text{ Sign extension}$$

$$DQSEZ = (DQI + SEZI) \,\&\, 65535$$

$$PK0 = DQSEZ \gg 15$$

$$SIGPK = \begin{cases} 1, & DQSEZ = 0 \\ 0, & \text{otherwise} \end{cases}$$

DELAY

See § 4.2.4 for specification.

FLOATA

Input: DQ

Output: DQO

Function: Convert 15-bit signed magnitude to floating point.

$DQS = DQ \gg 14$	
$MAG = DQ \ \& \ 16383$	Compute magnitude
$EXP = \begin{cases} 14, & 8192 \leq MAG \\ 13, & 4096 \leq MAG \leq 8191 \\ \cdot & \cdot \\ \cdot & \cdot \\ \cdot & \cdot \\ 2, & 2 \leq MAG \leq 3 \\ 1, & MAG = 1 \\ 0, & MAG = 0 \end{cases}$	Compute exponent
$MANT = \begin{cases} 1 \ll 5, & MAG = 0 \\ (MAG \ll 6) \gg EXP, & \text{otherwise} \end{cases}$	Compute mantissa with a 1 in the most significant bit.
$DQO = (DQS \ll 10) + (EXP \ll 6) + MANT$	Combine sign bit, 4 exponent bits and 6 mantissa bits into one 11-bit word

---

FLOATB

Input: SR

Output: SRO

Function: Convert 16-bit two's complement to floating point.

$SRS = SR \gg 15$	
$MAG = \begin{cases} SR, & SRS = 0 \\ (65536 - SR) \ \& \ 32767, & SRS = 1 \end{cases}$	Compute magnitude
$EXP = \begin{cases} 15, & 16384 \leq MAG \\ 14, & 8192 \leq MAG \leq 16383 \\ \cdot & \cdot \\ \cdot & \cdot \\ \cdot & \cdot \\ 2, & 2 \leq MAG \leq 3 \\ 1, & MAG = 1 \\ 0, & MAG = 0 \end{cases}$	Compute exponent
$MANT = \begin{cases} 1 \ll 5, & MAG = 0 \\ (MAG \ll 6) \gg EXP, & \text{otherwise} \end{cases}$	Compute mantissa with a 1 in the most significant bit
$SRO = (SRS \ll 10) + (EXP \ll 6) + MANT$	Combine sign bit, 4 exponent bits and 6 mantissa bits into one 11-bit word

FMULT

Inputs: An or Bn, SRn or DQn

Output: WAn or WBn

Note – Equations are given for An, SRn and WAn. The equations are also valid when substituting Bn for An, DQn for SRn and WBn for WAn.

Function: Multiply predictor coefficients with corresponding quantized difference signal or reconstructed signal. Multiplication is done in floating point format.

$$AnS = An \gg 15$$

$$AnMAG = \begin{cases} An \gg 2 & AnS = 0 \\ (16384 - (An \gg 2))\ \&\ 8191, & AnS = 1 \end{cases}$$

| Convert two's complement to signed magnitude

$$AnEXP = \begin{cases} 13, & 4096 \leqslant AnMAG \\ 12, & 2048 \leqslant AnMAG \leqslant 4095 \\ \cdot & \cdot \\ \cdot & \cdot \\ \cdot & \cdot \\ 2, & 2 \leqslant AnMAG \leqslant 3 \\ 1, & AnMAG = 1 \\ 0, & AnMAG = 0 \end{cases}$$

| Compute exponent

$$AnMANT = \begin{cases} 1 \ll 5, & AnMAG = 0 \\ (AnMAG \ll 6) \gg AnEXP, & \text{otherwise} \end{cases}$$

| Compute mantissa with a 1 in the most significant bitt

$$SRnS = SRn \gg 10$$
$$SRnEXP = (SRn \gg 6)\ \&\ 15$$
$$SRnMANT = SRn\ \&\ 63$$

| Split floating point word into sign bit, exponent and mantissa

$$WAnS = SRnS \text{ ** } AnS$$
$$WAnEXP = SRnEXP + AnEXP$$
$$WAnMANT = ((SRnMANT * AnMANT) + 48) \gg 4$$

| Perform floating point multiplication

$$WAnMAG = \begin{cases} (WAnMANT \ll 7) \gg (26 - WAnEXP), & WAnEXP \leqslant 26 \\ ((WAnMANT \ll 7) \ll (WAnEXP - 26))\ \&\ 32767, & WAnEXP > 26 \end{cases}$$

| Convert floating point to magnitude

$$WAn = \begin{cases} WAnMAG, & WAnS = 0 \\ (65536 - WAnMAG)\ \&\ 65535, & WAnS = 1 \end{cases}$$

| Convert magnitude to two's complement

LIMC

Input: A2T

Output: A2P

Function: Limits on a_2 coefficient of second order predictor.

A2UL = 12288 | Upper limit of +0.75

A2LL = 53248 | Lower limit of −0.75

$$A2P = \begin{cases} A2LL, & 32768 \leqslant A2T \leqslant A2LL \\ A2UL, & A2UL \leqslant A2T \leqslant 32767 \\ A2T, & \text{otherwise} \end{cases}$$

LIMD

Inputs: A1T, A2P

Output: A1P

Function: Limits on a_1 coefficient of second order predictor.

OME = 15360 | (1 − epsilon) where epsilon = 1/16

A1UL = (OME + 65536 − A2P) & 65535 | Compute upper limt

A1LL = (A2P + 65536 − OME) & 65535 | Compute lower limit

$$A1P = \begin{cases} A1LL, & 32768 \leqslant A1T \text{ and } A1T \leqslant A1LL \\ A1UL, & A1UL \leqslant A1T \text{ and } A1T \leqslant 32767 \\ A1T, & \text{otherwise} \end{cases}$$

TRIGB

Inputs: TR, AnP or BnP or EDP

Output: AnR or BnR or TDR

Note – Equation is given for AnP and AnR. Equation is also valid when substituting BnP and BnR or TDP and TDR for AnP and AnR respectively.

Function: Predictor trigger block

$$AnR = \begin{cases} AnP, & TR = 0 \\ 0, & TR = 1 \end{cases}$$

UPA1

Inputs: PK0, PK1, A1, SIGPK

Output: A1T

Function: Update a_1 coefficient of second order predictor.

PKS = PK0 ** PK1 | 1-bit "exclusive or"

$$UGA1 = \begin{cases} 192, & PKS = 0 \text{ and } SIGPK = 0 \\ 65344, & PKS = 1 \text{ and } SIGPK = 0 \\ 0, & SIGPK = 1 \end{cases}$$ | Gain = ± 3/256

A1S = A1 ≫ 15

$$ULA1 = \begin{cases} (65536 - (A1 \gg 8))\ \&\ 65535, & A1S = 0 \\ (65536 - ((A1 \gg 8) + 65280))\ \&\ 65535, & A1S = 1 \end{cases}$$ | Leak factor = 1/256

UA1 = (IGA1 + I+A1) & 65535
A1T = (A1 + UA1) & 65535 | Compute update

UPA2

Inputs: PK0, PK1, PK2, A1, A2, A2, SIGPK

Output: A2T

Function: Update a_2 coefficient of second order predictor.

PKS1 = PK0 ** PK1 | 1-bit "exclusive or"

PKS2 = PK0 ** PK2 | 1-bit "exclusive or"

$$UGA2A = \begin{cases} 16384, & PKS2 = 0 \\ 114688, & PKS2 = 1 \end{cases}$$

$A1S = A1 \gg 15$

If A1S = 0, then

$$FA1 = \begin{cases} A1 \ll 2, & A1 \leqslant 8191 \\ 8191 \ll 2, & A1 \geqslant 8192 \end{cases}$$ | Implement $f(a_1)$ with limiting at +1/2

If A1S = 1, then

$$FA1 = \begin{cases} (A1 \ll 2) \,\&\, 131071, & A1 \geqslant 57345 \\ 24577 \ll 2, & A1 \leqslant 57344 \end{cases}$$ | Implement $f(a_1)$ with limiting at −1/2

$$FA = \begin{cases} FA1, & PKS1 = 1 \\ (131072 - FA1) \,\&\, 131071, & PKS1 = 0 \end{cases}$$ | Attach sign to result of $f(a_1)$

UGA2B = (UGA2A + FA) & 131071

$UGA2S = UGA2B \gg 16$

$$UGA2 = \begin{cases} UGA2B \gg 7, & UGA2S = 0 \text{ and } SIGPK = 0 \\ (UGA2B \gg 7) + 64512, & UGA2S = 1 \text{ and } SIGPK = 0 \\ 0, & SIGPK = 1 \end{cases}$$ | Gain calculation, gain = ± 1/128

$A2S = A2 \gg 15$

$$ULA2 = \begin{cases} (65536 - (A2 \gg 7)) \,\&\, 65535, & A2S = 0 \\ (65536 - ((A2 \gg 7) + 65024)) \,\&\, 65535, & A2S = 1 \end{cases}$$ | Leak factor is 1/128

UA2 = (UGA2 + ULA2) & 65535

A2T = (A2 + UA2) & 65535 | Compute update

UPB

Inputs: Un, Bn, DQ

Output: BnP

Function: Update for coefficients of sixth order predictor.

DQMAG = DQ & 16383

$$UGBn = \begin{cases} 128, & Un = 0 \text{ and } DQMAG \neq 0 \\ 65408, & Un = 1 \text{ and } DQMAG \neq 0 \\ 0, & DQMAG = 0 \end{cases}$$ | Gain = ± 1/128 or 0

BnS = Bn ≫ 15

$$ULBn = \begin{cases} (65536 - (Bn \gg 8)) \,\&\, 65535, & BnS = 0 \\ (65536 - ((Bn \gg 8) + 65280)) \,\&\, 65535, & BnS = 1 \end{cases}$$ | Leak factor = 1/256

UBn = (UGBn + ULBn) & 65535
BnP = (Bn + UBn) & 65535 | Compute update

XOR

Inputs: DQn, DQ

Output: Un

Function: One bit "exclusive or" of sign of difference signal and sign of delayed difference signal.

DQS = DQ ≫ 14

DQnS = DQn ≫ 10

Un = DQS ** DQnS | 1-bit "exclusive or"

4.2.7 *Tone and transition detector*

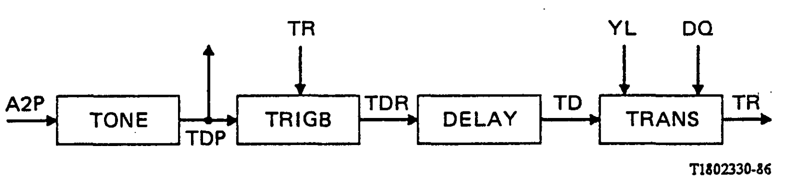

FIGURE 10/G.721

Tone and transition detector

DELAY

See § 4.2.4 for specification.

TONE

Input: A2P

Output: TDP

Function: Partial band signal detection

$$TDP = \begin{cases} 1, & 32768 \leqslant A2P \text{ and } A2P < 53760 \\ 0, & \text{otherwise} \end{cases}$$

TRANS

Inputs: TD, YL, DQ

Output: TR

Function: Transition detector.

DQMAG = DQ & 16383

YLINT = YL ⪢ 15

YLFRAC = (YL ⪢ 10) & 31

THR1 = (32 + YLFRAC) ⪡ YLINT

$$THR2 = \begin{cases} 31 \lll 9, & YLINT > 8 \\ THR1, & \text{otherwise} \end{cases}$$

DQTHR = (THR2 + (THR2 ⪢ 1)) ⪢ 1

$$TR = \begin{cases} 1, & DQMAG > DQTHR \text{ and } TD = 1 \\ 0, & \text{otherwise} \end{cases}$$

TRIGB

See § 4.2.6 for specification.

4.2.8 *Output PCM format conversion and synchronous coding adjustment*

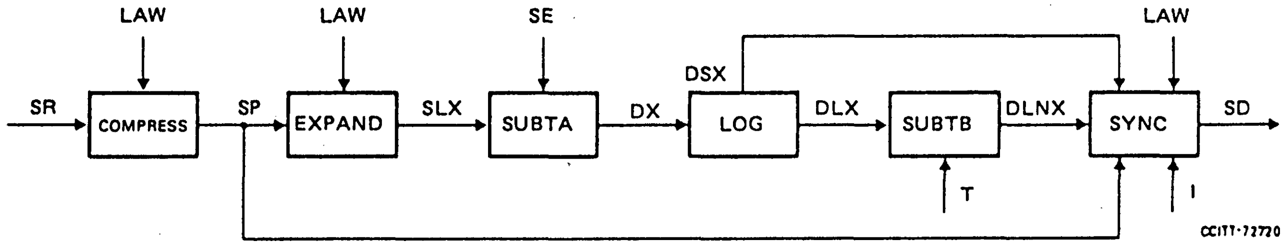

FIGURE 11/G.721

Output PCM format conversion and synchronous coding adjustment

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COMPRESS (decoder only)

Inputs: SR, LAW

Output: SP

Function: Convert from uniform PCM to either A-law or μ-law PCM.

$\text{IS} = \text{SR} \gg 15$

$$\text{IM} = \begin{cases} \text{SR}, & \text{IS} = 0 \\ (65536 - \text{SR})\ \&\ 32767, & \text{IS} = 1 \end{cases}$$

| Convert two's complement to signed magnitude

$$\text{IMAG} = \begin{cases} \text{IM}, & \text{LAW} = 0 \\ \text{IM} \gg 1, & \text{LAW} = 1 \text{ and } \text{IS} = 0 \\ (\text{IM} + 1) \gg 1, & \text{LAW} = 1 \text{ and } \text{IS} = 1 \end{cases}$$

| μ-law
| A-law

then quantize IMAG (see note below) according to Recommendation G.711 using decision values (column 5 of Tables 1a, 1b, 2a and 2b/G.711) in the following way:

SP =
- character signal after even bit inversion deduced from Table 1a/G.711 (column 6), IS = 0 and LAW = 1
- character signal after even bit inversion deduced from Table 1b/G.711 (column 6), IS = 1 and LAW = 1
- character signal of Table 2a/G.711 (column 6), IS = 0 and LAW = 0
- character signal of Table 2b/G.711 (column 6), IS = 1 and LAW = 0

Note – When IMAG is outside the range defined by the virtual decision level, SP must be set equal to the maximum PCM code word. For the purpose of clarification, examples of conversion for both A-law (after even bit inversion) and μ-law in the vicinity of the origin are given in the table below:

IS	IMAG	PCM code word SP	
		A-law	μ-law
0	3	11010100	11111101
0	2	11010100	11111110
0	1	11010101	11111110
0	0	11010101	11111111
1	1	01010101	01111110
1	2	01010101	01111110
1	3	01010100	01111101

EXPAND

See § 4.2.1 for specification. Substitute SP for S as input and SLX for SL as output.

LOG

See § 4.2.2 for specification. Substitute DX for D as input, DLX for DL and DSX for DS as outputs.

SUBTA

See § 4.2.1 for specification. Substitute SLX for SL as input and DX for D as output.

SUBTB

See § 4.2.2 for specification. Substitute DLX for DL as input and DLNX for DLN as output.

SYNC (decoder only)

Inputs: I, SP, DLNX, DSX, LAW

Output: SD

Function: Re-encode output PCM sample in decoder for synchronous tandem coding.

$$IS = I \gg 3$$

$$IM = \begin{cases} I + 8, & IS = 0 \\ I \,\&\, 7, & IS = 1 \end{cases}$$

ID is defined according to the following table:

DSX	DLNX	ID	
0	400-2047	15	
0	349- 399	14	
0	300- 348	13	
0	246- 299	12	
0	178- 245	11	
0	80- 177	10	
0	0- 79	9	– –| Positive portion of decision interval
0	3972-4095	9	– –| Negative portion of decision interval
0	2048-3971	7	
1	2048-3971	7	
1	3972-4095	6	– –| Negative portion of decision interval
1	0- 79	6	– –| Positive portion of decision interval
1	80- 177	5	
1	178- 245	4	
1	246- 299	3	
1	300- 348	2	
1	349- 399	1	
1	400-2047	0	

$$SD = \begin{cases} SP^+, & ID < IM \\ SP, & ID = IM \\ SP^-, & ID > IM \end{cases}$$

where

SP^+ = The PCM code word that represents the next more positive PCM output level (when SP represents the most positive PCM output level, then SP^+ is constrained to be SP).

SP^- = The PCM code word that represents the next more negative PCM output level (when SP represents the most negative PCM output level, then SP^- is constrained to be SP).

For the purposes of clarification, examples of re-encoding for both A-law (after even bit inversion) and μ-law in the vicinity of the origin are given in the table below:

	A-law		μ-law	
Comparison of ID and IM	SP	SD	SP	SD
ID > IM ID = IM ID < IM	11010101 » »	01010101 11010101 11010100	11111110 » »	11111111 11111110 11111101
ID > IM ID = IM ID < IM	01010101 » »	01010100 01010101 11010101	11111111 » »	01111110 11111111 11111110
ID > IM ID = IM ID < IM	01010100 » »	01010111 01010100 01010101	01111110 » »	01111101 01111110 01111111

Note – SP (and SD) represent character signals defined according to Tables 1/G.711 and 2/G.711. See sub-block COMPRESS above for the exact representation of SP (and SD).

APPENDIX I

(to Recommendation G.721)

Network aspects

The purpose of this Appendix is to give a broad outline of the interaction of 32 kbit/s ADPCM with other devices that are found in the telephony network and also the effect on specific signals found in the network. Some general guidance is also offered.

I.1 *General transmission consideration*

This Recommendation is applicable to transmission over 32 kbit/s channels. Consideration will have to be given to appropriate corrective action with, for example, the use of bit stealing techniques for the provision of a limited speed signalling facility. Without due consideration to the interaction serious performance degradation will occur.

Conversely a 64 kbit/s channel which is conveyed by a 32 kbit/s ADPCM channel (or channels) will not exhibit bit integrity.

I.2 *Interaction with other processes*

The synchronous coding adjustment is described in §§ 1.2 and 3.7 of the Recommendation. The favourable operation of this adjustment is dependent on the signals on the 32 kbit/s path and on the intermediate 64 kbit/s path both being uncorrupted by other digital processes. For example the use of digital pads, A-law to μ-law converters, echo cancellers or digital speech interpolation (DSI) at these intermediate points will inhibit the correct functioning of this adjustment. However, the performance will still be better than that achieved when an asynchronous connection is employed.

The use of a 32 kbit/s link to interconnect 64 kbit/s A-law PCM signals and 64 kbit/s μ-law signals has been found to be satisfactory for speech even though this will inhibit the correct operation of the synchronous coding adjustment between the 32 kbit/s link so used and the subsequent 32 kbit/s link.

The interactions between 32 kbit/s ADPCM and processes such as DSI and echo cancellation (e.g. quantization noise in the echo path) are still being studied.

The effect of large d.c. offsets (arising from PCM encoders) on the performance of 32 kbit/s ADPCM for low level signals is currently under study.

I.3 *Interaction with coding laws other than PCM*

Interconnection with coding laws other than PCM is not the subject of the Recommendation and analogue interconnection may need to be employed.

It follows that great care must be exercised when interconnection is made to coding laws which are not the subject of CCITT Recommendations.

I.4 *Speech performance*

Under error free transmission conditions the perceived quality of speech over 32 kbit/s ADPCM links is only slightly lower than that over 64 kbit/s PCM links. This will only be significant when numbers of such links are used in tandem and not when single links are used. Hence the numbers of such 32 kbit/s ADPCM links must be controlled on an international connection. With transmission error ratios higher than $1 \cdot 10^{-4}$ the perceived quality of speech over 32 kbit/s ADPCM links is better than that over 64 kbit/s PCM links. Precise limits for the international portion of the connection and the national extensions may be found in Recommendation G.113.

I.5 *Performance with non-speech services*

I.5.1 *Low-speed data*

Voiceband data performance up to 2400 bit/s using, for example modems to Recommendations V.21, V.22 *bis*, V.23 and V.26 *ter*, will not be subject to significant degradation over 32 kbit/s ADPCM links provided the numbers of such links do not exceed the limits of Recommendation G.113.

I.5.2 *High-speed data*

Voiceband data performance at 4800 bit/s using, for example modems to Recommendation V.27 *bis*, can be accommodated but will be subject to additional degradations over and above that expected from standard 64 kbit/s PCM links. More care will need to be exercised in using such a service.

9600 bit/s voiceband data transmission using modems to Recommendation V.29 will not be satisfactory. However, using other modulation techniques it may be possible to alleviate this difficulty.

I.5.3 *Voice-frequency telegraph*

24-channel voice-frequency telegraph to Recommendation R.35 cannot be satisfactorily conveyed over 32 kbit/s ADPCM links and it is, therefore, desirable to implement routing rules to avoid this combination.

I.5.4 *Dual tone multi-frequency (DTMF) signalling*

No major difficulties are likely to be experienced with DTMF signalling conveyed over 32 kbit/s ADPCM links. The use of DTMF for end-to-end signalling is limited by the number of links in tandem.

I.5.5 *Facsimile*

No serious degradation is to be expected when using this service with Group 2 facsimile apparatus to Recommendation T.3 in conjunction with 32 kbit/s ADPCM transcoding.

APPENDIX II

(to Recomendation G.721)

Digital test sequences

This Appendix gives information concerning the digital test sequences which have been chosen to aid verification of implementations of the algorithm. Copies of the sequences are available on flexible disks (see § II.2).

II.1 *Purpose and design strategy*

II.1.1 *Purpose of digital test sequences*

The use of digital sequences is the most suitable method of verifying the compliance of an implementation of the digital transcoding algorithm. With a limited number of test sequences it is not possible to demonstrate compliance with 100% confidence. However, the sequences chosen functionally exercise the major arithmetic components and thus give a reasonable level of confidence in full compliance with this Recommendation. The more general issues involved in testing such algorithms are the subject of further study.

II.1.2 *Test configurations and word formats*

Test sequences are derived for the two configurations shown in Figures II-1/G.721 and II-2/G.721 respectively with the word format of the various sequences as detailed in Table II-1/G.721. The configuration of Figure II-1/G.721 is the standard arrangement with the encoder transmitting (error-free) to the decoder. The configuration of Figure II-2/G.721 allows sequences of ADPCM words which would not normally emanate from an encoder.

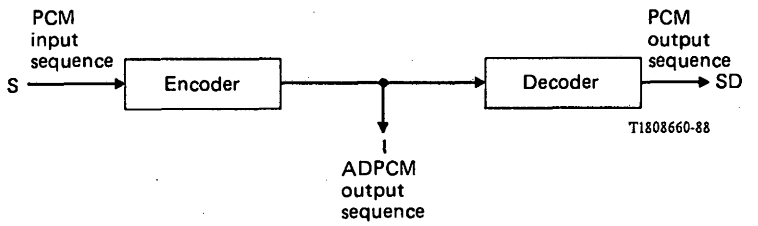


FIGURE II-1/G.721

Encoder and decoder configuration

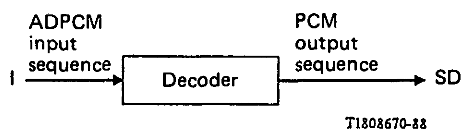


FIGURE II-2/G.721

Decoder only configuration

TABLE II-1/G.721

Word format of test sequences

Name	Description	Word format
S	PCM input word	Identical to that of SP described in the sub-block COMPRESS (§ 4.2.8)
I	ADPCM word	As specified in the sub-block RECONST (§ 4.2.3)
SD	PCM output word	Identical to that of SP described in the sub-block COMPRESS (§ 4.2.8)

II.1.3 *Input test sequences*

Three types of input sequences are used denoted I, II and III as described below.

Type I – This is a PCM input sequence, of length 16384 values, chosen to represent specific narrowband and broadband signal segments as detailed in Table II-2/G.721 and is applied to the test configuration of Figure II-1/G.721.

TABLE II-2/G.721

Sequence of narrow-band and broadband signal segments

Signal	Length
3504 Hz tone	1024
2054 Hz tone	1024
1504 Hz tone	1024
504 Hz tone	1024
254 Hz tone	1024
1254 Hz tone	1024
2254 Hz tone	1024
3254 Hz tone	1024
4000 Hz tone	512
DC, positive, low level	512
DC, value of zero	512
DC, negative, low level	512
4800 bit/s differential phase shift keyed voiceband data switched carrier	3072
4800 bit/s differential phase shift keyed voiceband data continuous carrier (with asynchronous switched carrier secondary channel)	3072
Total length of sequence	16 384

Type II – This is a PCM input sequence, of length 2048 values, chosen to represent overload signals and is applied to the test configuration of Figure II-1/G.721. It is a combination of three high level (> + 12 dBm0) single frequency tones at 404, 1004 and 3204 Hz, each of which appear several times in a different order with various durations. This sequence is generated digitally without analogue filtering but with the +3 dBm0 overload point enforced.

Type III – This is an ADPCM input sequence, of total length 16384 values, and is applied to the test configuration of Figure II-2/G.721. It is a combination of a polarity sequence and a sequence of 3-bit magnitudes. The polarity sequence consists of eight sub-sequences each of length 2048 as follows:

(1) + + + + + + + + ...
(2) + + + + − − − − + + + + − − − − ...
(3) − − + − − + − − + ...
(4) + + − − + + − − ...
(5) + + − − − + + − − − ...
(6) − − − − − + − + − − − − − + − + ...
(7) − − + − + − − + − + ...
(8) + − + − + − ...

The magnitude sequence consists of 27 concatenated sub-sequences of various lengths as detailed in Table II-3/G.721 (values in decimal integer form). It should be noted that the ADPCM values are in one's complement form.

TABLE II-3/G.721

Sequence of I value magnitude

Repetitive pattern	Length
00000	1024
alternating sixteen 0's, sixteen 1's	512
11111	512
alternating sixteen 1's, sixteen 2's	512
22222	512
alternating sixteen 2's, sixteen 3's	256
33333	1024
alternating sixteen 3's, sixteen 4's	512
44444	512
alternating sixteen 4's, sixteen 5's	512
55555	512
alternating sixteen 5's, sixteen 6's	256
66666	1024
alternating sixteen 6's, sixteen 7's	256
77777	1024
66666	1024
55555	1024
alternating sixteen 5's, sixteen 4's	512
alternating sixteen 4's, sixteen 3's	512
33333	512
22222	1024
alternating sixteen 2's, sixteen 1's	512
alternating sixteen 1's, sixteen 0's	512
00000	1024
alternating sixteen 5's, sixteen 7's	256
alternating sixteen 2's, sixteen 7's	256
alternating sixteen 1's, sixteen 6's	256
Total length of sequence	16 384

II.1.4 *Test sequence initialization*

For both configurations, the contents of all memory elements must be set to unique values prior to the start of one of the input test sequences described above. In order to accomplish this in a convenient manner, input initialization sequences have been designed that will drive all state variables to unique values. It should be noted that these values are not the same as the values obtained with the optional reset (listed in Table 3/G.721). There are two such initialization sequences, one PCM and one ADPCM sequence, for each of the μ-law and A-law PCM input formats. All of the initialization sequences are of length 3496. A general description of the signals making up the PCM initialization sequences is provided in Table II-4/G.721. The ADPCM initialization sequences were derived by encoding the PCM sequences through a standard implemantation of the encoder. In order to correctly generate an output test sequence, the desired input test sequence must be appended to the appropriate initialization sequence.

TABLE II-4/G.721

Components of PCM initializing sequences

PCM law	Signal	Number of samples
μ-law	Value of zero, PCM = FF (hex)	1000
	2800 Hz tone	448
	Negative value, PCM = 20 (hex)	1
	Positive overload, PCM = 80 (hex)	1
	Value of zero, PCM = FF (hex)	598
	2800 Hz Tone	448
	Negative value, PCM = 20 (hex)	1
	Positive overload, PCM = 80 (hex)	1
	Value of zero, PCM = FF (hex)	998
	Total length of sequence	3496
A-law	Value of zero, PCM = 55 (hex)	600
	2800 Hz tone	648
	Negative overload, PCM = 2A (hex)	2
	Value of zero, PCM = 55 (hex)	6
	Random combination of positive overload (AA) and negative overload (2A)	155
	Valuee of zero, PCM = 55 (hex)	637
	2800 Hz Tone	648
	Negative overload, PCM = 2A (hex)	2
	Value of zero, PMC = 55 (hex)	6
	Random combination of positive overload (AA) and negative overload (2A)	155
	Value of zero, PCM = 55 (hex)	637
	Total length of sequence	3496

II.2 *Format for test sequence distribution*

II.2.1 *Diskette interface and format*

Copies of the digital test sequences, on two 5-1/4 diskettes, are available from the ITU. One diskette contains only the μ-law sequences, while the other contains only the A-law sequences. The diskettes were created under the MS-DOS operating system (version 2 or newer), and the format is double-sided, double-density, 9-sectored, with 40 tracks per side.

II.2.2 *Directory and file format description*

Each diskette contains a README file, two initialization sequence files and eight test sequence files. The README file provides all the information necessary to use that particular diskette. All test and initialization sequence files are in ASCII notation. Each value (or sample) of the test sequence files uses hexadecimal representation with two hex characters for each 8-bit value. Every line in every file contains 32 values (or 64 hex characters) and is terminated by a line feed character. The only exceptions to the above are the last lines of the initialization sequences which contain only 8 values (or 16 characters). For files containing 4-bit ADPCM values, the most significant hex value is set to zero. Two more hex characters representing a checksum computation over the entire file are appended to the end of each file. Checksum is computed by summing every sample value (two hex characters comprise a sample value) in the file and then finding the remainder when divided by 255. All the details about the names, lengths, and contents of each file are listed in the Tables II-5 and II-6/G.721.

TABLE II-5/G.721

Directory of Diskette 1

File type	File name	No. of values	Description
Initialization sequences	INIT1.MU INIT2.MU	3 496 3 496	PCM initialization ADPCM initialization
μ-law input and output sequences (Table II-2/G.721)	VECTOR1.MU VECTOR2.MU VECTOR3.MU	16 384 16 384 16 384	μ-law PCM encoder input sequence Corresponding ADPCM encoder output sequence Corresponding μ-law PCM output sequence
μ-law decoder-only test sequences (Table II-3/G.721)	VECTOR4.MU VECTOR4.MU	16 384 16 384	ADPCM decoder input sequence Corresponding μ-law PCM output sequence
μ-law input and output overload sequences	VECTOR6.MU VECTOR7.MU VECTOR8.MU	2 048 2 048 2 048	μ-law PCM encoder input sequence Corresponding ADPCM output sequence Corresponding μ-law PCM output sequence

TABLE II-6/G.721

Directory of Diskette 2

File type	File name	No. of values	Description
Initialization sequences	INIT1.A INIT2.A	3 496 3 496	PCM initialization ADPCM initialization
A-Law input and output sequences (Tableau II-2/G.721)	VECTOR1.A VECTOR2.A VECTOR3.A	16 384 16 384 16 384	A-law PCM encoder input sequence Corresponding ADPCM encoder output sequence Corresponding A-law PCM output sequence
A-law decoder-only test sequences (Table II-3/G.721)	VECTOR4.A VECTOR5.A	16 384 16 384	ADPCM decoder input sequence Corresponding A-law PCM output sequence
A-law input and output overload sequences	VECTOR6.A VECTOR7.A VECTOR8.A	2 048 2 048 2 048	A-law PCM encoder input sequence Corresponding ADPCM output sequence Corresponding A-law PCM output sequence

7 kHz AUDIO-CODING WITHIN 64 KBIT/S

(Melbourne, 1988)

1 General

1.1 *Scope and outline description*

This Recommendation describes the characteristics of an audio (50 to 7 000 Hz) coding system which may be used for a variety of higher quality speech applications. The coding system uses sub-band adaptive differential pulse code modulation (SB-ADPCM) within a bit rate of 64 kbit/s. The system is henceforth referred to as 64 kbit/s (7 kHz) audio coding. In the SB-ADPCM technique used, the frequency band is split into two sub-bands (higher and lower) and the signals in each sub-band are encoded using ADPCM. The system has three basic modes of operation corresponding to the bit rates used for 7 kHz audio coding: 64, 56 and 48 kbit/s. The latter two modes allow an auxiliary data channel of 8 and 16 kbit/s respectively to be provided within the 64 kbit/s by making use of bits from the lower sub-band.

Figure 1/G.722 identifies the main functional parts of the 64 kbit/s (7 kHz) audio codec as follows:

i) 64 kbit/s (7 kHz) audio encoder comprising:
   - a transmit audio part which converts an audio signal to a uniform digital signal which is coded using 14 bits with 16 kHz sampling;
   - a SB-ADPCM encoder which reduces the bit rate to 64 kbit/s.

ii) 64 kbit/s (7 kHz) audio decoder comprising:
   - a SB-ADPCM decoder which performs the reverse operation to the encoder, noting that the effective audio coding bit rate at the input of the decoder can be 64, 56 or 48 kbit/s depending on the mode of operation;
   - a receive audio part which reconstructs the audio signal from the uniform digital signal which is encoded using 14 bits with 16 kHz sampling.

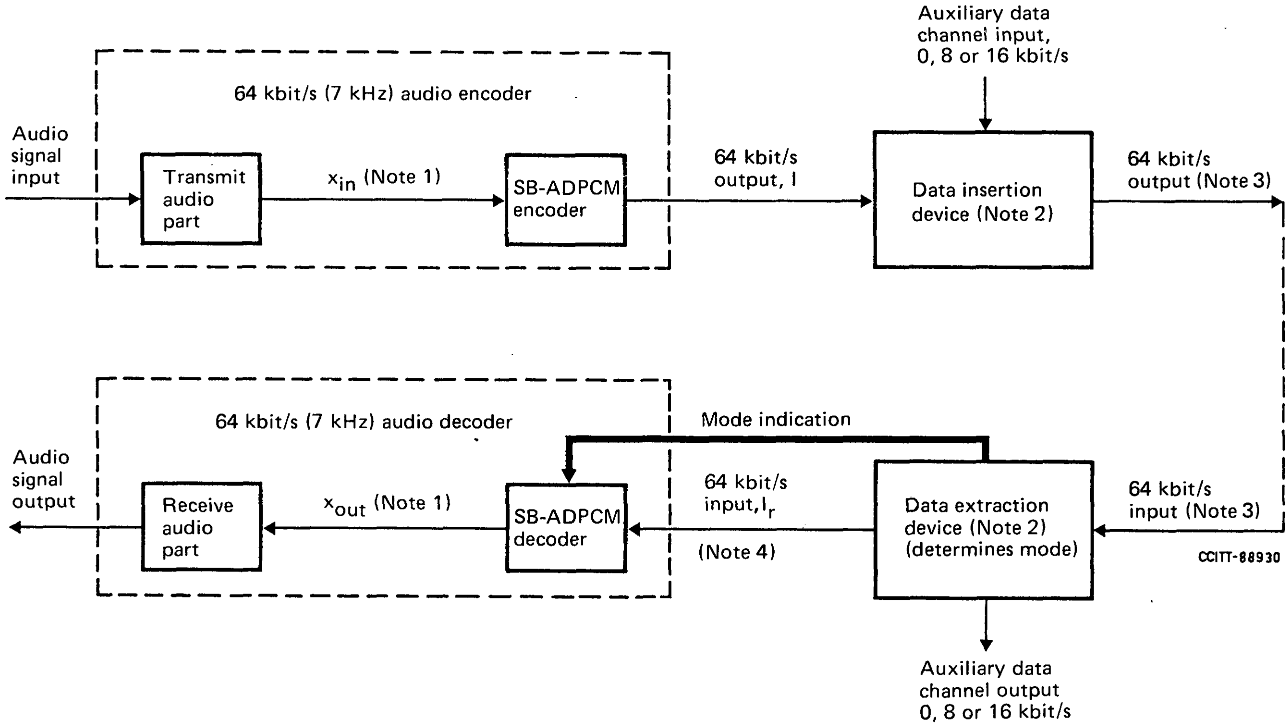
The following two parts, identified in Figure 1/G.722 for clarification, will be needed for applications requiring an auxiliary data channel within the 64 kbit/s:

- a data insertion device at the transmit end which makes use of, when needed, 1 or 2 audio bits per octet depending on the mode of operation and substitutes data bits to provide an auxiliary data channel of 8 or 16 kbit/s respectively;
- a data extraction device at the receive end which determines the mode of operation according to a mode control strategy and extracts the data bits as appropriate.

Paragraph 1.2 contains a functional description of the transmit and receive audio parts, § 1.3 describes the modes of operation and the implication of inserting data bits on the algorithms, whilst §§ 1.4 and 1.5 provide the functional descriptions of the SB-ADPCM encoding and decoding algorithms respectively. Paragraph 1.6 deals with the timing requirements. Paragraph 2 specifies the transmission characteristics of the 64 kbit/s (7 kHz) audio codec and of the transmit and receive audio parts, §§ 3 and 4 give the principles of the SB-ADPCM encoder respectively whilst §§ 5 and 6 specify the computational details of the Quadrature Mirror Filters (QMF) and of the ADPCM encoders and decoders respectively.

Networking aspects and test sequences are addressed in Appendices I and II respectively to this Recommendation.

Recommendation G.725 contains specifications for in-channel handshaking procedures for terminal identification and for mode control strategy, including interworking with existing 64 kbit/s PCM terminals.



Note 1 – x_{in} and x_{out} are digital signals uniformly coded with 14 bits and 16 kHz sampling.

Note 2 – These devices are only necessary for applications requiring an auxiliary data channel within the 64 kbit/s.

Note 3 – Comprises 64, 56 or 48 kbit/s for audio coding and 0, 8 or 16 kbit/s for data.

Note 4 – 64 kbit/s signal comprising 64, 56 or 48 kbit/s for audio coding depending on the mode of operation.

FIGURE 1/G.722

Simplified functional block diagram

1.2 *Functional description of the audio parts*

Figure 2/G.722 shows a possible arrangement of audio parts in a 64 kbit/s (7 kHz) audio coding terminal. The microphone, pre-amplifier, power amplifier and loudspeaker are shown simply to identify the audio parts and are not considered further in this Recommendation.

In order to facilitate the measurement of the transmission characteristics as specified in § 2, test points A and B need to be provided as shown. These test points may either be for test purposes only or, where the audio parts are located in different units from the microphone, loudspeaker, etc., correspond to physical interfaces.

The transmit and receive audio parts comprise either the following functional units or any equivalent items satisfying the specifications of § 2:

i) transmit:
   - an input level adjustment device,
   - an input anti-aliasing filter,
   - a sampling device operating at 16 kHz,
   - an analogue-to-uniform digital converter with 14 bits and with 16 kHz sampling;

ii) receive:
   - a uniform digital-to-analogue converter with 14 bits and with 16 kHz sampling,
   - a reconstructing filter which includes x/sin x correction,
   - an output level adjustment device.

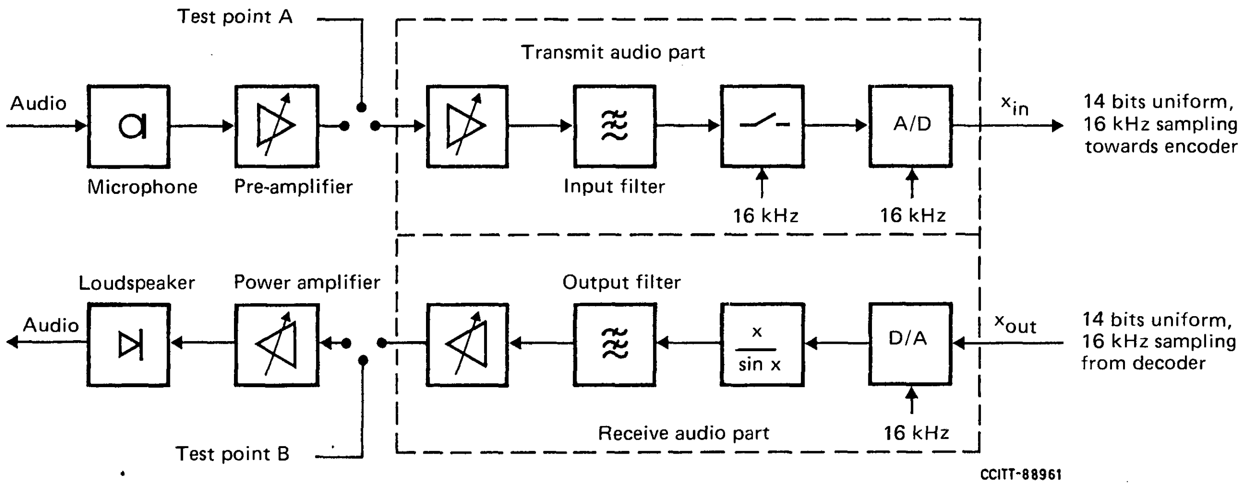


FIGURE 2/G.722

Possible implementation of the audio parts

1.3 *Possible modes of operation and implications of inserting data*

The three basic possible modes of operation which correspond to the bit rates available for audio coding at the input of the decoder are defined in Table 1/G.722.

TABLE 1/G.722

Basic possible modes of operation

Mode	7 kHz audio coding bit rate	Auxiliary data channel bit rate
1	64 kbit/s	0 kbit/s
2	56 kbit/s	8 kbit/s
3	48 kbit/s	16 kbit/s

See Appendix I for examples of applications using one or several of these modes and for their corresponding subjective quality.

The 64 kbit/s (7 kHz) audio encoder uses 64 kbit/s for audio coding at all times irrespective of the mode of operation. The audio coding algorithm has been chosen such that, without sending any indication to the encoder, the least significant bit or two least significant bits of the lower sub-band may be used downstream from the 64 kbit/s (7 kHz) audio encoder in order to substitute the auxiliary data channel bits. However, to maximize the audio performance for a given mode of operation, the 64 kbit/s (7 kHz) audio decoder must be optimized to the bit rate available for audio coding. Thus, this Recommendation describes three variants of the SB-ADPCM decoder and, for applications requiring an auxiliary data channel, an indication must be forwarded to select in the decoder the variant appropriate to the mode of operation. Figure 1/G.722 illustrates the arrangement. It should be noted that the bit rate at the input of the 64 kbit/s (7 kHz) audio decoder is always 64 kbit/s but comprising 64, 56 or 48 kbit/s for audio coding depending on the mode of operation. From an algorithm viewpoint, the variant used in the SB-ADPCM decoder can be changed in any octet during the transmission. When no indication about the mode of operation is forwarded to the decoder, the variant corresponding to Mode 1 should be used.

A mode mismatch situation, where the variant used in the 64 kbit/s (7 kHz) audio decoder for a given octet does not correspond to the mode of operation, will not cause misoperation of the decoder. However, to maximize the audio performance, it is recommended that the mode control strategy adopted in the data extraction device should be such as to minimize the duration of the mode mismatch. Appendix I gives further information on the effects of a mode mismatch. To ensure compatibility between various types of 64 kbit/s (7 kHz) audio coding terminals, it is recommended that, as a minimum, the variant corresponding to Mode 1 operation is always implemented in the decoder.

The mode control strategy could be derived from the auxiliary data channel protocol (see Recommendation G.725).

1.4 *Functional description of the SB-ADPCM encoder*

Figure 3/G.722 is a block diagram of the SB-ADPCM encoder. A functional description of each block is given below in §§ 1.4.1 to 1.4.4.

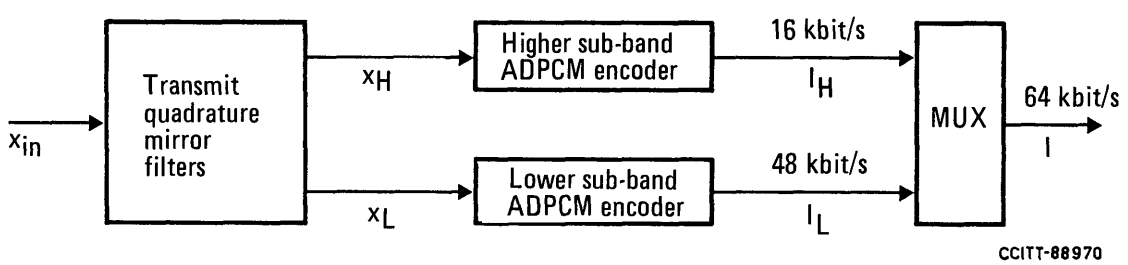


FIGURE 3/G.722

Block diagram of the SB-ADPCM encoder

1.4.1 *Transmit quadrature mirror filters* (QMFs)

The transmit QMFs comprise two linear-phase non-recursive digital filters which split the frequency band 0 to 8000 Hz into two sub-bands: the lower sub-band (0 to 4000 Hz) and the higher sub-band (4000 to 8000 Hz). The input to the transmit QMFs, x_{in}, is the output from the transmit audio part and is sampled at 16 kHz. The outputs, x_L and x_H, for the lower and higher sub-bands respectively, are sampled at 8 kHz.

1.4.2 *Lower sub-band ADPCM encoder*

Figure 4/G.722 is a block diagram of the lower sub-band ADPCM encoder. The lower sub-band input signal, x_L after subtraction of an estimate, s_L, of the input signal produces the difference signal, e_L. An adaptive 60-level non linear quantizer is used to assign six binary digits to the value of the difference signal to produce a 48 kbit/s signal, I_L.

In the feedback loop, the two least significant bits of I_L are deleted to produce a 4-bit signal I_{Lt}, which is used for the quantizer adaptation and applied to a 15-level inverse adaptive quantizer to produce a quantized difference signal, d_{Lt}. The signal estimate, s_L is added to this quantized difference signal to produce a reconstructed version, r_{Lt}, of the lower sub-band input signal. Both the reconstructed signal and the quantized difference signal are operated upon by an adaptive predictor which produce the estimate, s_L, of the input signal, thereby completing the feedback loop.

4-bit operation, instead of 6-bit operation, in the feedback loops of both the lower sub-band ADPCM encoder, and the lower sub-band ADPCM decoder allows the possible insertion of data in the two least significant bits as described in § 1.3 without causing misoperation in the decoder. Use of a 60-level quantizer (instead of 64-level) ensures that the pulse density requirements as described in Recommendation G.802 are met under all conditions and in all modes of operation.

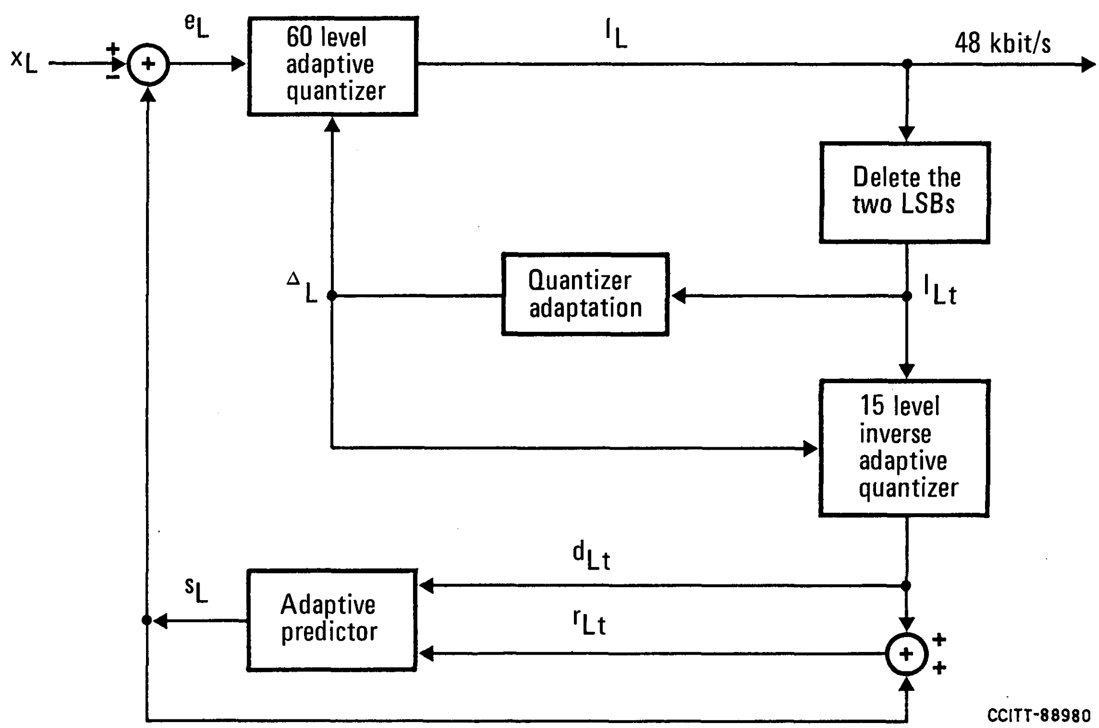


FIGURE 4/G.722

Block diagram of the lower sub-band ADPCM encoder

1.4.3 *Higher sub-band ADPCM encoder*

Figure 5/G.722 is a block diagram of the higher sub-band ADPCM encoder. The higher sub-band input signal, x_H after subtraction of an estimate, s_H, of the input signal, produces the difference signal, e_H. An adaptive 4-level non linear quantizer is used to assign two binary digits to the value of the difference signal to produce a 16 kbit/s signal, I_H.

An inverse adaptive quantizer produces a quantized difference signal, d_H, from these same two binary digits. The signal estimate, s_H, is added to this quantized difference signal to produce a reconstructed version, r_H, of the higher sub-band input signal. Both the reconstructed signal and the quantized difference signal are operated upon by an adaptive predictor which produces the estimate, s_H, of the input signal, thereby completing the feedback loop.

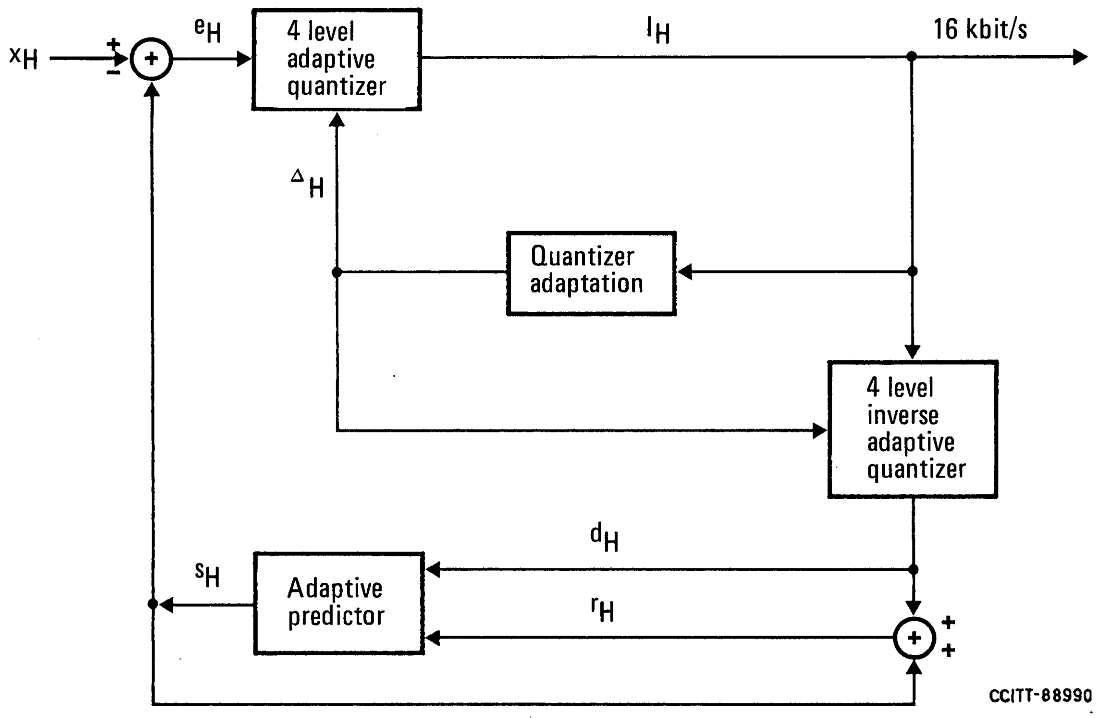


FIGURE 5/G.722

Block diagram of the higher sub-band ADPCM encoder

1.4.4 *Multiplexer*

The multiplexer (MUX) shown in Figure 3/G.722 is used to combine the signals, I_L and I_H, from the lower and higher sub-band ADPCM encoders respectively into a composite 64 kbit/s signal, I, with an octet format for transmission.

The output octet format, after multiplexing, is as follows:

$$I_{H1}\ I_{H2}\ I_{L1}\ I_{L2}\ I_{L3}\ I_{L4}\ I_{L5}\ I_{L6}$$

where I_{H1} is the first bit transmitted, and where I_{H1} and I_{L1} are the most significant bits of I_H and I_L respectively, whilst I_{H2} and I_{L6} are the least significant bits of I_H and I_L respectively.

1.5 *Functional description of the SB-ADPCM decoder*

Figure 6/G.722 is a block diagram of the SB-ADPCM decoder. A functional description of each block is given below in §§ 1.5.1 to 1.5.4.

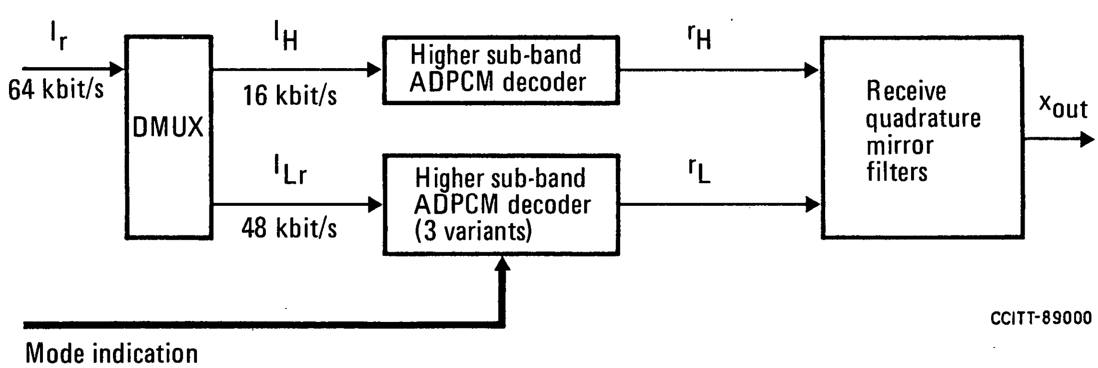


FIGURE 6/G.722

Block diagram of the SB-ADPCM decoder

1.5.1 *Demultiplexer*

The demultiplexer (DMUX) decomposes the received 64 kbit/s octet-formatted signal, I_r, into two signals, I_{Lr} and I_H, which form the codeword inputs to the lower and higher sub-band ADPCM decoders respectively.

1.5.2 *Lower sub-band ADPCM decoder*

Figure 7/G.722 is a block diagram of the lower sub-band ADPCM decoder. This decoder can operate in any of three possible variants depending on the received indication of the mode of operation.

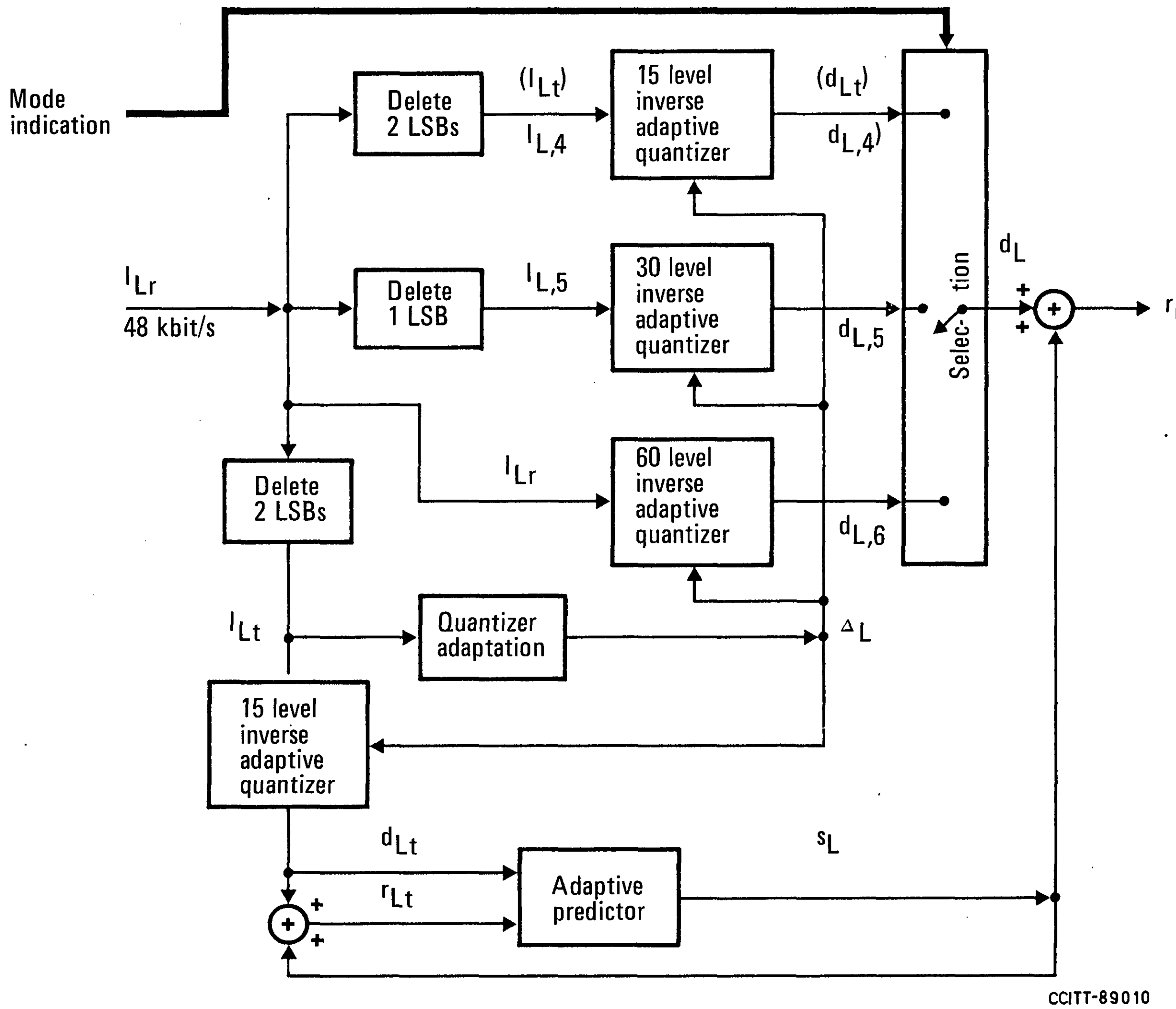


FIGURE 7/G.722

Block diagram of the lower sub-band ADPCM decoder

The path which produces the estimate, s_L, of the input signal including the quantizer adaptation, is identical to the feedback portion of the lower sub- band ADPCM encoder described in § 1.4.2. The reconstructed signal, r_L, is produced by adding to the signal estimate one of three possible quantized difference signals, $d_{L,6}$, $d_{L,5}$ or $d_{L,4}$ (= d_{Lt} - see note), selected according to the received indication of the mode of operation. For each indication, Table 2/G.722 shows the quantized difference signal selected, the inverse adaptive quantizer used and the number of least significant bits deleted from the input codeword.

TABLE 2/G.722

Lower sub-band ADPCM decoder variants

Received indication of mode of operation	Quantized difference signal selected	Inverse adaptive quantizer used	Number of least significant bits deleted from input codeword, I_{Lr}
Mode 1	$d_{L,6}$	60-level	0
Mode 2	$d_{L,5}$	30-level	1
Mode 3	$d_{L,4}$	15-level	2

Note – For clarification purposes, all three inverse quantizers have been indicated in the upper portion of Figure 7/G.722. In an optimized implementation, the signal d_{Lt}, produced in the predictor loop, could be substituted for $d_{L,4}$.

1.5.3 *Higher sub-band ADPCM decoder*

Figure 8/G.722 is a block diagram of the higher sub-band ADPCM decoder. This decoder is identical to the feedback portion of the higher sub-band ADPCM encoder described in § 1.4.3, the output being the reconstructed signal, r_H.

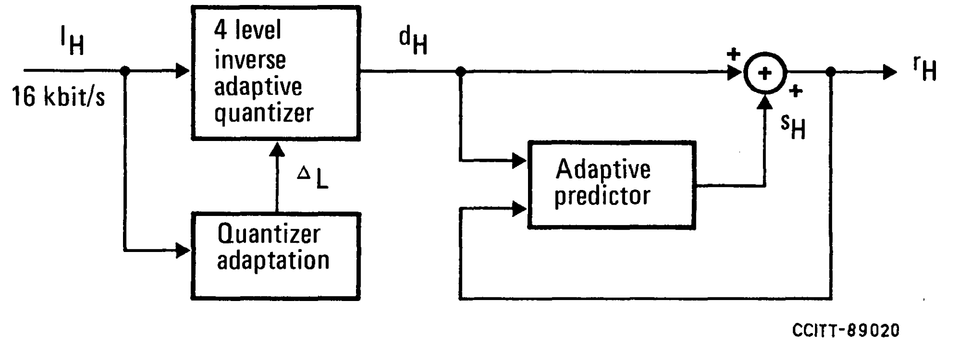


FIGURE 8/G.722

Block diagram of the higher sub-band ADPCM decoder

1.5.4 *Receive QMFs*

The receive QMFs shown in Figure 6/G.722 are two linear-phase non-recursive digital filters which interpolate the outputs, r_L and r_H, of the lower and higher sub-band ADPCM decoders from 8 kHz to 16 kHz and which then produce an output, x_{out}, sampled at 16 kHz which forms the input to the receive audio parts.

Excluding the ADPCM coding processes, the combination of the transmit and the receive QMFs has an impulse response which closely approximates a simple delay whilst, at the same time, the aliasing effects associated with the 8 kHz sub-sampling are cancelled.

1.6 *Timing requirements*

64 kHz bit timing and 8 kHz octet timing should be provided by the network to the audio decoder.

For a correct operation of the audio coding system, the precision of the 16 kHz sampling frequencies of the A/D and D/A converters must be better than $\pm 50 \cdot 10^{-6}$.

2 Transmission characteristics

2.1 *Characteristics of the audio ports and the test points*

Figure 2/G.722 indicates the audio input and output ports and the test points (A and B). It is for the designer to determine the characteristics of the audio ports and the test points (i.e. relative levels, impedances, whether balanced or unbalanced). The microphone, pre-amplifier, power amplifier and loudspeaker should be chosen with reference to the specifications of the audio parts: in particular their nominal bandwidth, idle noise and distortion.

It is suggested that input and ouput impedances should be high and low, respectively, for an unbalanced termination whilst for a balanced termination these impedances should be 600 ohms. However, the audio parts should meet all audio parts specifications for their respective input and output impedance conditions.

2.2 *Overload point*

The overload point for the analogue-to-digital and digital-to-analogue converters should be + 9 dBm0 ± 0.3 dB. This assumes the same nominal speech level (see Recommendation G.232) as for 64 kbit/s PCM, but with a wider margin for the maximum signal level which is likely to be necessary with conference arrangements. The measurement method of the overload point is under study.

2.3 *Nominal reference frequency*

Where a nominal reference frequency of 1000 Hz is indicated below, the actual frequency should be chosen equal to 1020 Hz. The frequency tolerance should be +2 to −7 Hz.

2.4 *Transmission characteristics of the 64 kbit/s (7 kHz) audio codec*

The values and limits specified below should be met with a 64 kbit/s (7 kHz) audio encoder and decoder connected back-to-back. For practical reasons, the measurements may be performed in a looped configuration as shown in Figure 9a)/G.722. However, such a looped configuration is only intended to simulate an actual situation where the encoder and decoder are located at the two ends of a connection.

These limits apply to operation in Mode 1.

2.4.1 *Nominal bandwidth*

The nominal 3 dB bandwidth is 50 to 7000 Hz.

2.4.2 *Attenuation/frequency distortion*

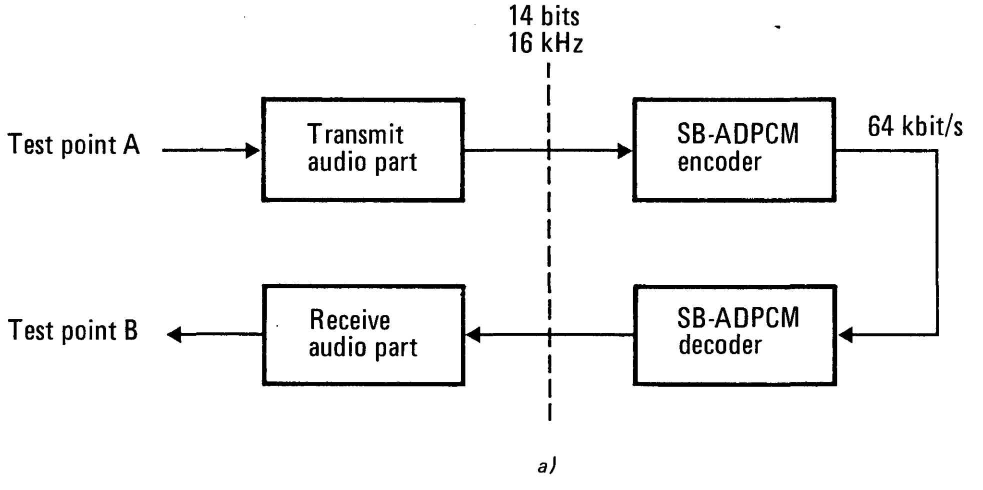
The variation with frequency of the attenuation should satisfy the limits shown in the mask of Figure 10/G.722. The nominal reference frequency is 1000 Hz and the test level is −10 dBm0.

2.4.3 *Absolute group delay*

The absolute group delay, defined as the minimum group delay for a sine wave signal between 50 and 7000 Hz, should not exceed 4 ms. The test level is −10 dBm0.

2.4.4 *Idle noise*

The unweighted noise power measured in the frequency range 50 to 7000 Hz with no signal at the input port (test point A) should not exceed −66 dBm0. When measured in the frequency range 50 Hz to 20 kHz the unweighted noise power should not exceed −60 dBm0.



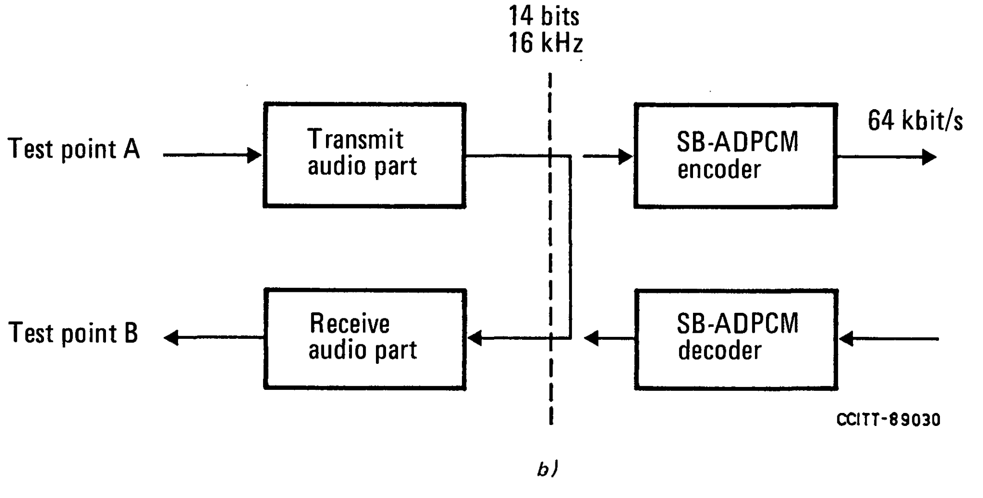


FIGURE 9/G.722

Looped measurement configurations

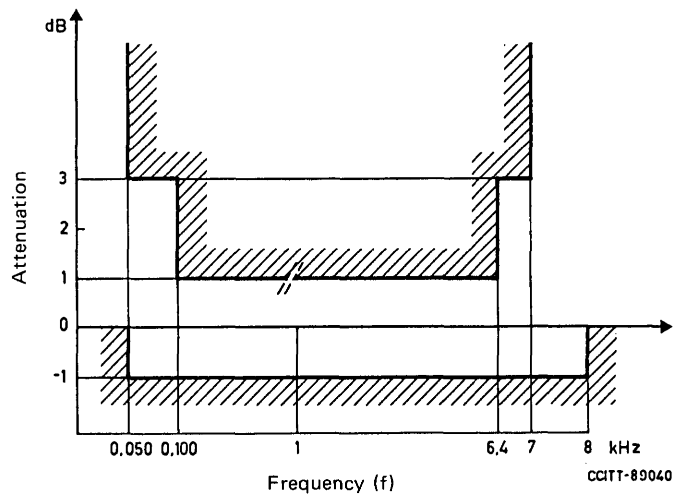


FIGURE 10/G.722

Attenuation distortion versus frequency

2.4.5 *Single frequency noise*

The level of any single frequency (in particular 8000 Hz, the sampling frequency and its multiples), measured selectively with no signal at the input port (test point A) should not exceed −70 dBm0.

2.4.6 *Signal-to-total distortion ratio*

Under study.

2.5 *Transmission characteristics of the audio parts*

When the measurements indicated below for the audio parts are from audio-to-audio, a looped configuration as shown in Figure 9b)/G.722 should be used. The audio parts should also meet the specifications of § 2.4 with the measurement configuration of Figure 9b)/G.722.

2.5.1 *Attenuation/frequency response of the input anti-aliasing filter*

The in-band and out-of-band attenuation/frequency response of the input anti-aliasing filter should satisfy the limits of the mask shown in Figure 11/G.722. The nominal reference frequency is 1000 Hz and the test level for the in-band characteristic is −10 dBm0. Appropriate measurements should be made to check the out-of-band characteristic taking into account the aliasing due to the 16 kHz sampling.

2.5.2 *Attenuation/frequency response of the output reconstructing filter*

The in-band and out-of-band attenuation/frequency response of the output reconstructing filter should satisfy the limits of the mask shown in Figure 12/G.722. The nominal reference frequency is 1000 Hz and the test level for the in-band characteristic is −10 dBm0. Appropriate measurements should be made to check the out-of-band characteristic taking into account the aliasing due to the 16 kHz sampling. The mask of Figure 12/G.722 is valid for the whole of the receive audio part including any pulse amplitude modulation distortion and x/sin x correction.

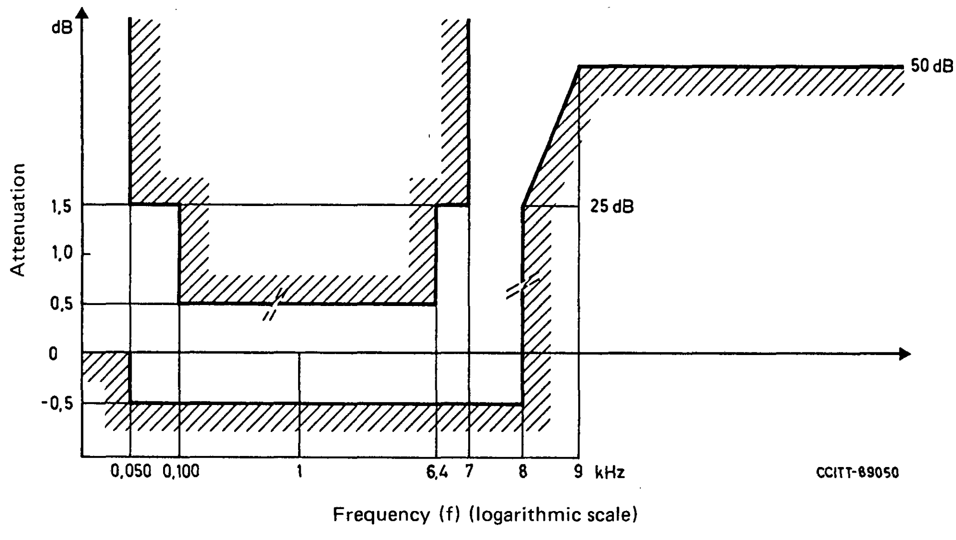


FIGURE 11/G.722

Attenuation/frequency response of the input antialiasing filter

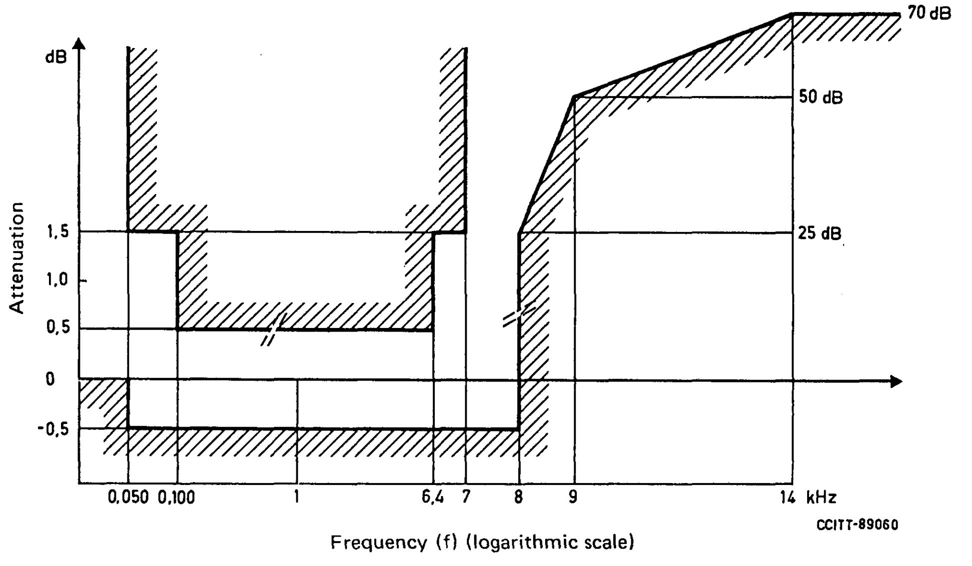


FIGURE 12/G.722

Attenuation/frequency response of the output reconstructing filter (including x/sin x correction)

2.5.3 *Group-delay distortion with frequency*

The group-delay distortion, taking the minimum value of group delay as a reference, should satisfy the limits of the mask shown in Figure 13/G.722.

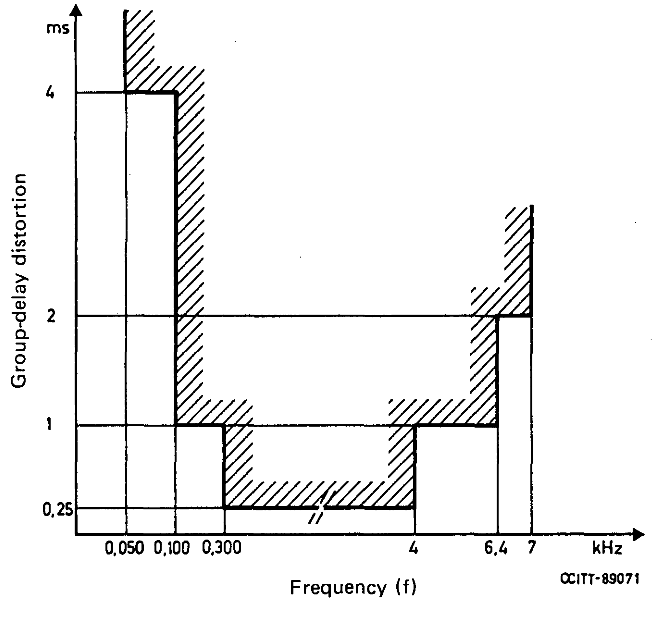


FIGURE 13/G.722

Group-delay distortion versus frequency

2.5.4 *Idle noise for the receive audio part*

The unweighted noise power of the receive audio part measured in the frequency range 50 to 7000 Hz with a 14-bit all-zero signal at its input should not exceed −75 dBm0.

2.5.5 *Signal-to-total distortion ratio as a function of input level*

With a sine wave signal at a frequency excluding simple harmonic relationships with the 16 kHz sampling frequency, applied to test point A, the ratio of signal-to-total distortion power as a function of input level measured unweighted in the frequency range 50 to 7000 Hz at test point B, should satisfy the limits of the mask shown in Figure 14/G.722. Two measurements should be performed, one at a frequency of about 1 kHz and the other at a frequency of about 6 kHz.

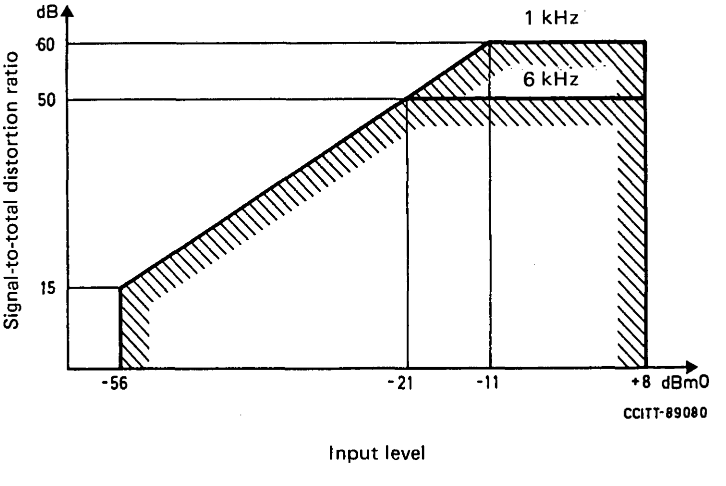


FIGURE 14/G.722

Signal-to-total distortion ratio as a function of input level

2.5.6 *Signal-to-total distortion ratio as a function of frequency*

With a sine wave signal at a level of −10 dBm0 applied to test point A, the ratio of signal-to-total distortion power as a function of frequency measured unweighted in the frequency range 50 to 7000 Hz at test point B should satisfy the limits of the mask shown in Figure 15/G.722.

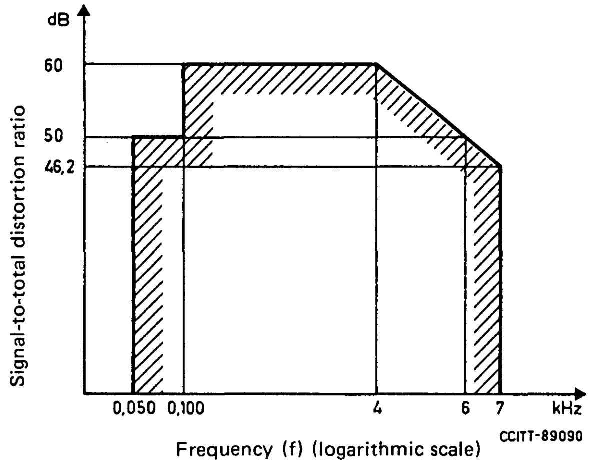


FIGURE 15/G.722

Signal-to-total distortion ratio as a function of frequency

2.5.7 *Variation of gain with input level*

With a sine wave signal at the nominal reference frequency of 1000 Hz, but excluding the sub-multiple of the 16 kHz sampling frequency, applied to test point A, the gain variation as a function of input level relative to the gain at an input level of −10 dBm0 measured selectively at test point B, should satisfy the limits of the mask shown in Figure 16/G.722.

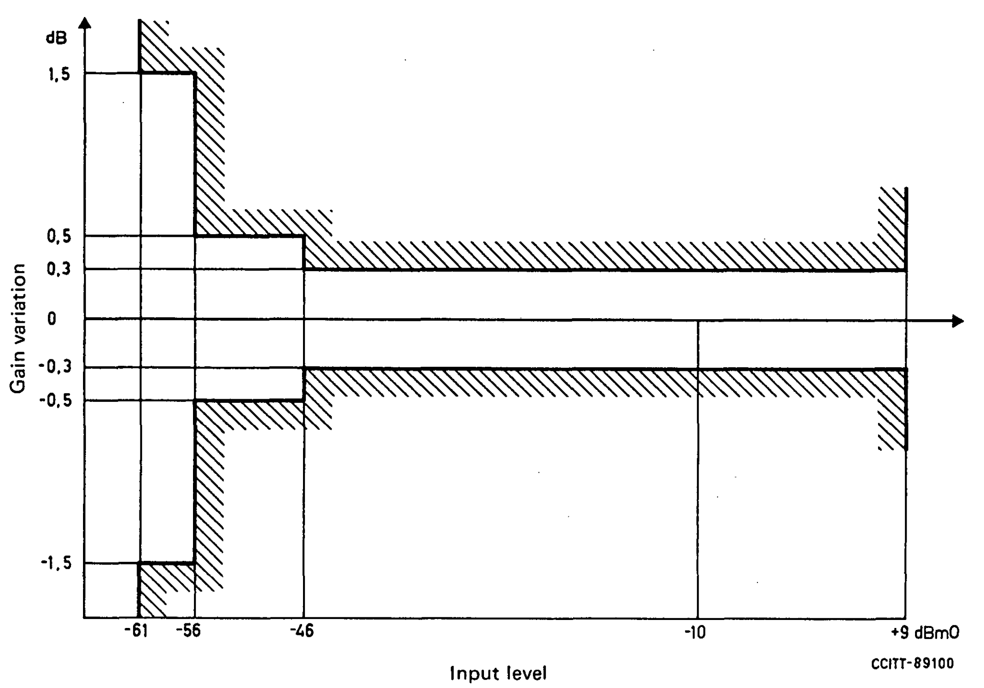


FIGURE 16/G.722

Variation of gain with input level

2.5.8 *Intermodulation*

Under study.

2.5.9 *Go/return crosstalk*

The crosstalk from the transmit direction to the receive direction should be such that, with a sine wave signal at any frequency in the range 50 to 7000 Hz and at a level of +6 dBm0 applied to test point A, the crosstalk level measured selectively at test point B should not exceed −64 dBm0. The measurement should be made with a 14-bit all-zero digital signal at the input to the receive audio part.

The crosstalk from the receive direction to the transmit direction should be such that, with a digitally simulated sine wave signal at any frequency in the range of 50 to 7000 Hz and a level of +6 dBm0 applied to the input of the receive audio part, the crosstalk level measured selectively and with the measurement made digitally at the output of the transmit audio part should not exceed −64 dBm0. The measurement should be made with no signal at test point A, but with the test point correctly terminated.

2.6 *Transcoding to and from 64 kbit/s PCM*

For compatibility reasons with 64 kbit/s PCM, transcoding between 64 kbit/s (7 kHz) audio coding and 64 kbit/s PCM should take account of the relevant specifications of Recommendations G.712, G.713 and G.714. When the audio signal is to be heard through a loudspeaker, more stringent specifications may be necessary. Further information may be found in Appendix I.

3 SB-ADPCM encoder principles

A block diagram of the SB-ADPCM encoder is given in Figure 3/G.722. Block diagrams of the lower and higher sub-band ADPCM encoders are given respectively in Figures 4/G.722 and 5/G.722.

Main variables used for the descriptions in §§ 3 and 4 are summarized in Table 3/G.722. In these descriptions, index (j) indicates a value corresponding to the current 16 kHz sampling interval, index $(j-1)$ indicates a value corresponding to the previous 16 kHz sampling interval, index (n) indicates a value corresponding to the current 8 kHz sampling interval, and index $(n-1)$ indicates a value corresponding to the previous 8 kHz sampling interval. Indices are not used for internal variables, i.e. those employed only within individual computational blocks.

3.1 *Transmit QMF*

A 24-coefficient QMF is used to compute the lower and higher sub-band signal components. The QMF coefficient values, h_i, are given in Table 4/G.722.

The output variables, $x_L(n)$ and $x_H(n)$, are computed in the following way:

$$x_L(n) = x_A + x_B \tag{3-1}$$

$$x_H(n) = x_A - x_B \tag{3-2}$$

$$x_A = \sum_{i=0}^{11} h_{2i} \cdot x_{in}(j - 2i) \tag{3-3}$$

$$x_B = \sum_{i=0}^{11} h_{2i+1} \cdot x_{in}(j - 2i - 1) \tag{3-4}$$

3.2 *Difference signal computation*

The difference signals, $e_L(n)$ and $e_H(n)$, are computed by subtracting predicted values, $s_L(n)$ and $s_H(n)$, from the lower and higher sub-band input values, $x_L(n)$ and $x_H(n)$:

$$e_L(n) = x_L(n) - s_L(n) \tag{3-5}$$

$$e_H(n) = x_H(n) - s_H(n) \tag{3-6}$$

TABLE 3/G.722

Variables used in the SB-ADPCM encoder and decoder descriptions

Variable	Description
x_{in}	Input value (uniform representation)
x_L, x_H	QMF output signals
S_{Lp}, S_{Hp}	Pole-predictor output signals
$a_{L,i}$, $a_{H,i}$	Pole-predictor coefficients
r_L, r_{Lt}, r_H	Reconstructed signals (non truncated and truncated)
$b_{L,i}$, $b_{H,i}$	Zero-predictor coefficients
d_L, d_{Lt}, d_H	Quantized difference signals (non truncated and truncated)
S_{Lz}, S_{Hz}	Zero-predictor output signals
S_L, S_H	Predictor output signals
e_L, e_H	Difference signals to be quantized
∇_L, ∇_H	Logarithmic quantizer scale factors
Δ_L, Δ_H	Quantizer scale factor (linear)
I_L, I_{Lt}, I_H	Codewords (non truncated and truncated)
P_{Lt}, P_H	Partially reconstructed signals
I_{Lr}	Received lower sub-band codeword
X_{out}	Output value (uniform)

Note – Variables used exclusively within one section are not listed. Subscripts L and H refer to lower sub-band and higher sub-band values. Subscript Lt denotes values generated from the truncated 4-bit codeword as opposed to the nontruncated 6-bit (encoder) or 6-, 5- or 4-bit (decoder) codewords.

TABLE 4/G.722

Transmit and receive OMF coefficient values

h_0 , h_{23}	0.366211E−03
h_1 , h_{22}	−0.134277E−02
h_2 , h_{21}	−0.134277E−02
h_3 , h_{20}	0.646973E−02
h_4 , h_{19}	0.146484E−02
h_5 , h_{18}	−0.190430E−01
h_6 , h_{17}	0.390625E−02
h_7 , h_{16}	0.441895E−01
h_8 , h_{15}	−0.256348E−01
h_9 , h_{14}	−0.982666E−01
h_{10}, h_{13}	0.116089E+00
h_{11}, h_{12}	0.473145E+00

3.3 *Adaptive quantizer*

The difference signals, $e_L(n)$ and $e_H(n)$, are quantized to 6 and 2 bits for the lower and higher sub-bands respectively. Tables 5/G.722 and 6/G.722 give the decision levels and the output codes for the 6- and 2-bit quantizers respectively. In these tables, only the positive decision levels are indicated, the negative levels can be determined by symmetry. m_L and m_H are indices for the quantizer intervals. The interval boundaries, $LL6$, $LU6$, HL and HU, are scaled by computed scale factors, $\Delta_L(n)$ and $\Delta_H(n)$ (see § 3.5). Indices, m_L and m_H, are then determined to satisfy the following:

$$LL6(m_L) \cdot \Delta_L(n) \leqslant e_L(n) < LU6(m_L) \cdot \Delta_L(n) \tag{3-7}$$

$$HL(m_H) \cdot \Delta_H(n) \leqslant e_H(n) < HU(m_H) \cdot \Delta_H(n) \tag{3-8}$$

for the lower and higher sub-bands respectively.

The output codes, ILN and IHN, represent negative intervals, whilst the output codes, ILP and IHP, represent positive intervals. The output codes, $I_L(n)$ and $I_H(n)$, are then given by:

$$I_L(n) = \begin{cases} ILP(m_L), \text{ if } e_L(n) \geqslant 0 \\ ILN(m_L), \text{ if } e_L(n) < 0 \end{cases} \tag{3-9}$$

$$I_H(n) = \begin{cases} IHP(m_H), \text{ if } e_H(n) \geqslant 0 \\ IHN(m_H), \text{ if } e_H(n) < 0 \end{cases} \tag{3-10}$$

for the lower and higher sub-bands respectively.

TABLE 5/G.722

Decision levels and output codes for the 6-bit lower sub-band quantizer

m_L	LL6	LU6	ILN	ILP
1	0.00000	0.06817	111111	111101
2	0.06817	0.14103	111110	111100
3	0.14103	0.21389	011111	111011
4	0.21389	0.29212	011110	111010
5	0.29212	0.37035	011101	111001
6	0.37035	0.45482	011100	111000
7	0.45482	0.53929	011011	110111
8	0.53929	0.63107	011010	110110
9	0.63107	0.72286	011001	110101
10	0.72286	0.82335	011000	110100
11	0.82335	0.92383	010111	110011
12	0.92383	1.03485	010110	110010
13	1.03485	1.14587	010101	110001
14	1.14587	1.26989	010100	110000
15	1.26989	1.39391	010011	101111
16	1.39391	1.53439	010010	101110
17	1.53439	1.67486	010001	101101
18	1.67486	1.83683	010000	101100
19	1.83683	1.99880	001111	101011
20	1.99880	2.19006	001110	101010
21	2.19006	2.38131	001101	101001
22	2.38131	2.61482	001100	101000
23	2.61482	2.84833	001011	100111
24	2.84833	3.14822	001010	100110
25	3.14822	3.44811	001001	100101
26	3.44811	3.86796	001000	100100
27	3.86796	4.28782	000111	100011
28	4.28782	4.99498	000110	100010
29	4.99498	5.70214	000101	100001
30	5.70214	∞	000100	100000

Note – If a transmitted codeword for the lower sub-band signal has been transformed, due to transmission errors to one of the four suppressed codewords "0000XX", the received code word is set at "111111".

TABLE 6/G.722

Decision levels and output codes for the 2-bit higher sub-band quantizer

m_H	HL	HH	IHN	IHP
1	0	1.10156	01	11
2	1.10156	∞	00	10

3.4 *Inverse adaptive quantizers*

3.4.1 *Inverse adaptive quantizer in the lower sub-band ADPCM encoder*

The lower sub-band output code, $I_L(n)$, is truncated by two bits to produce $I_{Lt}(n)$. The 4-bit codeword, $I_{Lt}(n)$, is converted to the truncated quantized difference signal, $d_{Lt}(n)$, using the $QL4^{-1}$ output values of Table 7/G.722, and scaled by the scale factor, $\Delta_L(n)$:

$$d_{Lt}(n) = QL4^{-1}[I_{Lt}(n)] \cdot \Delta_L(n) \cdot \mathrm{sgn}[I_{Lt}(n)] \qquad (3\text{-}11)$$

where sgn $[I_{Lt}(n))$ is derived from the sign of $e_L(n)$ defined in Equation 3-9.

There is a unique mapping, shown in Table 7/G.722, between four adjacent 6-bit quantizer intervals and the $QL4^{-1}$ output values. $QL4^{-1}[I_{Lt}(n)]$ is determined in two steps: first determination of the quantizer interval index, m_L, corresponding to $I_L(n)$ from Table 5/G.722, and then determination of $Q_L4^{-1}(m_L)$ by reference to Table 7/G.722.

TABLE 7/G.722

Output values and multipliers for 6, 5 and 4-bit lower sub-band inverse quantizers

m_L	$QL6^{-1}$	$QL5^{-1}$	$QL4^{-1}$	W_L
			0.0000	−0.02930
1	0.03409	0.06817		
2	0.10460			
3	0.17746	0.21389		
4	0.25300		0.29212	−0.01465
5	0.33124	0.37035		
6	0.41259			
7	0.49706	0.53929		
8	0.58518		0.63107	0.02832
9	0.67697	0.72286		
10	0.77310			
11	0.87359	0.92383		
12	0.97934		1.03485	0.08398
13	1.09036	1.14587		
14	1.20788			
15	1.33191	1.39391		
16	1.46415		1.53439	0.16309
17	1.60462	1.67486		
18	1.75585			
19	1.91782	1.99880		
20	2.09443		2.19006	0.26270
21	2.28568	2.38131		
22	2.49806			
23	2.73157	2.84833		
24	2.99827		3.14822	0.58496
25	3.29816	3.44811		
26	3.65804			
27	4.07789	4.28782		
28	4.64140		4.99498	1.48535
29	5.34856	5.70214		
30	6.05572			

3.4.2 *Inverse adaptive quantizer in the higher sub-band ADPCM encoder*

The higher sub-band output code, $I_H(n)$ is converted to the quantized difference signal, $d_H(n)$, using the $Q2^{-1}$ output values of Table 8/G.722 and scaled by the scale factor, $\Delta_H(n)$:

$$d_H(n) = Q2^{-1}\,[I_H(n)] \cdot \Delta_H(n) \cdot \mathrm{sgn}[I_H(n)] \tag{3-12}$$

where $\mathrm{sgn}[I_H(n)]$ is derived from the sign of $e_H(n)$ defined in Equation (3-10), and where $Q_2^{-1}[I_H(n)]$ is determined in two steps: first determine the quantizer interval index, m_H, corresponding to $I_H(n)$ from Table 6/G.722 and then determine $Q2^{-1}(m_H)$ by reference to Table 8/G.722.

TABLE 8/G.722

Output values and multipliers for the 2-bit higher sub-band quantizer

m_H	$Q2^{-1}$	W_H
1	0.39453	−0.10449
2	1.80859	0.38965

3.5 *Quantizer adaptation*

This block defines $\Delta_L(n)$ and $\Delta_H(n)$, the scaling factors for the lower and higher sub-band quantizers. The scaling factors are updated in the log domain and subsequently converted to a linear representation. For the lower sub-band, the input is $I_{Lt}(n)$, the codeword truncated to preserve the four most significant bits. For the higher sub-band, the 2-bit quantizer output, $I_H(n)$, is used directly.

Firstly the log scaling factors, $\Delta_L(n)$ and $\Delta_H(n)$, are updated as follows:

$$\nabla_L(n) = \beta \cdot \nabla_L(n-1) + W_L[I_{Lt}(n-1)] \tag{3-13}$$

$$\nabla_H(n) = \beta \cdot \nabla_H(n-1) + W_H[I_H(n-1)] \tag{3-14}$$

where W_L and W_H are logarithmic scaling factors multipliers given in Tables 7/G.722 and 8/G.722, and B is a leakage constant equal to 127/128.

Then the log scaling factors are limited, according to:

$$0 \leqslant \nabla_L(n) \leqslant 9 \tag{3-15}$$

$$0 \leqslant \nabla_H(n) \leqslant 11 \tag{3-16}$$

Finally, the linear scaling factors are computed from the log scaling factors, using an approximation of the inverse $\log_2$ function:

$$\Delta_L(n) = 2[\nabla_L(n) + 2] \cdot \Delta_{min} \tag{3-17}$$

$$\Delta_H(n) = 2\nabla_H(n) \cdot \Delta_{min} \tag{3-18}$$

where Δ_{min} is equal to half the quantizer step size of the 14 bit analogue-to-digital converter.

3.6 *Adaptive prediction*

3.6.1 *Predicted value computations*

The adaptive predictors compute predicted signal values, $s_L(n)$ and $s_H(n)$, for the lower and higher sub-bands respectively.

Each adaptive predictor comprises two sections: a second-order section that models poles, and a sixth-order section that models zeroes in the input signal.

The second order pole sections (coefficients $a_{L,i}$ and $a_{H,}i$) use the quantized reconstructed signals, $rL_t(n)$ and $r_H(n)$, for prediction. The sixth order zero sections (coefficients $b_{L,i}$) and $b_{H,}i$) use the quantized difference signals, $d_{Lt}(n)$ and $d_H(n)$. The zero-based predicted signals, $s_{Lz}(n)$ and $s_{Hz}(n)$, are also employed to compute partially reconstructed signals as described in § 3.6.2.

Firstly, the outputs of the pole sections are computed as follows:

$$s_{Lp} = \sum_{i=1}^{2} a_{L,i}(n - 1) \cdot r_{Lt}(n - i) \tag{3-19}$$

$$s_{Hp} = \sum_{i=1}^{2} a_{H,i}(n - 1) \cdot r_H(n - i) \tag{3-20}$$

Similarly, the outputs of the zero sections are computed as follows:

$$s_{Lz}(n) = \sum_{i=1}^{6} b_{L,i}(n - 1) \cdot d_{Lt}(n - i) \tag{3-21}$$

$$s_{Hz}(n) = \sum_{i=1}^{6} b_{H,i}(n - 1) \cdot d_H(n - i) \tag{3-22}$$

Then, the intermediate predicted values are summed to produce the predicted signal values:

$$s_L(n) = s_{Lp} + s_{Lz}(n) \tag{3-23}$$

$$s_H(n) = s_{Hp} + s_{Hz}(n) \tag{3-24}$$

3.6.2 *Reconstructed signal computation*

The quantized reconstructed signals, $r_{Lt}(n)$ and $r_H(n)$, are computed as follows:

$$r_{Lt}(n) = s_L(n) + d_{Lt}(n) \tag{3-25}$$

$$r_H(n) = s_H(n) + d_H(n) \tag{3-26}$$

The partially reconstructed signals, $p_{Lt}(n)$ and $p_H(n)$, used for the pole section adaptation, are then computed:

$$p_{Lt}(n) = d_{Lt}(n) + s_{Lz}(n) \tag{3-27}$$

$$p_H(n) = d_H(n) + s_{Hz}(n) \tag{3-28}$$

3.6.3 *Pole section adaptation*

The second order pole section is adapted by updating the coefficients, $a_{L,1}$, $a_{H,1}$, $a_{H,2}$, using a simplified gradient algorithm:

$$a_{L,1}(n) = (1 - 2^{-8})a_{L,1}(n - 1) + 3 \cdot 2^{-8} \cdot p_A \tag{3-29}$$

$$a_{L,2}(n) = (1 - 2^{-7})a_{L,2}(n - 1) + 2^{-7} \cdot p_B - 2^{-7} \cdot f \cdot p_A \tag{3-30}$$

where

$$p_A = \text{sgn2}[p_{Lt}(n)] \cdot \text{sgn2}[p_{Lt}(n - 1)] \tag{3-31}$$

$$p_B = \text{sgn2}[p_{Lt}(n)] \cdot \text{sgn2}[p_{Lt}(n - 2)] \tag{3-32}$$

with

$$\text{sgn2}(q) = \begin{cases} +1, & q \geqslant 0 \\ -1, & q < 0 \end{cases} \tag{3-33}$$

and

$$f = \begin{cases} 4a_{L,1}(n - 1), & |a_{L,1}| \leqslant 1/2 \\ 2\ \text{sgn}[a_{L,1}(n - 1)], & |a_{L,1}| > 1/2 \end{cases} \tag{3-34}$$

Then the following stability constraints are imposed:

$$|a_{L,2}| \leqslant 0{,}75 \tag{3-35}$$

$$|a_{L,1}| \leqslant 1 - 2^{-4} - a_{L,2} \tag{3-36}$$

$a_{H,1}(n)$ and $a_{H,2}(n)$ are similarly computed, replacing $a_{L,1}(n)$, $a_{L,2}(n)$ and $P_{Lt}(n)$ by $a_{H,1}(n)$, $a_{H,2}(n)$ and $P_H(n)$, respectively.

3.6.4 *Zero section adaptation*

The sixth order zero predictor is adapted by updating the coefficients $b_{L,i}$ and $b_{H,i}$ using a simplified gradient algorithm:

$$b_{L,i}(n) = (1 - 2^{-8})\ b_{L,i}(n - 1) + 2^{-7}\ \text{sgn3}[d_{Lt}(n)] \cdot \text{sgn2}[d_{Lt}(n - i)] \tag{3-37}$$

for $i = 1, 2 \ldots 6$

and with

$$\text{sgn3}(q) = \begin{cases} +1, & q > 0 \\ 0, & q = 0 \\ -1, & q < 0 \end{cases} \tag{3-38}$$

where $b_{L,i}(n)$ is implictly limited to $\pm$ 2.

$b_{H,i}(n)$ are similarly updated, replacing $b_{L,i}(n)$ and $d_{Lt}(n)$ by $b_{H,i}(n)$ and $d_H(n)$ respectively.

4 SB-ADPCM decoder principles

A block diagram of the SB-ADPCM decoder is given in Figure 6/G.722 and block diagrams of the lower and higher sub-band ADPCM decoders are given respectively in Figures 7/G.722 and 8/G.722.

The input to the lower sub-band ADPCM decoder, I_{Lr}, may differ from I_L even in the absence of transmission errors, in that one or two least significant bits may have been replaced by data.

4.1 *Inverse adaptive quantizer*

4.1.1 *Inverse adaptive quantizer selection for the lower sub-band ADPCM decoder*

According to the received indication of the mode of operation the number of least significant bits which should be truncated from the input codeword I_{Lr}, and the choice of the inverse adaptive quantizer are determined, as shown in Table 2/G.722.

For operation in mode 1, the 6-bit codeword, $I_{Lr}(n)$, is converted to the quantized difference, $d_L(n)$, according to $QL6^{-1}$ output values of Table 7/G.722, and scaled by the scale factor, $\Delta_L(n)$:

$$d_L(n) = QL6^{-1}\,[I_{Lr}(n)] \cdot \Delta_L(n) \cdot \mathrm{sgn}[I_{Lr}(n)] \tag{4-1}$$

where $\mathrm{sgn}[I_{Lr}(n)]$ is derived from the sign of $I_L(n)$ defined in equation (3-9).

Similarly, for operations in mode 2 or mode 3, the truncated codeword (by one or two bits) is converted to the quantized difference signal, $d_L(n)$, according to $QL5^{-1}$ or $QL4^{-1}$ output values of Table 7/G.722 respectively.

There are unique mappings, shown in Table 7/G.722, between two or four adjacent 6-bit quantizer intervals and the $QL5^{-1}$ or $QL4^{-1}$ output values respectively.

In the computations above, the output values are determined in two steps: first determination of the quantizer interval index, m_L, corresponding to $I_{Lr}(n)$ from Table 5/G.722, and then determination of the output values corresponding to m_L by reference to Table 7/G.722.

The inverse adaptive quantizer, used for the computation of the predicted value and for adaptation of the quantizer and predictor, is described in § 3.4.1, but with $I_L(n)$ replaced by $I_{Lr}(n)$.

4.1.2 *Inverse adaptive quantizer for the higher sub-band ADPCM decoder*

See § 3.4.2.

4.2 *Quantizer adaptation*

See § 3.5.

4.3 *Adaptive prediction*

4.3.1 *Predicted value computation*

See § 3.6.1.

4.3.2 *Reconstructed signal computation*

See § 3.6.2.

The output reconstructed signal for the lower sub-band ADPCM decoder, $r_L(n)$, is computed from the quantized difference signal, $d_L(n)$, as follows:

$$r_L(n) = s_L(n) + d_L(n) \tag{4-2}$$

4.3.3 *Pole section adaptation*

See § 3.6.3.

4.3.4 *Zero section adaptation*

See § 3.6.4.

4.4 *Receive QMF*

A 24-coefficient QMF is used to reconstruct the output signal, $x_{\mathrm{out}}(j)$, from the reconstructed lower and higher sub-band signals, $r_L(n)$ and $r_H(n)$. The QMF coefficient values, h_i, are the same as those used in the transmit QMF and are given in Table 4/G.722.

The output signals, $x_{out}(j)$ and $x_{out}(j+1)$, are computed in the following way:

$$x_{out}(j) = 2 \sum_{i=0}^{11} h_{2i} \cdot x_d(i) \tag{4-3}$$

$$x_{out}(j+1) = 2 \sum_{i=0}^{11} h_{2i+1} \cdot x_s(i) \tag{4-4}$$

where

$$x_d(i) = r_L(n-i) - r_H(n-i) \tag{4-5}$$

$$x_s(i) = r_L(n-i) + r_H(n-i) \tag{4-6}$$

5 Computational details for QMF

5.1 *Input and output signals*

Table 9/G.722 defines the input and output signals for the transmit and receive QMF. All input and output signals have 16-bit word lengths, which are limited to a range of −16384 to 16383 in 2's complement notation. Note that the most significant magnitude bit of the A/D output and the D/A input appears at the third bit location in XIN and XOUT, respectively.

TABLE 9/G.722

Representation of input and output signals

	Name	Binary representation	Description
Transmit QMF			
Input	XIN	S, S, −2, −3, ..., −14, −15	Input value (uniformly quantized)
Output	XL	S, S, −2, −3, ..., −14, −15	Output signal for lower sub-band encoder
Output	XH	S, S, −2, −3, ..., −14, −15	Output signal for higher sub-band encoder
Receive QMF			
	Name	Binary representation	Description
Input	RL	S, S, −2, −3, ..., −14, −15	Lower sub-band reconstructed signal
Input	RH	S, S, −2, −3, ..., −14, −15	Higher sub-band reconstructed signal
Output	XOUT	S, S, −2, −3, ..., −14, −15	Output value (uniformly quantized)

Note – XIN and XOUT are represented in a sign-extended 15-bit format, where the LSB is set to "0" for 14-bit converters.

5.2 *Description of variables and detailed specification of sub-blocks*

This section contains a detailed expansion of the transmit and receive QMF. The expansions are illustrated in Figures 17/G.722 and 18/G.722 with the internal variables given in Table 10/G.722, and the QMF coefficients given in Table 11/G.722. The word lengths of internal variables, XA, XB and WD must be equal to or greater than 24 bits (see Note). The other internal variables have a minimum of 16 bit word lengths. A brief functional description and the full specification is given for each sub-block.

The notations used in the block descriptions are as follows:

- $\gg$ n denotes an *n*-bit arithmetic shift right operation (sign extension),
- $+$ denotes arithmetic addition with saturation control which forces the result to the minimum or maximum representable value in case of underflow or overflow, respectively,
- $-$ denotes arithmetic subtraction with saturation control which forces the result to the minimum or maximum representable value in case of underflow or overflow, respectively.
- $*$ denotes arithmetic multiplication which can be performed with either truncation or rounding,
- $<$ denotes the "less than" condition as $x < y$; x is less than y,
- $>$ denotes the "greater than" condition, as $x > y$; x is greater than y,
- $=$ denotes the substitution of the right-hand variable for the left-hand variable.

Note 1 – Some freedom is offered for the implementation of the accumulation process in the QMF: the word lengths of the internal variables can be equal to or greater than 24 bits, and the arithmetic multiplications can be performed with either truncation or rounding. It allows a simplified implementation on various types of processors. The counterpart is that it excludes the use of digital test sequence for the test of the QMF.

TABLE 10/G.722

Representation of internal processing variables and QMF coefficients

Transmit QMF		
Name	Binary representation	Description
XA	S, −1, −2, −3, ..., −y+1, −y	Output signal of sub-block, ACCUMA
XB	S, −1, −2, −3, ..., −y+1, −y	Output signal of sub-block, ACCUMB
XIN1, XIN2, ..., XIN23	S, S, −2, −3, ..., −14, −15	Input signal with delays 1 to 23
Receive QMF		
Name	Binary representation	Description
XD, XD1, ..., XD11	S, −1, −2, −3, ..., −14, −15	Input signal for sub-block, ACCUMC, with delays 0 to 11
XOUT1	S, S, −2, −3, ..., −14, −15	8 kHz sampled output value
XOUT2	S, S, −2, −3, ..., −14, −15	8 kHz sampled output value
XS, XS1, ..., XS11	S, −1, −2, −3, ..., −14, −15	Input signal for sub-block, ACCUMD, with delays 0 to 11
WD	S, −1, −2, −3, ..., −y+1, −y	Partial sum
QMF coefficients		
Name	Binary representation	Description
H0, H1, ..., H23	S, −2, −3, −4, ..., −12, −13	Filter coefficient values

Note – y is equal to or greater than 23.

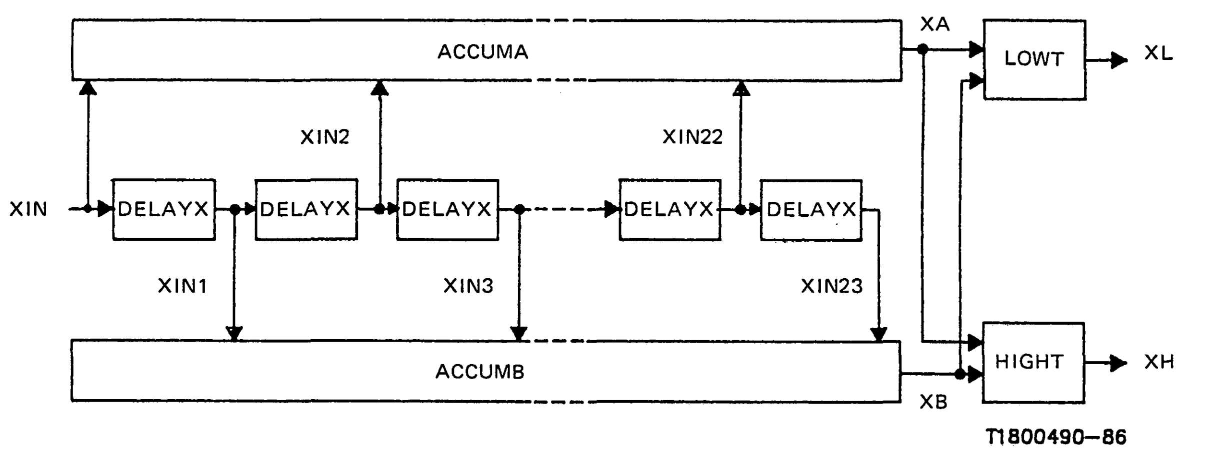
TABLE 11/G.722

QMF coefficient

Coefficient	Scaled values (see Note)
H0 , H23	3
H1 , H22	−11
H2 , H21	−11
H3 , H20	53
H4 , H19	12
H5 , H18	−156
H6 , H17	32
H7 , H16	362
H8 , H15	−210
H9 , H14	−805
H10 , H13	951
H11 , H12	3876

Note – QMF coefficients are scaled by 2^{13} with respect to the representation specified in Table 10/G.722.

5.2.1 *Description of the transmit QMF*



Note – XA and XB are computed with respect to the same 16 kHz input sampling instants and are output at an 8 kHz sampling rate.

FIGURE 17/G.722

Transmit QMF

DELAYX

Input: x

Output: y

Note – Index (j) indicates the current 16-kHz sample period, while index ($j - 1$) indicates the previous one.

Function: Memory block. For any input x, the output is given by:

$y(j) = x(j - 1)$

ACCUMA

Inputs: XIN, XIN2, XIN4, ..., XIN22

Output: XA

Note 1 – H0, H2, ..., H22 are obtained from Table 11/G.722.

Note 2 – The values XIN, XIN2, ..., XIN22 and H0, H2, ..., H22 may be shifted before multiplication, if so desired. The result XA must be rescaled accordingly, In performing these scaling operations the following rules must be obeyed:

1) the precision of XIN, XIN2, ..., XIN22 and H0, H2, ..., H22 as given in Table 9/G.722 and Table 10/G.722 must be retained,
2) the partial products and the ouptut signal XA must be retained to a significance of at least 2^{-23},
3) no saturation should occur in the calculation of the function XA.

Note 3 – No order of summation is specified in accumulating the partial products.

Function: Multiply the even order QMF coefficients by the appropriately delayed input signals, and accumulate these products.

XA = (XIN * H0) + (XIN2 * H2) + (XIN4 * H4) + ... + (XIN22 * H22)

ACCUMB

Inputs: XIN1, XIN3, XIN5, ..., XIN23

Output: XB

Note 1 – H1, H3, ..., H23 are obtained from Table 11/G.722.

Note 2 – The values XIN1, XIN3, ..., XIN23 and H1, H3, ..., H23 may be shifted before multiplication, if so desired. The result XB must be rescaled accordingly. In performing these scaling operations the following rules must be obeyed:

1) the precision of XIN1, XIN3, ..., XIN23 and H1, H3, ..., H23 as given in Table 9/G.722 and Table 10/G.722 must be retained,
2) the partial products and the output signal X3 must be retained to a significance of at least 2^{-23},
3) no saturation should occur in the calculation of the function XB.

Note 3 – No order of summation is specified in accumulating the partial products.

Function: Multiply the odd order QMF coefficients by the appropriately delayed input signals, and accumulate these products.

XB = (XIN1 * H1) + (XIN3 * H3) + (XIN5 * H5) + ... + (XIN23 * H23)

LOWT

Inputs: XA, XB

Output: XL

Function: Compute the lower sub-band signal component.

$XL = (XA + XB) \gg (y - 15)$

$$XL = \begin{cases} 16383, & \text{if } XL > 16383 \\ -16384, & \text{if } XL < -16384 \end{cases}$$

HIGHT

Inputs: XA, XB

Output: XH

Function: Compute the higher sub-band signal component.

$XH = (XA - XB) \gg (y - 15)$

$$XH = \begin{cases} 16383, & \text{if } XH > 16383 \\ -16384, & \text{if } XH < -16384 \end{cases}$$

5.2.2 *Description of the receive QMF*

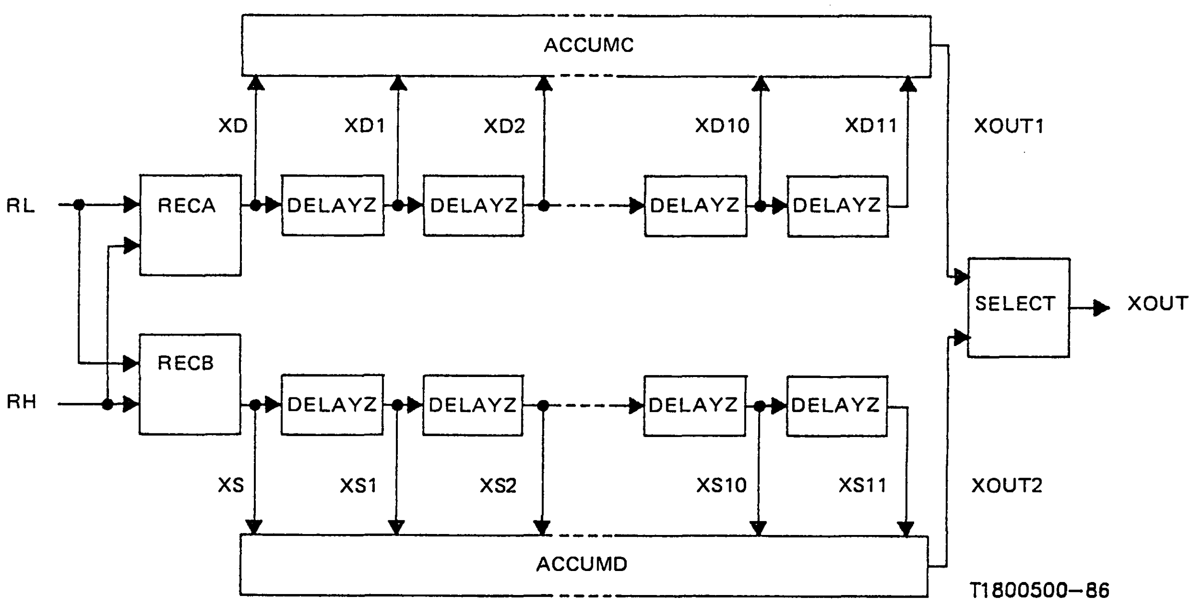


FIGURE 18/G.722

Receive QMF

RECA

Inputs: RL, RH

Output: XD

Function: Compute the input signal to the receive QMF

XD = RL − RH

RECB

Inputs: RL, RH

Output: XS

Function: Compute the input signal to the receive QMF

XS = RL + RH

DELAYZ

Input: x

Output: y

Note – Index (n) indicates the current 8-kHz sample period, while index (n − 1) indicates the previous one.

Function: Memory block. For any input x, the output is given by:

$y(n) = x(n-1)$

ACCUMC

Inputs: XD, XDi (i = 1 to 11)

Output: XOUT1

Note 1 – H0, H2, ..., H22 are obtained from Table 11/G.722.

Note 2 – The values XD, XD1, ..., XD11 and H0, H2, ..., H22 may be shifted before multiplication, if so desired. The result WD must be rescaled accordingly. In performing these scaling operations the following rules must be obeyed:

1) the precision of XD, XD1, ..., XD11 and H0, H2, ..., H22 as given in Table 9/G.722 and Table 10/G.722 must be retained,
2) the partial products and the output signal WD must be retained to a significance of at least 2^{-23};
3) no saturation should occur in the calculation of the function WD.

Note 3 – No order of summation is specified in accumulating the partial products.

Function: Multiply the even order QMF coefficients by the appropriately delayed input signals, and accumulate these products.

WD = (XD * H0) + (XD1 * H2) + (XD2 * H4) + ... + (XD11 * H22)

XOUT1 = WD >> (y − 16)

$$\text{XOUT1} = \begin{cases} 16383, & \text{if XOUT1} > 16383 \\ -16384, & \text{if XOUT1} < -16384 \end{cases}$$

ACCUMD

Inputs: XS, XSi (i = 1 to 11)

Output: XOUT2

Note 1 – H1, H3, ..., H23 are obtained from Table 11/G.722.

Note 2 – The values XS, XS1, ..., XS11 and H1, H3, ..., H23 may be shifted before multiplication, if so desired. The result WD must be rescaled accordingly. In performing these scaling operations the following rules must be obeyed:

1) the precision of XS, XS1, ..., XS11 and H1, H3, ..., H23 as given in Table 9/G.722 and Table 10/G.722 must be retained,
2) the partial products and the output signal WD must be retained to a significance of at least 2^{-23};
3) no saturation should occur in the calculation of the function WD.

Note 3 – No order of summation is specified in accumulating the partial products.

Function: Multiply the odd order QMF coefficients by the appropriately delayed input signals, and accumulate these products.

WD = (XS * H1) + (XS1 * H3) + (XS2 * H5) + ... + (XS11 * H23)

XOUT2 = WD ≫ (y – 16)

$$\text{XOUT2} = \begin{cases} 16383, & \text{if XOUT2} > 16383 \\ -16384, & \text{if XOUT2} < -16384 \end{cases}$$

SELECT

Inputs: XOUT1, XOUT2

Output: XOUT

Note 1 – Index (j) indicates the current 16-kHz sample period, while index (j + 1) indicates the next one. With respect to the input sampling instant XOUT1 is selected first, followed by XOUT2.

Function: Select one of the 8 kHz sampled input signals alternately to produce the 16 kHz sampled output signal.

XOUT(j) = XOUT1

XOUT(j + 1) = XOUT2

---

6 Computational details for lower and higher sub-band ADPCM

6.1 *Input and output signals*

Table 12/G.722 defines the input and output signals for the lower and higher sub-band encoders and decoders. The signal RS represents a reset function that sets all internal memory elements to a specified condition, so that encoders or decoders can be forced into a known state. The signal MODE represents a mode indication. The three basic modes of operation are described in Table 1/G.722. The mode identification is performed in every 8 kHz sampling interval.

TABLE 12/G.722

Input and output signals

Lower sub-band encoder		
	Name	Description
Input	XL	15-bit uniformly quantized input signal
Input	RS	Reset
Output	IL	6-bit ADPCM codeword
Higher sub-band encoder		
	Name	Description
Input	XH	15-bit uniformly quantized input signal
Input	RS	Reset
Output	IH	2-bit ADPCM codeword
Lower sub-band decoder		
	Name	Description
Input	ILR	Received 6-bit ADPCM codeword
Input	MODE	Mode indication
Input	RS	Reset
Output	RL	15-bit uniformly quantized output signal
Higher sub-band decoder		
	Name	Description
Input	IH	2-bit ADPCM codeword
Input	RS	Reset
Output	RH	15-bit uniformly quantized output signal

6.2 *Description of variables and detailed specification of sub-blocks*

This section contains a detailed expansion of all blocks in Figures 4/G.722, 5/G.722, 7/G.722 and 8/G.722 described in §§ 3 and 4. The expansions are illustrated in Figures 19/G.722 to 31/G.722 with the internal processing variables in Table 13/G.722, the constant values in Tables 14/G.722 and 15/G.722, and conversion tables in Tables 16/G.722 to 21/G.722. All internal variables have 16-bit word lengths, and are represented in 2's complement notation. Constant values with 13-bit precision as given in Tables 14/G.722 and 15/G.722 are used in sub-blocks with 16-bit representation, extending the sign to the first three MSBs. A brief functional description and full specification is given for each sub-block.

The notations used in the block descriptions are as follows:

$\ll n$	denotes an n-bit arithmetic shift left operation (zero fill),
$\gg n$	denotes an n-bit arithmetic shift right operation (sign extension); if n is negative, $\gg n$ means $\ll(-n)$;
$\ggg n$	denotes an n-bit logical shift right operation (zero fill),
$\lll n$	denotes an n-bit logical shift left operation (zero fill),
&	denotes the logical "and" operation,
+	denotes arithmetic addition. (The result is set at +32767 when overflow occurs, or at −32768 when underflow occurs.),
−	denotes arithmetic subtraction. (The result is set at +32767 when overflow occurs, or at −32768 when uderflow occurs.),
*	denotes the multiplication defined by the following arithmetic operation: $A * B = (A \text{ times } B) \gg 15$;
==	denotes the "equal to" condition,
!=	denotes the "not equal to" condition,
<	denotes the "less than" condition, as $x < y$; x is less than y;
>	denotes the "greater than" condition, as $x > y$; x is greater than y;
=	denotes the substitution of right-hand variable for the left-hand variable,
|	delineates comments to equations.

TABLE 13/G.722

Internal processing variables

Lower sub-band ADPCM		
Name	**Binary representation**	**Description**
AL1*, AL2*	S, 0, −1, −2, ..., −13, −14	Delayed second-order pole section coefficients
APL1, APL2	S, 0, −1, −2, ..., −13, −14	Second-order pole section coefficients
BL1*, ..., BL6*	S, 0, −1, −2, ..., −13, −14	Delayed sixth-order zero section coefficients
BPL1, ..., BPL6	S, 0, −1, −2, ..., −13, −14	Sixth-order zero section coefficients
DEPL	S, −4, −5, −6, ..., −17, −18	Quantizer scale factor
DETL*	S, −4, −5, −6, ..., −17, −18	Delayed quantizer scale factor
DLT	S, −1, −2, −3, ..., −14, −15	Quantized difference signal for the adaptative predictor with delay 0
DLT1*, ..., DLT6*	S, −1, −2, −3, ..., −14, −15	Quantized difference signal for the adaptative predictor with delays 1 to 6
DL	S, −1, −2, −3, ..., −14, −15	Quantized difference signal for decoder output
EL	S, −1, −2, −3, ..., −14, −15	Difference signal
NBL*	S, 3, 2, 1, 0, ..., −10, −11	Delayed logarithmic quantizer scale factor
NBPL	S, 3, 2, 1, 0, ..., −10, −11	Logarithmic quantizer scale factor
PLT	S, −1, −2, −3, ..., −14, −15	Partially reconstructed signal with delay 0
PLT1*, PLT2*	S, −1, −2, −3, ..., −14, −15	Partially reconstructed signal with delays 1 and 2
YL	S, −1, −2, −3, ..., −14, −15	Output reconstructed signal
RLT	S, −1, −2, −3, ..., −14, −15	Reconstructed signal for the adaptative predictor with delay 0
RLT1*, RLT2*	S, −1, −2, −3, ..., −14, −15	Reconstructed signal for the adaptative predictor with delays 1 and 2
SL	S, −1, −2, −3, ..., −14, −15	Predictor output value
SPL	S, −1, −2, −3, ..., −14, −15	Pole section outuput signal
SZL	S, −1, −2, −3, ..., −14, −15	Zero section output signal
AH1*, AH2*	S, 0, −1, −2, ..., −13, −14	Delayed second-order pole section coefficients
APH1, APH2*	S, 0, −1, −2, ..., −13, −14	Second-order pole section coefficients
BH1*, ..., BH6*	S, 0, −1, −2, ..., −13, −14	Delayed sixth-order zero section coefficients
BPH1, ..., BPH6	S, 0, −1, −2, ..., −13, −14	Sixth-order zero section coefficients
DEPH	S, −4, −5, −6, ..., −17, −18	Quantizer scale factor
DETH*	S, −4, −5, −6, ..., −17, −18	Delayed quantizer scale factor
DH	S, −1, −2, −3, ..., −14, −15	Quantizer difference signal with delay 0
DH1*, ..., DH6*	S, −1, −2, −3, ..., −14, −15	Quantized difference signal with delays 1 to 6
EH	S, −1, −2, −3, ..., −14, −15	Difference signal
NBH	S, 3, 2, 1, 0, ..., −10, −11	Delayed logarithmic quantizer scale factor
NBPH	S, 3, 2; 1, 0, ..., −10, −11	Logarithmic quantizer scale factor
PH	S, −1, −2, −3, ..., −14, −15	Partially reconstructed signal with delay 0
PH1*, PH2*	S, −1, −2, −3, ..., −14, −15	Partially reconstructed signal with delays 1 and 2
YH	S, −1, −2, −3, ..., −14, −15	Quantized reconstructed signal with delay 0
RH1*, RH2*	S, −1, −2, −3, ..., −14, −15	Quantized reconstructed signal with delays 1 and 2
SH	S, −1, −2, −3, ..., −14, −15	Predictor outuput value
SPH	S, −1, −2, −3, ..., −14, −15	Pole section output signal
SZH	S, −1, −2, −3, ..., −14, −15	Zero section output signal

Note – * indicates variables which should be initialized to a specific value when a reset condition is applied.

TABLEAU 14/G.722

Quantizer decision levels and output values

Quantizer constant representation		
Name	**Binary representation**	**Description**
Qi	S, 2, 1, 0, −1, ..., −8, −9	Quantizer decision level
QQi	S, 2, 1, 0, −1, ..., −8, −9	Inverse quantizer output
WL, WH	S, 0, −1, −2, ..., −10, −11	Logarithmic scaling factor multiplier

Lower sub-band quantizer					
Address	**Q6**	**QQ6**	**QQ5**	**QQ4**	**WL**
0				0	−60
1	35	17	35	150	−30
2	72	54	110	323	58
3	110	91	190	530	172
4	150	130	276	786	334
5	190	170	370	1121	538
6	233	211	473	1612	1198
7	276	254	587	2557	3042
8	323	300	714		
9	370	347	858		
10	422	396	1023		
11	473	447	1219		
12	530	501	1458		
13	587	558	1765		
14	650	618	2195		
15	714	682	2919		
16	786	750			
17	858	822			
18	940	899			
19	1023	982			
20	1121	1072			
21	1219	1170			
22	1339	1279			
23	1458	1399			
24	1612	1535			
25	1765	1689			
26	1980	1873			
27	2195	2088			
28	2557	2376			
29	2919	2738			
30		3101			

Higher sub-band quantizer			
Address	**Q2**	**QQ2**	**WH**
1	564	202	−214
2		926	798

TABLE 15/G.722

Log-to-linear conversion table

Conversion table constants		
Name	Binary representation	Description
ILA	S, −5, −6, −7, ..., −15, −16	353-entry table constants
ILB	S, 0, −1, −2, ..., −15, −16	32-entry table constants

ILA

i \ j	0	1	2	3	4	5	6	7
0	1	1	1	1	1	1	1	1
8	1	1	1	1	1	1	1	1
16	1	1	1	2	2	2	2	2
24	2	2	2	2	2	2	2	2
32	3	3	3	3	3	3	3	3
40	3	3	3	4	4	4	4	4
48	4	4	4	5	5	5	5	5
56	5	5	6	6	6	6	6	6
64	7	7	7	7	7	7	8	8
72	8	8	8	9	9	9	9	10
80	10	10	10	11	11	11	11	12
88	12	12	13	13	13	13	14	14
96	15	15	15	16	16	16	17	17
104	18	18	18	19	19	20	20	21
112	21	22	22	23	23	24	24	25
120	25	26	27	27	28	28	29	30
128	31	31	32	33	33	34	35	36
136	37	37	38	39	40	41	42	43
144	44	45	46	47	48	49	50	51
152	52	54	55	56	57	58	60	61
160	63	64	65	67	68	70	71	73
168	75	76	78	80	82	83	85	87
176	89	91	93	95	97	99	102	104
184	106	109	111	113	116	118	121	124
192	127	129	132	135	138	141	144	147
200	151	154	157	161	165	168	172	176
208	180	184	188	192	196	200	205	209
216	214	219	223	228	233	238	244	249
224	255	260	266	272	278	284	290	296
232	303	310	316	323	331	338	345	353
240	361	369	377	385	393	402	411	420
248	429	439	448	458	468	478	489	500
256	511	522	533	545	557	569	582	594
264	607	621	634	648	663	677	692	707
272	723	739	755	771	788	806	823	841

ILA								
i \ j	0	1	2	3	4	5	6	7
280	860	879	898	918	938	958	979	1001
288	1023	1045	1068	1092	1115	1140	1165	1190
296	1216	1243	1270	1298	1327	1356	1386	1416
304	1447	1479	1511	1544	1578	1613	1648	1684
312	1721	1759	1797	1837	1877	1918	1960	2003
320	2047	2092	2138	2185	2232	2281	2331	2382
328	2434	2488	2542	2598	2655	2713	2773	2833
336	2895	2959	3024	3090	3157	3227	3297	3370
344	3443	3519	3596	3675	3755	3837	3921	4007
352	4095							

ILB								
i \ j	0	1	2	3	4	5	6	7
0	2048	2093	2139	2186	2233	2282	2332	2383
8	2435	2489	2543	2599	2656	2714	2774	2834
16	2896	2960	3025	3091	3158	3228	3298	3371
24	3444	3520	3597	3676	3756	3838	3922	4008

Note 1 – A table address is obtained by adding i and j.

Note 2 – Either a 353-entry or a 32-entry table may be used in accordance with the choice of log-to-linear conversion method, Method 1 or Method 2 (see §§ 6.2.1.3 and 6.2.2.3)

TABLE 16/G.722

Conversion from quantizer intervals to 6-bit output codewords

SIL	MIL	IL	SIL	MIL	IL
−1	30	000100	0	1	111101
−1	29	000101	0	2	111100
−1	28	000110	0	3	111011
−1	27	000111	0	4	111010
−1	26	001000	0	5	111001
−1	25	001001	0	6	111000
−1	24	001010	0	7	110111
−1	23	001011	0	8	110110
−1	22	001100	0	9	110101
−1	21	001101	0	10	110100
−1	20	001110	0	11	110011
−1	19	001111	0	12	110010
−1	18	010000	0	13	110001
−1	17	010001	0	14	110000
−1	16	010010	0	15	101111
−1	15	010011	0	16	101110
−1	14	010100	0	17	101101
−1	13	010101	0	18	101100
−1	12	010110	0	19	101011
−1	11	010111	0	20	101010
−1	10	011000	0	21	101001
−1	9	011001	0	22	101000
−1	8	011010	0	23	100111
−1	7	011011	0	24	100110
−1	6	011100	0	25	100101
−1	5	011101	0	26	100100
−1	4	011110	0	27	100011
−1	3	011111	0	28	100010
−1	2	111110	0	29	100001
−1	1	111111	0	30	100000

TABLE 17/G.722

Conversion from 4-bit codewords to quantizer intervals

RIL	SIL	IL4
0000	0	0
0001	−1	7
0010	−1	6
0011	−1	5
0100	−1	4
0101	−1	3
0110	−1	2
0111	−1	1
1111	0	0
1110	0	1
1101	0	2
1100	0	3
1011	0	4
1010	0	5
1001	0	6
1000	0	7

Note – It is possible for the decoder to receive the codeword 0000 due to transmission errors.

TABLE 18/G.722

Conversion from 6-bit codewords to quantizer intervals

RIL	SIL	IL6
000000	−1	1
000001	−1	1
000010	−1	1
000011	−1	1
000100	−1	30
000101	−1	29
000110	−1	28
000111	−1	27
001000	−1	26
001001	−1	25
001010	−1	24
001011	−1	23
001100	−1	22
001101	−1	21
001110	−1	20
001111	−1	19
010000	−1	18
010001	−1	17
010010	−1	16
010011	−1	15
010100	−1	14
010101	−1	13
010110	−1	12
010111	−1	11
011000	−1	10
011001	−1	9
011010	−1	8
011011	−1	7
011100	−1	6
011101	−1	5
011110	−1	4
011111	−1	3

RIL	SIL	IL6
111110	−1	2
111111	−1	1
111101	0	1
111100	0	2
111011	0	3
111010	0	4
111001	0	5
111000	0	6
110111	0	7
110110	0	8
110101	0	9
110100	0	10
110011	0	11
110010	0	12
110001	0	13
110000	0	14
101111	0	15
101110	0	16
101101	0	17
101100	0	18
101011	0	19
101010	0	20
101001	0	21
101000	0	22
100111	0	23
100110	0	24
100101	0	25
100100	0	26
100011	0	27
100010	0	28
100001	0	29
100000	0	30

Note – It is possible for the decoder to receive the codewords 000000, 000001, 000010 and 000011 due to transmission errors.

TABLE 19/G.722

Conversion from 5-bit codewords to quantizer intervals

RIL	SIL	IL5		RIL	SIL	IL5
000000	−1	1		11111	−1	1
000001	−1	1		11110	0	1
000010	−1	15		11101	0	2
000011	−1	14		11100	0	3
000100	−1	13		11011	0	4
000101	−1	12		11010	0	5
000110	−1	11		11001	0	6
000111	−1	10		11000	0	7
001000	−1	9		10111	0	8
001001	−1	8		10110	0	9
001010	−1	7		10101	0	10
001011	−1	6		10100	0	11
001100	−1	5		10011	0	12
001101	−1	4		10010	0	13
001110	−1	3		10001	0	14
001111	−1	2		10000	0	15

Note – It is possible for the decoder to receive the codewords 00000 and 00001 due to transmission errors.

TABLE 20/G.722

Conversion from quantizer intervals to 2-bit output codewords

SIH	MIH	IH
−1	2	00
−1	2	01
0	1	11
0	2	10

TABLE 21/G.722

Conversion from 2-bit codewords to quantizer intervals

IH	SIH	IH2
00	−1	2
01	−1	1
11	0	1
10	0	2

6.2.1 *Description of the lower sub-band ADPCM*

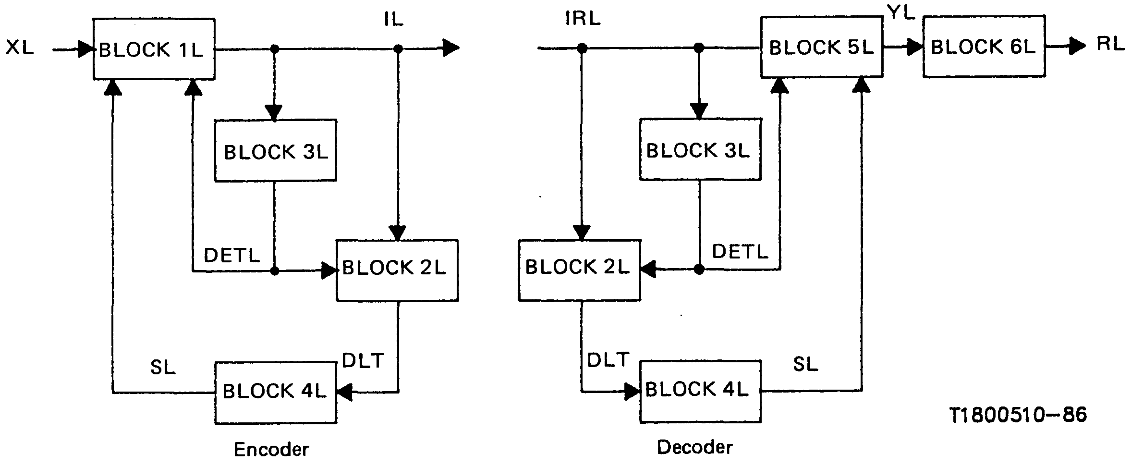


FIGURE 19/G.722

Lower sub-band ADPCM encoder and decoder

6.2.1.1 *Difference signal computation and quantization in the lower sub-band (BLOCK 1L)*

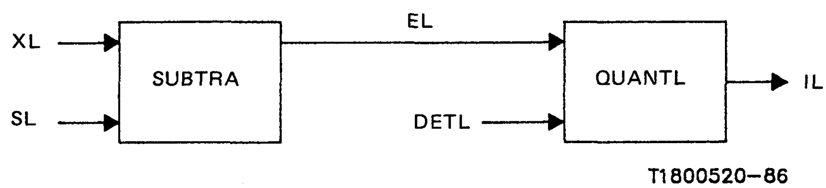


FIGURE 20/G.722

Difference signal computation and quantization in the lower sub-band

---

SUBTRA

Inputs: XL, SL

Output: EL

Function: Compute the difference signal by subtracting from the input signal its predicted value.

EL = XL – SL

QUANTL

Inputs: EL, DETL

Output: IL

Note 1 – If WD falls exactly on a higher decision level, LDU, the larger adjacent MIL is used.

Note 2 – When both the lower and higher decision levels, LDL and LDU, are the same value, the value of MIL is excluded from that to be chosen.

Function: Quantize the difference signal in the lower sub-band.

SIL = EL >> 15 | Sign of EL

$$WD = \begin{cases} EL, & \text{if } SIL == 0 \quad | \text{ Magnitude of EL} \\ 32767 - EL \ \& \ 32767, & \text{if } SIL == -1 \quad | \text{ (Magnitude of EL)} - 1 \end{cases}$$

Quantizer decision levels and corresponding MIL values:

WD		MIL.
Lower decision level (LDL)	Higher decision level (LDU)	
0	(Q6 (1) << 3) * DETL	1
(Q6 (1) << 3) * DETL	(Q6 (2) << 3) * DETL	2
(Q6 (2) << 3) * DETL	(Q6 (3) << 3) * DETL	3
(Q6 (3) << 3) * DETL	(Q6 (4) << 3) * DETL	4
(Q6 (4) << 3) * DETL	(Q6 (5) << 3) * DETL	5
:	:	:
:	:	:
(Q6 (26) << 3) * DETL	(Q6 (27) << 3) * DETL	27
(Q6 (27) << 3) * DETL	(Q6 (28) << 3) * DETL	28
(Q6 (28) << 3) * DETL	(Q6 (29) << 3) * DETL	29
otherwise		30

Q6 is obtained from Table 14/G.722.

IL is obtained from Table 16/G.722 using SIL and MIL.

6.2.1.2 *Inverse quantization of the difference signal in the lower sub-band (BLOCK 2L)*

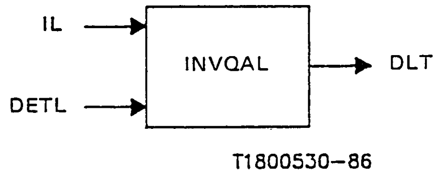


FIGURE 21/G.722

Inverse quantization of the difference signal in the lower sub-band

---

INVQAL

Inputs: IL (ILR in the decoder), DETL

Output DLT

Function: Compute the quantized difference signal for the adaptive predictor in the lower sub-band.

RIL = IL >>> 2	Delete 2 LSB
SIL and IL4 are obtained from Table 17/G.722 using RIL. Use IL4 as an address for QQ4 in Table 14/G.722	Derive sign of DLT
WD1 = QQ4(IL4) << 3	
$\text{WD2} = \begin{cases} \text{WD1} & \text{if SIL} == 0 \\ \text{WD1} & \text{if SIL} == -1 \end{cases}$	Scale table constant Attach sign
DLT = DETL * WD2	

6.2.1.3 *Quantizer scale factor adaptation in the lower sub-band (BLOCK 3L)*

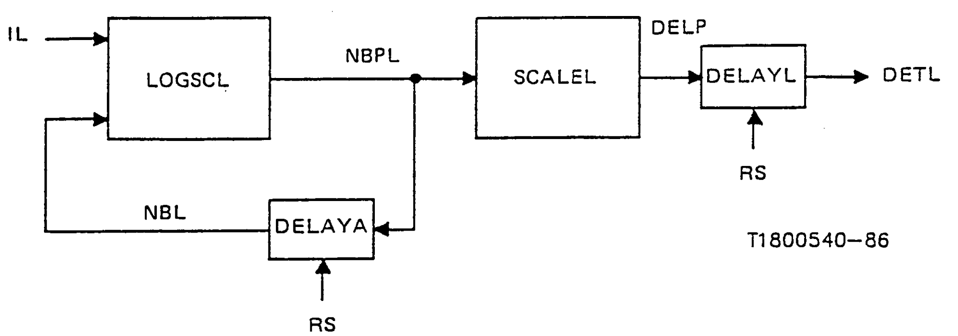


FIGURE 22/G.722

Quantizer scale factor adaptation in the lower sub-band

LOGSCL

Inputs: IL (ILR in the decoder), NBL

Output NBPL

Function: Update the logarithmic quantizer scale factor in the lower sub-band.

RIL = IL >>> 2	Delete 2 LSBs
IL4 is obtained from Table 17/G.722 using RIL. Use IL4 as an address for WL in Table 14/G.722	
WD = NBL * 32512 NBPL = WD + WL(IL4)	Leakage factor of 127/128. Add scale factor multiplier
$$NBPL = \begin{cases} 0, & \text{if } NBPL < 0 \\ 18432, & \text{if } NBPL > 18432 \end{cases}$$	Lower limit of 0, Upper limit of 9.

DELAYA

Inputs: x, RS

Output y

Function: Memory block. For any input x, the output is given by:

$$y(n) = \begin{cases} x(n-1), & \text{if } RS == 0 \\ 0, & \text{if } RS == 1 \end{cases}$$	Reset to 0.

SCALEL

Inputs: NBPL

Output: DEPL

Note – Either Method 1 or Method 2 is used.

Function: Compute the quantizer scale factor in the lower sub-band.

Method 1 (using 353-entry table)

WD1 = (NBPL >> 6) & 511 WD2 = WD1 + 64	Compute table address for ILA
Use WD2 as an address for ILA in Table 15/G.722	
DEPL = (ILA(WD2) + 1) << 2	Scaling by 2-bit shift

Method 2 (using 32-entry table)

WD1 = (NBPL >> 6) & 31 WD2 = NBPL >> 11	Fractional part of NBPL. Integer part of NBPL.
Use WD1 as an address for ILB in Table 15/G.722.	
WD3 = ILB(WD1 >> (8 – WD2)	Scaling with integer part
DEPL = WD3 << 2	Scaling by 2-bit shift

DELAYL

Inputs: x, RS

Output y

Function: Memory block. For the input x, the output is given by:

$$y(n) = \begin{cases} x(n-1), & \text{if } RS == 0 \\ 32, & \text{if } RS == 1 \end{cases}$$

Reset to minimun value

6.2.1.4 *Adaptive predictor and reconstructed signal calculator in the lower sub-band (BLOCK 4L)*

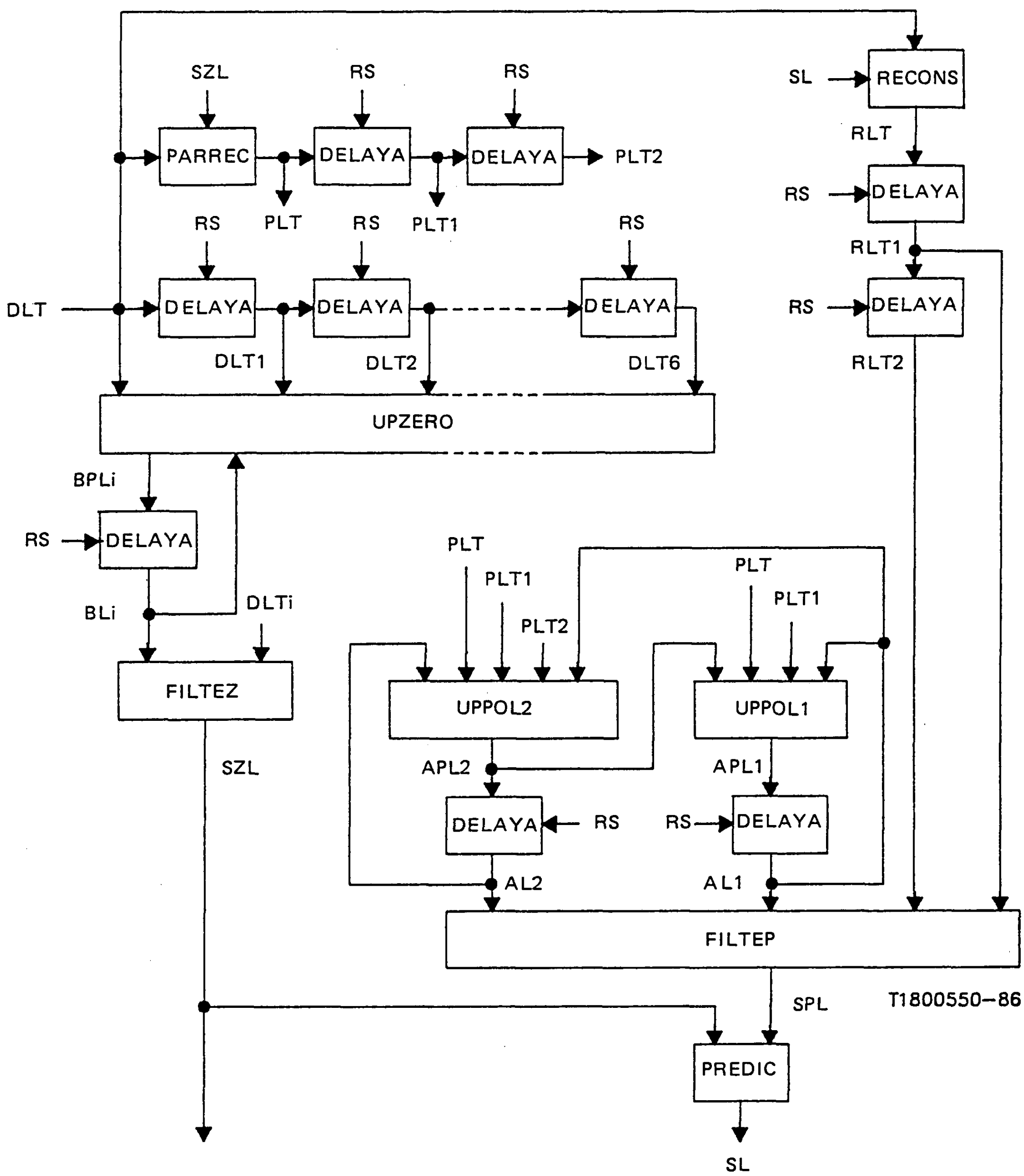


FIGURE 23/G.722

Adaptive predictor and reconstructed signal calculator in the lower sub-band

---

DELAYA

See § 6.2.1.3 for specification.

PARREC

Inputs: DLT, SZL

Output: PLT

Function: Compute partially reconstructed signal.

PLT = DLT + SZL

RECONS

Inputs: SL, DLT

Output: RLT

Function: Compute reconstructed signal for the adaptive predictor.

RLT = SL + DLT

UPZERO

Inputs: DLT, DLTi (i = 1 to 6), BLi (i = 1 to 6)

Output: BPLi (i = 1 to 6)

Function: Update sixth-order predictor (zero section) coefficients.

$\text{WD1} = \begin{cases} 0, & \text{if DLT == 0} \\ 128, & \text{if DLT != 0} \end{cases}$		Gain of zero Gain of 1/128
SG0 = DLT >> 15		Sign of DLT

Repeat the following computations for i = 1 to 6:

SGi = DLTi >> 15

$\text{WD2} = \begin{cases} \text{WD1}, & \text{if SG0 == SGi} \\ -\text{WD1}, & \text{if SG0 != SGi} \end{cases}$	Sign of DLTi Attach sign to WD1
WD3 = BLi * 32640	Leak factor of 255/256
BPLi = WD2 + WD3	Update zero-section coefficients

UPPOL2

Inputs: ALi (i = 1 and 2), PLT, PLTi (i = 1 and 2)

Output: APL2

Function: Update second predictor coefficient (pole section).

```
SG0 = PLT >> 15                                  | Sign of PLT
SG1 = PLT1 >> 15                                 | Sign of PLT1
SG2 = PLT2 >> 15                                 | Sign of PLT2

WD1 = AL1 + AL1                                  | Compute f(AL1)
WD1 = WD1 + WD1                                  | [Eq. (3-34) of § 3.6.3]

       { 0 - WD1         if SG0 == SG1           |
WD2 =  {                                         | Attach correct sign to f(AL1)
       { WD1,            if SG0 != SG1           |
                                                 |
WD2 = WD2 >> 7                                   | Gain of 1/128

       {  128,           if SG0 == SG2           | Attach sign to the constant
WD3 =  {                                         | of 1/128
       { -128,           if SG0 != SG2           |

WD4 = WD2 + WD3                                  | Compute gain factor
WD5 = AL2 * 32512                                | Leak factor of 127/128
APL2 = WD4 + WD5                                 | Update second pole section
                                                 | coefficient

       {  12288,         if APL2 >  12288        | Upper limit of +0.75
APL2 = {                                         |
       { -12288,         if APL2 < -12288        | Lower limit of -0.75
```

UPPOL1

Inputs: AL1, APL2, PLT, PLT1

Output: APL1

Function: Update first predictor coefficient (pole section).

```
SG0 = PLT >> 15                                  | Sign of PLT
SG1 = PLT1 >> 15                                 | Sign of PLT1

       {  192,           if SG0 == SG1           |
WD1 =  {                                         | Gain 3/256
       { -192,           if SG0 != SG1           |

WD2 = AL1 * 32640                                | Leak factor of 255/256
APL1 = WD1 + WD2                                 | Update first pole section
                                                 | coefficient
                                                 |
WD3 = 15360 - APL2                               | Compute (1-2^-4 - APL2)

       {  WD3,           if APL1 >  WD3          | Upper limit of APL1
APL1 = {                                         |
       { -WD3,           if APL1 < -WD3          | Lower limit of APL1
```

FILTEZ

Inputs: DLTi (i = 1 to 6), BLi (i = 1 to 6)

Output: SZL

Function: Compute predictor output signal (zero section).

WD1 = DLT1 + DLT1 WD1 = BL1 * WD1 WD2 = DLT2 + DLT2 WD2 = BL2 * WD2 : : : : : : : : : WD6 = DLT6 + DLT6 WD6 = BL6 * WD6	Compute partial zero section output
SZL = ((((WD6 + WD5) + WD4) + WD3) + WD2 + WD1	Sum the partial zero section outputs

FILTEP

Inputs: RLTi (i = 1 and 2), ALi (i = 1 and 2)

Output: SPL

Function: Compute predictor output signal (pole section).

WD1 = RLT1 + RLT1 WD1 = AL1 * WD1	Compute partial pole section output
WD2 = RLT2 + RLT2 WD2 = AL2 * WD2 SPL = WD1 + WD2	Sum the partial pole Section outputs

PREDIC

Inputs: SPL, SZL

Output: SL

Function: Compute the predictor output value.

SL = SPL + SZL

6.2.1.5 *Reconstructed signal calculator for the decoder output in the lower sub-band (BLOCK 5L)*

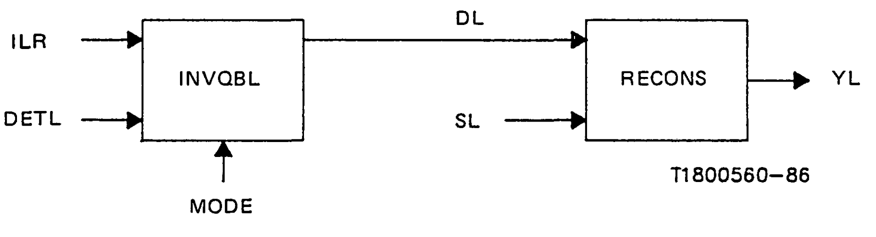


FIGURE 24/G.722

Reconstructed signal calculator for the decoder output in the lower sub-band

INVQBL

Inputs: ILR, DETL, MODE

Output: DL

Note – DL may be substituted by output signal (DLT) of sub-block INVQAL in the case of Mode 3.

Function: Compute quantized difference signal for the decoder output in the lower sub-band.

RIL = ILR SIL and IL6 are obtained from Table18//G.722 using RIL. Use IL6 as an address for QQ6 in Table 14/G.722. WD1 = QQ6(IL6) $\ll$ 3	– if MODE = = 1	6-bit codeword Scale table constant
RIL = IRL $\ggg$ 1 SIL and IL5 are obtained from Table 19/G.722 using RIL. Use IL5 as an address for QQ5 in Table 14/G.722 WD1 = QQ5(IL5) $\ll$ 3	– if MODE = = 2	5-bit codeword Scale table constant
RIL = IRL $\ggg$ 2 SIL and IL4 are obtained from Table 17/G.722 using RIL. Use IL4 as an address for QQ4 in Table 14/G.722 WD1 = QQ4(IL4) $\ll$ 3	– if MODE = = 3	4-bit codeword Scale table constant

$$WD2 = \begin{cases} WD1, & \text{if } SIL == 0 \\ -WD1, & \text{if } SIL == -1 \end{cases} \qquad \text{Attach sign}$$

DL = DETL * WD2

RECONS

See § 6.2.1.4 for specification. Substitute DL for DLT as input, YL for RLT as output.

6.2.1.6 *Reconstructed signal saturation in the lower sub-band (BLOCK 6L)*

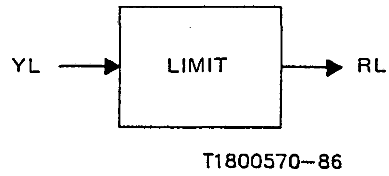


FIGURE 25/G.722

Reconstructed signal saturation in the lower sub-band

LIMIT

Inputs: YL

Output: RL

Function: Limit the output reconstructed signal.

RL = YL

$$RL = \begin{cases} 16383, & \text{if } YL > 16383 \quad | \text{ Upper limit} \\ -16384, & \text{if } YL < -16384 \quad | \text{ Lower limit} \end{cases}$$

6.2.2 *Description of the higher sub-band ADPCM*

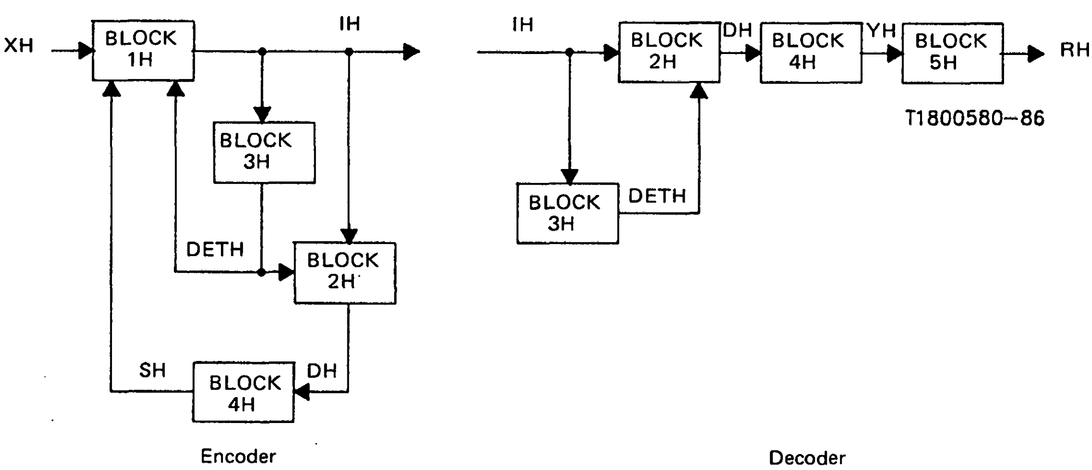


FIGURE 26/G.722

Higher sub-band ADPCM encoder and decoder

6.2.2.1 *Difference signal computation and quantization in the higher sub-band (BLOCK 1H)*

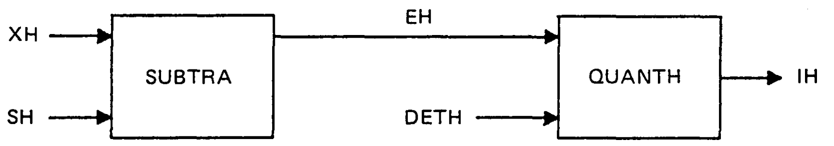


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FIGURE 27/G.722

Difference signal computation and quantization in the higher sub-band

---

SUBTRA

See § 6.2.1.1 for specification. Substitute XH for XL and SH for SL as inputs, and EH for EL as output.

QUANTH

Inputs: EH, DETH

Output: IH

Note – If WD falls exactly on a higher decision level, HDU, the larger adjacent MIH is used.

Function: Quantize the difference signal in the higher sub-band.

$SIH = EH \gg 15$ | Sign of EH

$$WD = \begin{cases} EH, & \text{if } SIH == 0 \\ 32767, - EH \,\&\, 32767 & \text{if } SIH == -1 \end{cases}$$

| Magnitude of EH

| (Magnitude of EH) – 1

Quantizer decision levels and corresponding MIH values:

WD		MIH
Lower decision level (HDL)	Higher decision level (HDU)	
0	(Q2 (1) ≪ 3) * DETH	1
otherwise		2

Q2 is obtained from Table 14/G.722.

IH is obtained from Table 20/G.722 using SIH and MIH.

6.2.2.2 *Inverse quantization of the difference signal in the higher sub-band (BLOCK 2H)*

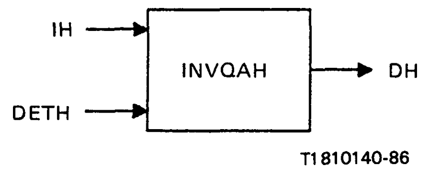


FIGURE 28/G.722

Inverse quantization of the difference signal in the higher sub-band

---

INVQAH

Inputs: IH, DETH

Output: DH

Function: Compute the quantized difference signal in the higher sub-band.

SIH and IH2 are obtained from Table 21/G.722 using IH. Use IH2 as an address for QQ2 in Table 14/G.722	Derive sign of DH
WD1 = QQ2(IH2) ≪ 3	Scale table constant
$WD2 = \begin{cases} WD1, & \text{if SIH} == 0 \\ -WD1, & \text{if SIH} == -1 \end{cases}$	Attach sign

DH = DETH * WD2

6.2.2.3 *Quantizer scale factor adaptation in the higher sub-band (BLOCK 3H)*

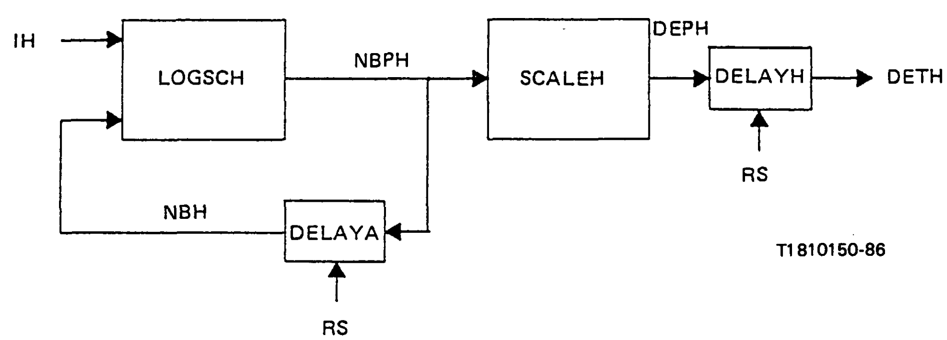


FIGURE 29/G.722

Quantizer scale factor adaptation in the higher sub-band

LOGSCH

Inputs: IH, NBH

Output: NBPH

Function: Update the logarithmic quantizer scale factor in the higher sub-band.

IH2 is obtained from
Table 21/G.722 in using IH.
Use IH2 as an address for WH
in Table 14/G.722.

WD = NBH * 32512	Leakage factor of 127/128
NBPH = WD + WH (IH2)	Add scale factor multiplier

$$NBPH = \begin{cases} 0, & \text{if } NBPH < 0 \\ 22528, & \text{if } NBPH > 22528 \end{cases}$$

| Lower limit of 0
| Upper limit of 11

DELAYA

See § 6.2.1.3 for specification.

SCALEH

Input: NBPH

Output: DEPH

Note – Either Method 1 or Method 2 is used.

Function: Compute the quantizer scale factor in the higher sub-band.

Method 1 (using 353-entry table)

WD = (NBPH ≫ 6) & 511	Compute table address for ILA

Use WD as an address for ILA
in Table 15/G.722.

DEPH = (ILA(WD) + 1) ≪ 2	Scaling by 2-bit shift

Method 2 (using 32-entry table)

WD1 = (NBPH ≫ 6) & 31	Fractional part of NBPH
WD2 = NBPH ≫ 11	Integer part of NBPH

Use WD1 as an address for ILB
in Table 15/G.722.

WD3 = ILB (WD1) ≫ (10 – WD2)	Scaling with integer part
DEPH = WD3 ≪ 2	Scaling by 2-bit shift

DELAYH

Inputs: x, RS

Output: y

Function: Memory block. For the input x, the output is given by:

$$y(n) = \begin{cases} x(n-1), & \text{if } RS == 0 \\ 8, & \text{if } RS == 1 \end{cases}$$

| Reset to minimum value

6.2.2.4 *Adaptive predictor and reconstructed signal calculator in the higher sub-band (BLOCK 4H)*

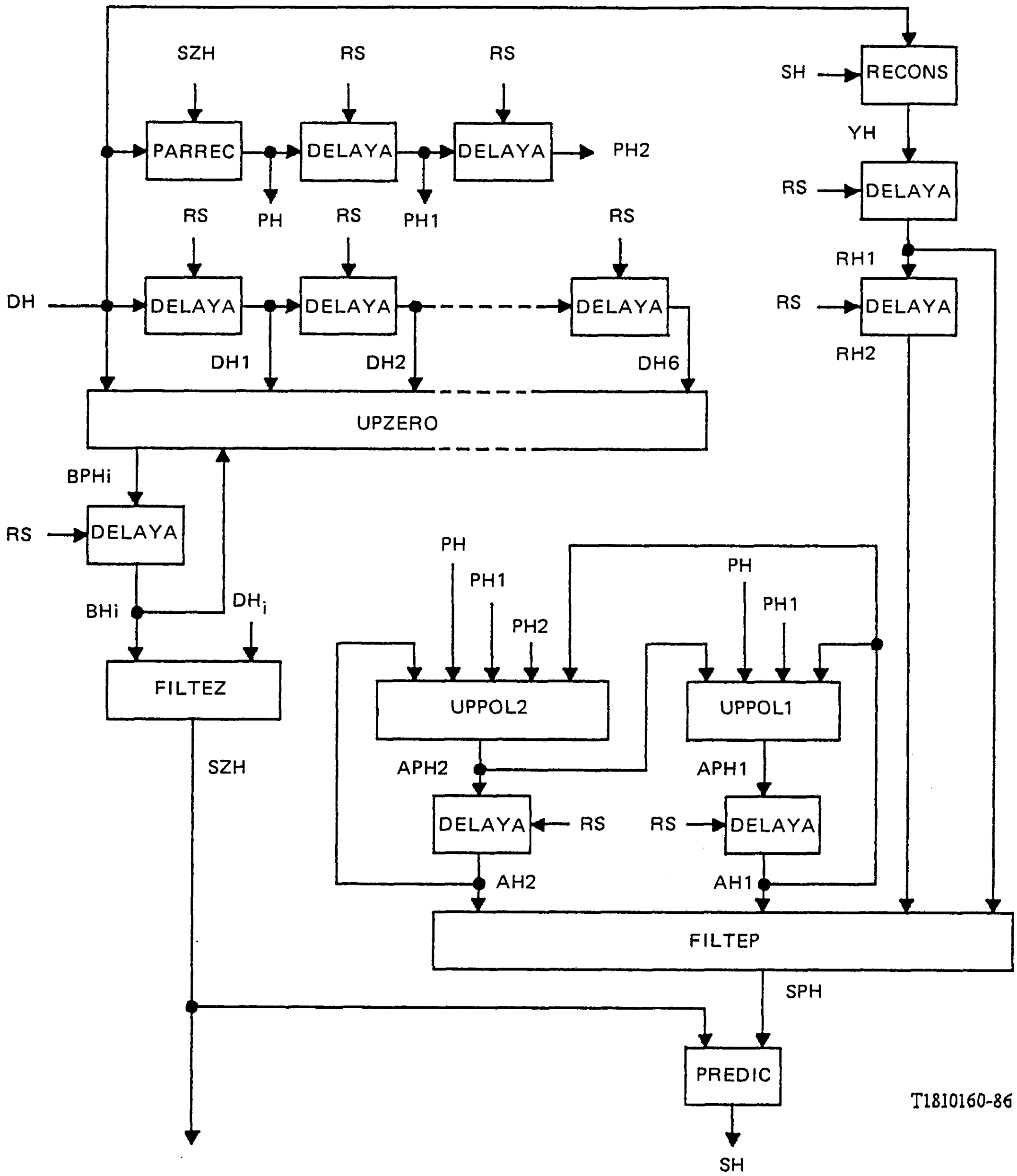


FIGURE 30/G.722

Adaptive predictor and reconstructed signal calculator in the higher sub-band

---

DELAYA

See § 6.2.1.3 for specification.

PARREC

See § 6.2.1.4 for specification. Substitute DH for DLT and SZH for SZL as inputs, and PH for PLT as output.

RECONS

See § 6.2.1.4 for specification. Substitute SH for SL and DH for DLT as inputs, and YH for RLT as output.

UPZERO

See § 6.2.1.4 for specification. Substitute DH for DLT, DHi for DLTi, and BHi for BLi as inputs, and BPHi for BPLi as outputs.

UPPOL2

See § 6.2.1.4 for specification. Substitute AHi for ALi, PH for PLT and PHi for PLTi as inputs, and APH2 for APL2 as output.

UPPOL1

See § 6.2.1.4 for specification. Substitute AH1 for AL1, APH2 for APL2, PH for PLT and PH1 for PLT1 as inputs, and APH1 for APL1 as output.

FILTEZ

See § 6.2.1.4 for specification. Substitute DHi for DLTi and BHi for BLi as inputs, and SZH for SZL as output.

FILTEP

See § 6.2.1.4 for specification. Substitute RHi for RLTi and AHi for ALi as inputs, and SPH for SPL as output.

PREDIC

See § 6.2.1.4 for specification. Substitute SPH for SPL and SZH for SZL as inputs, and SH for SL as output.

6.2.2.5 *Reconstructed signal saturation in the higher sub-band (BLOCK 5H)*

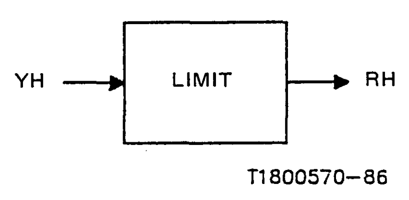


FIGURE 31/G.722

Reconstructed signal saturation in the higher sub-band

LIMIT

See § 6.2.1.6 for specification. Substitute YH for YL as input, and RH for RL as output.

APPENDIX I

(to Recommendation G.722)

Networking aspects

The purpose of this Appendix is to give a broad outline of the interaction of 64 kbit/s (7 kHz) audio coding with other parts of the digital network. Some general guidance is also offered.

The establishment of the connection is beyond the scope of this Recommendation.

I.1 *Network characteristics*

This Recommendation is applicable to systems operating in networks which exhibit each of the following characteristics:

i) availability of network octet timing at the terminals;

   Note – Octet timing may also be derived from control signals within the frame structure defined in Recommendation G.725;

ii) plesiochronous networking where the reference clocks meet the timing requirements given in Recommendation G.811, or synchronous networking;

iii) 64 kbit/s connection types having either of the following characteristics:

   – full 64 kbit/s transparency,

   – pulse density restriction as described in Recommendation G.802.

Note – 64 kbit/s (7 kHz) audio coding can also operate in networks where there is substitution of a signalling bit for the 8th bit of the octet as described in Recommendation G.704, § 3.1 or where there is 56 kbit/s transparency only. However, a reduction of the audio bit rate and auxiliary data channel capacity occurs and only two modes of operation, denoted 1 *bis* (unframed) and 3 *bis*, are possible as follows:

– Mode 1 *bis*: 56 kbit/s for audio coding and no data channel;

– Mode 3 *bis*: 48 kbit/s for audio coding, a 6.4 kbit/s data channel and 1.6 kbit/s for service channel framing and mode control.

I.2 *Integration into the telecommunications network*

It is foreseen that the 64 kbit/s (7 kHz) audio coding system will be used for point-to-point, multipoint and broadcast applications. Examples of particular uses are: commentary quality channels for broadcasting purposes and high quality speech for audio and video conferencing applications.

The coding system can operate over any 64 kbit/s bearer channel (see § I.1), e.g. the public switched telephone network, leased circuits or over an ISDN.

Processes such as digital speech interpolation, echo control and digital pads must be disabled for the transmission of 64 kbit/s (7 kHz) audio coding. The disabling protocol is not the subject of this Recommendation.

It should be noted however that signal processing may occur in a multipoint conference unit (see § I.7).

I.3 *Audio performance of the 64 kbit/s (7 kHz) audio coding system*

I.3.1 *Speech*

The speech performance of the 64 kbit/s (7 kHz) audo coding system has been quantified in terms of Q_W-values, where Q_W is a measure of the signal-to-correlated noise ratio of the wideband system, measured in dB. Detailed information on Q-value measurements may be found in Recommendation P.81. This Recommendation, although primarily intended for telephony bandwidth applications, has been used for the evaluation of wideband systems – signified by the subscript W – by use of an appropriate filter (50-7000 Hz).

For guidance purposes only, a Q_W value of 38 dB corresponds approximately to a 128 kbit/s (7 kHz) PCM system (sampling frequency 16 kHz, coding law as in Recommendation G.711), whereas a Q_W value of 45 dB is approximately equivalent to the audio parts of the coder interconnected without the intermediate SB-ADPCM coding process.

Table I-1/G.722 indicates the relative performance in Q_W values for nominal input values.

TABLE I-1/G.722

Relative levels of speech performance (Q_W values)

Mode of operation	Transcodings		
	1	4 Analogue according to Fig. I-1/G.722	4 Digital according to Fig. I-2/G.722
1 (64 kbit/s)	45	38	41
2 (56 kbit/s)	43	36	38
3 (48 kbit/s)	38	29	34

The performance of the 64 kbit/s (7 kHz) audio coding system has been found to be substantially unaffected by randomly distributed errors at BER levels as high as $1 \cdot 10^{-4}$. High error ratios approaching $1 \cdot 10^{-3}$ produce perceptible degradation which may be considered tolerable in certain applications.

No particular problems have been experienced in the multiple talker condition and hence correct operation under normal conference conditions can safely be assumed.

The performance under conditions of mode mismatch (i.e. where the variant used in the decoder for a given octet does not correspond to the mode of operation) is considered in § I.5.

I.3.2 *Music*

Although primarily designed for speech, no significant distortions may be expected when coding a wide range of music material in Mode 1. Further study on the effects on music signals is a matter of Study Group CMTT.

I.4 *Audio performance when interconnected with other coding systems on an analogue basis*

I.4.1 *64 kbit/s PCM*

Informal subjective tests carried out over a path consisting of an analogue interconnected combination of a 64 kbit/s PCM link conforming to Recommendation G.711 and a 64 kbit/s (7 kHz) audio coding link has indicated that no interworking problems will occur. However, the performance of the combination will not be better than that of 64 kbit/s PCM.

Interconnection of the two coding systems on a digital basis is the subject of § I.8.

I.4.2 *32 kbit/s ADPCM*

An analogue interconnected combination of a 32 kbit/s ADPCM link conforming to Recommendation G.721 and a 64 kbit/s (7 kHz) audio coding link is not expected to pose any interworking problems. However, the performance of the combination will not be better than that of 32 kbit/s ADPCM.

Interconnection of the two coding systems at a digital level is the subject of further study.

I.5 *Audio performance under mode switching*

It is recommended that mode switching should be performed synchronously between the transmitter and the receiver to maximize the audio performance. However, asynchronous mode switching may be considered since the condition of mode mismatch will probably be of limited duration and hence the corresponding performance is likely to be acceptable. Although not desirable, operation under permanent mode mismatch may be contemplated in exceptional circumstances. Table I-2/G.722 indicates the relative performance under all mode mismatch combinations for nominal input levels.

TABLE I-2/G.722

Relative speech performance under mode mismatch (Q_w values)

Bit rate used for audio reception	Bit rate used for audio transmission	
	56 kbit/s	48 kbit/s
64 kbit/s	41	35
56 kbit/s	–	36

Note – The bits not used for audio coding have been replaced by bits of a pseudorandom sequence.

I.6 *Auxiliary data channel performance*

The available combinations of audio and data channel bit rates depends on the connection types described in § I.1 iii).

The data channel is unaffected by the characteristics of the audio signal since the audio and data channels are effectively decoupled. The transparency of the data channel is limited only by the choice of signalling sequences which could be used to derive the terminal identification. If these sequences are chosen to be of a suitable format, the possibility of their simulation by audio or data bits can be made extremely low. Hence, for all practical purposes, the data channel may be assumed to be transparent.

The control of the data channel capacity is considered in Recommendation G.725.

Although the format of the data channel is not part of this Recommendation, it may be noted that the use of two completely independent 8 kbit/s data channels when the total data channel capacity is 16 kbit/s is not prohibited by the algorithm.

Under transmisssion error conditions the data channel is not subject to error multiplication due to the audio coding algorithm.

Note – It might be possible to obtain additional data channel capacity by substituting data for the two bits normally allocated to the higher sub-band with the consequent penalty of a reduction in the audio bandwidth. However, such an approach is likely to require a more stringent specification for the receive filter characteristics in order to minimize aliasing effects.

I.7 *Multi-point conference configuration*

The specific features of a multipoint conference arrangement including control of the data channel, echo control, and handling of control messages between terminals, are beyond the scope of this Recommendation. However, the audio coding algorithm has been chosen to maintain maximum flexibility for multipoint conference arrangements which are likely to emerge. There are a number of general guidelines which should be noted:

- To maximize audio performance, the highest audio bit rate possible, consistent with the transmitted data channel bit rate requirement, should be used for transmission into and out of the signal summing facility of the multipoint conference unit.

  Note – The signal summation must be carried out on a linear representation of the signals.

- The transmit and receive modes of a terminal or port of a multipoint conference unit do not necessarily have to be the same.

- Signal summing at the sub-band uniform PCM level is preferred for the following reasons:

  i) the hardware is minimized in the multipoint conference unit (MCU) by eliminating the need for quadrature mirror filters,

  ii) signal quality is maximized and additional signal delay is eliminated by avoiding additional filtering,

  iii) echo control is likely to be simpler to perform at the sub-band level.

  Figure I-3/G.722 indicates a possible arrangement at the multipoint conference bridge with signal summing at the sub-band level;

- For reasons of audio performance, the number of tandem connected multipoint conference units interconnected with 64 kbit/s (7 kHz) audio coding is limited to three, see Figure I-4/G.722).

- In the case where the multipoint conference unit includes 64 kbit/s PCM ports, digital transcoding principles equivalent to that described in § I.8 should be used to derive the higher and lower sub-band signals.

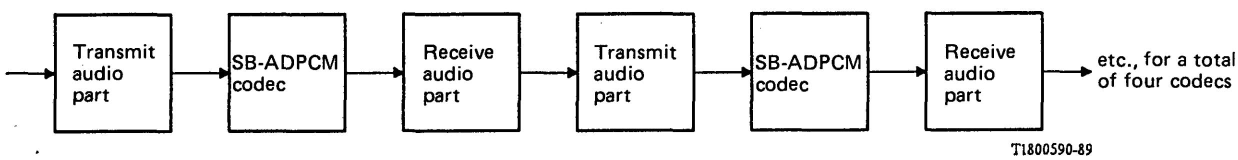


FIGURE I-1/G.722

Four transcodings (analogue interconnection)

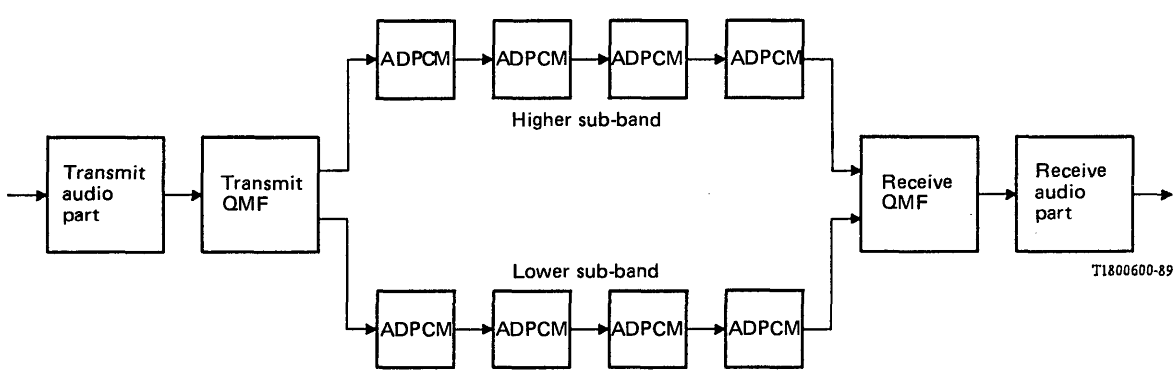


FIGURE I-2/G.722

Four transcodings (digital interconnection)

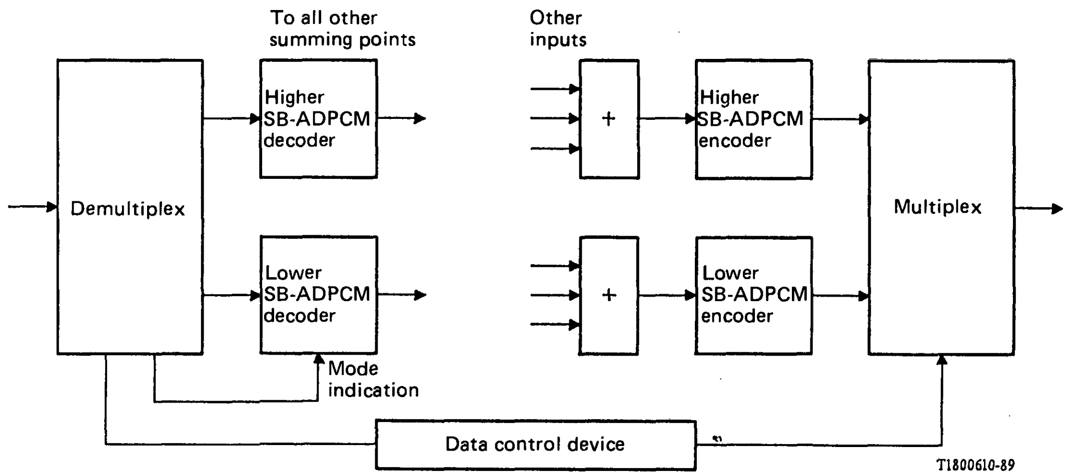


FIGURE I-3/G.722

Possible arrangement at a multipoint conference unit

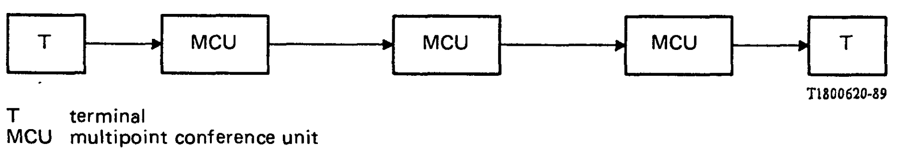


FIGURE I-4/G.722

Tandem connected multipoint conference units

I.8 *Digital transcoding between the 64 kbit/s (7 kHz) audio coding system and 64 kbit/s PCM*

Figure I-5/G.722 indicates the method recommended for the digital interconnection of the 64 kbit/s (7 kHz) audio coding system and 64 kbit/s PCM to Recommendation G.711.

The principle of transcoding from 64 kbit/s PCM to 64 kbit/s (7 kHz) audio coding involves the conversion from A-law or μ-law PCM to uniform PCM and the insertion of interleaved alternate samples of zero amplitude to the 8 kHz sampled uniform PCM signal to form a 16 kHz sampled signal. This signal is then passed through a digital low pass filter sampled at 16 kHz which does not significantly modify the baseband frequency response up to 3.4 kHz and which attenuates the frequency components above 4.6 kHz. The resulting signal is then applied to the sub-band ADPCM encoder as shown in Figure I.3/G.722.

It should be noted that the use of the lower sub-band alone to carry the information in a signal emanating from a 64 kbit/s PCM link to Recommendation G.711 should be avoided.

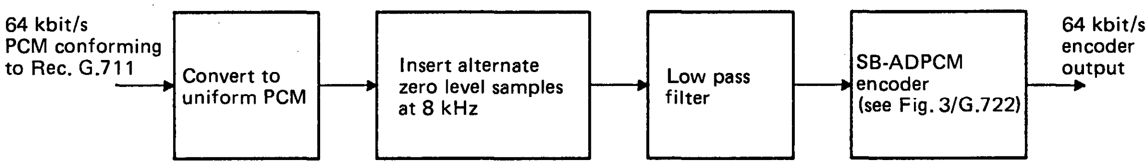
An alternative method of deriving two sub-band signals from a 64 kbit/s PCM signal using the low pass (LP) and high pass (HP) QM filter designs already employed for the 64 kbit/s (7 kHz) audio coding scheme is given in Figure I-6/G.722. The objective is to generate a higher sub-band signal which will eventually cancel the aliasing distortion introduced into the lower sub-band signal. The 64 kbit/s PCM signal is converted to uniform PCM and upsampled to 16 kHz by inserting alternate zero-valued samples. The factor 2 multiplier is inserted to preserve unity gain. The lower sub-band signal is derived by two identical stages of HP QM filtering following by 2:1 subsampling. The higher sub-band signal is derived by two filtering stages, HP followed by LP, a factor 1/2 gain reduction, sign inversion, followed by 2:1 subsampling. When these two signals are input to the QM synthesis filter of Recommendation G.722, an appropriate 7 kHz form of the original PCM is obtained.

Note that the upsampling and subsampling process should be synchronized so that instants of sample deletion correspond to the instants of zero-sample insertion.

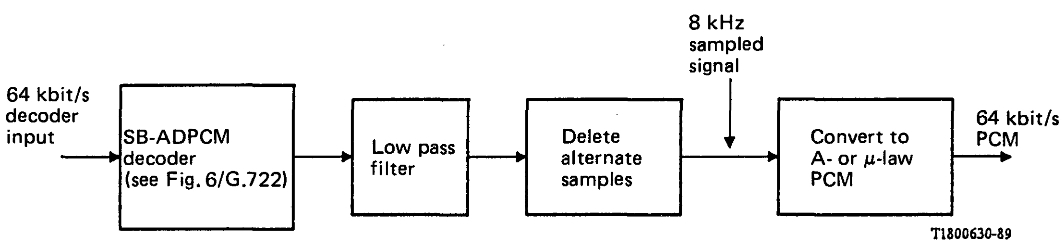
Transcoding from 64 kbit/s (7 kHz) audio coding to 64 kbit/s PCM can be achieved by taking the output signal from the sub-band ADPCM decoder and performing the following three processes in turn:

- digital low pass filtering (16 kHz sampling), which does not significantly modify the baseband frequency response up to 3.4 kHz and which attenuates the frequency components above 4.6 kHz;
- the deletion of alternate samples from the resulting 16 kHz sampled signal;
- conversion from the resulting 8 kHz sampled uniform PCM signal to A-law or μ-law PCM.

Note – The derivation of a 64 kbit/s PCM signal solely from the lower sub-band of the 64 kbit/s (7 kHz) signal is subject to further study.



a) 64 kbit/s PCM to 64 kbit/s (7 kHz) audio coding



b) 64 kbit/s (7 kHz) audio coding to 64 kbit/s PCM

FIGURE I-5/G.722

Digital transcoding between the 64 kbit/s (7 kHz) audio coding system and 64 kbit/s PCM conforming to Recommendation G.711

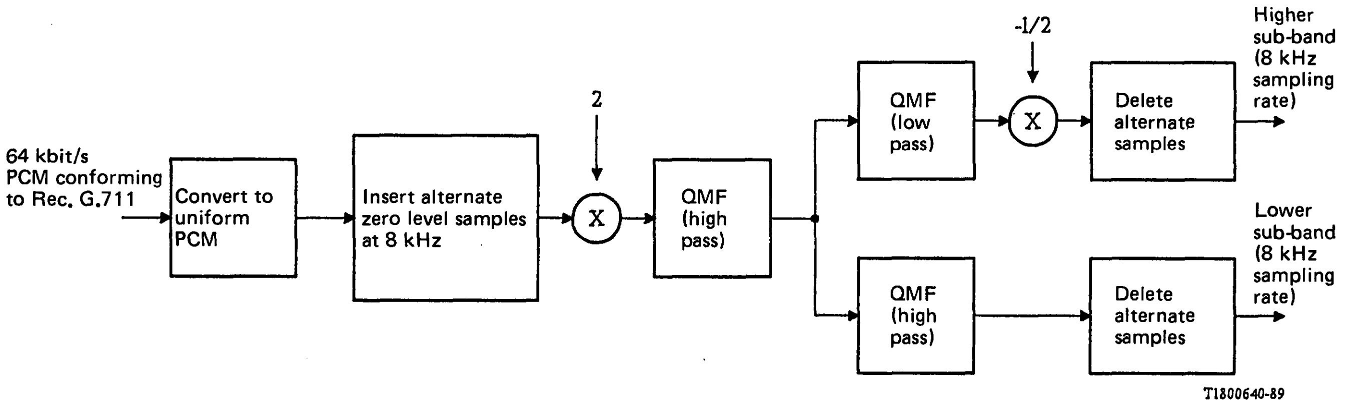


FIGURE I-6/G.722

An alternative method for digital transcoding between 64 kbit/s PCM conforming to Rec. G.711 and 64 kbit/s (7 kHz) audio coding

APPENDIX II

(to Recommendation G.722)

Digital test sequences

This Appendix gives information concerning the digital test sequences which should be used to aid verification of implementations of the ADPCM codec part of the wideband coding algorithm. Copies of the sequences are available on flexible disks (see § II.4).

II.1 *Input and output signals*

Table II-1/G.722 defines the input and output signals for the test sequences. It contains some signals (indicated by #) peculiar to these test sequences in order to facilitate the interface between the test sequence generator/receiver and the encoder/decoder. 16-bit word formats for these input and output signals are shown in Figures II-1/G.722, II-2/G.722 and II-3/G.722.

II.2 *Configuratins for the application of test sequences*

Two configurations (Configuration 1 and Configuration 2) are appropriate for use with test sequences. In both configurations, a TEST signal is used to make the encoder and decoder ready to be tested with the digital test sequences. When the TEST signal is provided, the QMFs are by-passed and the test sequences are applied directly to the ADPCM encoders or decoders. An RSS signal is extracted from the input test sequences X# (I# in decoder) and results in a reset signal RS for the encoder and decoder. The RS signal will be used to initialize state variables (those indicated by * in Table 13/G.722 to zero or specific values.

II.2.1 *Configuration 1*

Configuration 1 shown in Figure II-4/G.722 is a simplified version of Figures 4/G.722 and 5/G.722. The encoder input signals, XL and XH, are described in Table 12/G.722. These input signals are directly fed to the respective lower and higher sub-band ADPCM encoders, by-passing the QMF. The encoder output signals, IL and IH, are defined in the sub-block QUANTL and QUANTH, respectively.

This sequence is used for testing the quantizer/predictor feedback loop in the encoder.

TABLE II-1/G.722

Description of input and output signals for test sequence

Name	Description
XL	15-bit uniformly quantized input signal to the lower sub-band encoder
XH	15-bit uniformly quantized input signal to the higher sub-band encoder
X#	Input test sequence with 16-bit word format as shown in Figure II-1/G.722
IL	6-bit lower sub-band ADPCM codeword
ILR	Received 6-bit lower sub-band ADPCM codeword
IH	2-bit higher sub-band ADPCM codeword
I#	Output (in Configuration 1) and Input (en Configuration 2) test sequence with 16-bit word format as shown in Figure II-2/G.722
RL	15-bit uniformly quantized output signal from the lower sub-band decoder
RH	15-bit uniformly quantized output signal from the higher sub-band decoder
RL#	Output test sequence with 16-bit word format as shown in Figure II-3/G.722
RH#	Output test sequence with 16-bit word format as shown in Figure II-3/G.722
RSS	Reset/synchronization signal
VI	Valid data indication signal

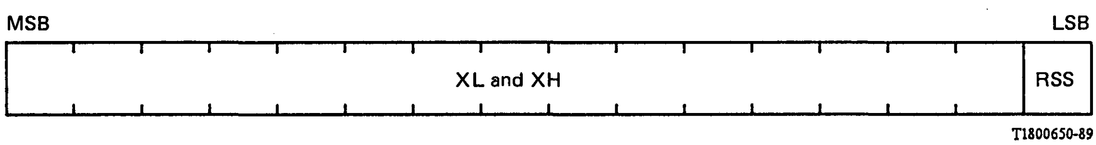
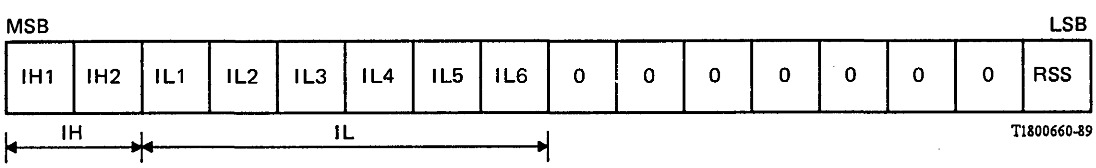


FIGURE II-1/G.722

Word format of X#



Note 1 – IH1 and IL1 are MSBs of IH and IL, respectively.

Note 2 – IL is read as ILR in Configuration 2.

FIGURE II-2/G.722

Word format of I#

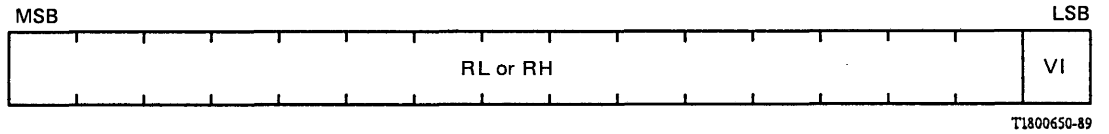


FIGURE II-3/G.722

Word format of RL# and RH#

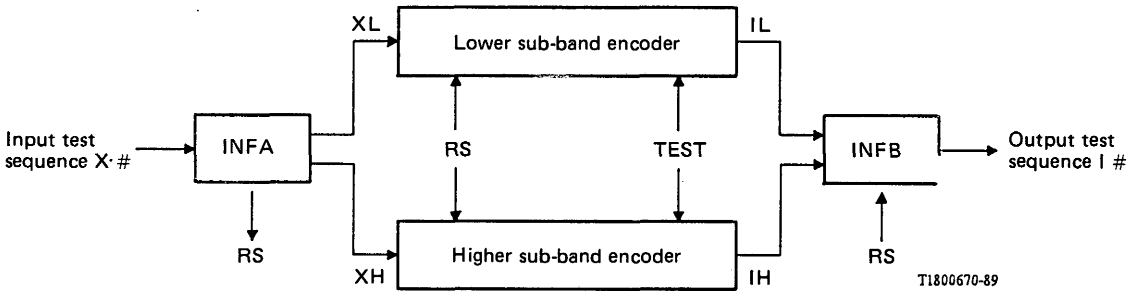


FIGURE II-4/G.722

Configuration 1 – encoder only

II.2.2 *Configuration 2*

Configuration 2 shown in Figure II-5/G.722 is a simplified version of Figures 7/G.722 and 8/G.722. The test signals, ILR and IH, and the MODE signal are described in Table 12/G.722. The corresponding decoder output signals, RL and RH, are defined in the sub-blocks LIMIT in §§ 6.2.1.6 and 6.2.2.5. For the lower sub-band, the ADPCM decoder output signals are derived for three basic modes of operation (Modes 1, 2 and 3). By-passing the QMF, the output signals, RL and RH, are separately obtained from the lower and higher sub-band ADPCM decoders, respectively.

Configuration 2 is used for testing the inverse quantizer operation and the predictor adaptation without a quantizer/predictor feedback loop in the decoder.

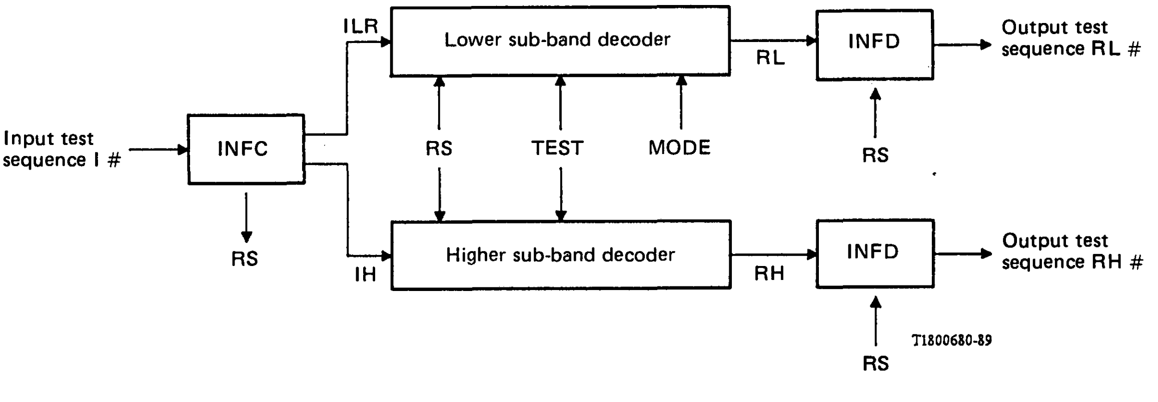


FIGURE II-5/G.722

Configuration 2 – decoder only
(RL and RL# are derived for Modes 1, 2 and 3)

II.2.3 *Reset/synchronization signal (RSS) and valid data indication (VI)*

All memory states in the two test configurations must be initialized to the exact states specified in this Recommendation prior to the start of an input test sequence in order to obtain the correct output values for the test.

In Configuration 1, the input test sequence, X#, is composed of encoder input test signals and the reset/synchronization signal (RSS) as shown in Figure II-1/G.722. The RSS signal is located at the first LSB of the input sequence. If RSS is "1", the lower and higher sub-band encoders are initialized, and the outputs of the encoders are set to "0", i.e., IH = "0" and IL = "0". This normally forbidden output code is used to indicate "non-valid data" of the outputs. After the RSS signal goes to "0", the input test sequence will be valid and the ADPCM algorithm begins to operate.

In Configuration 2, the input test sequence, I#, is composed of the first 8 bits of lower and higher sub-band decoder input codewords, and the last 8 bits consists of 7-bit zeroes and "RSS" in the LSB as shown in Figure II-2/G.722. The RSS signal has the same role as in Configuration 1. That is, if the RSS signal equals "1", the lower and higher sub-band decoders are initialized. After the RSS signal goes to "0", the ADPCM algorithm will be in the operational state. The output test sequences, RL# and RH#, are made up of a decoder output signal of 15 bits and a valid data indication signal (VI) as shown in Figure II-3/G.722. While the RSS signal to the decoder is "1", the signal "VI" is set to "1" and the decoder output set to "0", which indicates "non-valid data" of the output. When "VI" is "0", the output test sequence is valid.

In order to establish the connection between the test sequence generator/receiver and the encoder/decoder, four sub-blocks, INFA, INFB, INFC, INFD in Figures II-4/G.722 and II-5/G.722 are provided. A detailed expansion of these sub-blocks is described below using the same notations specified in § 6.2.

INFA

Input: X#

Outputs: XL, XH, RS

Function: Extract reset/synchronization signal and input signals to lower and higher sub-band ADPCM encoder.

```
RS = X# & 1                                | Extract RSS signal
XL = S# >> 1                               | Lower sub-band input signal
XH = XL                                    | Higher sub-band input signal
```

INFB

Inputs: IL, IH, RS

Outputs: I#

Function: Create an output test sequence by combining lower and higher sub-band ADPCM encoder output signals and the reset/synchronization signal.

$$I = \begin{cases} (IH <<< 6) + IL & \text{if RS == 0} \quad | \text{ Combine IH and IL} \\ 0 & \text{if RS == 1} \quad | \text{ Set output to zero} \end{cases}$$

$$I\# = (I <<< 8) + RS \qquad | \text{ Add RSS signal}$$

INFC

Input: I#

Outputs: ILR, IH, RS

Function: Extract reset/synchronization signal and input signals to lower and higher sub-band ADPCM decoder.

```
RS = I# & 1                      | Extract RSS signal
ILR = (I# >>> 8) & 63            | Lower sub-band ADPCM input
IH = I# >>> 14                   | Higher sub-band ADPCM input
```

INFD

Inputs: RL (RH in higher sub-band), RS

Output: RL#(RH# in higher sub-band)

Function: Create output test sequence by combining lower (higher) sub-band ADPCM decoder output signal and the valid data indication signal.

$$RLX = \begin{cases} RL \ll 1 & \text{if } RS == 0 \\ 0 & \text{if } RS == 1 \end{cases}$$ | Scaling by 1-bit shift | Set output to zero

RL# = RLX + RS | Add VI signal

II.3 *Test sequences*

II.3.1 *Input sequences for Configuration 1*

For Configuration 1, two types of input test sequences are provided:

1) sequence containing tones, d.c. and white noise,
2) sequence for testing overflow controls in the ADPCM encoders.

The first input sequence contains tones with various frequencies, DC and white noise with two levels. The signal segments and lengths are given in Table II-2/G.722.

The tones are used to move the predictor poles over their operating range and to test the stability control. Although the second pole coefficients are settled only in the vicinity of their lower limit for tone inputs, the upper limit is examined at the beginning of the d.c.-positive input. d.c. and white noise are used to vary the quantizer scale factors over their entire range.

The second input sequence permits testing of frequent overflows. The signal segments and lengths are given in Table II-3/G.722.

The sequences produces large prediction errors, so it is used to check the overflow controls in pole and zero section output computations.

In Configuration 1, the coefficient values of the zero predictor do not move to the range limits of -2 and $+2$.

II.3.2 *Input sequences for Configuration 2*

For Configuration 2, these types of input test sequences are provided:

1) The sequence generated by the encoder is used when applying the input test sequence described in Table II-2/G.722;
2) The sequence generated by the encoder is used when applying the input test sequence described in Table II-3/7G.722;
3) An artificial sequence containing consecutive sub-sequences is used that would not ordinarily emanate from an encoder.

The third test sequence, consisting of 16384 values, is described below.

TABLE II-2/G.722

Sequence of tones, d.c. and white noise

Signal segments	Length (16 bits words)
3504 Hz tone	1 024
2054 Hz tone	1 024
1504 Hz tone	1 024
504 Hz tone	1 024
254 Hz tone	1 024
1254 Hz tone	1 024
2254 Hz tone	1 024
3254 Hz tone	1 024
4000 Hz tone	512
d.c, positive, low level	512
d.c., value of zero	512
d.c., negative, low level	512
White noise, low level	3 072
White noise, high level	3 072
Total length of sequence	16 384

TABLE II-3/G.722

Overflow test sequence

Signal segments	Length (16 bits words)
−16 384, +16 383; repeated	639
0, −10 000, −8192	3
−16 384, +16 383, −16 384; repeated	126
Total length of sequence	768

II.3.2.1 *Lower sub-band ADPCM codewords*

The 6-bit lower sub-band decoder input sequence consists of an MSB sequence and a distinct sequence of the remaining 5 bits. The MSB sequence consists of eight artificial sub-sequences, each 2048 bits in length, as follows:

(1) 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 ....
(2) 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 ....
(3) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 ....
(4) 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 ....
(5) 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 ....
(6) 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 ....
(7) 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 ....
(8) 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 ....

These MSB sequences are used to force the coefficients of the zero predictor to vary across the entire range of $\pm$ 2.

The associated 5-bit word sequence consists of 64 concatenated artificial sub-sequences, each 256 values long, as described in Table II-4/G.722. This 5-bit word sequence was chosen to exercise the logarithmic quantizer scale factor over its entire range, and the log-to-linear conversion.

The composite sequence of ILR also tests the pole predictor and varies its coefficients over their allowable range. The sequences from sub-sequence numbers (56) to (64) test the conversion from the suppressed codewords, which can occur due to transmission errors, to specified quantizer intervals.

II.3.2.2 *Higher sub-band ADPCM codewords*

The 2-bit higher sub-band decoder input sequence consists of an MSB sequence and a distinct LSB sequence.

The MSB sequence consists of eight artificial sub-sequences, identical to those used in the MSB sequence for the lower sub-band ADPCM.

The LSB sequence consists of 8 concatenated artificial sub-sequences, each 2048 bits long, as follows:

(1) 1 1 1 1 1 1 ......
(2) alternating sixteen 1s, sixteen 0s
(3) 0 0 0 0 0 0 ......
(4) alternating eight 1s, eight 0s
(5) 0 0 0 0 0 0 ......
(6) alternating four 1s, four 0s
(7) 1 1 1 1 1 1 ......
(8) alternating two 1s, two 0s.

The role of the composite sequence formed by appending the 1-bit LSB to the 1-bit MSB is equivalent to that for the lower sub-band ADPCM codeword described in § II.3.2.1.

II.4 *Format for test sequence distribution*

II.4.1 *Disk interface and format*

Copies of the digital test sequences, on three 5¼″ flexible disk cartridge, are available from the ITU.

The operating system is the PC-DOS or MS-DOS (Version 2.0 or greater). MS-DOS 5¼″ disk format is used.

The following format is used:

– 2 sides 5¼″ flexible disk
– 40 tracks per side
– 9 sectors per track
– 512 bytes per sector.

The files are written in ASCII text in order to be dumped, listed or edited easily.

TABLE II-4/G.722

Sequence of last 5 bits of ILR

Repetitive pattern, each 256 values long	
(1) 31 31 31 31 31 31	(33) 15 15 15 15 15 15 . . . .
(2) alternating sixteen 31's, sixteen 30's	(34) alternating sixteen 15's, sixteen 14's
(3) 30 30 30 30 30 30	(35) 14 14 14 14 14 14 . . . .
(4) alternating sixteen 30's, sixteen 29's	(36) alternating sixteen 14's, sixteen 13's
(5) 29 29 29 29 29 29	(37) 13 13 13 13 13 13 . . . .
(6) alternating sixteen 29's, sixteen 28's	(38) alternating sixteen 13's, sixteen 12's
(7) 28 28 28 28 28 28	(39) 12 12 12 12 12 12 . . . .
(8) alternating sixteen 28's, sixteen 27's	(40) alternating sixteen 12's, sixteen 11's
(9) 27 27 27 27 27 27	(41) 11 11 11 11 11 11 . . . .
(10) alternating sixteen 27's, sixteen 26's	(42) alternating sixteen 11's, sixteen 10's
(11) 26 26 26 26 26 26	(43) 10 10 10 10 10 10 . . . .
(12) alternating sixteen 26's, sixteen 25's	(44) alternating sixteen 10's, sixteen 9's
(13) 25 25 25 25 25 25	(45) 9 9 9 9 9 9 . . . .
(14) alternating sixteen 25's, sixteen 24's	(46) alternating sixteen 9's, sixteen 9's
(15) 24 24 24 24 24 24	(47) 8 8 8 8 8 8 . . . .
(16) alternating sixteen 24's, sixteen 23's	(48) alternating sixteen 8's, sixteen 7's
(17) 23 23 23 23 23 23	(49) 7 7 7 7 7 7 . . . .
(18) alternating sixteen 23's, sixteen 22's	(50) alternating sixteen 7's, sixteen 6's
(19) 22 22 22 22 22 22	(51) 6 6 6 6 6 6 . . . .
(20) alternating sixteen 22's, sixteen 21's	(52) alternating sixteen 6's, sixteen 5's
(21) 21 21 21 21 21 21	(53) 5 5 5 5 5 5 . . . .
(22) alternating sixteen 21's, sixteen 20's	(54) alternating sixteen 5's, sixteen 4's
(23) 20 20 20 20 20 20	(55) 4 4 4 4 4 4 . . . .
(24) alternating sixteen 20's, sixteen 19's	(56) alternating sixteen 4's, sixteen 3's
(25) 19 19 19 19 19 19	(57) 3 3 3 3 3 3 . . . .
(26) alternating sixteen 19's, sixteen 18's	(58) alternating sixteen 3's, sixteen 2's
(27) 18 18 18 18 18 18	(59) 2 2 2 2 2 2 . . . .
(28) alternating sixteen 18's, sixteen 17's	(60) alternating sixteen 2's, sixteen 1's
(29) 17 17 17 17 17 17	(61) 1 1 1 1 1 1 . . . .
(30) alternating sixteen 17's, sixteen 16's	(62) alternating sixteen 1's, sixteen 0's
(31) 16 16 16 16 16 16	(63) 0 0 0 0 0 0 . . . .
(32) alternating sixteen 16's, sixteen 15's	(64) alternating sixteen 0's, sixteen 3's

II.4.2 *Type of files provided*

The test sequences are arranged into 7 files. These 17 files are classified in 3 groups according to the following description:

Class T1: Source files to be input to the ADPCM codec. Class T1 includes 2 files to be used in Configuration 1 (encoder only) and 1 file to be used in Configuration 2 (decoder only).

Class T2: Combined source-comparison files. There are 2 files in class T2. Both are used for comparison purposes at the output of the encoder in Configuration 1. Also they are used as source files to test the decoder in Configuration 2.

Class T3: Comparison files used to check the output of the decoder in different modes. There are 9 files in class T3 to test the lower sub-band decoder and 3 files in the same class to test the higher sub-band decoder. In class T3, the suffix H or L in the file name distinguishes the higher and lower sub-band. Also a number from 1 to 3 in the file name indicates the corresponding mode used for the test.

II.4.3 *Directory of the test sequence files*

This section gives the name and the content of each file provided for the digital test sequences. Figure II-6/G.722 shows which files are to be used in the different configurations of test.

Class T1 file names

T1C1.XMT: 16 416 test values (16-bit words) containing various frequencies, d.c., white noise for encoder test.

T1C2.XMT: 800 test values (16-bit words) containing the artificial sequence to test overflow in the encoder.

T1D3.COD: 16 416 test values (16-bit words) containing the artificial sequence for the decoder test. The most sifnificant 8 bits contain the ADPCM code (IH, IL) and the least significant 8 bits contain the RSS information (reset/synchronisation signal).

Class T2 file names

T2R1.COD: 16 416 test values (16-bit words) containing the output code for the T1C1.XMT file. This file is also used as an input to test the decoder, and consequently has the same structure as the T1D3.COD file.

T2R2.COD: 800 test values (16 bit words) containing the output code for the T1C2.XMT file. This file is also used as source to test the decoder and consequently has the same structure as the T1D3.COD file.

Class T3 file names

T3L1.RC1 16 416 test values (16-bit words) containing the output of the lower sub-band decoder in Mode 1 when the file T2R1.COD is used as an input.

T3L1.RC2 same meaning as for T3L1.RC1 file but when Mode 2 is used.

T3L1.RC3 same meaning as for T3L1.RC1 file but when Mode 3 is used.

T3H1.RC0 16 416 test values (16-bit words) containing the output of the higher sub-band decoder when the file T2R1.COD is used as an input.

T3L2.RC1 800 test values (16-bit words) containing the output of the lower sub-band decoder in Mode 1 when the file T2R2.COD is used as an input.

T3L2.RC2 same meaning as for T3L2.RC1 file but when Mode 2 is used.

T3L2.RC3 same meaning as for T3L2.RC1 file but when Mode 3 is used.

T3H2.RC0 800 test values (16-bit words) containing the output of the higher sub-band decoder when the file T2R2.COD is used as an input.

T3L3.RC1 — 16416 test values (16-bit words) containing the output of the lower sub-band decoder in Mode 1 when the file T1D3.COD is used as an input.

T3L3.RC2 — same meaning as for T3L3.RC1 file but when Mode 2 is used.

T3L3.RC3 — same meaning as for T3L3.RC1 file but when Mode 3 is used.

T3H3.RC0 — 16416 test values (16-bit words) containing the output of the higher sub-band decoder when the file T1D3.COD is used as an input.

Note – Mode indication must be set by the user of the digital test sequences.

Source file	CONFIGURATION 1	Comparison file
T1C1.XMT	⟶	T2R1.COD
T1C2.XMT	⟶	T2R2.COD

Source file	CONFIGURATION 2		Comparison file
T2R1.COD	lower sub-band Mode 1	⟶	T3L1.RC1
	lower sub-band Mode 2	⟶	T3L1.RC2
	lower sub-band Mode 3	⟶	T3L1.RC3
	higher sub-band	⟶	T3H1.RC0
T2R2.COD	lower sub-band Mode 1	⟶	T3L2.RC1
	lower sub-band Mode 2	⟶	T3L2.RC2
	lower sub-band Mode 3	⟶	T3L2.RC3
	higher sub-band	⟶	T3H2.RC0
T1D3.COD	lower sub-band Mode 1	⟶	T3L3.RC1
	lower sub-band Mode 2	⟶	T3L3.RC2
	lower sub-band Mode 3	⟶	T3L3.RC3
	higher sub-band	⟶	T3H3.RC0

FIGURE II-6/G.722

Configuration of test

II.4.4 *File format description*

All the files are written in ASCII with a line structure. The first two lines of each file give some information on the file content. The following format is used for the two first lines:

```
/* CCITT 64 KBIT/S SB-ADPCM        DIGITAL TEST SEQUENCE        G.722 */
/* FILE NAME: xxxx.eee        DATE: mm-dd-yy        VERSION:  V 1.0 */
```

For the subsequent lines of the file, 16 test values (16-bit words, 64 hexadecimal characters) are followed by a checksum on 1 byte (2 hexadecimal characters), a carriage return (ASCII code 0D in hexadecimal), and a line feed (ASCII code 0A in hexadecimal). These last two characters are non-printable.

The checksum is the two's complement of the least significant 8 bits of the summation of all the preceding characters (ASCII codes) in the line. If the least significant 8 bits of the summation are all zero, the corresponding two's complement is set all zero.

At the end of each file, a line of comment closes the file. This line is:

```
/* END OF FILE:  xxxx.eee
```

II.4.5 *Internal line description*

II.4.5.1 *File with extension .XMT*

- 16 words of 16 bits with the LSB set to 1, all others set to zero (RSS = 1: reset mode);
- 16384 or 768 words of 16 bits of digital test sequence with RSS = 0 (RSS is the LSB of the lower byte of the word);
- 16 words of 16 bits with the LSB set to 1, all others set to 0 (marks for end of test sequence).

II.4.5.2 *File with extension .COD*

- 16 words of 16 bits with the LSB set to 1, all others set to 0 (RSS = 1: reset mode and the ADPCM code set to 0);
- 16384 or 768 words of 16 bits of ditigal test sequence with RSS = 0 (RSS is the LSB of the lower byte of the word and the upper byte is the ADPCM code);
- 16 words of 16 bits with the LSB set to 1, all others set to zero (marks for end of test sequence).

II.4.5.3 *File with extension .RCx*

- 16 words of 16 bits with the LSB set to 1, all others set to 0 (this means that these words are non-valid data);
- 16384 or 768 words of 16 bits of ditigal test sequence with the LSB of the lower byte set to 0 to indicate valid data;
- 16 words of 16 bits with the LSB set to 1, all others set to 0 (marks for end of test sequence).

II.4.6 *Distribution of the CCITT digital test sequences*

The distribution of the digital test sequences comprises three 5¼" MS-DOS flexible disks (2 sides, 360 K formatted). The directories of the disks are given in Table II-5/G.722.

TABLE II-5/G.722

Directory digital test sequence diskettes

	Directory		
	Filename	Extension	Number of bytes
Disk 1	T1C1	XMT	69 973
	T1C2	XMT	3 605
	T1D3	COD	69 973
	T2R1	COD	69 973
	T2R2	COD	3 605
Disk 2	T3L1	RC1	69 973
	T3L1	RC2	69 973
	T3L1	RC3	69 973
	T3H1	RC0	69 973
	T3L2	RC1	3 605
	T3L2	RC2	3 605
Disk 3	T3L2	RC3	3 605
	T3H2	RC0	3 605
	T3L3	RC1	69 973
	T3L3	RC2	69 973
	T3L3	RC3	69 973
	T3H3	RC0	69 973

Recommendation G.723

EXTENSIONS OF RECOMMENDATION G.721 ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION TO 24 AND 40 kbit/s FOR DIGITAL CIRCUIT MULTIPLICATION EQUIPMENT APPLICATION

(Melbourne, 1988)

1 General

This Recommendation extends the Adaptive Differential Pulse Code Modulation (ADPCM) algorithm as specified in Recommendation G.721 to include the conversion of a 64 kbit/s A-law or μ-law PCM channel to and from a 24 kbit/s or 40 kbit/s channel.

The principal application of 24 kbit/s channels if for overload channels carrying voice in Digital Circuit Multiplication Equipment (DCME).

The principal application of 40 kbit/s channels is to carry data modem signals in DCME, especially for modems operating at greater than 4800 bit/s.

Paragraph 2 of this Recommendation describes the changes in principles needed for encoding and decoding in 24 and 40 kbit/s operation. § 3 provides the changed computational details for 24 kbit/s coding and Section 4 provides the changed details for 40 kbit/s coding. Appendices I and II address network aspects and digital test sequences.

Note 1 – Prior to the definition of this Recommendation, other ADPCM algorithms of similar performance have been incorporated in DCME designs and used in telecommunication networks. These algorithms may be considered by bilateral agreement for limited DCME applications, under certain circumstances. Technical descriptions providing information on two such algorithm approaches can be found in COM XVIII No. 101 and COM XVIII No. 102.

Note 2 – The assignment of 24, 32 and 40 kbit/s DCME channels and the associated selection of coding rates are beyond the scope of this Recommendation.

2 Changes to the ADPCM principles

Figure 2/G.721 and Figure 3/G.721 provide block schematics of the encoder and decoder respectively.

2.1 *Changes to principles for 24 kbit/s*

To achieve 24 kbit/s operation, the adaptive quantizer is modified to produce a 3-bit quantized output $I(k)$, where $I(k)$ takes on one of seven non-zero values. $I(k)$ is fed to the inverse adaptive quantizer, the adaptation speed control and the quantizer scale factor adaptation blocks; each of which is modified to operate on a 3-bit $I(k)$ having any of the eight possible values. $I(k) = 000$ is a legitimate input to these blocks when used in the decoder, due to transmission errors.

Specifically, § 2.3 of Recommendation G.721 is the same except that Table 1/G.721 becomes Table 1/G.723.

TABLE 1/G.723

Quantizer normalized input/output characteristic for 24 kbit/s operation

Normalized quantizer input range $\log_2 \mid d(k) \mid - y(k)$	$\mid I(k) \mid$	Normalized quantizer output $\log_2 \mid d_q(k) \mid - y(k)$
[2.58 + ∞)	3	2.91
[1.70, 2.58)	2	2.13
[0.06, 1.70)	1	1.05
(– ∞, 0.06)	0	– ∞

Recommendation G.721, § 2.5 is the same except that the discrete function $W(I)$ is defined as follows:

$\mid I(k) \mid$	3	2	1	0
$W(I)$	36.38	8.56	1.88	–0.25

Recommendation G.721, § 2.6 is the same except that $F[I(k)]$ is defined by:

$\|I(k)\|$	3	2	1	0
$F[I(k)]$	7	2	1	0

2.2 *Changes to principles for 40 kbit/s*

The 40 kbit/s operation is achieved by modifying the adaptive quantizer to produce a 5-bit quantized output $I(k)$, where $I(k)$ takes on one of 31 non-zero values. $I(k)$ is fed to the inverse adaptive quantizer, the adaptation speed control and the quantizer scale factor adaptation blocks; each of which is modified to operate on a 5-bit $I(k)$ having one of 32 possible values. $I(k) = 00000$ is a legitimate input to these blocks when used in the decoder, due to transmission errors.

Specifically, Recommendation G.721, § 2.3 is the same except that Table 1/G.721 becomes Table 2/G.723.

TABLE 2/G.723

Quantizer normalized input/output characteristic for 40 kbit/s operation

Normalized quantizer input range $\log_2 \|d(k)\| - y(k)$	$\|I(k)\|$	Normalized quantizer output $\log_2 \|d_q(k)\| - y(k)$
[4.31 + ∞)	15	4.42
[4.12, 4.31)	14	4.21
[3.91, 4.12)	13	4.02
[3.70, 3.91)	12	3.81
[3.47, 3.70)	11	3.59
[3.22, 3.47)	10	3.35
[2.95, 3.22)	9	3.09
[2.64, 2.95)	8	2.80
[2.32, 2.64)	7	2.48
[1.95, 2.32)	6	2.14
[1.54, 1.95)	5	1.75
[1.08, 1.54)	4	1.32
[0.52, 1.08)	3	0.81
[−0,13, 0.52)	2	0.22
[−0.96, −0.13)	1	−0.52
(−∞, −0.96)	0	−∞

Recommendation G.721, § 2.5 is the same except that the discrete function $W(I)$ is defined as follows:

$\|I(k)\|$	15	14	13	12	11	10	9	8
$W(I)$	43.50	33.06	27.50	22.38	17.50	13.69	11.19	8.81

$\|I(k)\|$	7	6	5	4	3	2	1	0
$W(I)$	2.48	2.14	1.75	1.32	0.81	0.22	−0.52	$-\infty$

Recommendation G.721, § 2.6 is the same except that $F[I(k)]$ is defined by:

$\|I(k)\|$	15	14	13	12	11	10	9	8
$F[I(k)]$	6	6	5	4	3	2	1	1

$\|I(k)\|$	7	6	5	4	3	2	1	0
$F[I(k)]$	1	1	1	0	0	0	0	0

In addition, for 40 kbit/s coding, the adaptive predictor is changed to decrease the leak factor used for zeroes coefficient operation. Equation (2-12) of Recommendation G.721 becomes:

$$b_i(k) = (1 - 2^{-9})b_i(k - 1) + 2^{-7}\text{sgn}[d_q(k)\text{sgn}[d_q(k - i)]$$

3 Computational details for 24 kbit/s ADPCM

The computational details of the 24 kbit/s ADPCM are identical to the computational details of the 32 kbit/s ADPCM (§ 4 of Recommendation G.721) with the exception of the following items:

- The ADPCM word defined as variable I in Table 2/G.721 has 3 bits for both the encoder and decoder.
- The blocks QUAN, RECONST, FUNCTW, FUNCTF and SYNC are modified according to the changes in principles described in § 2.1 above. Paragraphs 3.1 to 3.5 below detail the changes.

3.1 *Changes to the adaptive quantizer*

The following block replaces the block QUAN in § 4.2.2 of Recommendation G.721:

QUAN (encoder only)

Inputs: DLN, DS

Output: I

Function: Quantize difference signal in the logarithmic domain.

Quantizer decision levels and 3-bit outputs:

DS	DLN	I 123	
0	331-2047	011	
0	218- 330	010	
0	8- 217	001	
0	0- 7	111	– – | Positive portion of interval
0	2048-4095	111	– – | Negative portion of interval
1	2048-4095	111	– – | Negative portion of interval
1	0- 7	111	– – | Positive portion of interval
1	8- 217	110	
1	218- 330	101	
1	331-2047	100	

Note – The I values are transmitted starting with bit 1.

3.2 *Changes to the inverse adaptive quantizer*

The following block replaces the block RECONST in § 4.2.3 of Recommendation G.721:

RECONST

Input: I

Outputs: DQLN, DQS

Function: Reconstruction of quantized difference signal in the logarithmic domain.

DQS = I >> 2

Quantizer output levels:

I 123	DQS	DQLN
011	0	373
010	0	273
001	0	135
000	0	2048
111	1	2048
110	1	135
101	1	273
100	1	373

Not 1 – The I values are received starting with bit 1.

Note 2 – It is possible for the decoder to receive the code word 000 because of transmission disturbances (e.g. line bit errors).

3.3 *Changes to the quantizer scale factor adaptation*

The following block replaces the block FUNCTW in § 4.2.4 of Recommendation G.721:

FUNCTW

Input: I

Output: WI

Function: Map quantizer output into logarithmic version of scale factor multipler.

IS= I >> 2

$$IM = \begin{cases} I \,\&\, 3, & IS = 0 \\ (7 - I) \,\&\, 3, & IS = 1 \end{cases}$$

$$WI = \begin{cases} 582, & IM = 3 \\ 137, & IM = 2 \\ 30, & IM = 1 \\ 4092, & IM = 0 \end{cases} \quad \Bigg| \text{ Scale factor multipliers}$$

3.4 *Changes to the adaptation speed control*

The following block replaces the block FUNCTF in § 4.2.5 of Recommendation G.721:

FUNCTF

Input: I

Output: FI

Function: Map quantizer output into the F(I) function.

IS = I >> 2

$$IM = \begin{cases} I \,\&\, 3, & IS = 0 \\ (7 - I) \,\&\, 3, & IS = 1 \end{cases}$$

$$FI = \begin{cases} 0, & IM = 0 \\ 1, & IM = 1 \\ 2, & IM = 2 \\ 7, & IM = 3 \end{cases}$$

3.5 *Changes to the output PCM format conversion and synchronous coding adjustment*

The following block replaces the block SYNC in § 4.2.8 of Recommendation G.721:

SYNC (decoder only)

Inputs: I, SP, DLNX, DSX, LAW

Output: SD

Function: Re-encode output PCM sample in decoder for synchronous tandem coding.

IS = I >> 2

$$IM = \begin{cases} I + 4, & IS = 0 \\ I \,\&\, 3, & IS = 1 \end{cases}$$

ID is defined according to the following table:

DSX	DLNX	ID	
0	331-2047	7	
0	218- 330	6	
0	8- 217	5	– – | Positive portion of decision interval
0	0- 7	3	– – | Negative portion of decision interval
0	2048-4095	3	– – | Negative portion of decision interval
1	2048-4095	3	– – | Positive portion of decision interval
1	0- 7	3	
1	8- 217	2	
1	218- 330	1	
1	331-2047	0	

$$SD = \begin{cases} SP^{+}, & ID < IM \\ SP, & ID = IM \\ SP^{-}, & ID > IM \end{cases}$$

where

SP^{+} = the PCM code word that represents the next more positive PCM output level (when SP represents the most positive PCM output level, then SP^{+} is constained to be SP),

SP^{-} = the PCM code word that represents the next more negative PCM output level (when SP represents the most negative PCM output level, then SP^{-} is constrained to be SP).

For the purposes of clarification, examples of re-encoding for both A-law (after even bit inversion) and μ-law in the vicinity of the origin are given in the table below:

Comparison of ID and IM	A-law		μ-law	
	SP	SD	SP	SD
ID > IM	11010101	01010101	11111110	11111111
ID = IM	"	11010101	"	11111110
ID < IM	"	11010100	"	11111101
ID > IM	01010101	01010100	11111111	01111110
ID = IM	"	01010101	"	11111111
ID < IM	"	11010101	"	11111110
ID > IM	01010100	01010111	01111110	01111101
ID = IM	"	01010100	"	01111110
ID < IM	"	01010101	"	01111111

Note – SP (and SD) represent character signals defined according to Tables 1/G.711 and 2/G.711. See sub-block COMPRESS (§ 4.2.8 of Rec. G.721) for the exact representation of SP (and SD).

---

4 Computational details for 40 kbit/s ADPCM

The computational details of the 40 kbit/s ADPCM are identical to the computational details of the 32 kbit/s ADPCM (§ 4 of Recommendation G.721) with the exception of the following items:

– The ADPCM word defined as variable I in Table 2/G.721 has 5 bits for both the encoder and decoder.

– The larger output levels in the inverse quantizer necessitate a 1-bit increase in the length of the binary representation of the quantized difference signal DQ. Corresponding changes in Table 3/G.721 and blocks ANTILOG, ADDB, ADDC, FLOATA, UPB, XOR and TRANS are detailed in § 4.1.

– The blocks QUAN, RECONST, FUNCTW, FUNCTF, UPB and SYNC are modified according to the changes in principles described in § 2.2. Paragraphs 4.2 to 4.7 detail the changes.

4.1 *Changes related to the increased binary length of DQ*

Note – All of the changes in § 4.1 can remain in effect during operation at 24 and 32 kbit/s without affecting compliance to Recommendation G.721 at 32 kbit/s or this Recommendation at 24 kbit/s.

i) Replace line describing the variable DQ in Table 3/G.721 by:

Name	Bits (see note)	Binary representation	Optional reset values	Description
DQ	16 SM	S,14,..,0		Quantized difference signal

ii) The following equation replaces the equation for DQ in block ANTILOG in § 4.2.3 of Recommendation G.721:

$$DQ = (DQS << 15) + DQMAG \qquad | \text{ Attach sign bit to signed magnitude word}$$

iii) The following equations replace the equations for DQS and DQI in block ADDB in § 4.2.6 of Recommendation G.721:

$$DQS = DQ >> 15$$

$$DQI = \begin{cases} DQ, & DQS = 0 \\ (65536 - (DQ \ \& \ 32767)) \ \& \ 65535, & DQS = 1 \end{cases} \qquad | \text{ Convert signed magnitude to two's complement}$$

iv) The following equations replace the equations for DQS and DQI in bloc ADDC in § 4.2.6 of Recommendation G.721:

$$DQS = DQ >> 15$$

$$DQI = \begin{cases} DQ, & DQS = 0 \\ (65536 - (DQ \ \& \ 32767)) \ \& \ 65535, & DQS = 1 \end{cases} \qquad | \text{ Convert signed magnitude to two's complement}$$

v) The following equations replace the equations for DQS, MAG and EXP in block FLOATA in § 4.2.6 of Recommendation G.721:

$$DQS = DQ >> 15$$

$$MAG = DQ \ \& \ 32767 \qquad | \text{ Compute magnitude}$$

$$EXP = \begin{cases} 15, & 16384 \leqslant MAG \\ 14, & 8192 \leqslant MAG \leqslant 16383 \\ 13, & 4096 \leqslant MAG \leqslant 8191 \\ \vdots & \vdots \\ 2, & 2 \leqslant MAG \leqslant 3 \\ 1, & MAG = 1 \\ 0, & MAG = 0 \end{cases} \qquad | \text{ Compute exponent}$$

vi) The following equation replaces the equation for DQMAG in block UPB in § 4.2.6 of Recommendation G.721:

$$DQMAG = DQ \ \& \ 32767$$

vii) The following equation replaces the equation for DQS in block XOR in § 4.2.6 of Recommendation G.721:

$$DQS = DQ >> 15$$

viii) The following equations replace the equations for DQMAG and THR2 in block TRANS in § 4.2.7 of Recommendation G.721:

$$DQMAG = DQ \ \& \ 32767$$

$$THR2 = \begin{cases} 31 << 10, & YLINT > 9 \\ THR1, & \text{otherwise} \end{cases}$$

4.2 *Changes to the adaptive quantizer*

The following block replaces the block QUAN in § 4.2.2 of Recommendation G.721:

QUAN (encoder only)

Inputs: DLN, DS

Output: I

Function: Quantize difference signal in the logarithmic domain.

Quantizer decision levels and 5-bit outputs:

DS	DLN	I 12345	
0	553-2047	01111	
0	528- 552	01110	
0	502- 527	01101	
0	475- 501	01100	
0	445- 474	01011	
0	413- 444	01010	
0	378- 412	01001	
0	339- 377	01000	
0	298- 338	00111	
0	250- 297	00110	
0	198- 249	00101	
0	139- 197	00100	
0	68- 138	00011	
0	0- 67	00010	– – | Positive portion of interval
0	4080-4095	00010	– – | Negative portion of interval
0	3974-4079	00001	
0	2048-3973	11111	
1	2048-3973	11111	
1	3974-4079	11110	
1	4080-4095	11101	– – | Negative portion of interval
1	0- 67	11101	– – | Positive portion of interval
1	68- 138	11100	
1	139- 197	11011	
1	198- 249	11010	
1	250- 297	11001	
1	298- 338	11000	
1	339- 377	10111	
1	378- 412	10110	
1	413- 444	10101	
1	445- 474	10100	
1	475- 501	10011	
1	502- 527	10010	
1	528- 552	10001	
1	553-2047	10000	

Note – The I values are transmitted starting with bit 1.

4.3 *Changes to the inverse adaptive quantizer*

The following block replaces the block RECONST in § 4.2.3 of Recommendation G.721:

RECONST

Input: I

Outputs: DQLN, DQS

Function: Reconstruction of quantized difference signal in the logarithmic domain.

DQS = I >> 4

Quantizer output levels:

I 12345	DQS	DQLN
01111	0	566
01110	0	539
01101	0	514
01100	0	488
01011	0	459
01010	0	429
01001	0	395
01000	0	358
00111	0	318
00110	0	274
00101	0	224
00100	0	169
00011	0	104
00010	0	28
00001	0	4030
00000	0	2048
11111	1	2048
11110	1	4030
11101	1	28
11100	1	104
11011	1	169
11010	1	224
11001	1	274
11000	1	318
10111	1	358
10110	1	395
10101	1	429
10100	1	459
10011	1	488
10010	1	514
10001	1	539
10000	1	566

Not 1 – The I values are received starting with bit 1.

Note 2 – It is possible for the decoder to receive the code word 00000 because of transmission disturbances (e.g. line bit errors).

4.4 *Changes to the quantizer scale factor adaptation*

The following block replaces the block FUNCTW in § 4.2.4 of Recommendation G.721:

FUNCTW

Input: I

Output: WI

Function: Map quantizer output into logarithmic version of scale factor multiplier.

IS = I >> 4

$$IM = \begin{cases} I \,\&\, 15, & IS = 0 \\ (31 - I) \,\&\, 15, & IS = 1 \end{cases}$$

$$WI = \begin{cases} 696, & IM = 15 \\ 529, & IM = 14 \\ 440, & IM = 13 \\ 358, & IM = 12 \\ 280, & IM = 11 \\ 219, & IM = 10 \\ 179, & IM = 9 \\ 141, & IM = 8 \\ 100, & IM = 7 \\ 58, & IM = 6 \\ 41, & IM = 5 \\ 40, & IM = 4 \\ 39, & IM = 3 \\ 24, & IM = 2 \\ 14, & IM = 1 \\ 14, & IM = 0 \end{cases} \quad \text{Scale factor multipliers}$$

4.5 *Changes to the adapation speed control*

The following block replaces the block FUNCTF in § 4.2.5 of Recommendation G.721:

FUNCTF

Input: I

Output: FI

Function: Map quantizer output into the F(I) function.

IS = I >> 4

$$IM = \begin{cases} I \,\&\, 15, & IS = 0 \\ (31 - I) \,\&\, 15, & IS = 1 \end{cases}$$

$$FI = \begin{cases} 0, & 0 \leqslant IM \leqslant 4 \\ 1, & 5 \leqslant IM \leqslant 9 \\ 2, & IM = 10 \\ 3, & IM = 11 \\ 4, & IM = 12 \\ 5, & IM = 13 \\ 6, & IM = 14 \\ 6, & IM = 15 \end{cases}$$

4.6 *Changes to adaptive predictor and reconstructed signal calculator*

The following block replaces the block UPB in § 4.2.6 of Recommendation G.721:

UPB

Inputs: Un, Bn, DQ

Output: BnP

Function: Update for coefficients of sixth order predictor.

DQMAG = DQ & 32767

$$UGBn = \begin{cases} 128, & Un = 0 \text{ and } DQMAG \neq 0 \\ 65408, & Un = 1 \text{ and } DQMAG \neq 0 \\ 0, & DQMAG = 0 \end{cases}$$ | Gain = ± 1/128 or 0

BnS = Bn >> 15

$$ULBn = \begin{cases} (65536 - (Bn >> 9)) \,\&\, 65535, & BnS = 0 \\ (65536 - ((Bn >> 9) + 65408)) \,\&\, 65535, & BnS = 1 \end{cases}$$ | Leak factor = 1/512

UBn = (UGBn + ULBn) & 65535 | Compute update

BnP = (Bn + UBn) & 65535

4.7 *Changes to the output PCM format conversion and synchronous coding adjustment*

The following block replaces the block SYNC in § 4.2.8 of Recommendation G.721:

SYNC (decoder only)

Inputs: I, SP, DLNX, DSX, LAW

Output: SD

Function: Re-encode output PCM sample in decoder for synchronous tandem coding.

$IS = I >> 4$

$$IM = \begin{cases} I + 16, & IS = 0 \\ I \,\&\, 15, & IS = 1 \end{cases}$$

ID is defined according to the following table:

DSX	DLNX	ID	
0	553-2047	31	
0	528- 552	30	
0	502- 527	29	
0	475- 501	28	
0	445- 474	27	
0	413- 444	26	
0	378- 412	25	
0	339- 377	24	
0	298- 338	23	
0	250- 297	22	
0	198- 249	21	
0	139- 197	20	
0	68- 138	19	
0	0- 67	18	– – | Positive portion of decision interval
0	4080-4095	18	– – | Negative portion of decision interval
0	3974-4079	17	
0	2048-3973	15	
1	2048-3973	15	
1	3974-4079	14	
1	4080-4095	13	– – | Negative portion of devision interval
1	0- 67	13	– – | Positive portion of decision interval
1	68- 138	12	
1	139- 197	11	
1	198- 249	10	
1	250- 297	9	
1	298- 338	8	
1	339- 377	7	
1	378- 412	6	
1	413- 444	5	
1	445- 474	4	
1	475- 501	3	
1	502- 527	2	
1	528- 552	1	
1	553-2047	0	

$$SD = \begin{cases} SP^+, & ID < IM \\ SP, & ID = IM \\ SP^-, & ID > IM \end{cases}$$

where

SP^+ = the PCM code word that represents the next more positive PCM output level (when SP represents the most positive PCM output level, then SP^+ is constrained to be SP),

SP^- = the PCM code word that represents the next more negative PCM output level (when SP represents the most negative PCM output level, then SP^- is constrained to be SP).

For the purposes of clarification, examples of re-encoding for both A-law (after even bit inversion) and μ-law in the vicinity of the origin are given in the table below:

Comparison of ID and IM	A-law		μ-law	
	SP	SD	SP	SD
ID > IM	11010101	01010101	11111110	11111111
ID = IM	"	11010101	"	11111110
ID < IM	"	11010100	"	11111101
ID > IM	01010101	01010100	11111111	01111110
ID = IM	"	01010101	"	11111111
ID < IM	"	11010101	"	11111110
ID > IM	01010100	01010111	01111110	01111101
ID = IM	"	01010100	"	01111110
ID < IM	"	01010101	"	01111111

Note – SP (and SD) represent character signals defined according to Tables 1/G.711 and 2/G.711. See sub-block COMPRESS (Rec. G.721, § 4.2.8) for the exact representation of SP (and SD).

APPENDIX I

(to Recommendation G.723)

Network aspects

The purpose of this Appendix is to give a broad outline of the interaction of 24 and 40 kbit/s ADPCM with other devices that are found in the telephony network and also the effect of specific signals found in the network. Some general guidance is also offered.

I.1 *General transmission considerations*

The 24 kbit/s coding is intended for use with DCME overload channels. It is recommended that 24 kbit/s and 32 kbit/s coding be alternated rapidly such that at least 3.5 to 3.7 bits/sample are used on average (for further study). The method of alternation is for further study. The effect on speech quaity of this alternation is not expected to be significant. The use of 24 kbit/s coding for data transmission is not recommended.

The 40 kbit/s coding is intended for use with DCME data modem channels, especially for modem operation at speeds greater than 4800 bit/s. Preliminary tests indicate that for voice the 40 kbit/s ADPCM coding performs approximately as well as 64 kbit/s PCM according to Recommendation G.711.

I.2 *Encoder/decoder synchronization*

The encoder and its respective decoder must always operate at the same bit rate, (i.e. 24, 32 or 40 kbit/s), or otherwise severe mistracking may occur.

I.3 *Synchronous coding adjustment*

The synchronous coding adjustment will work correctly when an ADPCM encoder/decoder pair is connected by a bit-transparent PCM path to another encoder/decoder pair operating at the same rate. When two encoder/decoder pairs are operating at different rates, the synchronous tandeming property is not guaranteed to be established.

I.4 *Data performance*

Voiceband data at speeds up to 12 000 bit/s can be accommodated by 40 kbit/s ADPCM. The performance of V.33 modems operating at 14 400 bit/s over 40 kbit/s ADPCM is for further study.

I.5 *Dual tone multi-frequency (DTMF) signalling*

Under normal DCME operating conditions, no significant problem with DTMF signalling is expected.

I.6 *Facsimile*

No significant degradation is to be expected when using this service with Group 2 of Group 3 facsimile apparatus according to Recommendation T.3 or T.4, in conjunction with 40 kbit/s ADPCM coding.

APPENDIX II

(to Recommendation G.723)

Digital test sequences

Digital test sequences equivalent to those of Appendix II to Recommendation G.721 have been chosen to aid verification of implementations of the 24 kbit/s and 40 kbit/s algorithms.

The test sequences are available on two additional pairs of flexible disks: one pair for 24 kbit/s coding and another pair for 40 kbit/s coding. Each diskette contains a README file which provides all the information necessary to use that particular diskette.

Copies of the digital test sequences on 5¼″ diskettes are available from the ITU.

CHARACTERISTICS OF A 48-CHANNEL LOW BIT RATE ENCODING PRIMARY MULTIPLEX OPERATING AT 1544 kbit/s

(Melbourne, 1988)

1 General

1.1 *Fundamental characteristics*

The 48-channel primary multiplexer provides conversion between 48 voice-frequency channels and one 1544 kbit/s ADPCM stream. In the 1544 kbit/s stream, the voice-frequency signals are coded according to the PCM encoding law defined in Recommendation G.711 and the ADPCM encoding law defined in Recommendation G.721. In addition, it may be arranged to provide limited 64 kbit/s unrestricted channel transfer capacity for baseband digital channel.

Figure 1/G.724 represents the nomenclature used.

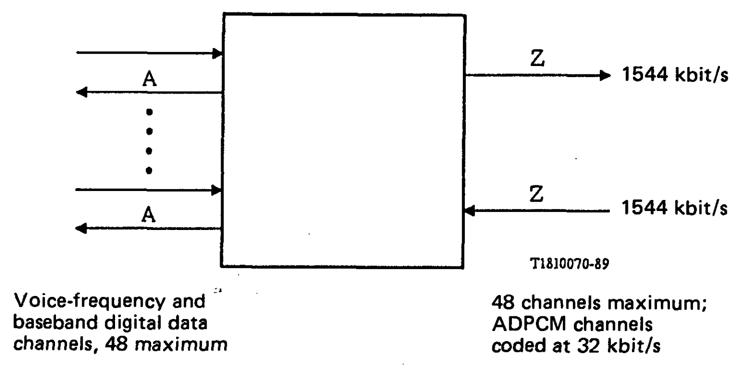


FIGURE 1/G.724

48-channel low bit rate encoding primary multiplex

The 1544 kbit/s stream associated with port Z can be partitioned into four independent 384 kbit/s entities defined as time-slot groupings. Each 384 kbit/s time-slot grouping consists of twelve 32 kbit/s time slots which can be used to transport up to 12 voice-frequency channels or 11 voice-frequency channels plus their channel associated a-b-c-d signalling information. Therefore, the 1544 kbit/s stream associated with port Z will have a maximum channel capacity of between 44 and 48 voice-frequency channels.

Note 1 – Administrations should take into account the guidance given in Recommendation G.721 concerning the use and transmission performance of 32 kbit/s ADPCM.

Note 2 – It should be noted that the primary multiplex equipment described in this Recommendation has a limited capability of transparently transporting 64 kbit/s data channel, and this should be taken into account in the planning of networks which are likely to evolve into an ISDN (see § 4.2).

1.2 *Timing signal*

It should be possible to derive the transmit timing signal from an incoming digital signal or from an external source.

2 Characteristics of port A interfaces

Analogue: Refer to § 3 of Recommendation G.712 and § 3 of Recommendation G.713.

Digital: Refer to § 1 of Recommendation G.703.

3 End-to-end analogue transmission performance

For further study.

4 Characteristics of a 1544 kbit/s signal organized in 32 kbit/s and/or 64 kbit/s timeslots (port Z)

4.1 *Interface Z*

The electrical characteristics of the 1544 kbit/s interface are in accordance with § 2 of Recommendation G.703.

4.2 *Frame structure*

4.2.1 *Frame structure at 1544 kbit/s*

Refer to § 3.2.1 of Recommendation G.704 for frame structure and use of derived channel time slots.

4.2.2 *Frame structure at 384 kbit/s*

Refer to § 3.2.3 of Recommendation G.704 for frame structure at 348 kbit/s.

4.3 *Loss and recovery of frame and multiframe alignment*

4.3.1 *Loss and recovery of 1544 kbit/s frame and multiframe alignment*

The criteria for loss and recovery of the frame alignment and multiframe alignment signal for port Z are in accordance with § 2.1 of Recommendation G.706 for the 24-frame multiframe and for the 12-frame multiframe.

4.3.2 *Loss and recovery of signalling grouping channel multiframe alignment*

The criteria for loss and recovery of the signalling grouping channel multiframe alignment signal are in accordance with § 3.2.6 of Recommendation G.704.

4.4 *Signalling*

Refer to § 3.2.4 of Recommendation G.704 for signalling in the 384 kbit/s stream.

5 Other characteristics of the low bit rate encoding primary multiplex equipment

5.1 *48-channel frame structure*

In the case where streams A are each carrying 48 voice-frequency signals and no channel associated signalling information is present, stream Z will transmit the full complement of 48 channels. When channel associated signalling is present, this is conveyed in the last 4-bit time slot of each time-slot grouping. Table 1/G.724 shows the correspondence between the VF channels and the 32 kbit/s ADPCM channels in stream Z.

5.2 *Direct time-slot transfer*

It should be possible to select and pass voice-frequency and baseband digital A streams through the Z stream at 64 kbit/s. Furthermore, it should be possible to pass through at least one such 64 kbit/s channel in each time-slot grouping in stream Z.

TABLE 1/G.724

Organization of the 1544 kbit/s frame for up to 48 channels at 32 kbit/s in stream Z

4-bit time slot of stream Z	1	2	3	4	5	6	7	8	9	10	11	12
Voice-frequency channels of stream A	1A	2A	3A	4A	5A	6A	7A	8A	9A	10A	11A	12A or SGC

Time-slot grouping 1

4-bit time slot of stream Z	13	14	15	16	17	18	19	20	21	22	23	24
Voice-frequency channels of stream A	13A	14A	15A	16A	17A	18A	19A	20A	21A	22A	23A	24A or SGC

Time-slot grouping 2

4-bit time slot of stream Z	25	26	27	28	29	30	31	32	33	34	35	36
Voice-frequency channels of stream A	25A	26A	27A	28A	29A	30A	31A	32A	33A	34A	35A	36A or SGC

Time-slot grouping 3

4-bit time slot of stream Z	37	38	39	40	41	42	43	44	45	46	47	48
Voice-frequency channels of stream A	37A	38A	39A	40A	41A	42A	43A	44A	45A	46A	47A	48A or SGC

Time-slot grouping 4

SGC Signalling grouping channel.

Note – Selection of the time-slot grouping format to include the signalling grouping channel is made on a per-time-slot grouping basis, independent of the other time-slot groupings.

5.3 *Signalling grouping channel alarm indications*

A time-slot grouping alarm is declared when the signalling grouping channel multiframe alignment signal is lost for an interval of between 2 to 3 seconds.

When signalling grouping channel multiframe alignment is lost (as per § 3.2.6 of Recommendation G.704), updating of the channel-associated signalling bits on the receive side of stream A will be disabled.

The time-slot grouping alarm is released when signalling grouping channel multiframe alignment has been re-acquired for an interval of between 10 to 20 seconds.

When signalling grouping channel multiframe alignment is declared (as per § 3.2.6 of Recommendation G.704, updating of the channel-associated signalling bits on the receive side of stream A will be enabled.

On the send side, M_1 is set to 1 to transmit a time-slot grouping alarm to the remote end when the near end is in time-slot grouping alarm. On the receive side, a remote time-slot grouping alarm is declared when M_1, M_2 or M_3 has been set for 335 to 1000 milliseconds. Remote time-slot grouping alarm is released when M_1, M_2 and M_3 has been reset for 20 to 1000 milliseconds.

5.4 *Fault conditions and consequent actions*

5.4.1 *1544 kbit/s fault conditions associated with stream Z*

A summary of the 1544 kbit/s fault conditions associated with the receive side of stream Z and the consequent actions are listed in Table 2/G.724.

The primary multiplex shall detect the following 1544 kbit/s fault conditions associated with stream Z:

i) loss of incoming signals at 1544 kbit/s;

ii) loss of 1544 kbit/s frame alignment;

iii) 1544 kbit/s alarm indication signal (AIS) received;

iv) 1544 kbit/s alarm indication received from the remote end.

5.4.2 *Consequent actions associated with stream Z*

Upon detection of 1544 kbit/s fault conditions in stream Z, appropriate actions should be taken which are in accordance with § 4.2 of Recommendation G.733. In addition, the following consequent actions should be taken as indicated in Table 2/G.724:

i) declare a 1544 kbit/s alarm on the receive side of port Z;

ii) send a 1544 kbit/s alarm indication to the remote end on the send side of port Z in accordance with § 4.2.4 of Recommendation G.733;

iii) declare a remote 1544 kbit/s alarm on the receive side of port Z.

5.4.3 *Fault conditions associated with the signalling grouping channel*

A summary of the signalling grouping channel fault conditions associated with the receive side of stream Z and the consequent actions are listed In Table 3/G.724.

The transcoder shall detect the following signalling grouping channel fault conditions associated with stream Z.

i) loss of signalling grouping channel multiframe alignment on a single time-slot grouping;

ii) remote time-slot grouping alarm indication (M_1) receive from the remote end on a single time-slot grouping;

iii) signalling grouping channel AIS (M_2) receive from the remote end on a single time-slot grouping;

iv) Remote signalling grouping channel AIS (M_3) received from the remote end on a single time-slot grouping.

TABLE 2/G.724

1544 kbit/s fault conditions associated with stream Z and consequent actions

Fault conditions \ Consequent actions	Declare 1544 kbit/s alarm on Z (i)	Send 1544 kbit/s alarme indication to remote end on Z (ii)	Declare remote 1544 kbit/s alarm on Z (iii)
Loss of incoming signal at 1544 kbit/s (i)	Yes	Yes	
Loss of 1544 kbit/s frame alignment (ii)	Yes	Yes	
1544 kbit/s AIS received (iii)	Yes	Yes	
1544 kbit/s alarm indication received from remote end (iv)			Yes

5.4.4 *Consequent actions associated with the signalling grouping channel*

Upon detection of signalling grouping channel fault conditions in stream Z, the following consequent actions shall be taken as indicated in Table 3/G.724:

i) declare a time-slot grouping alarm on the associated time-slot grouping;

ii) send a time-slot grouping alarm indication to the remote end by forcing the M_1 bit within the affected signalling grouping channel to 1;

iii) condition the data in the affected channels on the receive side of streams A to provide a signal that is compatible with downstream equipment;

iv) condition the channel-associated signalling in affected channels on the receive side of stream A to provide a signalling that is compatible with downstream equipment;

v) declare a remote time-slot grouping alarm condition on the associated time-slot grouping to indicate the reception of a remote time-slot grouping alarm indication to the M_1 bit of the affected signalling grouping channel;

vi) declare a signalling grouping channel AIS condition on the associated time-slot grouping to indicate the reception of a signalling grouping channel AIS indication in the M_2 bit of the affected signalling rouping channel;

vii) declare a remote signalling grouping channel AIS condition on the associated time-slot grouping to indicate the reception of a remote signalling grouping channel AIS indication in the M_3 bit of the affected signalling grouping channel.

5.5 *Jitter*

For further study.

TABLE 3/G.724

Signalling grouping channel fault conditions associated with stream Z and consequent actions

Fault conditions \ Consequent actions	Declare time-slot grouping alarm (i)	Send time-slot grouping alarm indication to remote end (ii)	Condition affected channels on A (iii)	Condition signalling in affected channels on A (iv)	Declare remote time-slot grouping alarm (v)	Declare signalling grouping channel AIS (vi)	Declare remote signalling grouping channel AIS (vii)
Loss of signalling grouping channel multiframe alignment (single time-slot grouping) (i)	Yes	Yes	Yes	Yes			
Remote time-slot grouping alarm indication received (single time-slot grouping) (ii)			Yes	Yes	Yes		
Signalling grouping channel AIS received (signle time-slot grouping) (iii)			Yes	Yes		Yes	
Remote signalling grouping channel AIS received (single time-slot grouping) (iv)			Yes	Yes			Yes

SYSTEM ASPECTS FOR THE USE OF THE 7 kHz AUDIO CODEC WITHIN 64 kbit/s

(Melbourne, 1988)

1 General

This Recommendation should be associated with Recommendation G.722 *7 kHz audio coding within 64 kbit/s* and Recommendation H.221 *Frame structure for a 64 kbit/s channel in audiovisual teleservices.*

A number of applications utilizing wideband (7 kHz) speech have been identified including high quality telephony, audio conferencing (with or without various kinds of visual aids), speech channel of visual telephony, audiographic conferencing and so on. More applications will undoubtedly emerge in the future.

To provide these services a scheme is recommended in which the 64 kbit/s channel accommodates speech, and optionally data at several rates, in a number of different modes. Signalling procedures are required to establish a compatible mode upon call setup, to switch between modes during a call, and to allow for call transfer. In the future ISDN, D-channel signalling may be used for some of these procedures. However, before the signalling facilities of the ISDN become available, in channel signalling must be provided.

All audio and audio-visual terminals using G.722 audio coding and/or G.711 speech coding should be compatible to permit connection between any two terminals. This implies that a common mode of operation has to be established for the call. The initial mode might be the only one used during a call or, alternatively, switching to another mode can occur as needed, depending on the capabilities of the teminals. Thus, for these terminals, an in-channel procedure for dynamic mode switching is required even in a ISDN environment.

The following paragraphs develop these considerations and describe recommended in-channel procedures.

2 Transmission modes and terminal types

2.1 *Transmission modes*

The following modes of operation are defined:

Mode 0 – 64 kbit/s narrowband audio according to Recommendation G.711 (A- or μ-law);

Mode 1 – 64 kbit/s 7 kHz audio according to Recommendation G.722;

Mode 2 – 56 kbit/s 7 kHz audio according to Recommendation G.722 + up to 6.4 kbit/s data;

Mode 3 – 48 kbit/s 7 kHz audio according to Recommendation G.722 + up to 14.4 kbit/s data.

For both Modes 2 and 3, an additional 1.6 kbit/s capacity is reserved for service channel framing and mode control.

Additional modes may be defined (see Recommendation H.221) having other speech bit rates, or data bit rates up to a full 64 kbit/s data path.

For analogue telephone terminal it may be assumed that the speech signal is converted to PCM according to Recommendation G.711 at a digital network interface. These terminal are viewed as working in Mode 0, when connected to wideband speech terminal.

2.2 *Terminal types*

Three types of terminals are defined thus far, according to their modes of operations:

Type 0 – A digital telephone set working in Mode 0 only (or an analogue telephone set connected via a PCM interface);

Type 1 – A 7 kHz audio terminal capable of working in Mode 1 or in Mode 0;

Type 2 – A member of a family of 7 kHz audio/data terminals capable of working at least in Modes 0, 1, 2 and 3. Further modes may also be implemented. Dynamic mode switching between different modes must be provided.

In order to establish a mode of operation with the highest possible performance, terminals of Type 1 and Type 2 must be able to identify the terminal type at the far end, and they must indicate their own type to the far end terminal.

2.3 *Establishment of compatible modes of operation*

At the beginning of the communication phase of a call, all terminals start to work in Mode 0. Terminals of Type 1 and Type 2 will then begin an initialization procedure.

This procedure (further described in § 5) consists of:

- the transmission of information concerning the capabilities of the respective terminal for audio coding and/or data transmission;
- the determination of a suitable transmission mode consistent with the known capabilities of both terminals (an example of agreed mode is given in Table 1/G.725); and
- switching to this mode.

The terminals connected to a call may change during the call. This may require reinitialization in order to identify the terminal type and to re-establish the common mode of operation. In particular, this feature is used for Mode 0 forcing, which is necessary in the case of a call transfer (see § 7).

TABLE 1/G.725

Mode of operation upon completion of the initialization procedure

<table>
<tr><td colspan="2" rowspan="2">Agreed mode of operation</td><td colspan="3">Identified terminal type at the far end</td></tr>
<tr><td>Type 2</td><td>Type 1</td><td>Type 0</td></tr>
<tr><td rowspan="2">Type of local terminal</td><td>Type 2</td><td>Mode 2</td><td rowspan="2">Mode 1</td><td rowspan="2">Mode 0</td></tr>
<tr><td>Type 1</td><td></td></tr>
</table>

3 Frame structure

The frame structure described in Recommendation H.221 is used for dynamic mode switching and mode initialization (see the following sections) and more generally to allocate sub-channels in connections of Type 2 terminals.

Recommendation H.221 defines a bit rate allocation signal (BAS) which is used to allocate subchannels and to indicate the audio coding algorithm. Table 2/G.725 gives the coding of the BAS for the attribute 000 (audio coding) as applicable to terminals to Recommendation G.722. Only a BAS beginning with 000 should be taken into account as to the audio coding mode itself. In this respect, a BAS with another attribute does not modify the audio coding mode.

TABLE 2/G.725

BAS code values affecting the audio coding mode

BAS code	Octet format								Audio coding	Mode	Information rates			Framed	Comments
	Bit position										Audio	Application channel	Data channel		
	1	2	3	4	5	6	7	8							
00000100	P	P	P	P	P	P	P	P	G 711-A	0	64	0	0	No	Note 1
00000101	P	P	P	P	P	P	P	P	G 711-μ	0	64	0	0	No	Note 1
00000110	H	H	L	L	L	L	L	L	G 722	1	64	0	0	No	Note 1
00001000	H	H	L	L	L	L	L	S	G 722	2	56	6.4	0	Yes	
00001001	H	H	L	L	L	L	D	S	G 722	3	48	6.4	8	Yes	
00011000	H	H	L	L	L	L	L	S	G 722	2	56	0	6.4	Yes	Note 2
00011001	H	H	L	L	L	L	D	S	G 722	3	48	0	14.4	Yes	Note 2

P PCM
S Service channel
H Higher sub-band
L Lower sub-band
D Data channel

Note 1 – Attribute values 001xx imply switching to an unframed mode. In the receive direction, reverting to a framed mode can only be achieved by recovering frame and multiframe alignment.

Note 2 – The application channel is merged with the data channel to form a single data path.

A second BAS attribute 100 (audio capability) is defined and is intended to be used for signalling terminal capabilties to the distant terminal. When received, this attribute does not affect the current audio coding mode. However, it may lead to the initiation of a specific action to be carried out by the terminal. This feature is utilized in the mode initialization procedure and in the Mode 0 forcing procedure (see § 5). The coding of the BAS for attribute values assigned for audio capability is shown in Table 3/G.725.

TABLE 3/G.725

BAS code values for audio capability

BAS code	Audio coding capability	Comments
10000000	Neutral	No change of audio capability
10000001	Type 0, A-law	
10000010	Type 0, μ-law	
10000011	Type 1	
10000100	Type 2	
10000101	Reserved	
10000110	Reserved	
10000111	Reserved for national use	

The third bit of the H.221 frame alignment signal (FAS) in odd frames, herein called the A-bit, is set to 1 on loss of frame or multiframe alignment, and is set to 0 on acquiring both frame and multiframe alignment. Optionally, the terminal may set the A-bit to 0 on acquiring framing and before acquiring multiframing. A terminal which is receiving a frame signal with the A-bit set to 0 can assume that the distant terminal is able to act upon a change of BAS.

4 Basic sequences for in-channel procedures

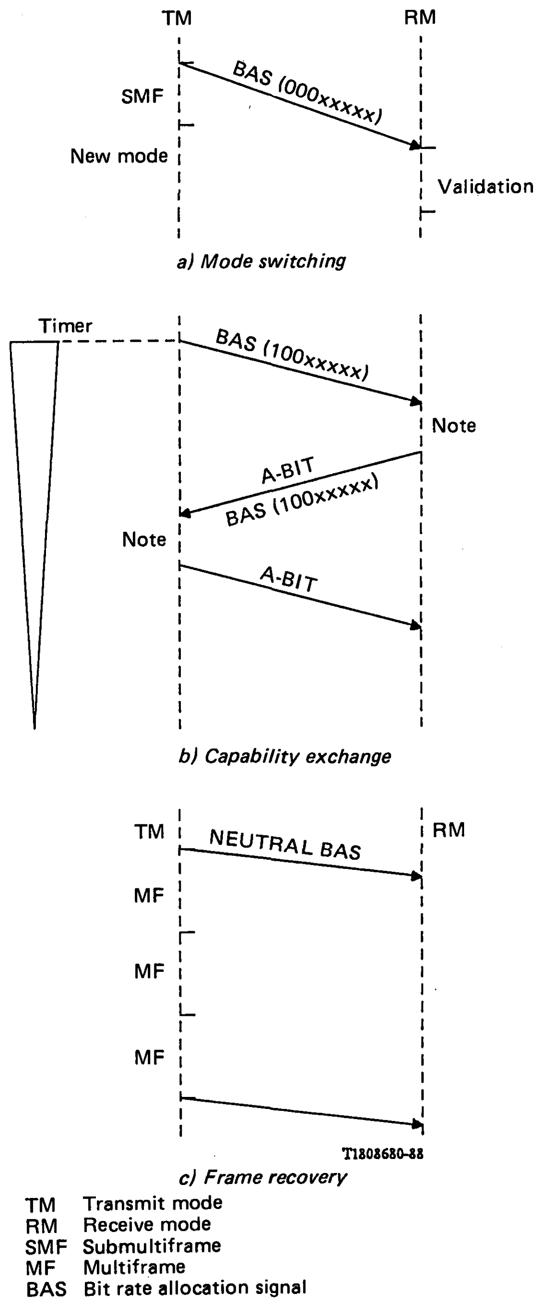
Three signalling sequences are defined in this section. These sequences are used as the building blocks for the procedures defined in §§ 5 and 6. The sequences are described in Figure 1/G.725.

4.1 *Mode switching sequence*

Mode switching is defined in Recommendation H.221 and is done using eight-bit BAS codes, with audio coding attribute (000).

In the present submultiframe the transmitting terminal sends a BAS code to signal the mode of operation in which it will transmit during the next submultiframe.

The receiving terminal decodes and validates the BAS code during the present submultiframe, and switches its receive mode to the signalled mode of operation at the beginning of the next submultiframe. If the receiving terminal does not receive a valid BAS code due to transmission errors, it continues its present mode of operation during the next submultiframe.



Note – Exact timing of the A-bit indication depends on the implementation.

FIGURE 1/G.725

Basic sequences for in-channel procedures

4.2 *Capability exchange sequence*

The capability exchange sequence forces framing in both direction of transmission, and the exchange of terminal type indication using the BAS code with the audio capability attribute (100).

The terminal which initiates the capability exchange sequence sets a times T1 (value: 10 seconds) and transmits in a framed mode with the BAS signal stating its current capability.

When the distant terminal decodes the audio capability BAS code in two consecutive submultiframes, it starts the capability exchange sequence. One of the three cases may occur:

- Within the timer expiration period, multiframe alignment[1] has been achieved, the A-bit has received with a value of 0, and the audio capability BAS code of the distant terminal has been validated in two consecutive submultiframes. In this case the sequence completed successfully.
- The timer has expired without multiframe alignment[1]. In this case, the sequence failed.
- The times has expired with multiframe alignment[1] achieved, but without either the validation of the A-bit as 0 or the receiving of the distant terminal's audio capability BAS code (or both). In this case, the sequence is restarted.

4.3 *Frame recovery sequence*

When a terminal is transmitting in an unframed mode and wishes to institute framing in its transmitting direction, it superimposes the frame structure over the transmitting information using the neutral audio capability BAS code. This audio capability BAS code is transmitting for at least 3 multiframes (48 frames).

5 **Initialization and Mode 0 forcing**

Recommendation G.722 terminals will be connected to digital networks where other kinds of terminals will also be connected, e.g. Type 0 terminals, data terminals, telematic terminals, servers, etc. When compatibility between the different services involving those terminals is required, initialization procedure is necessary. When automatic compatibility is required, a procedure based on the sequences defined in § 4 is used.

For call transfer or mode mismatch recovery, it is necessary for terminals to operate in the common Mode 0 and thus a Mode 0 forcing procedure is required, again based on the sequences defined in § 4.

At the commencement of the call there is a need for an initialization procedure to ensure that the two connected terminals can operate in the most suitable common mode.

5.1 *Mode initialization procedure*

The mode initialization procedure ensures that both terminal have been informed of the capabilities of the other terminal, and switched to the highest common audio mode in both directions of transmission. In case of two Type 2 terminals, both directions of transmission will be in either Mode 1, Mode 2, or Mode 3, but symmetry is not required. The procedure can be initiated by both terminals independently. However, even if it is initiated by only one terminal, it will still achieve the same results as a procedure that was initiated independently, due to the symmetric operation of the capability exchange sequence.

At the beginning of the mode initialization procedure, the terminal starts transmitting in Mode 0, while initiating the capability exchange sequence (§ 4.2). The receive part is in frame search and the receive audio is in Mode 0. If the capability exchange sequence has terminated successfully, the mode switching sequence (§ 4.1) is executed in order to switch to a common working mode. The initialization procedure is completed when both terminals have switched to their common working mode(s), according to their capabilities.

If the capability exchange sequence failed, i.e. no framing was detected on the incoming path within the timer expiration period, the terminals shall continue transmitting in Mode 0, but without framing.

5.2 *Mode 0 forcing procedure*

Where it is necessary to ensure that both terminals are operating in Mode 0 (for instance before call transfer), this procedure is used.

[1] Optionally, frame alignment may be sufficient.

For the forcing terminal, BAS 10000010 (Type 0 terminal) is sent to the terminal which is to be forced to Mode 0, using the capability exchange sequence (see Figure 1b/G.725). When this is complete, both terminals execute the mode switching sequence (see Figure 1a/G.725) with the BAS value of 00000100 or 0000101 to switch transmission to Mode 0, since PCM is now the only common mode of operation.

At the completion of the mode-switching sequence, both terminals are operating in Mode 0. Changes of network configuration can now be achieved (see § 7).

5.3 *Mode mismatch recovery procedure*

In the case where mode mismatch between Mode 0 and Mode 1 has been detected in the receiver (e.g. by examining the energy level or by monitoring the statistics of the decoded output), the Mode 0 forcing procedure may be used to establish a common working mode. The audio output has to be muted starting from the detection of the mismatch until the establishment of the common Mode 0. Following this procedure, reinitialization can be achieved by using the mode initialization procedure.

5.4 *Recovery from unexpected loss of frame alignment*

If a terminal unexpected loses frame alignment on its receive path, a timer T2 is set (value: 0.1 seconds). During this time the status of the framing in the receive direction is monitored:

- if framing is recovery before the time expires, the normal operation is continued;
- if framing is not recovered before the timer expires, the terminal goes to the Mode 0 forcing procedures. The audio output should be muted starting from the expiry of the timer until the Mode 0 forcing procedure is completed. Following this procedure, reinitialization can be achieved by using the mode initialization procedure.

6 Dynamic mode switching procedure for Type 2 terminals

The dynamic mode switching procedure makes use of the frame structure specified in Recommendation H.221 as described in § 3, and of the sequences defined in § 4.

When the terminal is receiving in a framed mode, and is capable of decoding the A-bit, mode switching should be delayed if the A-bit is set to 1; eventually the mode mismatch recovery procedure as described in § 5.3 might be used.

6.1 *Dynamic mode switching from a framed mode to another framed mode*

The mode switching sequence (see Figure 1a/G.725) is used.

At the transmitting terminal, of a BAS is transmitted to signal a new audio mode, the audio encoder must operate in the appropriate audio encoding mode (Recommendation G.711, A- or μ-law; Recommendation G.722, mode 1) from the first octet of the next submultiframe.

Similarly, at the receiving terminal, if the received BAS signals a new audio-mode, the audio decoder must operate in the appropriate audio decoding mode (Recommendation G.711, A- or μ-law; Recommendation G.722, Modes 1, 2 or 3; muted audio) from the first octet of the next submultiframe.

6.2 *Dynamic mode switching from a framed mode to an unframed mode*

As in § 6.1, the mode switching sequence is used.

However, as the BAS for signalling an unframed mode is transmitted for a single submultiframe, a mode mismatch may occur in severe error conditions. Optionally, two methods may be alternatively or simultaneously used to improve the reliability of the switching:

i) If the distant terminal is transmitting in an unframed mode, the capability exchange sequence (see Figure 1b/G.725) is used first in order to be able to decode the A-bit in the receive direction and to be sure that multiframing is aligned in the distant terminal. The mode switching sequence may then be transmitted.

ii) The new BAS value in the mode switching sequence may be repeated several times. This will cause a temporary mismatch on the least significant bit.

6.3 *Dynamic mode switching from an unframed mode to a framed mode*

The frame recovery sequence (see Figure 1c/G.725) and the mode switching sequence are sequentially transmitted.

Alternatively, another method may be used. The capability exchange sequence is used, followed by the mode switching sequence. This requires a bi-direction link and provides a more reliable procedure. However it causes an unneeded mode change in the distant terminal.

6.4 *Dynamic mode switching from an unframed mode to another unframed mode*

The frame recovery sequence and mode switching sequence are sequentially transmitted.

Alternatively, the alternate methods mentioned in § 6.3 may be used.

Additionally, the option of § 6.2 may be applied.

7 **Network considerations: call connection, disconnection, and call transfer**

7.1 *Call connection*

It is assumed that the terminals for switched network operation will have a signalling arrangement for originating calls over the network

In the case that the network provides an indication that the connection is established, the originating terminal will set its transmit and receive audio modes to Mode 0, and begin the mode initialization procedure following the connection establishment indication. Where the network does not provide an indication of connection establishment, the originating terminal will begin the mode initialization procedure of § 5.1 immediately.

Upon answering a call, the terminal will begin the mode initialization procedure.

Terminals for use on leased circuits may have a means for sending the alerting signal to the distant terminal and for answering the alerting signal. In this case, the sending of the alerting signal is equivalent to dialling and the foregoing procedures apply.

Whenever a terminal is manually reset, or recovers from a fault condition, the terminal will begin the Mode 0 forcing procedure of § 5.2. Then the terminal will begin the mode initialization procedure after 2 seconds.

7.2 *Terminal disconnection*

When a terminal disconnects from a call, the terminal must first initiate the Mode 0 forcing procedure, await completion of the procedure, and then the actual disconnection may occur.

7.3 *Call transfer*

As a consequent of the above, the terminal which continues to participate in a transferred call will be receiving in a Mode 0-forced state, and therefore will be transmitting its audio capability BAS in framed Mode 0. When the transferred-to terminal answers, mode re-initialization will occur in both directions.

7.4 *Conferencing*

Conferencing will be accomplished by means of a multipoint conference unit (MCU). Each terminal will be connected to a port of the MCU by a switched connection or a leased circuit. Each connection between the terminal and the MCU is considered to be a point-to-point connection as far as call connection, terminal disconnection, and call transfer procedures are concerned.

7.5 *PCM format conversion*

In the above procedures, no automatic method for establishing A-law or μ-law compatible PCM operation is defined. Instead, Type 1 and Type 2 terminals should be capable of working in both A-law and μ-law PCM.

The originating Type 1 or Type 2 terminals is responsible for selecting the PCM coding law. This is important, especially in cases of connection to a Type 0 terminal or interworking to the analog network, if no format conversion is provided by the network because a bit transparent link was requested by the originating terminal when trying to place a 7 kHz audio call.

The following guidelines should be used in making the selection:

1) If there is an indication regarding the default PCM format in the zone of the distant terminal before the call is established (e.g. from manual selection by the user, or from analysis of dialed digits, or from the network), then the PCM format of the distant terminal should be used whenever the call is in PCM.

2) If there is no indication before the call is established, the terminal should default to the PCM coding law of its own zone, while monitoring the statistics of the incoming signal (see Appendix I). If the monitoring suggests that the other coding law should be used, the terminal should switch to the other PCM mode. If the capability exchange sequence in the mode initialization procedure is completed successfully (i.e. the distant terminal is a Type 1 or Type 2 terminal), then the terminal may use any PCM law. Otherwise, the coding law determined by the statistical monitoring should prevail throughout the call.

In a teleconference call, the network bridge is responsible for providing compatible connections.

APPENDIX I

(to Recommendation G.725)

An algorithm to determine whether an incoming bit stream was encoded by μ-law or A-law PCM

This Appendix gives information concerning a method to determine the PCM coding law from the observation of the incoming bit streams. It should be used in the absence of other indications regarding the PCM coding law.

I.1 *Basic determination algorithm*

The following algorithm determines whether an incoming bit stream was encoded by μ-law or A-law PCM. The algorithm comprises two stages:

i) data accumulation;

ii) decision.

A decision can be made after data has been accumulated for 10 ms or longer. Decisions can be produced several times with an increasing amount of accumulated data. The period in which data is accumulated is called the test period.

Data accumulation

For each incoming sample, observe the combination in bits 2, 3 and 4. (Bit 1 is defined as the most significant bit. Bits 2, 3 and 4 are the segment number, as defined in Recommendation G.711.) Count the number of occurrences of each segment number throughtout the test period. That is, obtain 8 numbers corresponding to the numbers of occurrences of each of the possible combinations.

Decision

1) Place the counters as illustrated in the μ-law column of Figure I-1/G.725. If there is a counter that contains a number greater than zero above a counter that contains zero, then the μ-law hypothesis is "improbable".

2) Place the counters as illustrated in the A-law column of Figure I-1/G.725 (the arrangement in the figure includes even-bit inversion, specified in Recommendation G.711). If there is a counter that contains a number greater than zero above a counter that contains zero, then the A-law hypothesis is "improbable".

3) If only one coding law hypothesis is probable, decide accordingly.

4) If neither coding law hypothesis is probable, the test period was too short. Obtain more data, then repeat the decision process.

5) If both coding laws are probable, then select a counter to represent each coding law according to the following:

- If all 8 counters contain numbers greater than 0, then counter 000 represents μ-law, and counter 010 represents A-law.
- If 4 counters contain numbers greater than 0, then counter 100 represents μ-law, and counter 110 represents A-law.

Compare the numbers in the two representative counters. Decide on the coding law represented by the counter containing the smaller number.

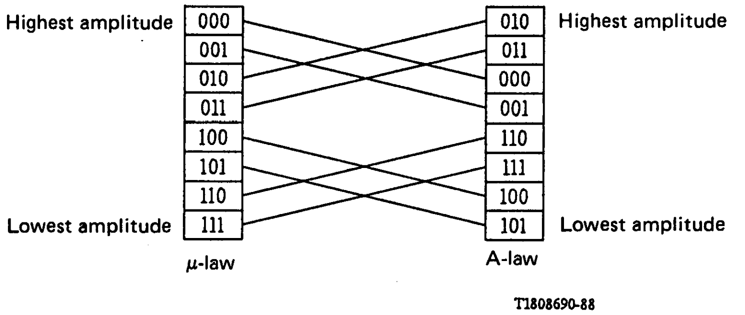


FIGURE I-1/G.725

Order of segments according to amplitude, μ-law and A-law PCM

I.2 *Possible extensions and refinements*

The list below specifies some possible extensions to the algorithm. These extensions may be used to produce a result based on additional data. The exact way one might use this data is beyond the scope of this appendix.

i) It is possible to obtain separate count for positive and negative samples, i.e. take into consideration bit 1 (sign bit) of the samples.

ii) It is possible to define a threshold other than zero for consideration of a non-zero counter (i.e. consider all counters that contain numbers less than the threshold as if they contained zero). This extension may be useful in preventing spurious bit errors from affecting the decision.

iii) The decision criterion in step 5 of § I.1 is less robust than that of step 3. The following enhancements to steps 5 may be considered:

- In order to avoid an erroneous decision because of close valued numbers when the step 5 criterion is employed, it is possible to require that the difference between numbers in the two representative counters exceed a certain threshold. Alternatively (taking the above suggestion to the extreme), it is possible not to decide at all according to the step 5 criterion, and to discard the data if both coding laws produce allowed distributions.
- It is possible to represent each coding law with two counters, rather than one. In case of 8 non-zero counters, counter 001 (for A-law), in addition to the comparison given in the algorithm. In case of 4 non-zero counters, counter 101 (for μ-law) is compared against counter 111 (for A-law), in addition to the comparison given in the algorithm. It is also possible to use the sum of the two representative counters of each coding law in a comparison.

I.3 *Proposed use of the algorithm*

1) The algorithm should be used only by the originating terminal.
2) For the first 10 ms, use the default coding law (according to the zone), while accumulating data.
3) After 10 ms, use the accumulated data to make the first decision.
4) If the decision requires a mode switch, then switch the transmit and receive side to the propor law, If the capability exchange sequence is operation when the switch is required, switch the transmission without using the mode switching procedure. Otherwise, use the mode switching procedure.
5) Monitor the decision until framing is recovered, or for 200 ms after the beginning of reception of information from the distant terminal (in cases where ther is no indication to that effect, start the 200 ms timer only after there is sufficient confidence that the arriving signal was originating by the distant terminal). If framing is not established by the expiration of the 200 ms timer, continue to use the coding law determined by the algorithm.

7.3 Principal characteristics of primary multiplex equipment

Recommendation G.731

PRIMARY PCM MULTIPLEX EQUIPMENT FOR VOICE FREQUENCIES

(Geneva, 1972; further amended)

The CCITT,

considering

that pulse code modulation (PCM) multiplex equipments are already used in various countries, in particular to provide a large number of short-distance telephone circuits on certain pairs in existing cables, and in order to minimize the number of different PCM multiplex equipments providing circuits which may be used in international connections,

recommends

that Administrations concerned should make their choice between the two primary PCM multiplex equipments described in Recommendations G.732 and G.733.

Recommendation G.732

CHARACTERISTICS OF PRIMARY PCM MULTIPLEX EQUIPMENT OPERATING AT 2048 kbit/s

(Geneva, 1972; further amended)

1 General characteristics

1.1 *Fundamental characteristics*

The encoding law used is the A-law as specified in Recommendation G.711. The sampling rate, load capacity and the code are also specified in that Recommendation.

The number of quantized values is 256.

Note – The inversion of bits 2, 4, 6, and 8 is covered by the encoding law and is applicable only to voice-channel time slots.

1.2 *Bit rate*

The nominal bit rate is 2048 kbit/s. The tolerance on this rate is ± 50 parts per million (ppm).

1.3 *Timing signal*

It should be possible to derive the transmitting timing signal of a PCM multiplex equipment from an internal source, from the incoming digital signal and also from an external source.

Note – Further study is required on the effect of jitter of the incoming signal on the timing signal, and on the measures to be taken in case of loss of the incoming signal or the external source.

2 Frame structure

Refer to §§ 3.3.1 and 3.3.2 of Recommendation G.704 for frame structure and use of derived channel time slots.

Note – If channel time slot 16 which is assigned to signalling as covered in § 5 below is not needed for signalling it may be used for purposes other than a voice channel encoded within the PCM multiplex equipment.

3 Loss and recovery of frame alignment

The strategy for the loss and recovery of frame alignment should be according to Recommendation G.706, § 4.1.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The PCM multiplex equipment should detect the following fault conditions:

4.1.1 Failure of power supply.

4.1.2 Failure of codec (except when using single-channel codecs).

As a minimum requirement this fault condition should be recognized when, for at least one signal level in the range −21 to −6 dBm0, the signal-to-quantizing noise ratio performance of the local codec is 18 dB or more below the level recommended in Recommendation G.712.

4.1.3 Loss of incoming signal at the 64 kbit/s input port (time slot 16).

Note 1 – The detection of this fault condition is not mandatory when channel associated signalling is used and the signalling multiplex is situated within a few metres of the PCM multiplex equipment.

Note 2 – The detection of this fault condition is not mandatory when contradirectional interfaces are used.

4.1.4 Loss of the incoming signal at 2048 kbit/s.

Note – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

4.1.5 Loss of frame alignment.

4.1.6 Excessive bit error ratio detected by monitoring the frame alignment signal.

4.1.6.1 With a random bit error ratio of $\leq 10^{-4}$, the probabiliy of activating the indication of fault condition within a few seconds should be less than 10^{-6}.

With a random bit error ratio of $\geq 10^{-3}$, the probability of activating the indication of fault condition within a few seconds should be higher than 0.95.

4.1.6.2 With a random bit error ratio of $\geqslant 10^{-3}$, the probability of deactivating the indication of fault condition within a few seconds should be almost 0.

With a random bit error ratio of $\leqslant 10^{-4}$, the probability of deactivating the indication of fault condition within a few seconds should be higher than 0.95.

Note – The activating and the deactivating period specified as "a few seconds" is intended to be in the order of 4 to 5 seconds.

4.1.7 Alarm indication received from the remote PCM multiplex equipment (see § 4.2.3 below).

4.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 1/G.732. The consequent actions are as follows:

4.2.1 Service alarm indication generated to signify that the service provided by the PCM multiplex is no longer available. This indication should be forwarded at least to the switching and/or signalling multiplex equipment depending upon the arrangements provided. The indication should be given as soon as possible and not later than 2 ms after detection of the relevant fault condition.

This specification, taking into account the specification given in § 3 above, is equivalent to recommending that the average time to detect a loss of frame alignment and to give the relevant indication should not be greater than 3 ms.

When using common-channel signalling, the indication should be forwarded to the switching equipment by means of a separate interface on the PCM multiplex equipment.

4.2.2 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the Alarm Indication Signal (AIS) (see General Notes below to § 4.2) is detected, the prompt maintenance alarm indication associated with loss of frame alignment (see § 4.1.5 above) and excessive error ratio (see § 4.1.6 above) should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 1/G.732 with the two fault conditions.

Note – The location and provision of any visual and/or audible alarm activated by the alarm indications given in §§ 4.2.1 and 4.2.2 above, is left to the discretion of each Administration.

4.2.3 Alarm indication to the remote end, transmitted by changing bit 3 of channel time-slot 0 from the state 0 to the state 1 in those frames not containing the frame alignment signal. This should be effected as soon as possible.

4.2.4 Transmission suppressed at the analogue outputs.

4.2.5 AIS applied to time-slot 16 64 kbit/s output (see General Notes below to § 4.2). This action should be taken as soon as possible and not later than 2 ms after the detection of the fault condition.

4.2.6 AIS applied to time slot 16 of the output 2048 kbit/s composite signal (if supervision of the incoming 64 kbit/s signal is provided).

General Notes to § 4.2

Note 1 – Yhe equivalent binary content of the AIS is a continuous stream of binary 1s. The strategy for detecting the presence of the AIS should be such that the AIS is detectable, even in the presence of an error ratio of $1 \cdot 10^{-3}$. However, a signal with all bits except the frame alignment in the 1 state, should not be mistaken as an AIS.

Note 2 – All timing requirements quoted apply equally to restoration, subsequent to the fault condition clearing.

5 Signalling

5.1 *Signalling arrangement*

Refer to § 3.3.3 of Recommendation G.704. Channel time slot 16 may be used to provide an interface at 64 kbit/s which shall be suitable for use with either common channel or channel associated signalling.

TABLE 1/G.732

Fault conditions and consequent actions for the PCM multiplex equipment

Equipment part	Fault conditions (see § 4.1)	Consequent actions (see § 4.2)					
		Service alarm indication generated	Prompt maitenance alarm indication generated	Alarm indication to the remote end transmitted	Transmission suppressed at the analogue outputs	AIS applied to 64 kbit/s output (time slot 16)	AIS applied to time slot 16 of the 2048 kbit/s composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes	Yes (if practicable)	Yes (if practicable)	Yes (if practicable)	Yes (if practicable)
	Failure of codec	Yes	Yes	Yes	Yes		
Multiplexer only	Loss of incoming signal at 64 kbit/s input time slot 16 (see Notes under § 4.1.3)		Yes				Yes
Demultiplexer only	Loss of incoming signal at 2048 kbit/s	Yes	Yes	Yes	Yes	Yes	
	Loss of trame alignment	Yes	Yes	Yes	Yes	Yes	
	Error ratio 10^{-3} on the frame alignment signal	Yes	Yes	Yes	Yes	Yes	
	Alarm indication received from the remote end (bit 3 of time slot 0)	Yes					

Note – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

5.2 *Loss and recovery of multiframe alignment in case of channel associated signalling*

Multiframe alignment should be assumed to have been lost when two consecutive multiframe alignment signals have been received with an error.

Multiframe alignment should be assumed to have been recovered as soon as the first correct multiframe alignment signal is detected.

Note – To avoid a condition of spurious multiframe alignment, the following procedure may be used in addition to the above:

- Multiframe alignment should be assumed to have been lost when, for a period of one or two multiframes, all the bits in time slot 16 are in state 0.
- Multiframe alignment should be assumed to have been recovered only when at least one bit in state 1 is present in the time slot 16 preceding the multiframe alignment signal first detected.

5.3 *Fault conditions and consequent actions in case of channel associated signalling*

5.3.1 *Fault conditions*

The signalling multiplex equipment should detect the following fault conditions:

5.3.1.1 Failure of power supply.

5.3.1.2 Loss of 64 kbit/s incoming signal at the input of the signalling demultiplexer.

Note 1 – The detection of this fault condition is not mandatory when the signalling multiplex equipment is situated within a few metres of the PCM multiplex equipment or when this fault condition results in an indication of loss of multiframe alignment.

Note 2 – Where separate circuits are used for the digital signal and the timing signal then loss of either or both should constitute loss of the incoming signal.

5.3.1.3 Loss of multiframe alignment.

5.3.1.4 Alarm indication received from the remote signalling multiplex equipment (see § 5.3.2.3 below).

5.3.1.5 Receipt of the service alarm indication from the PCM multiplex equipment (see § 4.2.1 above).

5.3.2 *Consequent actions*

Further to the detection of a fault condition appropriate actions should be taken as specified in Table 2/G.732. The consequent actions are as follows:

5.3.2.1 Service alarm indication to be forwarded to the switching equipment depending upon the switching and signalling arrangements provided.

5.3.2.2 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenace attention is required locally. If provision is made for detecting the AIS, then on the reception of the AIS, the prompt maintenance alarm indication should be inhibited in the case of loss of multiframe (see § 5.3.1.3 above).

Note – The location and provision of any visual and or audible alarms activated by the alarm indications given in §§ 5.3.2.1 and 5.3.2.2 above is left to the discretion of each Administration.

5.3.2.3 Alarm indication to the remote signalling multiplex equipment, generated by changing from the state 0 to the state 1 bit 6 of channel time slot 16 of frame 0 of the multiframe (see Table 7/G.704); this should be effected as soon as possible.

5.3.2.4 Application of the condition corresponding to state 1 on the line to all receive signalling channels. This condition should be forwarded as soon as possible and not later than 3 ms after the detection of the fault condition.

Note – All timing requirements quoted apply equally to restoration, subsequent to the fault condition clearing.

6 Interfaces

The analogue interfaces should be in accordance with Recommendations G.712, G.713, G.714 and G.715. The digital interfaces at 2048 kbit/s should be in accordance with Recommendation G.703. The digital interfaces at 64 kbit/s should be of either the codirectional or the contradirectional type specified in Recommendation G.703. The specifications for 64 kbit/s interfaces are not mandatory for channel associated signalling. The interface for external synchronization of the transmitting timing signal should be in accordance with Recommendation G.703.

TABLE 2/G.732

Fault conditions and consequent actions for channel-associated signalling multiplex equipment

Equipment part	Fault conditions (see § 5.3.1)	Consequent actions (see § 5.3.2)			
		Service alarm indication generated	Prompt maintenance alarm indication generated	Alarm indication to the remote end transmitted	Application of state, equivalent to state 1, on line to all receive signalling channels
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes	Yes (if practicable)	Yes (if practicable)
Demultiplexer only	Loss of incoming signal	Yes	Yes	Yes	Yes
	Loss of multiframe alignment	Yes	Yes	Yes	Yes
	Alarm indication received from the remote signalling multiplex equipment	Yes			Yes
	Receipt of the service alarm indication from PCM mux	Yes			Yes

Note – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

7 Jitter

7.1 *Jitter at 2048 kbit/s output*

In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 100$ kHz.

7.2 *Jitter at 64 kbit/s output (for interfaces according to Rec. G.703)*

7.2.1 In the case where the incoming 2048 kbit/s signal has no jitter, the peak-to-peak jitter at the 64 kbit/s output should not exceed 0.025 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 10$ kHz. The equivalent binary content of the test signal applied to the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151.

Note – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

7.2.2 The jitter transfer function between the 2048 kbit/s input and the 64 kbit/s output should not exceed −29.6 dB when measured over the frequency range f_0 to 10 kHz. The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

Note 3 – The jitter reduction of 1/32 due to demultiplexing is equivalent to −30.1 dB.

Recommendation G.733

CHARACTERISTICS OF PRIMARY PCM MULTIPLEX EQUIPMENT OPERATING AT 1544 kbit/s

(Geneva, 1972; further amended)

1 General characteristics

1.1 *Fundamental characteristics*

The encoding law used is the μ-law as specified in Recommendation G.711. The sampling rate, load capacity and the code are also specified in that Recommendation.

The number of quantized values is 255. Two character signals are reserved for zero value (11111111 and 01111111).

In some networks the all-0 character signal (00000000) is eliminated to avoid loss of timing information to the digital line, resulting in 254 quantized values.

1.2 *Bit rate*

The nominal bit rate is 1544 kbit/s. The tolerance on this rate is ± 50 parts per million (ppm).

1.3 *Timing signal*

It should be possible to derive the transmitting timing signal of a PCM multiplex equipment from an internal source, from the incoming digital signal and also from an external source.

2 Frame structure

Refer to §§ 3.1.1 and 3.1.2 of Recommendation G.704 for frame structure and use of derived channel time slots.

3 Loss and recovery of frame alignment

The strategy for the loss and recovery of frame alignment should be according to Recommendation G.706, § 2.1.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The PCM multiplex equipment should detect the following conditions:

4.1.1 Failure of power supply.

4.1.2 Loss of incoming signals at 1544 kbit/s.

4.1.3 Loss of frame alignment.

4.1.4 Alarm indication received from the remote PCM multiplex equipment.

4.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 1/G.733. The consequent actions are as follows:

4.2.1 A service alarm indication should be generated to signify that the service provided by the PCM multiplex is no longer available. This indication should be forwarded to the switching and/or signalling equipment depending upon the arrangement provided.

4.2.2 The service alarm described in § 4.2.1 above should be used to automatically remove the associated circuits from service and to restore them to service when frame alignment has been recovered.

Note – The removal of the associated circuits described in § 4.2.2 above should be done in such a way that the circuits are not needlessly removed in the case of a brief isolated loss of frame alignment but are removed in the case of a permanent or intermittent loss of frame alignment.

It is also important to minimize the impact of signalling errors which may occur during periods of loss of frame alignment. These functions should be provided in the PCM multiplex equipment or in the switching/signalling equipment.

4.2.3 A prompt maintenance alarm indication should be generated to signify that performance is below acceptable standards and maintenance attention is required locally.

4.2.4 An alarm indication to the remote end should be generated by either forcing bit 2 in every channel time slot to the value 0 or by modifying the *S*-bit as described in § 3.1.3.2.2 of Recommendation G.704 for the 12 frame multiframe or by sending a frame alignment alarm sequence (111111100000000) as described in § 3.1.1.3 (A)-(3) of Recommendation G.704 for the 24-frame multiframe.

4.2.5 Transmission should be suppressed at the analogue outputs.

4.2.6 *Rapid indication of loss of frame alignment*

An indication should be given to the Signalling System No. 6 equipment (digital version) when the PCM multiplex equipment (local end only) detects a loss of frame alignment. The average time to detect and give an indication of random bits in the frame alignment signal bit positions should not be greater than 3 ms. This indication will serve the same function as that provided by the data carrier failure alarm in the analogue version (see Recommendation Q.275 [1]).

5 Signalling

5.1 *Signalling arrangement*

Refer to § 3.1.3 of Recommendation G.704.

5.2 *Loss of multiframe alignment in case of channel associated signalling on 12 frame multiframe*

Loss of multiframe alignment is assumed to have taken place when loss of frame alignment occurs.

5.3 *Minimization of quantizing distortion in case of channel associated signalling*

In the signalling frame only seven bits are available for encoding of voice frequencies. In order to minimize the quantizing distortion, the decoder output values are shifted slightly. All even numbered decoder output values y_n, are changed to be equal to the next higher decision value, i.e. x_{n+1}. All odd numbered decoder output values y_{n+1} are changed to be equal to the same numbered decision value, i.e. x_{n+1}, as shown on Figure 1/G.733.

When suppression of the all 0 character signal is required, the value of the seventh bit is forced to be 1 when all the other bits of the character signal have the value 0.

TABLE 1/G.733

Fault conditions and consequent actions for the PCM multiplex equipment

Equipment part	Fault conditions	Consequent actions			
		Service alarm indication generated	Prompt maintenance alarm indication	Alarm indication to the remote end generated	Transmission suppressed at the analogue outputs
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes	Yes (if practicable)	Optional
Demultiplexer only	Loss of incoming signals at 1544 kbit/s	Yes	Yes	Yes	Yes
	Loss of frame alignment	Yes	Yes	Yes	Yes
	Alarme indication received from the remote end	Optional	Yes		Optional

Note 1 – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 2 – Indications of additional fault conditions, such as codec failure and excessive bit errors, are left to the discretion of individual Administrations.

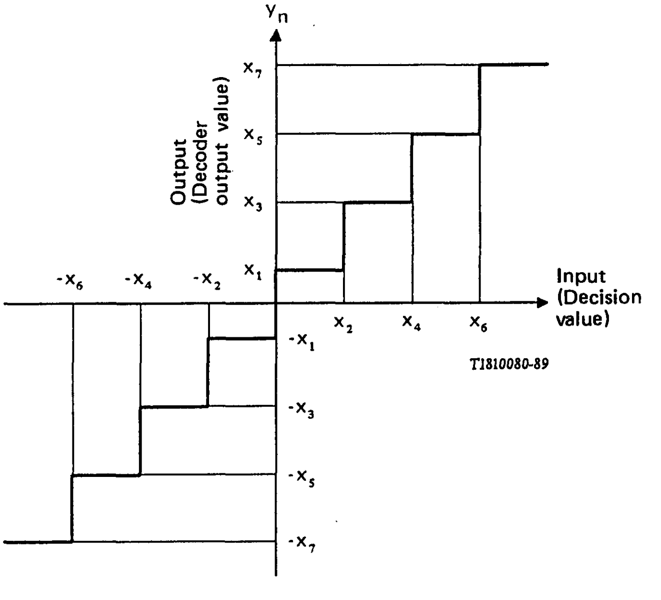


FIGURE 1/G.733

Seven-bit codec transfer characteristic

6 Interfaces

Analogue: Refer to Recommendations G.712, G.713 and G.714.

Digital: Refer to Recommendation G.703.

Reference

[1] CCITT Recommendation *Data channel failure detection*, Vol. VI, Rec. Q.275.

Recommendation G.734

CHARACTERISTICS OF SYNCHRONOUS DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 1544 kbit/s

(former Recommendation G.736 of Volume III of the Yellow Book)

1 General characteristics

This Recommendation defines the characteristics of a synchronous multiplex equipment currently used for applications in dedicated data networks, to combine up to 23 tributary channels at 64 kbit/s in a 1544 kbit/s digital stream.

Note – For applications within an ISDN, it is expected that a 24-channel multiplex will be used that has a frame structure conforming to Recommendation G.733.

1.1 *Bit rate*

The nominal bit rate is 1544 kbit/s.

Note – The tolerance on this rate should be studied and specified.

1.2 *Timing signals*

It should be possible to derive the multiplexer timing signals from the composite clock signal of a centralized clock source as specified in Recommendation G.703, and from the 1544 kbit/s incoming digital stream.

Note – The desirability of also providing a 1544 kHz transmitting timing signal from a centralized clock source should be further studied.

2 Frame structure

2.1 *Number of bits per channel time slot*

There are eight bits per channel time slot, numbered from one to eight.

2.2 *Number of channel time slots per frame*

There are 24 time slots per frame, numbered from 1 to 24. Successive bits for bytes 1 to 24 should be consecutively numbered from 2 to 193. The first bit should be reserved for optional use. The frame repetition rate is 8000 Hz.

2.3 *Channel time slot assignment*

2.3.1 Channel time slots 1 to 23 are assigned to tributaries.

2.3.2 Channel time slot 24 is assigned to frame alignment and service digits. Two alternative methods, as given in Tables 1/G.734 and 2/G.734 for allocation of these signals and associated frame alignment strategy are recommended.

TABLE 1/G.734

Allocation of time slot 24, Method 1

Bit number of time slot 24							
1	2	3	4	5	6	7	8
Frame alignment signal					Service digits		
1	0	1	1	1			0

Note – Loss of frame alignment should be assumed to have taken place when more than three of twelve successive frames have an error in the frame alignment signal and/or in bit 1 of the 193-bit frame. Frame alignement should be assumed to have been recovered when four consecutive correct frame alignment signals have been received.

TABLE 2/G.734

Allocation of time slot 24, Method 2

Frame number	Bit number of time slot 24							
	1	2	3	4	5	6	7	8
1	Service digits			Frame alignment signal				
				0	0	1	0	1
2				1	1	0	1	0

Note – Loss of frame alignment should be assumed to have taken place when seven consecutive pairs of the frame alignment signal (00101, 11010) have been incorrectly received in their predicted positions. Frame alignment should be assumed to have been recovered when two consecutive correct pairs of frame alignment signals have been received.

2.4 *Service digits*

The use of service digits in channel time slot 24 is under study.

Note – The first bit could be considered for framing algorithms.

3 Fault conditions and consequent action

3.1 *Fault conditions*

The digital multiplex equipment should detect the following fault conditions:

- failure of power supply,
- loss of the incoming signal at 1544 kbit/s,
- loss of frame alignment,
- loss of timing signals supplied from the centralized clock,
- alarm indication received from the remote digital multiplex equipment.

Some of the above fault conditions may optionally be detected by auxiliary equipment normally used in association with the digital multiplex equipment.

3.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 3/G.734.

TABLE 3/G.734

Fault conditions and consequent actions for the digital multiplex equipment

Equipment part	Fault conditions	Consequent action (see Notes 1 and 2)		
		Prompt maintenance alarm indication generated	Alarm indication to the remote end transmitted (see Note 3)	Multiplex out-of-sync signal applied to 64 kbit/s output (see Note 4)
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes (if practicable)	Yes (if practicable)
Demultiplexer only	Loss of incoming signal at 1544 kbit/s	Yes	Yes	Yes
	Loss of frame alignment	Yes	Yes	Yes
	Alarm indication receive from the remote end	Yes		

Note 1 – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 2 – These consequent actions may optionally be taken by auxiliary equipment normally used in conjunction with the digital multiplex equipment.

Note 3 – The alarm indication to the remote end may be generated by changing a service bit of time slot 24 from the state 1 to the state 0, if possible.

Note 4 – The binary content of the multiplex out-of-sync signal is under study. One Administration uses 00011010.

4 Multiplexing method

Cyclic byte interleaving in the tributary numbering order should be used. The digital multiplex equipment should translate any incoming byte that contains only 0s into the zero byte suppression code.

Note 1 – The content of the zero byte suppression code is under study.

Note 2 – Further study is needed for the case when the zero suppression code must be extracted.

5 Input jitter and wander

The amount of jitter and wander that should be tolerated at the input of the demultiplexer should be according to Recommendation G.824, § 3.1.1.

6 Digital interface

The digital interface at 64 kbit/s and 1544 kbit/s should be in accordance with Recommendation G.703.

Recommendation G.735

CHARACTERISTICS OF PRIMARY PCM MULTIPLEX EQUIPMENT OPERATING AT 2048 kbit/s AND OFFERING SYNCHRONOUS DIGITAL ACCESS AT 384 kbit/s AND/OR 64 kbit/s

(former Recommendation G.737 of Volume III of the Yellow Book)

This Recommendation gives the characteristics of a PCM multiplex equipment operating at 2048 kbit/s and providing one or several of the following internal digital access options:

– bidirectional synchronous 64 kbit/s channels (see Figure 1a/G.735);

– unidirectional synchronous 384 kbit/s channels (see Figure 1b/G.735).

The 384 kbit/s channel is based on the allocation of 6 × 64 kbit/s time slots, e.g. for setting up sound-programme circuits according to Recommendations J.41 and J.42.

Because these circuits are specified as unidirectional, the equipment for insertion/extraction has to be separated as shown in Figure 1b/G.735.

1 General characteristics

1.1 *Fundamental characteristics for voice channel encoding*

The encoding law used is the A-law as specified in Recommendation G.711. The sampling rate, load capacity and the code are also specified in that Recommendation.

The number of quantized values is 256.

Note – The inversion of bits 2, 4, 6 and 8 is covered by the encoding law and is applicable only to voice channel time slots.

1.2 *Bit rate*

The nominal bit rate is 2048 kbit/s. The tolerance on this rate is ± 50 parts per million (ppm).

1.3 *Timing signal*

It should be possible to derive the transmit timing signal from any of the following:

a) from the received 2048 kbit/s signal,

b) from an external source at 2048 kHz (see § 5),

c) from an internal oscillator.

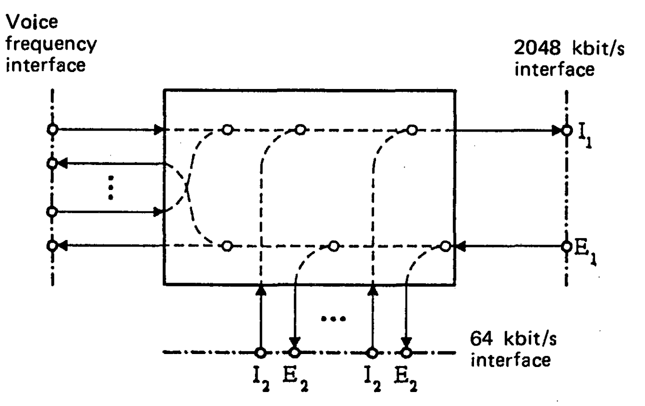
Note – The provision of a timing signal output, available for the purpose of synchronizing other equipments, is an option that might be required depending upon national synchronization arrangements.

1.4 *Types of access:*

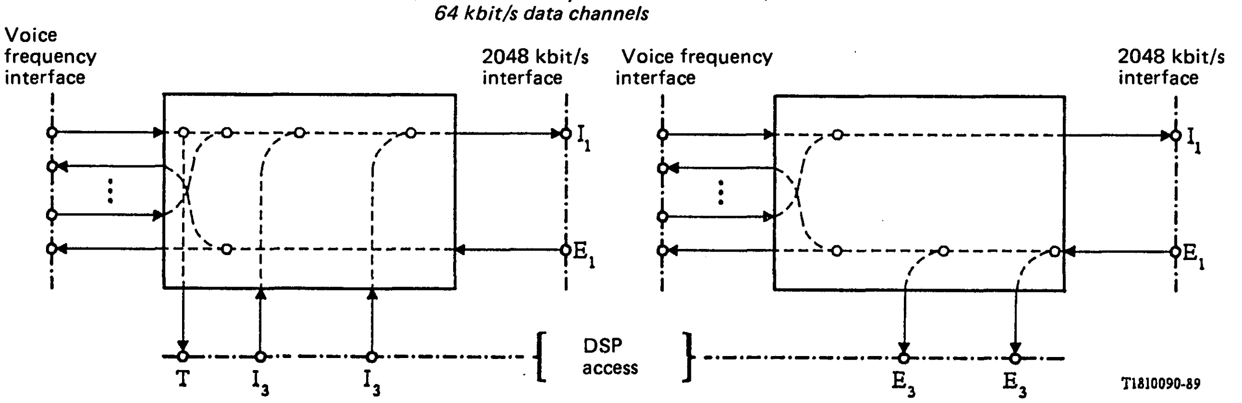
a) access for bidirectional synchronous 64 kbit/s channels (see Figure 1a/G.735);

b) access for unidirectional synchronous 384 kbit/s channels (see Figure 1b/G.735).

Note – The synchronous insertion of a digital sound programme signal into a 384 kbit/s channel requires the internal regeneration of a timing signal T synchronized by the 2048 kbit/s signal I_1. The timing signal is used for synchronizing the sampling frequency of the analogue/digital converters producing the digital sound programme signal.



a) Bidirectional synchronous insertion/extraction of 64 kbit/s data channels



b) Unidirectional synchronous insertion and extraction of digital sound-programme (DSP) into/out of a 384 kbit/s channel

I, E insertion side; extraction side
I_1, E_1 2048 kbit/s interface
I_2, E_2 64 kbit/s interface
I_3, E_3 synchronous digital sound programme access
T timing signal

FIGURE 1/G.735

PCM multiplex equipment operating at 2048 kbit/s and offering access to digital sound-programme signals and/or to synchronous 64 kbit/s data channels

2 Frame structure and use of derived channel time slots

2.1 *Frame structure of 2048 kbit/s signal*

Refer to § 2.3 of Recommendation G.704. Bit 1 of the frame should be used in accordance with § 2.3.3 of Recommendation G.704, i.e. for a CRC check bit procedure.

2.2 *Use of derived channel time slots*

2.2.1 *Telephone channels*

It should be possible to assign channel time slots 1 to 15 and 17 to 31 to thirty telephone channels numbered from 1 to 30.

2.2.2 *64 kbit/s access*

The number of accessible channel time slots should be at least four and the equipment shall allow access to any of channel time slots 1 to 15 and 17 to 31.

Note – Equipment exists which provides access to at least four channel time slots in the following order of priority: 6 – 22 – 14 – 30 – 2 – 18 – 10 – 26 – 4 – 20 – 12 – 28 – 8 – 24 – 5 – 21 – 13 – 29 – 1 – 17 – 9 – 25 – 3 – 19 – 11 – 27 – 7 – 23 – 15 – 31.

2.2.3 *384 kbit/s access*

The time slot allocation for digital channels with a bit rate at 384 kbit/s is given in Table 1/G.735.

TABLE 1/G.735

384 kbit/s channels (Note 1)					Digital sound-programme access points
A	B	C	D	E	
1-2-3 17-18-19	4-5-6 20-21-22	7-8-9 23-24-25	10-11-12 26-27-28	13-14-15 29-30-31	I3, T, E3 Figure 1b/G.735

Note 1 – The five possible 384 kbit/s channels in a 2048 kbit/s stream are numbered A to E. Preferably the channel pairs A-B and C-D should be used for stereophonic transmission.

Note 2 – If the channel time slot 16 which is assigned to signalling as covered in § 5 is not needed for signalling, it may be used for purposes other than a voice channel encoded within the PCM multiplex equipment.

3 Frame alignment and CRC procedures

An illustration of the procedure is given in Figure 2/G.706.

3.1 *Loss of frame alignment*

Refer to § 4.1.1 of Recommendation G.706.

3.2 *Recovery of frame alignment*

Refer to § 4.1.2 of Recommendation G.706.

3.3 *CRC multiframe alignment in TSO*

Refer to § 4.2 of Recommendation G.706.

3.4 *CRC bit monitoring*

Refer to § 4.3 of Recommendation G.706.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The PCM multiplex equipment should detect the following fault conditions:

4.1.1 Failure of power supply.

4.1.2 Failure of codec (except when using single channel codecs).

As a minimum requirement, this fault condition should be recognized when for at least one signal level in the range −21 to −6 dBm0, the signal-to-quantizing noise ratio performance of the local codec is 18 dB or more below the level recommended in Recommendation G.712.

4.1.3 Loss of incoming signals at the 64 kbit/s and 384 kbit/s tributary input ports.

Note 1 – This detection is not mandatory when contradirectional interfaces are used.

Note 2 – The detection of this fault condition is not mandatory for channel time slot 16 when channel associated signalling is used and the signalling multiplex equipment is situated within a few metres of the PCM multiplex equipment.

4.1.4 Loss of the incoming signal at 2048 kbit/s.

Note 1 – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

Note 2 – Where separate circuits are used for the digital signal and the timing signal, the loss of either or both should constitute loss of the incoming signal.

4.1.5 Loss of frame alignment.

4.1.6 Excessive bit error ratio detected by monitoring the frame alignment signal.

4.1.6.1 With a random bit error ratio of $\leq 10^{-4}$, the probability of activating the indication of fault condition within a few seconds should be less than 10^{-6}.

With a random bit error ratio of $\geq 10^{-3}$, the probability of activating the indication of fault condition within a few seconds should be higher than 0.95.

4.1.6.2 With a random bit error ratio of $\geq 10^{-3}$, the probability of deactivating the indication of fault condition within a few seconds should be almost 0.

With a random bit error ratio of $\leq 10^{-4}$, the probability of deactivating the indication of fault condition within a few seconds should be higher than 0.95.

Note – The activating and the deactivating period specified as "a few seconds" is intended to be in the order of 4 to 5 seconds.

4.1.7 Alarm indication received from the remote PCM multiplex equipment (see § 4.2.3).

4.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 2/G.735. The consequent actions are as follows:

4.2.1 Service alarm indication generated to signify that the service provided by the PCM multiplex is no longer available. This indication should be forwarded at least to the switching and/or signalling multiplex equipment depending upon the arrangements provided. The indication should be given as soon as possible and not later than 2 ms after detection of the relevant fault condition.

This specification, taking into account the specification given in § 4.2.5, is equivalent to recommending that the average time to detect a loss of frame alignment or a loss of the incoming 2048 kbit/s signal and to give the relevant indication should not be greater than 3 ms.

When using common channel signalling the indication should be forwarded to the switching equipment by means of a separate interface on the PCM multiplex equipment.

4.2.2 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the AIS (see General Notes below to § 4.2) at 2048 kbit/s input is detected, the prompt maintenance alarm indication associated with loss of frame alignment (see § 4.1.5) and excessive error ratio (see § 4.1.6) should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 2/G.735 with the two fault conditions.

Note – The location and provision of any visual and/or audible alarm activated by the alarm indications given in §§ 4.2.1 and 4.2.2, is left to the discretion of each Administration.

4.2.3 Alarm indication to the remote end transmitted by changing bit 3 of channel time slot 0 from the state 0 to the state 1 in those frames not containing the frame alignment signal. This should be effected as soon as possible.

4.2.4 Transmission suppressed at the analogue voice-frequency outputs.

4.2.5 AIS applied to all 64 kbit/s and 384 kbit/s outputs (see General Notes below § 4.2). For 64 kbit/s outputs, this action should be taken as soon as possible and not later than two ms after the detection of the fault condition.

4.2.6 AIS applied to relevant time slots in the composite 2048 kbit/s output signal (if suspension of incoming 64 kbit/s and/or 384 kbit/s signals is provided).

General Notes to § 4.2

Note 1 – The equivalent binary content of the alarm indication signal (AIS) is a continuous stream of binary 1s. The strategy for detecting the presence of the AIS should be such that with a high probability the AIS is detectable even in the presence of random errors having a mean error rate of 1 in 10^3. Nevertheless, a signal in which all the binary elements, with the exception of the frame alignment signal, are in the state 1, should not be taken as an AIS.

Note 2 – All timing requirements quoted apply equally to restoration, subsequent to the fault condition clearing.

5 Signalling

Text as in Recommendation G.732.

6 Interfaces

6.1 *Audio frequency interface*

The analogue audio frequency interfaces should be in accordance with Recommendations G.712, G.713, G.714 and G.715.

6.2 *Digital interfaces*

The digital interfaces at 2048 kbit/s should be in accordance with Recommendation G.703.

The digital interfaces at 64 kbit/s should be of either the codirectional or the contradirectional type specified in Recommendation G.703. The specifications for 64 kbit/s interfaces are not mandatory for channel associated signalling. The interface for external synchronization of the transmitting timing signal should be in accordance with Recommendation G.703.

The need to define a digital interface operating at 384 kbit/s is under study.

Note 1 – It should be noted that, according to the principle of minimizing the number of different types of interfaces, the information rate of 384 kbit/s will be offered to customers at the user/network interface level using the 2048 kbit/s interface as defined in Recommendations I.431 and G.703.

Note 2 – In the case of the 64 kbit/s codirectional interface, the design of the input ports should take account of the need to provide octet alignment, to allow controlled slips when the tributary timing and that of the multiplexer timing source are plesiochronous, and to absorb jitter and wander up to the limits given in Recommendation G.823.

TABLE 2/G.735

Fault conditions and consequent actions for the PCM multiplex equipment

Equipment part	Fault conditions (see § 4.1)	Consequent actions (see § 4.2)					
		Service alarm indication generated	Prompt maintenance alarm indication generated	Alarm indication remote end transmitted	Transmission suppressed at the analogue voice-frequency outputs	AIS applied to all 64 kbit/s and 384 kbit/s outputs	AIS to the relevant time slot of the 2048 kbit/s composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes	Yes (if practicable)	Yes (if practicable)	Yes (if practicable)	Yes (if practicable)
	Failure of codec	Yes	Yes	Yes	Yes		
Multiplexer only	Loss of incoming signal at 64 kbit/s and/or 384 kbit/s inputs (see Note under § 4.1.3)		Yes				Yes
Demultiplexer only	Loss of incoming signal at 2048 kbit/s	Yes	Yes	Yes	Yes	Yes	
	Loss of frame alignment (see Note 2 of Rec. G.706, § 4.2)	Yes	Yes (see § 4.2.2)	Yes	Yes	Yes	
	Error ratio $1 \cdot 10^{-3}$ on the frame alignment signal	Yes	Yes (see § 4.2.2)	Yes	Yes	Yes	
	Alarm indication received from the remote end	Yes					

Note – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

7 Jitter

7.1 *Jitter at 2048 kbit/s output*

7.1.1 In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from f_1 = 20 Hz to f_4 = 100 kHz. See Figure 2/G.823.

7.1.2 In the case where the transmitting timing signal is derived from an external source having no jitter, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from f_1 = 20 Hz to f_4 = 100 kHz.

7.1.3 In the case where the transmitting timing signal is derived from the incoming 2048 kbit/s signal having no jitter, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.10 UI when it is measured within the frequency range from f_1 = 20 Hz to f_4 = 100 kHz. The equivalent binary content of the test signal applied at the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151.

Note – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

7.2 *Jitter at tributary outputs*

7.2.1 *Jitter at 64 kbit/s output*

In the case where the incoming 2048 kbit/s signal has no jitter, the peak-to-peak jitter at the 64 kbit/s output should not exceed 0.025 UI when it is measured within the frequency range from f_1 = 20 Hz to f_4 = 10 kHz. The equivalent binary content of the test signal applied to the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151.

Note – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

7.2.2 *Jitter at 384 kbit/s output*

Since the physical and electrical characteristics of a 384 kbit/s interface are identical to those of the 2048 kbit/s interface, the specification of this parameter is the same as that given in § 7.1.3 above.

7.3 *Jitter transfer functions*

7.3.1 The jitter transfer function between the 2048 kHz external synchronisation signal and the 2048 kbit/s output signal should not exceed the gain/frequency limits given in Figure 2/G.735. The 2048 kHz signal shall be modulated with sinusoidal jitter.

Some Administrations require that equipment be fitted with jitter reducers. In this case, the jitter transfer junction should not exceed the gain/frequency limits given in Figure 3/G.735.

7.3.2 In the case where the transmitting timing is derived from the incoming signal, the jitter transfer junction between the 2048 kbit/s input and 2048 kbit/s output shall be as specified in § 7.3.1.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

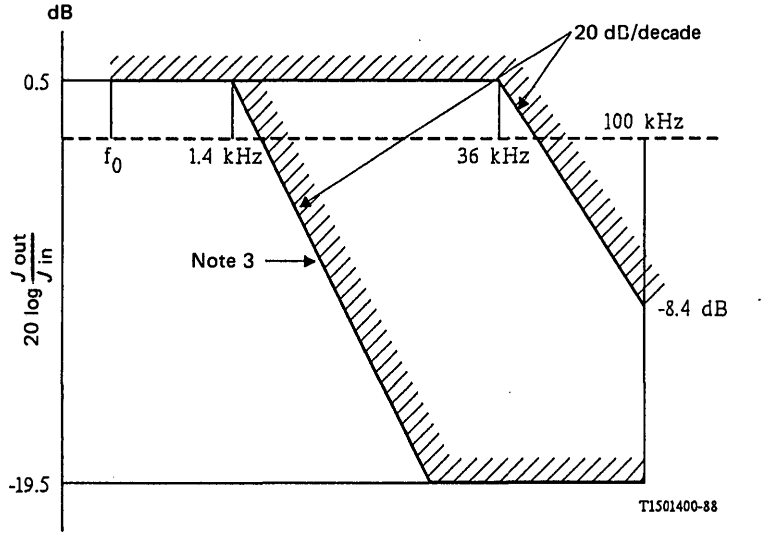
7.3.3 The jitter transfer function between the 2048 kbit/s and the 64 kbit/s output should not exceed −29.6 dB when measured over the frequency range f_0 to 10 kHz. The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

Note 3 – The jitter reduction of 1/32 due to demultiplexing is equivalent to −30.1 dB.

7.3.4 Since the physical and electrical characteristics of a 384 kbit/s interface are identical to those of the 2048 kbit/s interface, the jitter transfer function between the 2048 kbit/s input and the 384 kbit/s output is the same as that given in §§ 7.3.1 and 7.3.2 above.

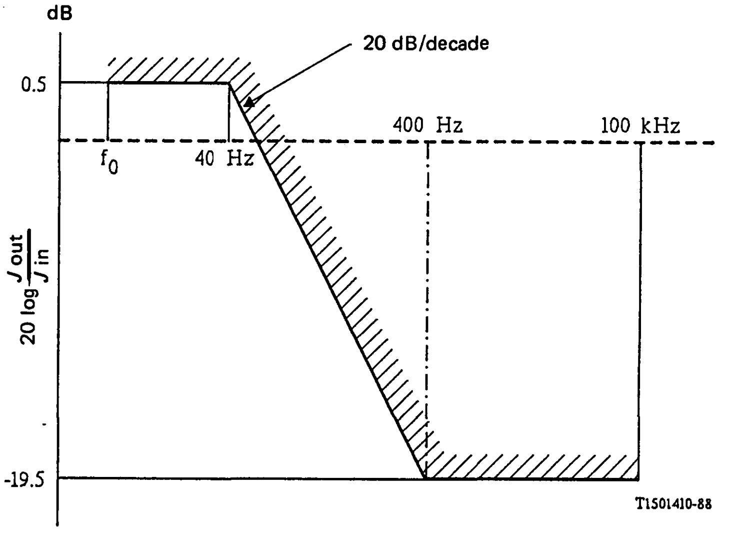


Note 1 — The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 — To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency but not wider than 40 Hz.

Note 3 — For interfaces within national boundaries, this characteristic may be used.

FIGURE 2/G.735



Note 1 — The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 — To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

FIGURE 3/G.735

CHARACTERISTICS OF A SYNCHRONOUS DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 2048 kbit/s

(former Recommendation G.738 of Volume III of the Yellow Book)

This Recommendation gives the characteristics of a synchronous digital multiplex equipment, to combine up to 31 tributary channels at 64 kbit/s in a 2048 kbit/s digital stream. It is foreseen that in the future the need may arise to devote *n* 64 kbit/s time slots to services requiring more than a single 64 kbit/s channel. The additions to this Recommendation to allow this facility (e.g. definition of proper interfaces at $n \times 64$ kbit/s) are under study.

1 General characteristics

1.1 *Bit rate*

The nominal bit rate is 2048 kbit/s. The tolerance on this rate is ± 50 parts per million (ppm).

1.2 *Timing signal*

It should be possible to derive the transmit timing signal from any of the following:

a) from the received 2048 kbit/s signal,

b) from an external source at 2048 kHz (see § 5),

c) from an internal oscillator.

Note 1 – The possibility of also deriving the transmitting timing signal from a 64 kbit/s tributary is under study.

Note 2 – The provision of a timing signal output, available for the purpose of synchronizing other equipments, is an option that might be required depending upon national synchronization arrangements.

2 Frame structure

Refer to §2.3 of Recommendation G.704 for frame structure and for use of derived channel time slots. Bit 1 of the frame should be used in accordance with § 2.3.3 of Recommendation G.704, i.e. for a CRC check bit procedure.

Note – In case of interconnection with multiplex equipment using time slot 16 for internal purposes, the use of this time slot for a 64 kbit/s tributary could be excluded.

3 Frame alignment and CRC procedures

An illustration of the procedure is given in Figure 2/G.706.

3.1 *Loss of frame alignment*

Refer to § 4.1.1 of Recommendation G.706.

3.2 *Recovery of frame alignment*

Refer to § 4.1.2 of Recommendation G.706.

3.3 *CRC multiframe alignment in TS0*

Refer to § 4.2 of Recommendation G.706.

3.4 *CRC bit monitoring*

Refer to § 4.3 of Recommendation G.706.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The digital muldex should detect the following fault conditions:

4.1.1 Failure of power supply.

4.1.2 Loss of the incoming signal at the 64 kbit/s tributary input port.

Note – This detection is not mandatory when contradirectional interfaces are used.

4.1.3 Loss of the incoming signal at 2048 kbit/s.

Note 1 – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

Note 2 – Where separate circuits are used for the digital signal and the timing signal, the loss of either or both should constitute loss of the incoming signal.

4.1.4 Loss of frame alignment at 2048 kbit/s.

4.1.5 Excessive bit error ratio detected by monitoring the frame alignment signal.

4.1.5.1 With a random bit error ratio of $\leq 10^{-4}$, the probability of activating the indication of fault condition within a few seconds should be less than 10^{-6}.

With a random bit error ratio of $\geq 10^{-3}$, the probability of activating the indication of fault condition within a few seconds should be higher than 0.95.

4.1.5.2 With a random bit error ratio of $\geq 10^{-3}$, the probability of desactivating the indication of fault condition within a few seconds should be almost 0.

With a random bit error ratio of $\leq 10^{-4}$, the probability of of desactivating the indication of fault condition within a few seconds should be higher than 0.95.

Note – The activating and the deactivating period specified as "a few seconds" is intended to be in the order of 4 to 5 seconds.

4.1.6 Alarm indication received from the remote digital muldex (see § 4.2).

4.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 1/G.736. The consequent actions are as follows:

4.2.1 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the AIS (see General Notes below to § 4.2) at 2048 kbit/s input is detected, the prompt maintenance alarm indication associated with loss of frame alignment (see § 4.1.4) and excessive error ratio (see § 4.1.5) should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 1/G.736 with the two fault conditions.

Note – The location and provision of any visual and/or audible alarm activated by the alarm indications given in § 4.2.1 is left to the discretion of each Administration.

4.2.2 Alarm indication to the remote end transmitted by changing bit 3 of channel time slot 0 from the state 0 to the state 1 in those frames not containing the frame alignment signal. This should be effected as soon as possible.

4.2.3 AIS applied to all 64 kbit/s outputs (see General Notes below to § 4.2). This action should be taken as soon as possible and not later than 2 ms after the detection of the fault condition.

4.2.4 AIS applied to relevant time slots in the composite 2048 kbit/s output signal (if supervision of incoming 64 kbit/s signal is provided).

General Notes to § 4.2

Note 1 – The equivalent binary content of the alarm indication signal (AIS) is a continuous stream of binary 1s. The strategy for detecting the presence of the AIS should be such that with a high probability the AIS is detectable even in the presence of random errors having a mean error ratio $1 \cdot 10^{-3}$. Nevertheless, a signal in which all the binary elements, with the exception of the frame alignment signal, are in the state 1, should not be taken as an AIS.

Note 2 – All timing requirements quoted apply equally to restoration, subsequent to the fault condition clearing.

TABLE 1/G.736

Fault conditions and consequent actions for the 2048 kbit/s synchronous digital multiplex equipment

Equipment part	Fault conditions (see § 4.1)	Consequent actions (see § 4.2)			
		Prompt maintenance alarm indication generated	Alarm indication to the remote end transmitted	AIS applied to all 64 kbit/s outputs	AIS applied to the relevant time slot of the 2048 kbit/s composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes (if practicable)	Yes (if practicable)	Yes (if practicable)
Multiplexer only	Loss of incoming signal at a 64 kbit/s input (see Note under § 4.1.2)	Yes			Yes
Demultiplexer only	Loss of incoming signal at 2048 kbit/s	Yes	Yes	Yes	
	Loss of frame alignment (see Note 2 of Rec. G.706, § 4.2)	Yes (see § 4.2.1)	Yes	Yes	
	Error ratio $1 \cdot 10^{-3}$ on the frame alignment signal	Yes (see § 4.2.1)	Yes	Yes	
	Alarm indication received from the remote end				

Note – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if the condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

5 Interfaces

The digital interfaces at 2048 kbit/s should be in accordance with Recommendation G.703.

The digital interfaces at 64 kbit/s should be of either the codirectional or the contradirectional type specified in Recommendation G.703. The interface for external synchronization of the transmitting timing signal should be in accordance with G.703.

Note 2 – In the case of the 64 kbit/s codirectional interface, the design of the input ports should take account of the need to provide octet alignment, to allow controlled slips when the tributary timing and that of the multiplexer timing source are plesiochronous, and to absorb jitter and wander up to the limits given in Recommendation G.823.

6 Jitter

6.1 *Jitter at 2048 kbit/s output*

6.1.1 In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 100$ kHz. See Figure 2/G.823.

6.1.2 In the case where the transmitting timing signal is derived from an external source having no jitter, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 100$ kHz.

6.1.3 In the case where the transmitting timing signal is derived from the incoming 2048 kbit/s signal having no jitter, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.10 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 100$ kHz. The equivalent binary content of the test signal applied at the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendatoin O.151.

Note – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

6.2 *Jitter at 64 kbit/s output*

In the case where the incoming 2048 kbit/s signal has no jitter, the peak-to-peak jitter at the 64 kbit/s output should not exceed 0.025 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 10$ kHz. The equivalent binary content of the test signal applied to the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15} - 1$ as specified in Recommendation O.151.

Note – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

6.3 *Jitter transfer functions*

6.3.1 The jitter transfer function between the 2048 kHz external synchronisation signal and the 2048 kbit/s output signal should not exceed the gain/frequency limits given in Figure 1/G.736. The 2048 kHz signal shall be modulated with sinusoidal jitter.

Some Administrations require that equipment be fitted with jitter reducers. In this case, the jitter transfer function should not exceed the gain/frequency limits given in Figure 2/G.736.

6.3.2 In the case where the transmitting timing is derived from the incoming signal, the jitter transfer junction between the 2048 kbit/s input and 2048 kbit/s output shall be as specified in § 6.3.1.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

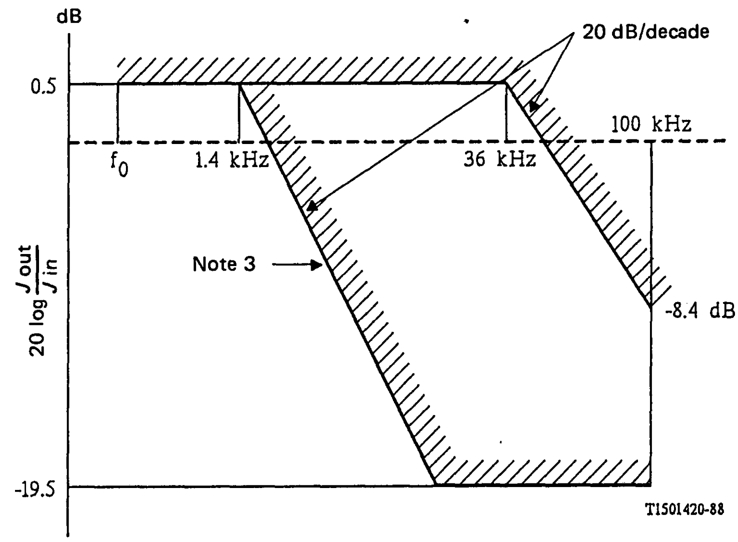
Note 2 – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

6.3.3 The jitter transfer function between the 2048 kbit/s and the 64 kbit/s output should not exceed -29.6 dB when measured over the frequency range f_0 to 10 kHz. The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

Note 3 – The jitter reduction of 1/32 due to demultiplexing is equivalent to –30.1 dB.

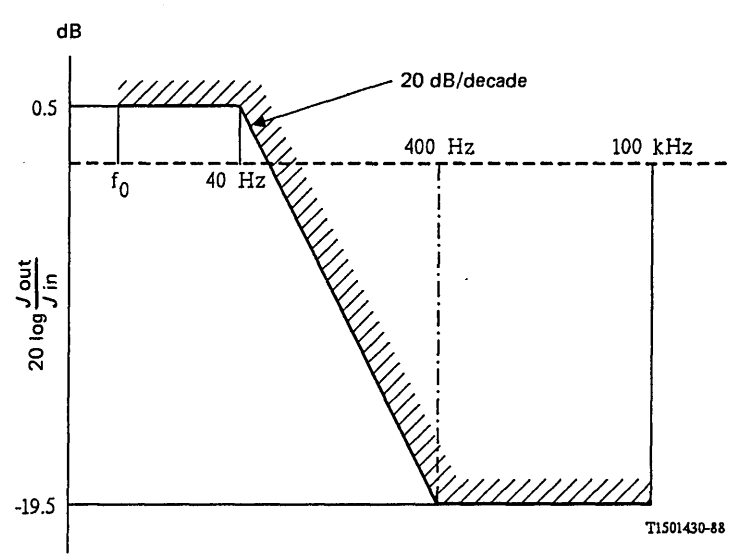


Note 1 – The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 – To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

Note 3 – For interfaces within national boundaries, this characteristic may be used.

FIGURE 1/G.736



Note 1 – The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 – To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

FIGURE 2/G.736

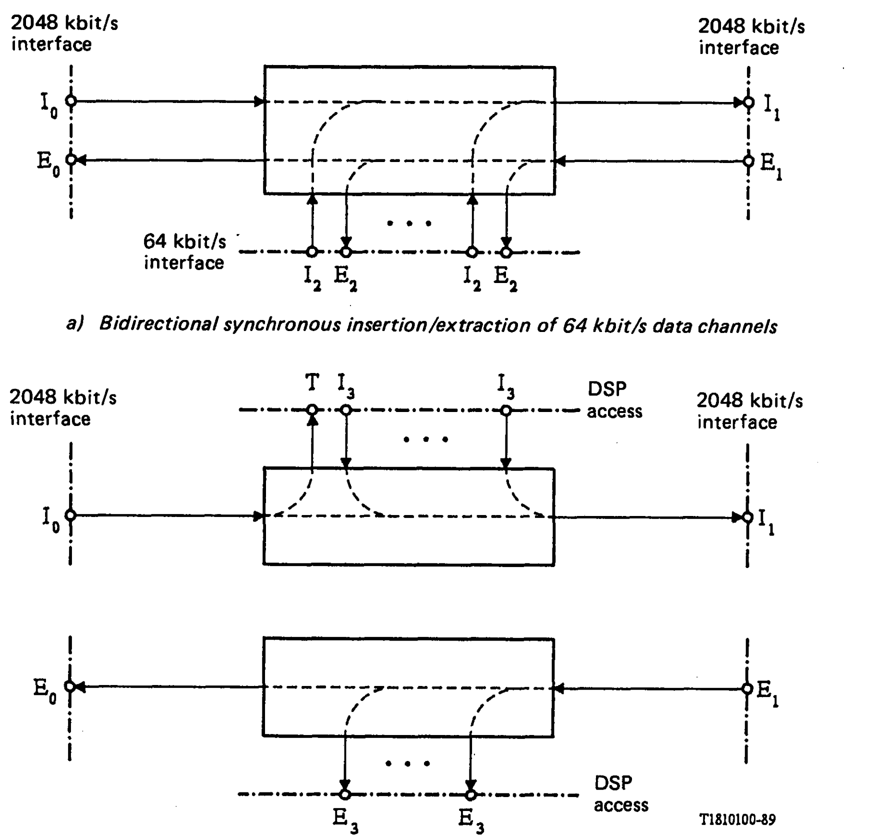
CHARACTERISTICS OF AN EXTERNAL ACCESS EQUIPMENT OPERATING AT 2048 kbit/s OFFERING SYNCHRONOUS DIGITAL ACCESS AT 384 kbit/s AND/OR 64 kbit/s

(former Recommendation G.739 of Volume III of the Yellow Book)

This Recommendation gives the characteristics of equipment (external to PCM muldexes) operating at 2048 kbit/s and providing one or several of the following tributaries into/from channel time slots of a 2048 kbit/s composite signal:

– bidirectional synchronous 64 kbit/s access (Figure 1a/G.737);
– unidirectional synchronous 384 kbit/s access (Figure 1b/G.737).

The 384 kbit/s channel is based on the allocation of 6 × 64 kbit/s time slots, e.g. for setting up sound-programme circuits according to Recommendations J.41 and J.42. Because these circuits are specified as unidirectional the equipment for insertion/extraction has to be separated as shown in Figure 1b/G.737.



a) Bidirectional synchronous insertion/extraction of 64 kbit/s data channels

b) Unidirectional synchronous insertion and extraction of a digital sound-programme (DSP) signal into/out of a 384 kbit/s channel

I_0, I_1 Insertion side
E_0, E_1 Extraction side
I_2, E_2 64 kbit/s interface
I_3, E_3 Synchronous digital sound-programme access
T Timing signal

FIGURE 1/G.737

External access equipment for 64 and 384 kbit/s channels

1 General characteristics

1.1 *Bit rate*

The nominal bit rate is 2048 kbit/s. The tolerance on this rate is ± 50 parts per million (ppm).

1.2 *Types of external access*

a) Bidirectional synchronous insertion/extraction of 64 kbit/s data channels (see Figure 1a/G.737).

Note 1 – The timing signal for the insertion side should be derived from the 2048 kbit/s incoming signal at the insertion side (I_0): the timing signal for the extraction side should be derived from the 2048 kbit/s incoming signal at the extraction side (E_1).

Note 2 – The provision of a timing signal output, available for the purpose of synchronizing other equipments, is an option that might be required depending upon national synchronization arrangements.

Note 3 – Further study is required on the possible need for an internal clock.

b) Unidirectional synchronous insertion and extraction of a digital sound-programme signal into/out of a 384 kbit/s channel (see Figure 1b/G.737).

Note – The synchronous insertion equipment for 384 kbit/s signals requires the internal regeneration of a timing signal synchronized by the 2048 kbit/s input signal I_0. This timing signal output of the synchronous insertion equipment is used for synchronizing the sampling frequency of the analogue/digital converter.

2 Frame structure and use of derived channel time slots

2.1 *Frame structure of the 2048 kbit/s signal*

Refer to § 2.3 of Recommendation G.704. Bit 1 of the frame should be used in accordance with § 2.3.3 of Recommendation G.704, i.e. for a CRC check bit procedure.

2.2 *Use of derived channel time slots*

Time slots not accessed flow transparently through the equipment.

Note – Further study is required as to whether the binary content of time slots used at the access points should be replaced, after extraction from the composite signal, by the AIS.

2.2.1 *64 kbit/s access*

The number of accessible channel time slots should be at least four and the equipment shall allow access to any of channel time slots 1 to 15 and 17 to 31.

Note – Equipment exists which provides access to at least four channel time slots in the following order of priority: 6 – 22 – 14 – 30 – 2 – 18 – 10 – 26 – 4 – 20 – 12 – 28 – 8 – 24 – 5 – 21 – 13 – 29 – 1 – 17 – 9 – 25 – 3 – 19 – 11 – 27 – 7 – 23 – 15 – 31.

2.2.2 *384 kbit/s access*

The time slot allocation for digital channels with a bit rate at 384 kbit/s is given in Table 1/G.737.

TABLE 1/G.737

384 kbit/s channels (Note 1)					Digital sound-programme access points
A	B	C	D	E	
1-2-3 17-18-19	4-5-6 20-21-22	7-8-9 23-24-25	10-11-12 26-27-28	13-14-15 29-30-31	I3, T, E3 Figure 1b/G.735

Note 1 – The five possible 384 kbit/s channels in a 2048 kbit/s stream are numbered A to E. Preferably the channel pairs A-B and C-D should be used for stereophonic transmission.

Note 2 – If the channel time slot 16 which is assigned to signalling as covered in § 5 is not needed for signalling, it may be used for purposes other than a voice channel encoded within the PCM multiplex equipment.

3 Frame alignment and CRC procedures both at insertion (I_0) and extraction (E_1) sides

An illustration of the procedure is given in Figure 2/G.706.

3.1 *Loss of frame alignment*

Refer to § 4.1.1 of Recommendation G.706.

3.2 *Recovery of frame alignment*

Refer to § 4.1.2 of Recommendation G.706.

3.3 *CRC multiframe alignment in TSO*

Refer to § 4.2 of Recommendation G.706.

3.4 *CRC bit monitoring*

Refer to § 4.3 of Recommendation G.706.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The equipment should detect the following fault conditions:

4.1.1 Failure of power supply.

4.1.2 Loss of incoming signal at I_2 or I_3.

Note – This detection is not mandatory when contradirectional interfaces are used.

4.1.3 Loss of the incoming signal at 2048 kbit/s both at insertion (I_0) and extraction (E_1) sides.

Note 1 – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

Note 2 – Where separate circuits are used for the digital signal and the timing signal, the loss of either or both should constitute loss of the incoming signal.

4.1.4 Loss of frame alignment both at insertion (I_0) and extraction (E_1) sides.

4.1.5 Excessive bit error ratio detected by monitoring the frame alignment signal at both the insertion (I_0) and extraction (E_1) sides.

Note – The detection of this fault condition at insertion side (I_0) depends on the type of application of this equipment in a network and therefore is not mandatory.

4.1.5.1 With a random bit error ratio of $\leqslant 10^{-4}$, the probability of activating the indication of fault condition within a few seconds should be less than 10^{-6}.

With a random bit error ratio of $\geqslant 10^{-3}$, the probability of activating the indication of fault condition within a few seconds should be higher than 0.95.

4.1.5.2 With a random bit error ratio of $\geqslant 10^{-3}$, the probability of deactivating the indication of fault condition within a few seconds should be almost 0.

With a random bit error ratio of $\leqslant 10^{-4}$, the probability of deactivating the indication of fault condition within a few seconds should be higher than 0.95.

Note – The activating and the deactivating period specified as "a few seconds" is intended to be in the order of 4 to 5 seconds.

4.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 2/G.737. The consequent actions are as follows:

4.2.1 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the AIS at the 2048 kbit/s inputs (I_0, E_1) is detected (see General Notes below to § 4.2), the prompt maintenance alarm indication associated with loss of frame alignment (see § 4.1.4) and excessive error ratio (see § 4.1.5) should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 2/G.737 with the two fault conditions.

Note – The location and provision of any visual and/or audible alarm activated by the alarm indications given in § 4.2.1 is left to the discretion of each Administration.

4.2.2 AIS applied to E_2 or E_3 outputs (see General Notes below to § 4.2). This action should be taken as soon as possible and not later than 2 ms after the detection of the fault condition.

4.2.3 AIS applied to relevant time slots in the composite 2048 kbit/s output signal at insertion side (I_1) if supervision of the incoming I_2 and I_3 signal is provided.

4.2.4 Inhibition of I_2 or I_3 digital information insertion.

4.2.5 Both 2048 kbit/s signals are bypassed.

Note – The provision of this consequent action depends on the type of application of this equipment in a network and therefore is not mandatory.

4.2.6 AIS applied to the 2048 kbit/s output, extraction side (E_0).

Note – The provision of this consequent action depends on the type of application of this equipment in a network and therefore is not mandatory.

4.2.7 AIS applied to the 2048 kbit/s output, insertion side (I_1).

Note – The provision of this consequent action depends on the type of this equipment in a network and therefore is not mandatory.

General Note to § 4.2

Note 1 – The equivalent binary content of the alarm indication signal (AIS) is a continuous stream of binary 1s. The strategy for detecting the presence of the AIS should be such that with a high probability the AIS is detectable even in the presence of random errors having a mean error ratio $1 \cdot 10^{-3}$. Nevertheless, a signal in which all the binary elements, with the exception of the frame alignment signal, are in the state 1, should not be taken as an AIS.

Note 2 – All timing requirements quoted apply equally to restoration, subsequent to the fault condition clearing.

5 **Interfaces**

The digital interfaces at 2048 kbit/s should be in accordance with Recommendation G.703.

The digital interfaces at 64 kbit/s should be either of the codirectional or the contradirectional type specified in Recommendation G.703.

The need to define a digital interface operating at 384 kbit/s is under study.

Note 1 – It should be noted that according to the principle of minimizing the number of different types of interfaces, the information rate of 384 kbit/s will be offered to customers at the user/network interface level using the 2048 kbit/s interface as defined in Recommendations I.431 and G.703.

Note 2 – In the case of the 64 kbit/s codirectional interface, the design of the input ports should take account of the need to provide octet alignment, to allow controlled slips when the tributary timing and that of the multiplexer timing source are plesiochronous, and to absorb jitter and wander up to the limits given in Recommendation G.823.

TABLE 2/G.737

Fault conditions and consequent actions for the external access equipment

Fault conditions (see § 4.1)		Consequent actions (see § 4.2)				Both 2048 kbit/s signal are bypassed (see Note under § 4.2.5)	AIS applied to the 2048 kbit/s output, extraction side (E_0) (see Note under § 4.2.6)	AIS applied to the 2048 kbit/s output, insertion side (I_1) (see Note under § 4.2.7)
		Prompt maintenance alarms indication generated	AIS applied to E_2 or E_3 outputs	Inhibition of digital information insertion I_2, I_3	AIS applied to the relevant time slot of the 2048 kbit/s composite signal at insertion side (I_1)			
Failure of power supply		Yes				Yes	Yes (if practicable)	Yes (if practicable)
Loss of incoming signal at I_2 or I_3 inputs (see Note under § 4.1.2)		Yes			Yes			
Loss of incoming signal at 2048 kbit/s	Extr.s. (E_1)	Yes	Yes				Yes	
	Ins.s. (I_0)	Yes		Yes				Yes
Loss of frame alignment (see Note 2 of Rec. G.706, § 4.2)	Extr. s. (E_1)	Yes (see § 4.2.1)	Yes				Yes	
	Ins. s. (I_0)	Yes (see § 4.2.1)		Yes				Yes
Error ratio 1.10^{-3} on the frame alignment signal (see Note under § 4.1.5)	Extr.s. (E_1)	Yes (see § 4.2.1)	Yes				Yes	
	Ins.s. (I_0)	Yes (see § 4.2.1)		Yes				Yes

Note – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

6 Jitter

6.1 *Jitter at 2048 kbit/s output*

When there is no jitter on the 2048 kbit/s inputs (I_0, E_1) the peak-to-peak jitter at the 2048 kbit/s outputs (I_1, E_0) should not exceed 0.10 UI when it is measured within the frequency range from f_1 = 20 Hz to f_4 = 100 kHz. The equivalent binary content of the test signal applied at the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151. See Figure 2/G.823.

Note – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

6.2 *Jitter at E_2 and E_3 outputs*

6.2.1 The jitter at the E_2 (64 kbit/s) output when there is no jitter at the 2048 kbit/s input (E_1) should not exceed 0.025 UI when measured within the frequency range from f_1 = 20 Hz to f_4 = 10 kHz. The equivalent binary content of the test signal applied at the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151.

Note – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

6.2.2 Since the physical and electrical characteristics of a 384 kbit/s interface are identical to those of the 2048 kbit/s interface, the jitter at the E_3 (synchronous 384 kbit/s) output when there is no jitter at the 2048 kbit/s input (E_1) is according to § 6.1 above.

6.3 *Jitter transfer functions*

6.3.1 The jitter transfer function between the 2048 kbit/s input (I_0, E_1) and the output (I_1, E_0) should not exceed the gain/frequency limits given in Figure 2/G.737.

Some Administrations require that equipment be fitted with jitter reducers. In this case, the jitter transfer function should not exceed the gain/frequency limits given in Figure 3/G.737.

Note 1 – The 2048 kHz signal shall be modulated with sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

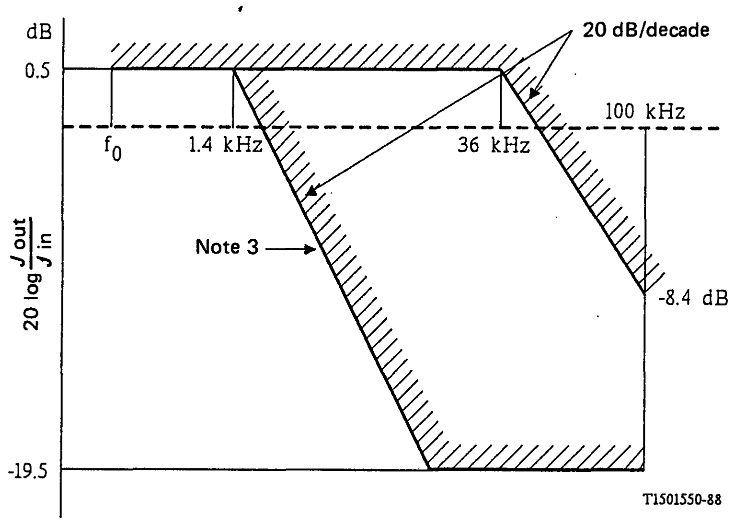
6.3.2 The jitter transfer function between the 2048 kbit/s input (E_1) and the E_2 (64 kbit/s) output should not exceed -29.6 dB when measured over the frequency range f_0 to 10 kHz. The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

Note 3 – The jitter reduction of 1/32 due to demultiplexing is equivalent to -30.1 dB.

6.3.3 Since the physical and electrical characteristics of a 384 kbit/s interface are identical to those of the 2048 kbit/s interface, the jitter transfer function between the 2048 kbit/s input (E_1) and E_3 (synchronous 384 kbit/s) output is according to § 6.3.1 above.

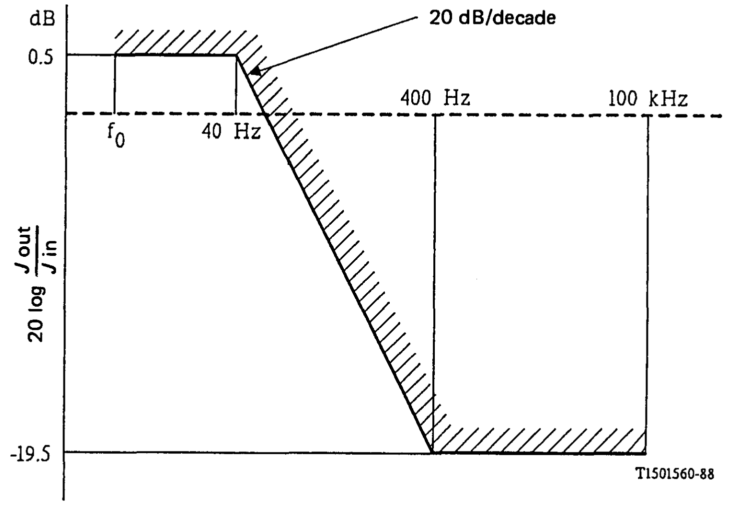


Note 1 – The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 – To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

Note 3 – For interfaces within national boundaries, this characteristic may be used.

FIGURE 2/G.737



Note 1 – The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 – To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

FIGURE 3/G.737

CHARACTERISTICS OF PRIMARY PCM MULTIPLEX EQUIPMENT OPERATING AT 2048 kbit/s AND OFFERING SYNCHRONOUS DIGITAL ACCESS AT 320 kbit/s AND/OR 64 kbit/s

(Melbourne, 1988)

This Recommendation gives the characteristics of a PCM multiplex equipment operating at 2048 kbit/s and providing one or several of the following internal digital access options:

– bidirectional synchronous 64 kbit/s channels (see Figure 1a/G.738);

– unidirectional synchronous 320 kbit/s channels (see Figure 1b/G.738).

The 320 kbit/s channel is based on the allocation of 5 × 64 kbit/s time slots, e.g. for setting up sound-programme circuits according to Recommendations J.43 and J.44. Because these circuits are specified as unidirectional, the equipment for insertion/extraction has to be separated as shown in Figure 1b/G.738.

1 General characteristics

1.1 *Fundamental characteristics for voice-channel encoding*

The encoding law used is the A-law as specified in Recommendation G.711. The sampling rate, load capacity and the code are also specified in that Recommendation.

The number of quantized values is 256.

Note – The inversion of bits 2, 4, 6 and 8 is covered by the encoding law and is applicable only to voice-channel time slots.

1.2 *Bit rate*

The nominal bit rate is 2048 kbit/s. The tolerance on this rate is ± 50 parts per million (ppm).

1.3 *Timing signal*

It should be possible to derive the transmit timing signal from any of the following:

a) from the received 2048 kbit/s signal;

b) from an external source at 2048 kHz (see § 5);

c) from an internal oscillator.

Note – The provision of a timing signal output, available for the purpose of synchronizing other equipments, is an option that might be required depending upon national synchronization arrangements.

1.4 *Types of access*

a) access for bidirectional synchronous 64 kbit/s channels (see Figure 1a/G.738);

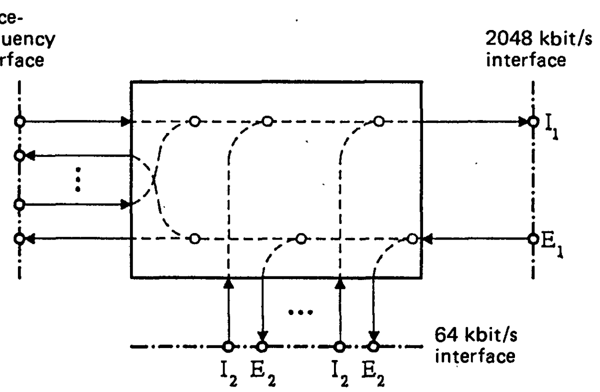
b) access for unidirectional synchronous 320 kbit/s channels (see Figure 1b/G.738).

Note – The synchronous insertion of a digital sound-programme signal into a 320 kbit/s channel requires the internal regeneration of a timing signal T synchronized by the 2048 kbit/s signal I_1. The timing signal is used for synchronizing the sampling frequency of the analogue/digital converters producing the digital sound-programme signal.

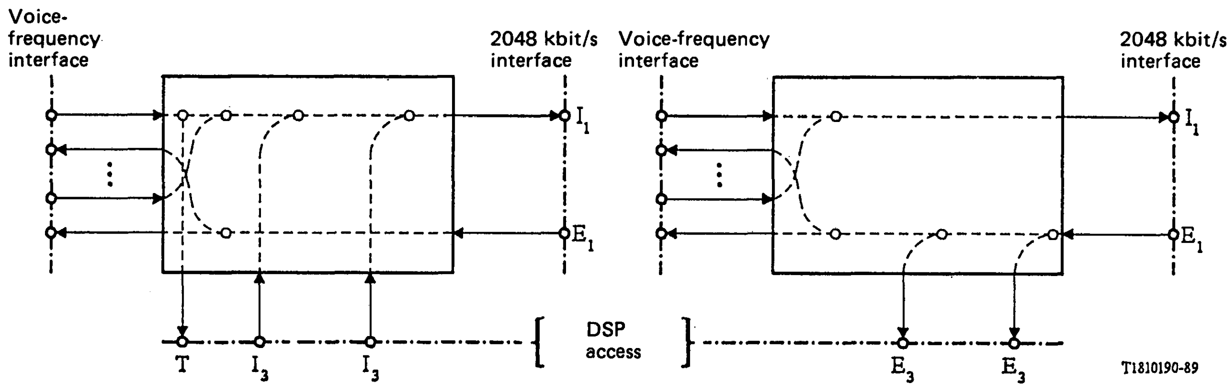
2 Frame structure and use of derived channel time slots

2.1 *Frame structure of 2048 kbit/s signal*

Refer to § 2.3 of Recommendation G.704. Bit 1 of the frame should be used in accordance with § 2.3.3 of Recommendation G.704, i.e. for a CRC check bit procedure.



a) Bidirectional synchronous insertion/extraction of 64 kbit/s data channels



b) Unidirectional synchronous insertion and extraction of digital sound-programme (DSP) into/out of a 320 kbit/s channel

I, E Insertion side; extraction side
I_1, E_1 2048 kbit/s interface
I_2, E_2 64 kbit/s interface
I_3, E_3 Synchronous digital sound-programme signal access
T Timing signal

FIGURE 1/G.738

PCM multiplex equipment operating at 2048 kbit/s and offering access to digital sound-programme signals and/or to synchronous 64 kbit/s data channels

2.2 *Use of derived channel time slots*

2.2.1 *Telephone channels*

It should be possible to assign channel time slots 1 to 15 and 17 to 31, to 30 telephone channels numbered from 1 to 30.

2.2.2 *64 kbit/s access*

The number of accessible channel time slots should be at least four and the equipment shall allow access to any of channel time slots 1 to 15 and 17 to 31.

Note – Equipment exists which provides access to at least four channel time slots in the following order of priority: 6 – 22 – 14 – 30 – 2 – 18 – 10 – 26 – 4 – 20 – 12 – 28 – 8 – 24 – 5 – 21 – 13 – 29 – 1 – 17 – 9 – 25 – 3 – 19 – 11 – 27 – 7 – 23 – 15 – 31.

2.2.3 *320 kbit/s access*

The time slot allocation for digital channels with bit rate at 320 kbit/s is given in Table 1/G.738.

TABLE 1/G.738

320 kbit/s channels (Note 1)						Digital sound-programme access points
A	B	C	D	E	F	
1 - 2 - 3 - 4 - 5	6 - 7 - 8 - 9 - 10	11 - 12 - 13 - 14 - 15	17 - 18 - 19 - 20 - 21	22 - 23 - 24 - 25 - 26	27 - 28 - 29 - 30 - 31	I3, T, E3 Figure 1b/G.738

Note 1 – The six possible 320 kbit/s channels in a 2048 kbit/s stream are numbered A to F. Preferably the channel pairs A-B, C-D and E-F should be used for stereophonic transmission.

Note 2 – If the channel time slot 16 which is assigned to signalling as covered in § 5 is not needed for signalling, it may be used for purposes other than a voice channel encoded within the PCM multiplex equipment.

3 Frame alignment and CRC procedures

An illustration of the procedure is given in Figure 2/G.706.

3.1 *Loss of frame alignment*

Refer to § 4.1.1 of Recommendation G.706.

3.2 *Recovery of frame alignment*

Refer to § 4.1.2 of Recommendation G.706.

3.3 *CRC multiframe alignment in TSO*

Refer to § 4.2 of Recommendation G.706.

3.4 *CRC bit monitoring*

Refer to § 4.3 of Recommendation G.706.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The PCM multiplex equipment should detect the following conditions:

4.1.1 Failure of power supply.

4.1.2 Failure of codec (except when using single channel codecs).

As a minimum requirement, this fault condition should be recognized when for at least one signal level in the range −21 to −6 dBm0, the signal-to-quantizing noise ratio performance of the local codec is 18 dB or more below the level recommended in Recommendation G.712.

4.1.3 Loss of incoming signals at the 64 kbit/s and 320 kbit/s tributary input ports.

Note 1 – This detection is not mandatory when contradirectional interfaces are used.

Note 2 – The detection of this fault condition is not mandatory for channel time slot 16 when channel associated signalling is used and the signalling multiplex equipment is situated within a few metres of the PCM multiplex equipment.

4.1.4 Loss of the incoming signal at 2048 kbit/s.

Note 1 – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

Note 2 – Where separate circuits are used for the digital signal and the timing signal, the loss of either or both should constitute loss of the incoming signal.

4.1.5 Loss of frame alignment.

4.1.6 Excessive bit error ratio detected by monitoring the frame alignment signal.

4.1.6.1 With a random bit error ratio of $\leq 10^{-4}$, the probability of activating the indication of fault condition within a few seconds should be less than 10^{-6}.

With a random bit error ratio of $\geq 10^{-3}$, the probability of activating the indication of fault condition within a few seconds should be higher than 0.95.

4.1.6.2 With a random bit error ratio of $\geq 10^{-3}$, the probability of deactivating the indication of fault condition within a few seconds should be almost 0.

With a random bit error ratio of $\leq 10^{-4}$, the probability of deactivating the indication of fault condition within a few seconds should be higher than 0.95.

Note – The activating and deactivating period specified as "a few seconds" is intended to be in the order of 4 to 5 seconds.

4.1.7 Alarm indication received from the remote PCM multiplex equipment (see § 4.2.3).

4.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 2/G.738. The consequent actions are as follows:

4.2.1 Service alarm indication generated to signify that the service provided by the PCM multiplex is no longer available. This indication should be forwarded at least to the switching and/or signalling multiplex equipment depending upon the arrangements provided. The indication should be given as soon as possible and not later than 2 ms after detection of the relevant fault condition.

This specification, taking into account the specification given in § 4.2.5, is equivalent to recommending that the average time to detect a loss of frame alignment or a loss of the incoming 2048 kbit/s signal and to give the relevant indication should not be greater than 3 ms.

When using common channel signalling the indication should be forwarded to the switching equipment by means of separate interface on the PCM multiplex equipment.

4.2.2 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the AIS at 2048 kbit/s input is detected (see General Notes below to § 4.2), the prompt maintenance alarm indication associated with loss of frame alignement (see § 4.1.5) and excessive error ratio (see § 4.1.6) should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 2/G.738 with the two fault conditions.

Note – The location and provision of any visual and/or audible alarm activated by the alarm indications given in § 4.2.1 and § 4.2.2, is left to the discretion of each Administration.

4.2.3 Alarm indication to the remote end, transmitted by changing bit 3 of channel time slot 0 from the state 0 to the state 1 in those frames not containing the frame alignment signal. This should be effected as soon as possible.

TABLE 2/G.738

Fault conditions and consequent actions for the PCM multiplex equipment

Equipment part	Fault conditions (see § 4.1)	Consequent actions (see § 4.2)					
		Service alarm indication generated	Prompt maintenance alarm indication	Alarm indication remote end transmitted	Transmission suppressed at the analogue voice-frquency outputs	AIS applied to 64 kbit/s and 320 kbit/s outputs	AIS applied to the relevant time slot of the 2048 kbit/s composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes	Yes (if practicable)	Yes (if practicable)	Yes (if practicable)	Yes (if practicable)
	Failure of codec	Yes	Yes	Yes	Yes		
Multiplexer only	Loss of incoming signal at 64 kbit/s and/or 320 kbit/s inputs (see Notes under § 4.1.3)		Yes				Yes
Demultiplexer only	Loss of incoming signal at 2048 kbit/s	Yes	Yes	Yes	Yes	Yes	
	Loss of frame alignment (see Note 2 Rec. G.706, § 4.2)	Yes	Yes (see § 4.2.2)	Yes	Yes	Yes	
	Error ratio $1 \cdot 10^{-3}$ on the frame alignment signal	Yes	Yes (see § 4.2.2)	Yes	Yes	Yes	
	Alarm indication received from the remote end	Yes					

Note – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should not be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

4.2.4 Transmission suppressed at the analogue voice-frequency outputs.

4.2.5 AIS applied to all 64 kbit/s and 320 kbit/s outputs (see General Notes below to § 4.2). For 64 kbit/s outputs this actions should be taken as soon as possible and not later than 2 ms after the detection of the fault condition.

4.2.6 AIS applied to relevant time slots in the composite 2048 kbit/s output signal (if suspension of incoming 64 kbit/s and 320 kbit/s signals is provided).

General Notes to § 4.2

Note 1 – The equivalent binary content of the alarm indication signal (AIS) is a continuous stream of binary 1s. The strategy for detecting the presence of AIS should be such that with a high probability the AIS is detectable even in the presence of random errors having a mean error rate of 1 in 10^3. Nevertheless, a signal in which all the binary elements, with the exception of the frame alignment signal, are in the state 1, should not be taken as an AIS.

Note 2 – All timing requirements quoted apply equally to restoration, subsequent to the fault condition clearing.

5 Signalling

Text as in Recommendation G.732.

6 Interfaces

6.1 *Audio frequency interface*

The analogue audio frequency interfaces should be in accordance with Recommendations G.712, G.713, G.714 and G.715.

6.2 *Digital interfaces*

The digital interfaces at 2048 kbit/s should be in accordance with Recommendation G.703.

The digital interfaces at 64 kbit/s should be of either the codirectional or the contradirectional type specified in Recommendation G.703. The specification for 64 kbit/s interfaces are not mandatory for channel-associated signalling. The interface for external synchronization of the transmitting timing signal should be in accordance with Recommendation G.703.

The need to define a digital interface operating at 320 kbit/s is under study.

Note 1 – It should be noted that, according to the principle of minimizing the number of different types of interfaces, the information rate of 320 kbit/s will be offered to customers at the user/network interface level using the 2048 kbit/s interface as defined in Recommendation I.431 and Recommendation G.703.

Note 2 – In the case of the 64 kbit/s codirectional interface, the design of the input ports should take into account the need to provide octet alignment, to allow controlled slips when the tributary timing and that of the multiplexer timing source are plesiochronous, and to absorb jitter and wander up to the limits given in Recommendation G.823.

7 Jitter

7.1 *Jitter at 2048 kbit/s output*

7.1.1 In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from f_1 = 20 Hz to f_4 = 100 kHz. See Figure 2/G.823.

7.1.2 In the case where the transmitting timing signal is derived from an external source having no jitter, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from f_1 = 20 Hz to f_4 = 100 kHz.

7.1.3 In the case where the transmitting timing signal is derived from the incoming 2048 kbit/s signal having no jitter, the peak-to-peak jitter at the 2048 kbit/s output should not exceed 0.10 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 100$ kHz. The equivalent binary content of the test signal applied at the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151.

Note – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

7.2 *Jitter at tributary outputs*

7.2.1 *Jitter at 64 kbit/s output*

In the case where the incoming 2048 kbit/s signal has no jitter, the peak-to-peak jitter at the 64 kbit/s output should not exceed 0.025 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 10$ kHz. The equivalent binary content of the test signal applied to the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151.

Note – In order to carry out this measurement without invoking AIS at the 64 kbit/s output it will normally be necessary to include a frame alignment signal in the test signal.

7.2.2 *Jitter at 320 kbit/s output*

Since the physical and electrical characteristics of a 320 kbit/s interface are identical to those of the 2048 kbit/s interface, the specification of this parameter is the same as that given in § 7.1.3 above.

7.3 *Jitter transfer functions*

7.3.1 The jitter transfer function between the 2048 kbit/s external synchronization signal and the 2048 kbit/s output signal should not exceed the gain/frequency limits given in Figure 2/G.738. The 2048 kHz signal shall be modulated with sinusoidal jitter.

Some Administrations require that equipment be fitted with jitter reducers. In this case, the jitter transfer functions should not exceed the gain/frequency limits given in Figure 3/G.738.

7.3.2 In the case where the transmitting timing is derived from the incoming signal, the jitter transfer function between the 2048 kbit/s input and the 2048 kbit/s output shall be as specified in § 7.3.1.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

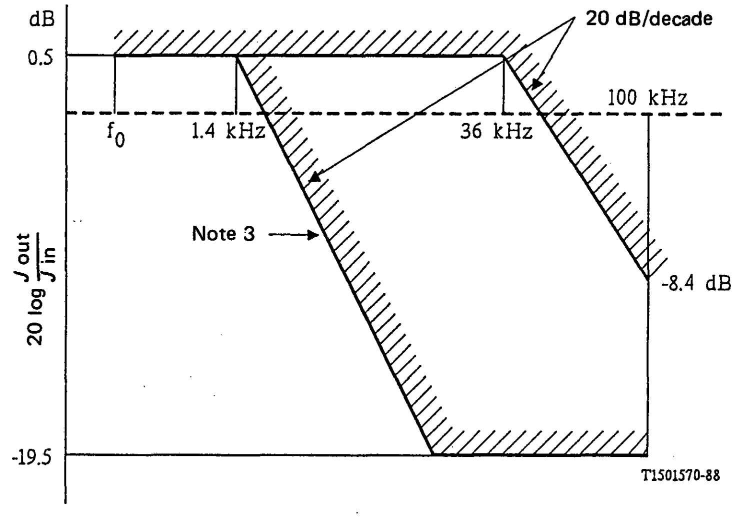
7.3.3 The jitter transfer function between the 2048 kbit/s input and the 64 kbit/s output should not exceed -29.6 dB when measured over the frequency range f_0 to 10 kHz. The frequency f_0 should be less than 20 Hz and as low as possbile (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignement signal in the test signal.

Note 3 – The jitter reduction of 1/32 due to demultiplexing is equivalent to -30.1 dB.

7.3.4 Since the physical and electrical characteristics of a 320 kbit/s interface are identical to those of 2048 kbit/s interface, the jitter transfer function between 2048 kbit/s input and 320 kbit/s output is the same as that given in §§ 7.3.1 and 7.3.2 above.

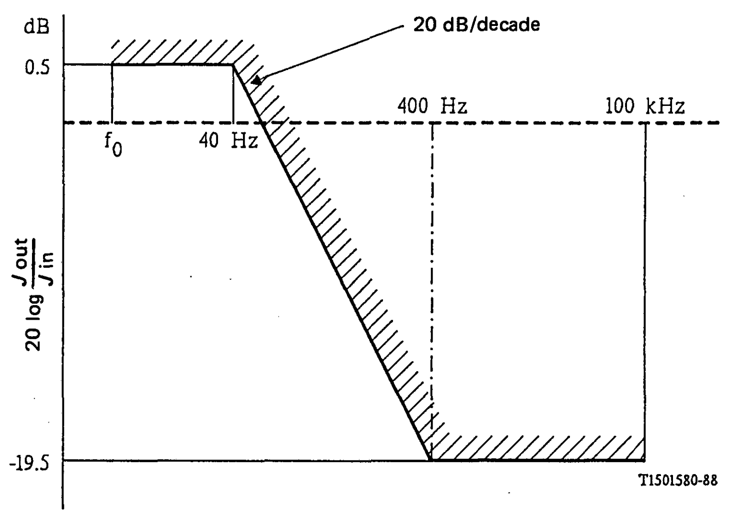


Note 1 — The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 — To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

Note 3 — For interfaces within national boundaries, this characteristic may be used.

FIGURE 2/G.738



Note 1 — The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 — To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

FIGURE 3/G.738

CHARACTERISTICS OF AN EXTERNAL ACCESS EQUIPMENT OPERATING AT 2048 kbit/s OFFERING SYNCHRONOUS DIGITAL ACCESS AT 320 kbit/s AND/OR 64 kbit/s

(Melbourne, 1988)

This Recommendation gives the characteristics of equipment (external to PCM muldexes) operating at 2048 kbit/s and providing one or several of the following tributaries into/from channel time slots of a 2048 kbit/s composite signal:

– bidirectional synchronous 64 kbit/s access (Figure 1a/G.739);
– unidirectional synchronous 320 kbit/s access (Figure 1b/G.739).

The 320 kbit/s channel is based on the allocation of 5 × 64 kbit/s time slots, e.g. for setting up sound-programme circuits according to Recommendations J.43 and J.44. Because these circuits are specified as unidirectional, the equipment for insertion/extraction has to be separated as shown in Figure 1b/G.739.

1 General characteristics

1.1 *Bit rate*

The nominal bit rate is 2048 kbit/s. The tolerance on this rate is ± 50 parts per million (ppm).

1.2 *Types of external access*

a) Bidirectional synchronous insertion/extraction of 64 kbit/s data channels (see Figure 1a/G.739).

Note 1 – The timing signal for the insertion side should be derived from the 2048 kbit/s incoming signal at the insertion side (I_0); the timing signal for the extraction side should be derived from the 2048 kbit/s incoming signal at the extraction side (E_1).

Note 2 – The provision of a timing signal output, available for the purpose of synchronizing other equipments, is an option that might be required depending upon national synchronization arrangements.

Note 3 – Further study is required on the possible need for an internal clock.

b) Unidirectional synchronous insertion and extraction of a digital sound-programme signal into/out of a 320 kbit/s channel (see Figure 1b/G.739).

Note – The synchronous insertion equipment for 320 kbit/s signals requires the internal regeneration of a timing signal synchronized by the 2048 kbit/s input signal I_0. This timing signal output of the synchronous insertion equipment is used for synchronizing the sampling frequency of the analogue/digital converter.

2 Frame structure and use of derived channel time slots

2.1 *Frame structure of the 2048 kbit/s signal*

Refer to § 2.3 of Recommendation G.704. Bit 1 of the frame should be used in accordance with § 2.3.3 of Recommendation G.704, i.e. for a CRC check bit procedure.

2.2 *Use of derived channel time slots*

Time slots not accessed flow transparently through the equipment.

Note – Further study is required as to whether the binary content of time slots used at the access points should be replaced, after extraction from the composite signal, by the AIS.

2.2.1 *64 kbit/s access*

The number of accessible channel time slots should be at least four and the equipment shall allow access to any of channel time slots 1 to 15 and 17 to 31.

Note – Equipment exists which provides access to at least four channel time slots in the following order of priority: 6 – 22 – 14 – 30 – 2 – 18 – 10 – 26 – 4 – 20 – 12 – 28 – 8 – 24 – 5 – 21 – 13 – 29 – 1 – 17 – 9 – 25 – 3 – 19 – 11 – 27 – 7 – 23 – 15 – 31.

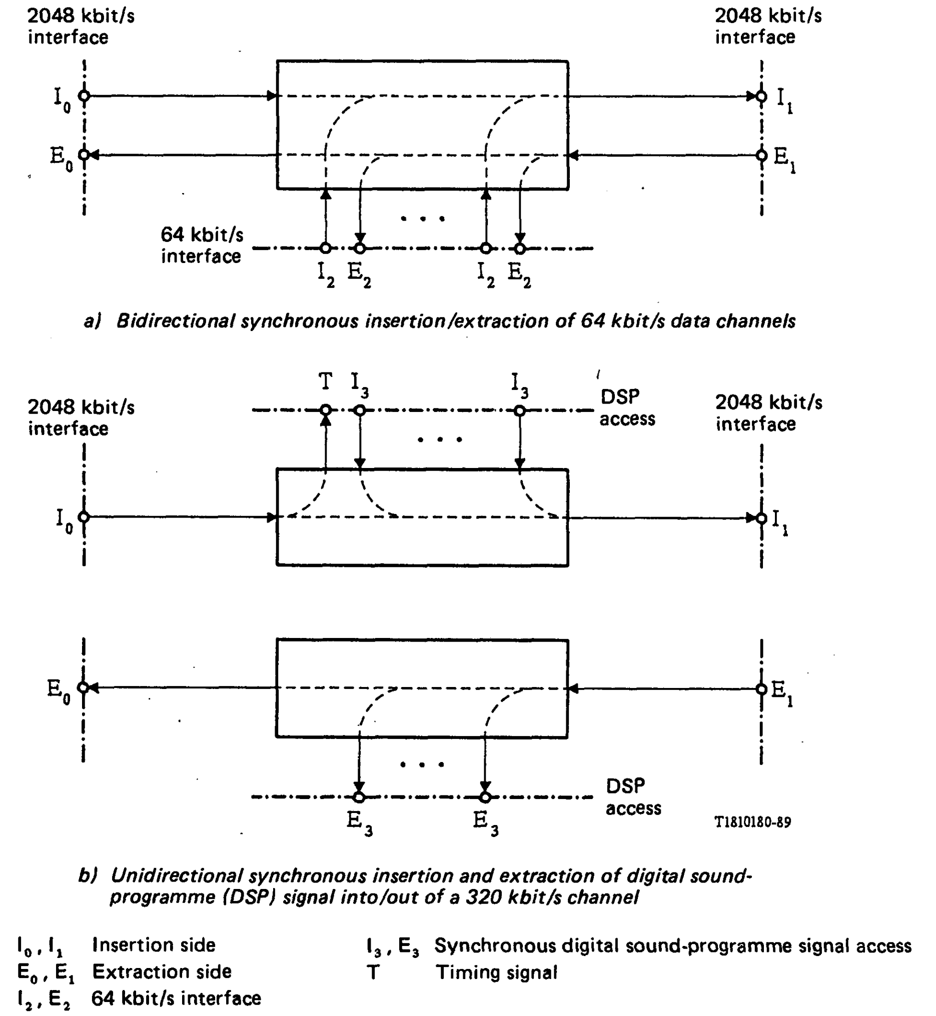


FIGURE 1/G.739

External access equipment for 64 and 320 kbit/s channels

2.2.2 *320 kbit/s access*

The time slot allocation for digital channels with bit rate at 320 kbit/s is given in Table 1/G.739.

TABLE 1/G.739

320 kbit/s channels (Note 1)						Digital sound-programme access points
A	B	C	D	E	F	
1 - 2 - 3 - 4 - 5	6 - 7 - 8 - 9 - 10	11 - 12 - 13 - 14 - 15	17 - 18 - 19 - 20 - 21	22 - 23 - 24 - 25 - 26	27 - 28 - 29 - 30 - 31	I3, T, E3 Figure 1b/G.738

Note 1 – The six possible 320 kbit/s channels in a 2048 kbit/s stream are numbered A to F. Preferably the channel pairs A-B, C-D and E-F should be used for stereophonic transmission.

Note 2 – If the channel time slot 16 which is assigned to signalling as covered in § 5 is not needed for signalling, it may be used for purposes other than a voice channel encoded within the PCM multiplex equipment.

3 Frame alignment and CRC procedures both at insertion (I_0) and extraction (E_1) sides

An illustration of the procedure is given in Figure 2/G.706.

3.1 *Loss of frame alignment*

Refer to § 4.1.1 of Recommendation G.706.

3.2 *Recovery of frame alignment*

Refer to § 4.1.2 of Recommendation G.706.

3.3 *CRC multiframe alignment in TSO*

Refer to § 4.2 of Recommendation G.706.

3.4 *CRC bit monitoring*

Refer to § 4.3 of Recommendation G.706.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The equipment should detect the following conditions:

4.1.1 Failure of power supply.

4.1.2 Loss of incoming signal at I_2 or I_3.

Note – This detection is not mandatory when contradirectional interfaces are used.

4.1.3 Loss of the incoming signal at 2048 kbit/s both at insertion (I_0) and extraction (E_1) sides.

Note 1 – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

Note 2 – Where separate circuits are used for the digital signal and the timing signal, the loss of either or both should constitute loss of the incoming signal.

4.1.4 Loss of frame alignment both at insertion (I_0) and extraction (E_1) sides.

4.1.5 Excessive bit error ratio detected by monitoring the frame alignment signal at both the insertion (I_0) and extraction (E_1) sides.

Note – The detection of this fault condition at insertion side (I_0) depends on the type of application of this equipment in a network and therefore is not mandatory.

4.1.5.1 With a random bit error ratio of $\leq 10^{-4}$, the probability of activating the indication of fault condition within a few seconds should be less than 10^{-6}.

With a random bit error ratio of $\geq 10^{-3}$, the probability of activating the indication of fault condition within a few seconds should be higher than 0.95.

4.1.5.2 With a random bit error ratio of $\geq 10^{-3}$, the probability of deactivating the indication of fault condition within a few seconds should be almost 0.

With a random bit error ratio of $\leq 10^{-4}$, the probability of deactivating the indication of fault condition within a few seconds should be higher than 0.95.

Note – The activating and deactivating period specified as "a few seconds" is intended to be in the order of 4 to 5 seconds.

4.2 *Consequent actions*

Further to the detection of fault condition, appropriate actions should be taken as specified in Table 2/G.739. The consequent actions are as follows:

4.2.1 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the AIS at the 2048 kbit/s inputs (I_0, E_1) is detected (see General Notes below to § 4.2), the prompt maintenance alarm indication associated with loss of frame alignment (see § 4.1.4) and excessive error rate (see § 4.1.5) should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 2/G.739 with the two fault conditions.

Note – The location and provision of any visual and/or audible alarm activated by the alarm indications given in § 4.2.1 is left to the discretion of each Administration.

4.2.2 AIS applied to E_2, E_3 outputs (see General Notes below to § 4.2). This action should be taken as soon as possible and not later than 2 ms after the detection of the fault condition.

4.2.3 AIS applied to relevant time slots in the composite 2048 kbit/s output signal at insertion side (I_1) if supervision of the incoming I_2 and I_3 signal is provided.

4.2.4 Inhibition of I_2 or I_3 digital information insertion.

4.2.5 Both 2048 kbit/s signals are bypassed.

Note – The provision of this consequent action depends on the type of application of this equipment in a network and therefore is not mandatory.

4.2.6 AIS applied to the 2048 kbit/s output, extraction side (E_0).

Note – The provision of this consequent action depends on the type of application of this equipment in a network and therefore is not mandatory.

4.2.7 AIS applied to the 2048 kbit/s output, insertion side (I_1).

Note – The provision of this consequent action depends on the type of this equipment in a network and therefore is not mandatory.

General Notes to § 4.2

Note 1 – The equivalent binary content of the alarm indication signal (AIS) is a continuous stream of binary 1s. The strategy for detecting the presence of the AIS should be such that with a high probability the AIS is detectable even in the presence of random errors having a mean error ratio 1×10^{-3}. Nevertheless, a signal in which all the binary elements, with the exception of the frame alignment signal, are in the state 1, should not be taken as an AIS.

Note 2 – All timing requirements quoted apply equally to restoration, subsequent to the fault condition clearing.

5 **Interfaces**

The digital interfaces at 2048 kbit/s should be in accordance with Recommendation G.703.

The digital interfaces at 64 kbit/s should be either of the codirectional or the contradirectional type specified in Recommendation G.703.

The need to define a digital interface operating at 320 kbit/s is under study.

Note 1 – It should be noted that according to the principle of minimizing the number of different types of interfaces, the information rate of 320 kbit/s will be offered to customers at the user/network interface level using the 2048 kbit/s interface as defined in Recommendations I.431 and G.703.

Note 2 – In the case of the 64 kbit/s codirectional interface, the design of the input ports should take into account the need to provide octet alignment, to allow controlled slips when the tributary timing and that of the multiplexer timing source are plesiochronous, and to absorb jitter and wander up to the limits given in Recommendation G.823.

TABLE 2/G.739

Fault conditions and consequent actions for the external access equipment

Fault conditions (see § 4.1)		Consequent actions (see § 4.2): Prompt maintenance alarms indication generated	AIS applied to E_2 or E_3 outputs	Inhibition of digital information insertion I_2, I_3	AIS applied to the relevant time slot of the 2048 kbit/s composite signal at insertion side (I_0)	Both 2048 kbit/s signals are bypassed (see Note under § 4.2.5)	AIS applied to the 2048 kbit/s output, extraction side (E_0) (see Note under § 4.2.6)	AIS applied to the 2048 kbit/s output, insertion side (I_1) (see Note under § 4.2.7)
Failure of power supply		Yes				Yes	Yes (if practicable)	Yes (if practicable)
Loss of incoming signal at I_2 or I_3 inputs (see Note under § 4.1.2)		Yes			Yes			
Loss of incoming signal at 2048 kbit/s	Extr.s. (E_1)	Yes	Yes				Yes	
	Ins.s. (I_0)	Yes		Yes				Yes
Loss of frame alignment (see Note 2 of Rec. G.706, § 4.2)	Extr.s. (E_1)	Yes (see § 4.2.1)	Yes				Yes	
	Ins.s. (I_0)	Yes (see § 4.2.1)		Yes				Yes
Error ratio $1 \cdot 10^{-3}$ on the frame alignment signal (see Note under § 4.1.5)	Extr.s. (E_1)	Yes (see § 4.2.1)	Yes				Yes	
	Ins.s. (I_0)	Yes (see § 4.2.1)		Yes				Yes

Note – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should not be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

6 Jitter

6.1 *Jitter at 2048 kbit/s output*

When there is no jitter on the 2048 kbit/s inputs (I_0, E_1) the peak-to-peak jitter at the 2048 kbit/s outputs (I_1, E_0) should not exceed 0.10 UI when it is measured within the frequency range from f_1 = 20 Hz to f_4 = 100 kHz. The equivalent binary content of the test signal applied at the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation 0.151. See Figure 2/G.823.

Note – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

6.2 *Jitter at E_2 and E_3 outputs*

6.2.1 The jitter at the E_2 (64 kbit/s) output when there is no jitter at the 2048 kbit/s input (E_1) should not exceed 0.025 UI when measured within the frequency range from f_1 = 20 Hz to f_4 = 100 kHz. The equivalent binary content of the test signal applied at the 2048 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151.

Note – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

6.2.2 Since the physical and electrical characteristics of a 320 kbit/s interface are identical to those of the 2048 kbit/s interface, the jitter at the E_3 (synchronous 320 kbit/s) output when there is no jitter at the 2048 kbit/s input (E_1) is according to § 6.1 above.

6.3 *Jitter transfer functions*

6.3.1 The jitter transfer function between the 2048 kbit/s input (I_0, E_1) and the output (I_1, E_0) should not exceed the gain/frequency limits given in Figure 2/G.739.

Some Administrations require that equipment be fitted with jitter reducers. In this case, the jitter transfer function should not exceed the gain/frequency limits given in Figure 3/G.739.

Note 1 – The 2048 kHz signal shall be modulated with sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – It may be necessary to include a frame alignment signal in the test signal to enable the measurement to be carried out.

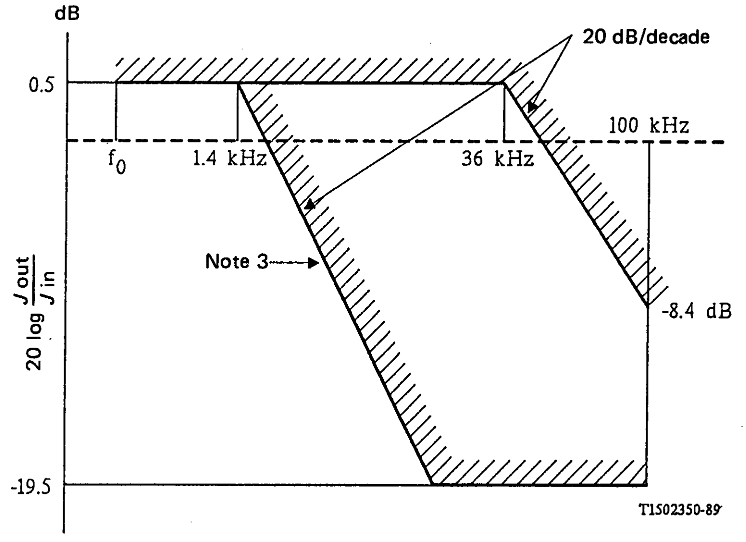
6.3.2 The jitter transfer function between the 2048 kbit/s input (E_1) and the E_2 (64 kbit/s) output should not exceed −29.6 dB when measured over the frequency range f_0 to 10 kHz. The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 1 – The 2048 kbit/s test signal shall be modulated by sinusoidal jitter. The equivalent binary content of the test signal shall be 1000.

Note 2 – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

Note 3 – The jitter reduction of 1/32 due to demultiplexing is equivalent to −30.1 dB.

6.3.3 Since the physical and electrical characteristics of a 320 kbit/s interface are identical to those of the 2048 kbit/s interface, the jitter transfer function between the 2048 kbit/s input (E_1) and E_3 (synchronous 320 kbit/s) output is according to § 6.3.1 above.

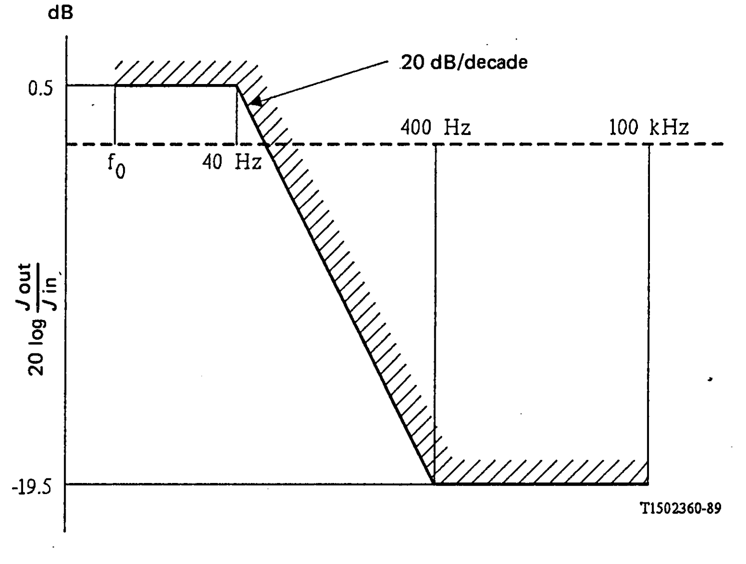


Note 1 — The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 — To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

Note 3 — For interfaces within national boundaries, this characteristic may be used.

FIGURE 2/G.739



Note 1 — The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 — To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

FIGURE 3/G.739

7.4 Principal characteristics of second order multiplex equipments

Recommendation G.741

GENERAL CONSIDERATIONS ON SECOND ORDER MULTIPLEX EQUIPMENTS

(Geneva, 1972; further amended)

The CCITT,

considering

(a) that different primary and second order multiplex equipments exist, depending upon the characteristics of different networks and the various types of signals to be transmitted in those networks;

(b) that, although studies will continue with the aim of reducing the differences between various systems, the existing situation cannot be changed in the near future;

recommends the following

(1) when two countries, both using 2048 kbit/s primary multiplex equipments such as the PCM multiplex equipment according to Recommendation G.732, have to be connected by a digital path at the second order bit rate, that bit rate should be 8448 kbit/s;

(2) when two countries, both using 1544 kbit/s primary multiplex equipments such as the PCM multiplex equipment according to Recommendation G.733, have to be connected by a digital path at the second order bit rate, that bit rate should be 6312 kbit/s.

In the meantime, it is extremely desirable to define a preferred method of interconnecting different systems.

Recommendations G.742 and G.743 give the characteristics of second order digital multiplex equipments using positive justification, and Recommendation G.745 gives the characteristics of second order multiplex equipment using positive/zero/negative justification. Recommendations G.744, G.746 and G.747 give the characteristics of second order PCM multiplex equipments. Paragraphs 2 and 4 of Recommendation G.705 give the characteristics required to terminate 6312 kbit/s and 8448 kbit/s digital paths on a digital exchange.

Recommendation G.742

SECOND ORDER DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 8448 kbit/s AND USING POSITIVE JUSTIFICATION

(Geneva, 1972; further amended)

1 General

The second order digital multiplex equipment using positive justification, described below, is intended for use on digital paths between countries using 2048 kbit/s primary multiplex equipments.

2 Bit rate

The nominal bit rate should be 8448 kbit/s.

The tolerance on that rate should be ± 30 parts per million (ppm).

3 Frame structure

Table 1/G.742 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the bunched frame alignment signal.

TABLE 1/G.742

8448-kbit/s multiplexing frame structure

Tributary bit rate (kbit/s)	2048
Number of tributaries	4
Frame structure	Bit number
	Set I
Frame alignment signal (1111010000)	1 to 10
Alarm indication to the remote digital multiplex equipment	11
Bit reserved for national use	12
Bits from tributaries	13 to 212
	Set II
Justification control bits C_{j1} (see Note)	1 to 4
Bits from tributaries	5 to 212
	Set III
Justification control bits C_{j2} (see Note)	1 to 4
Bits from tributaries	5 to 212
	Set IV
Justification control bits C_{j2} (see Note)	1 to 4
Bits from tributaries available for justification	5 to 8
Bits from tributaries	9 to 212
Frame length	848 bits
Bits per tributary	206 bits
Maximum justification rate per tributary	10 kbit/s
Nominal justification ratio	0.424

Note – C_{ji} indicates the *i*th justification control bit of the *j*th tributary.

4 Loss and recovery of frame alignment and consequent action

Loss of frame alignment should be assumed to have taken place when four consecutive frame alignment signals have been incorrectly received in their predicted positions.

When frame alignment is assumed to be lost, the frame alignment device should decide that such alignment has effectively been recovered when it detects the presence of three consecutive frame alignment signals.

The frame alignment device having detected the appearance of a single correct frame alignment signal, should begin a new search for the frame alignment signal when it detects the absence of the frame alignment signal in one of the two following frames.

Note – As it is not strictly necessary to specify the detailed frame alignment strategy, any suitable frame alignment strategy may be used provided the performance achieved is at least as efficient in all respects as that obtained by the above frame alignment strategy.

5 Multiplexing method

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended.

The justification control signal should be distributed and use the C_{jn}-bits (n = 1, 2, 3, see Table 1/G.742).

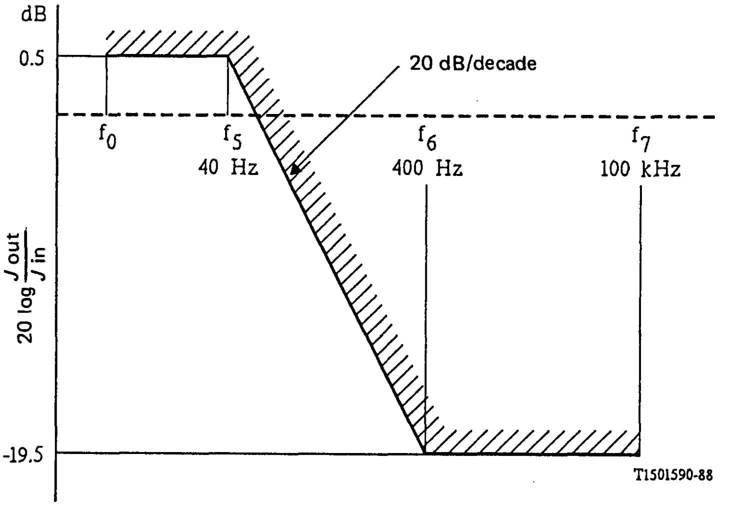
Positive justification should be indicated by the signal 111, no justification by the signal 000. Majority decision is recommended.

Table 1/G.742 gives the maximum justification rate per tributary and the nominal justification ratio.

6 Jitter

6.1 *Jitter transfer characteristic*

A 2048 kbit/s signal, modulated by sinusoidal jitter, should be subject to a muldex jitter transfer characteristic within the gain/frequency limits given in Figure 1/G.742. The equivalent binary content of the test signal should be 1000.



Note 1 – The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 – To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

Note 3 – The need to tolerate spurious responses greater than −19.5 dB in the frequency range f_6 to f_7 is for further study.

FIGURE 1/G.742

6.2 *Tributary output jitter*

The peak-to-peak jitter at a tributary output in the absence of input jitter should not exceed 0.25 UI when measured in the frequency range up to 100 kHz.

When measured with an instrument incorporating a bandpass filter having a lower cutoff frequency of 18 kHz, a roll-off of 20 dB/decade and an upper limit of 100 kHz, the peak-to-peak output jitter should not exceed 0.05 UI with a probability of 99.9% during a measurement period of 10 s.

Note – For interfaces meeting the national high Q option, detailed in Recommendation G.703, the lower cutoff frequency for the above measurement should be 700 Hz.

6.3 *Multiplex signal output jitter*

In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 8448 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 400$ kHz.

7 Digital interfaces

The digital interfaces at 2048 kbit/s and 8448 kbit/s should be in accordance with Recommendation G.703.

8 Timing signal

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal source.

9 Service digits

Two bits per frame are available for service functions. Bit 11 of Set I is used to transmit an alarm indication to the remote multiplex equipment when specific fault conditions are detected in the multiplex equipment (see § 10 below). Bit 12 of Set I is reserved for national use. On the digital path crossing the border, this bit is fixed at 1.

10 Fault conditions and consequent conditions

10.1 *Fault conditions*

The digital multiplex equipment should detect the following fault conditions:

10.1.1 Failure of power supply.

10.1.2 Loss of an incoming signal at 2048 kbit/s at the input of the multiplexer.

Note – Where separate circuits are used for the digital signal and the timing signal then loss of either or both should constitute loss of the incoming signal.

10.1.3 Loss of the incoming signal at 8448 kbit/s at the input of the demultiplexer.

Note 1 – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

Note 2 – Where separate circuits are used for the digital signal and the timing signal, then loss of either or both should constitute loss of the incoming signal.

10.1.4 Loss of frame alignment.

10.1.5 Alarm indication received from the remote multiplex equipment at the 8448 kbit/s input of the demultiplexer (see § 10.2.2 below).

10.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified by Table 2/G.742. The consequent actions are as follows:

10.2.1 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the Alarm Indication Signal (AIS) (see Note 2 under § 10.2.5 below) at 8448 kbit/s is detected at the input of the demultiplexer, the prompt maintenance alarm indication associated with loss of frame alignment should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 2/G.742 with the fault condition.

Note – The location and provision of any visual and/or audible alarm activated by this maintenance alarm indication is left to the discretion of each Administration.

10.2.2 Alarm indication to the remote multiplex equipment generated by changing from the state 0 to the state 1 bit 11 of Set I at the 8448 kbit/s output of the multiplexer.

10.2.3 AIS (see Notes 1 and 2 below) applied to all four 2048 kbit/s tributary outputs from the demultiplexer.

10.2.4 AIS (see Notes 1 and 2 below) applied to the 8448 kbit/s output of the multiplexer.

10.2.5 AIS (see Note 2 below) applied to the time slots of the 8448 kbit/s signal at the output of the multiplexer, corresponding to the relevant 2048 kbit/s tributary.

The method of transmitting the AIS at the output port of the multiplexer in time slots corresponding to a faulty input tributary, should be such that the status of the justification control digits is controlled so as to ensure that the AIS is within the tolerance specified for that tributary.

TABLE 2/G.742

Fault conditions and consequent actions

Equipment part	Fault condition (see § 10.1)	Consequent actions (see § 10.2)				
		Prompt maintenance alarm indication generated	Alarm indication to the remote multiplex equipment generated	AIS applied		
				To all the tributaries	To the composite signal	To the relevant time slots of the composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes		Yes, if practicable	Yes, if practicable	
Multiplexer only	Loss of incoming signal on a tributary	Yes				Yes
Demultiplexer only	Loss of incoming signal at 8448 kbit/s	Yes	Yes	Yes		
	Loss of frame alignment	Yes	Yes	Yes		
	Alarm indication received from the remote multiplex equipment					

Note — A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 1 — The bit rate of the AIS at the output of the multiplexer equipment or at the output of the demultiplexer equipment should be in accordance with the interface specifications.

Note 2 — The equivalent binary content of the AIS at 2048 kbit/s and 8448 kbit/s is nominally a continuous stream of 1s. The strategy for detecting the presence of the AIS should be such that the AIS is detectable even in the presence of an error ratio $1 \cdot 10^{-3}$. However, a signal, with all bits except the frame alignment signal in the 1s state, should not be mistaken for an AIS.

10.3 *Time requirements*

The fault detection and the application of the consequent actions listed in §§ 10.2.2 to 10.2.5, including the detection of AIS, should be completed within a time limit of 1 ms.

SECOND ORDER DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 6312 kbit/s AND USING POSITIVE JUSTIFICATION

(Geneva, 1972; further amended)

1 General

The second order digital multiplex equipment using positive justification described below, is intended for use on digital paths between countries using 1544 kbit/s primary multiplex equipments.

2 Bit rate

The nominal bit rate should be 6312 kbit/s.

The tolerance on that rate should be ± 30 parts per million (ppm).

3 Frame structure

Table 1/G.743 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the distributed frame and multiframe alignment signals.

4 Loss and recovery of frame and multiframe alignment and consequent action

The frame alignment recovery time should not exceed 16 ms. The signal to be applied to the tributaries during the out-of-frame-alignment time should be studied.

Once frame alignment is established, multiframe alignment should be recovered in less than 420 microseconds.

5 Multiplexing method

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended.

The justification control signal should be distributed and use the C_{jn}-bits ($n = 1, 2, 3$, see Table 1/G.743).

Positive justification should be indicated by the signal 111, no justification by the signal 000. Majority decision is recommended.

Table 1/G.743 gives the maximum justification rate per tributary and the nominal justification ratio.

6 Jitter

6.1 *Specifications at the input ports*

The digital signal presented at the input ports shall be as defined in Recommendation G.703 modified by the transmission characteristic of the interconnecting cable. The input ports shall be able to tolerate a digital signal with these electrical characteristics but modified by sinusoidal jitter up to the limits specified by the amplitude frequency relationship in Figure 1/G.743. The equivalent binary content of the signal, with jitter modulation, applied to the inputs shall be a pseudo-random bit sequence of length $2^{15} - 1$.

Note – The signal with jitter modulation applied to the demultiplexer input shall contain the bits necessary for framing and justification in addition to information bits.

TABLE 1/G.743

6312-kbit/s multiplexing frame structure

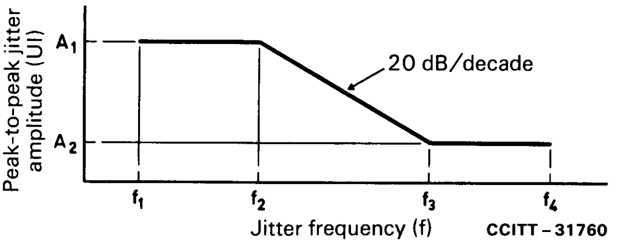
Tributary bit rate (kbit/s)	1544
Number of tributaries	4
Frame structure (see Notes 1 and 2)	Bit number
	Set I
Bit for multiframe alignment signal (M_j) (see Note 1)	1
Bits from tributaries	2 to 49
	Set II
1st bit for justification control signal (C_{j1})	1
Bits from tributaries	2 to 49
	Set III
1st bit for frame alignment signal (F_0) (see Note 3)	1
Bits from tributaries	2 to 49
	Set IV
2nd bit for justification control signal (C_{j2})	1
Bits from tributaries	2 to 49
	Set V
3rd bit for justification control signal (C_{j3})	1
Bits from tributaries	2 to 49
	Set VI
2nd bit for frame alignment signal (F_1) (see Note 3)	1
Bits from tributaries (see Note 4)	2 to 49
Frame length	294 bits
Multiframe length	1176 bits
Bits per tributary per multiframe (including justification)	288 bits
Maximum justification rate per tributary	5367 bit/s
Nominal justification ratio	0.334

Note 1 – This frame is repeated 4 times to form a multiframe with designated $j = 1, 2, 3, 4$. The multiframe alignment signal is a $011x$-pattern. x may be used as an alarm service digit.

Note 2 – The bits from the second and fourth tributaries are inverted logically before multiplexing with the bits from the first and third tributaries.

Note 3 – The frame alignment is $F_0 = 0$ and $F_1 = 1$.

Note 4 – The bit available for the justification of tributary j is the first time slot of tributary j following F_1 in the jth frame.



Input	A_1 (UI)	A_2 (UI)	f_1 (Hz)	f_2 (Hz)	f_3 (kHz)	f_4 (kHz)
1544 kbit/s	2	0.05	10	200	8	40
6312 kbit/s (provisional)	8	0.05	10	200	32	160

UI Unit interval

FIGURE 1/G.743

Lower limit of maximum tolerable input jitter

6.2 *Multiplex signal output jitter*

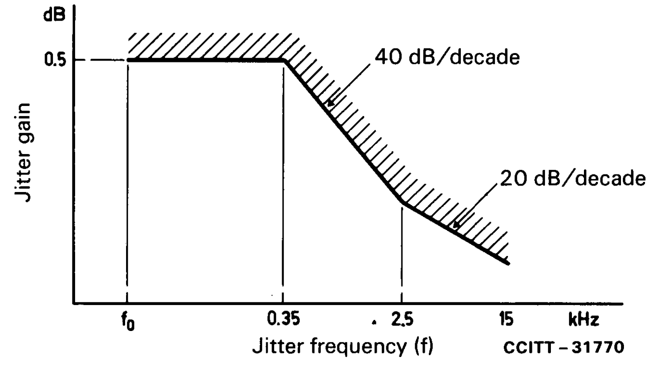
The jitter at the 6312 kbit/s output of the multiplexer should not exceed 0.01 UI rms.

6.3 *Demultiplexer output jitter with no multiplexer or demultiplexer input jitter*

With no jitter at the input to the multiplexer and demultiplexer, the jitter at the demultiplexer output should not exceed 1/3 unit intervals peak-to-peak.

6.4 *Demultiplexer jitter transfer characteristic*

The gain of the jitter transfer characteristic should not exceed the limits given in Figure 2/G.743.



Note – The frequency f_0 should be as low as possible taking into account the limitations of measuring equipment.

FIGURE 2/G.743

Demultiplexer transfer characteristic

7 Digital interfaces

The digital interfaces at 1544 kbit/s and 6312 kbit/s should be in accordance with Recommendation G.703.

8 Timing signal

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal source.

9 Service digits

The service digits are reserved for national use.

10 Fault conditions and consequent actions

10.1 *Fault conditions*

The digital multiplex equipment should detect the following fault conditions.

10.1.1 Failure of power supply.

10.1.2 Loss of frame alignment at the demultiplexer.

It may also be equipped to detect the following fault conditions.

10.1.3 Loss or degradation of incoming 1544 kbit/s signal.

10.1.4 Loss or degradation of incoming 6312 kbit/s signal.

10.1.5 Failure of the multiplex or demultiplex as evidenced by incorrect multiplexing or demultiplexing action.

10.1.6 Failure of standby (if the multiplex is so equipped).

10.2 *Consequent actions*

On the detection of a fault condition, the following appropriate actions should be taken:

10.2.1 For a multiplex equipped with automatic changeover, the consequent actions are specified in Table 2/G.743. For a multiplex so equipped, a switch to a standby is performed in the event of a failure of the multiplex equipment in service. A maintenance alarm is generated if a switch takes place, or if the standby fails. A prompt maintenance alarm is generated if an incoming signal fails, or if service is lost due to inability to complete automatic changeover to the standby.

10.2.2 For a multiplex not equipped with automatic changeover, a prompt maintenance alarm is generated in response to any fault condition detected. Such multiplexers will normally be equipped to detect power failure and loss or degradation of incoming signal at the demultiplexer.

10.2.3 The provision of an Alarm Indication Signal (AIS) to the 1544 kbit/s tributary outputs from the demultiplexer is under study. An AIS, suitable for use without special detectors at the primary PCM multiplex might be provided on an optional basis.

TABLE 2/G.743

Fault conditions and consequent actions for a multiplex equipped with automatic changeover

Equipment part	Fault condition (see § 10.1)	Consequent actions (see § 10.2.1)			
		Prompt maintenance alarm indication generated	Deferred maintenance alarm indication generated	Alarm indication to the remote multiplex equipment generated (if so equipped)	Automatic changeover actuated
Multiplexer demultiplexer	Failure of power supply	No	Yes		Yes
Multiplexer only	Loss or degradation of incoming signal on a tributary	Yes			No
Demultiplexer only	Loss or degradation of incoming signal at 6312 kbit/s		Yes	Yes	No
	Alarm indication received from the remote multiplex equipment (if so equipped)		Yes		

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Recommendation G.744

SECOND ORDER PCM MULTIPLEX EQUIPMENT OPERATING AT 8448 kbit/s

(Geneva, 1976; amended at Geneva, 1980 and at Melbourne, 1988)

1 General characteristics

1.1 *Fundamental characteristics*

The encoding law used is the A-law as specified in Recommendation G.711. The sampling rate, load capacity and the code are also specified in that Recommendation.

The number of quantized values is 256.

Note – The inversion of bits 2, 4, 6 and 8 is covered by the encoding law and is applicable only to voice-channel time slots.

1.2 *Bit rate*

The nominal bit rate is 8448 kbit/s. The tolerance on this rate is ± 30 parts per million (ppm).

1.3 *Timing signal*

It should be possible to derive the transmitting timing signal of a PCM multiplex equipment from an internal source, from the incoming digital signal and also from an external source.

Note – Further study is required on the effect of jitter of the incoming signal on the timing signal, and on the measures to be taken in case of loss of the incoming signal or the external source.

2 Frame structure

Refer to §§ 3.4.1 and 3.4.2 of Recommendation G.704 for frame structure and use of derived channel time slots.

3 Loss and recovery of frame alignment

Loss of frame alignment should be assumed to have taken place when four consecutive frame alignment signals have been incorrectly received in their predicted positions.

When frame alignment is assumed to be lost, the frame alignment device should decide that such alignment has effectively been recovered when it detects the presence of three consecutive frame alignment signals.

The frame alignment device having detected the appearance of a single correct frame alignment signal, should begin a new search for the frame alignment signal when it detects the absence of the frame alignment signal in one of the two following frames.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The PCM multiplex equipment should detect the following fault conditions.

4.1.1 Failure of power supply.

4.1.2 *Failure of codec (except when using single-channel codecs)*

As a minimum requirement, this fault condition should be recognized when, for at least one signal level in the range −21 to −6 dBm0, the signal-to-quantizing noise ratio performance of the local codec is 18 dB or more below the level recommended in Recommendation G.712.

4.1.3 *Loss of incoming signal at the 64 kbit/s input port (time slots 67 to 70)*

Note 1 – The detection of this fault condition is not mandatory when channel associated signalling is used and the signalling multiplex is situated within a few metres of the PCM multiplex equipment.

Note 2 – The detection of this fault condition is not mandatory when contradirectional interfaces are used.

4.1.4 Loss of the incoming signal at 8448 kbit/s.

Note 1 – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

Note 2 – Where separate circuits are used for the digital signal and the timing signal, then loss of either or both should constitute loss of the incoming signal.

4.1.5 Loss of frame alignment.

4.1.6 Excessive bit error ratio detected by monitoring the frame alignment signal.

4.1.6.1 With a random bit error of $\leq 10^{-4}$, the probability of activating the indication of fault condition within a few seconds should be less than 10^{-6}.

With a random bit error of $\geq 10^{-3}$, the probability of activating the indication of fault condition within a few seconds should be higher than 0.95.

4.1.6.2 With a random bit error ratio of $\geq 10^{-3}$, the probability of deactivating the indication of fault condition within a few seconds should be almost 0.

With a random bit error of $\geq 10^{-4}$, the probability of deactivating the indication of fault condition within a few seconds should be higher than 0.95.

Note – The activating and the deactivating period specified as "a few seconds" is intended to be in the order of 4 to 5 seconds.

4.1.7 Alarm indication received from the remote end (see § 4.2.3 below).

4.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 1/G.744. The consequent actions are as follows:

4.2.1 Service alarm indication generated to signify that the service provided by the PCM multiplex is no longer available. This indication should be forwarded at least to the switching and/or signalling multiplex equipment depending upon the arrangements provided. The indication should be given as soon as possible and not later than 2 ms after detection of the relevant fault condition.

This specification, taking into account the specification given in § 3 above, is equivalent to recommending that the average time to detect a loss of frame alignment or a loss of the incoming 8448-kbit/s signal and to give the relevant indication should not be greater than 3 ms.

When using common channel signalling, the indication should be forwarded to the switching equipment by means of a separate interface on the PCM multiplex equipment.

4.2.2 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the Alarm Indication Signal (AIS) (see General Note below to § 4.2) is detected the prompt maintenance alarm indication, associated with loss of frame alignment (see § 4.1.5 above) and excessive error rate (see § 4.1.6 above), should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 1/G.744 with the two fault conditions.

Note – The location and provision of any visual and/or audible alarms activated by the alarm indications given in §§ 4.2.1 and 4.2.2, is left to the discretion of each Administration.

4.2.3 Alarm indication to the remote end generated by changing bit 7 of channel time slot 66 from the state 0 to the state 1. This should be effected as soon as possible.

4.2.4 Transmission suppressed at the analogue outputs.

4.2.5 AIS applied to time slots 67 to 70 of the 64 kbit/s outputs when not used for speech (see General Note below to § 4.2). This action should be taken as soon as possible and not later than 2 ms after the detection of the fault condition.

4.2.6 AIS applied to time slots 67 to 70 of the output 8448 kbit/s composite signal when these are not used for speech (if supervision of incoming 64 kbit/s signal is provided).

General Note to § 4.2 – The equivalent binary content of the AIS is a continuous stream of binary 1s.

The strategy for detecting the presence of the AIS should be such that the AIS is detectable, even in the presence of an error ratio $1 \cdot 10^{-3}$. However, a signal with all bits except the frame alignment in the 1s state, should not be mistaken for an AIS.

Note – All timing requirements quoted apply equally to restoration, subsequent to the fault condition clearing.

TABLE 1/G.744

Fault conditions and consequent actions for the PCM multiplex equipment

Equipment part	Fault condition (see § 4.1)	Consequent action (see § 4.2)					
		Service alarm indication generated	Prompt maintenance alarm indication generated	Alarm indication to the remote end generated	Transmission suppressed at the analogue outputs	AIS applied to 64-kbit/s outputs (time slots 67 to 70)	AIS applied to time slots 67 to 70 of the 8448 kbit/s composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes	Yes, if practicable	Yes, if practicable	Yes, if practicable	Yes, if practicable
	Failure of codec	Yes	Yes	Yes	Yes		
Multiplexer only	Loss of incoming signal at 64-kbit/s inputs time slots 67 to 70 (see notes under § 4.1.3)		Yes				Yes
Demultiplexer only	Loss of incoming signal at 8448 kbit/s	Yes	Yes	Yes	Yes	Yes	
	Loss of frame alignment	Yes	Yes	Yes	Yes	Yes	
	Error rate 1 in 10^{-3} for the alignment signal	Yes	Yes	Yes	Yes	Yes	
	Alarm indication received from the remote end (bit 7 of time slot 66)	Yes					

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

5 Signalling

5.1 *Signalling arrangement*

Refer to § 3.4.3 of Recommendation G.704. Channel time-slots 67 to 70 may be used to provide an interface at 64 kbit/s which shall be suitable for use with either common channel or channel-associated signalling or other services as required.

5.2 *Loss and recovery of multiframe alignment in case of channel associated signalling*

For multiframe alignment each 64 kbit/s channel should be treated separately. For each channel, multiframe alignment should be assumed to have been lost when two consecutive multiframe alignment signals have been received with an error.

Multiframe alignment should be assumed to have been recovered as soon as the first correct multiframe signal is detected.

Note – To avoid a condition of spurious multiframe alignment, the following procedure may be used, in addition to the above:

- Multiframe alignment should be assumed to have been lost when, for a period of one or two multiframes, all the bits in the relevant channel time slots 67, 68, 69 or 70 are at the state 0.
- Multiframe alignment should be assumed to have been recovered, only when at least one bit in the state 1 is present in the relevant time slots 67, 68, 69 or 70 preceding the multiframe alignment signal first detected.

5.3 *Fault conditions and consequent actions in case of channel associated signalling*

The fault conditions and consequent actions for each 64 kbit/s signalling channel and for each signalling multiplex equipment are the same as recommended in Recommendation G.732, § 5.3.

6 Interfaces

The analogue interfaces should be in accordance with Recommendations G.712, G.713 and G.714. The digital interfaces at 8448 kbit/s should be in accordance with Recommendation G.703. The digital interfaces at 64 kbit/s should be of either the codirectional or the contradirectional type specified in Recommendation G.703. The specifications for 64 kbit/s interfaces are not mandatory for channel associated signalling.

7 Jitter

7.1 *Multiplex signal output jitter at 8448 kbit/s output*

In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 8448 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 400$ kHz.

7.2 *Jitter at 64 kbit/s output* (for interfaces according to Rec. G.703)

7.2.1 In the case where the incoming 8448 kbit/s signal has no jitter, the peak-to-peak jitter at the 64 kbit/s output should not exceed 0.025 UI when it is measured within the frequency range from $f_1 = 20$ Hz to $f_4 = 10$ kHz. The equivalent binary content of the test signal applied to the 8448 kbit/s input shall be a pseudo-random bit sequence of length $2^{15}-1$ as specified in Recommendation O.151.

Note – In order to carry out this measurement without invoking AIS at the 64 kbit/s output, it will normally be necessary to include a frame alignment signal in the test signal.

7.2.2 The jitter transfer function between the 8448 kbit/s input and the 64 kbit/s output is under study.

Recommendation G.745

SECOND ORDER DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 8448 kbit/s AND USING POSITIVE/ZERO/NEGATIVE JUSTIFICATION

(Geneva, 1976; amended at Geneva, 1980 and at Melbourne, 1988)

1 General

The second order digital multiplex equipment using positive/zero/negative justification, considered below, is intended for use on digital paths between countries using 2048 kbit/s primary multiplex equipments, such as the PCM multiplex equipment described in Recommendation G.732 or any identical equipment.

2 Bit rate

The nominal bit rate should be 8448 kbit/s. The tolerance on that rate should be ± 30 parts per million (ppm).

3 Frame structure

Table 1/G.745 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the bunched frame alignment signal.

4 Loss and recovery of frame alignment and consequent action

Loss of frame alignment should be assumed to have taken place when five consecutive frame alignment signals have been incorrectly received in their predicted positions.

Recovery of frame alignment should take place in the case of receiving without errors at least two consecutive frame signals in their predicted positions.

As soon as frame alignment has been lost and until it has been recovered, a definite pattern should be sent to all tributaries from the output of the demultiplexer. The equivalent binary content of this pattern, called the Alarm Indication Signal (AIS), at 2048 kbit/s is a continuous stream of binary 1s.

5 Multiplexing method

Cyclic bit interleaving in the tributary numbering order and positive/zero/negative justification with two-command control are recommended.

The justification control signal should be distributed and use the C_{jn}-bits ($n = 1, 2, 3$, see Table 1/G.745). Correction of one error in command is possible.

Positive justification should be indicated by the signal 111, transmitted in each of two consecutive frames; negative justification should be indicated by the signal 000 transmitted in each of two consecutive frames, and no justification by the signal 111 in one frame followed by 000 in the next frame. Bits 5, 6, 7 and 8 in Set IV (see Table 1/G.745) are used for negative justification of tributaries 1, 2, 3 and 4 respectively, and bits 9 to 12 for positive justification of the same tributaries.

Besides, when information from tributaries 1, 2, 3 and 4 is not transmitted, bits 5, 6, 7 and 8 in Set IV are available for transmitting information concerning the type of justification (positive or negative) in frames containing commands of positive justification control and intermediate amount of jitter in frames containing commands of negative justification.

Table 1/G.745 gives the maximum justification rate per tributary.

6 Jitter

The amount of jitter that should be tolerated at the input of the multiplexer and the demultiplexer should be according to Rec. G.823, § 3.1.1. The amount of jitter at the output of the multiplexer and the demultiplexer should be studied and specified.

7 Digital interface

The digital interfaces at 2048 kbit/s and 8448 kbit/s should be in accordance with Recommendation G.703.

8 Timing signal

It might be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal one.

9 Service digits

Some spare bits per frame are available for service functions (bits from 5 to 8 in Set II and bit 8 in Set III) for national and international use. Bits 5, 6, 7 and 8 in Set II are available for a digital service channel between two terminals (using 32 kbit/s Adaptive Delta Modulation) and bit 8 in Set III is available for ringing up a digital service channel. Utilization of other spare bits is under study.

TABLE 1/G.745

8448-kbit/s digital multiplexing frame structure using positive/zero/negative justification

Tributary bit rate (kbit/s)	2048
Number of tributaries	4
Frame structure	Bit number
	Set I
Frame alignment signal (11100110)	1 to 8
Bits from tributaries	9 to 264
	Set II
Justification control bits C_{j1} (see Note)	1 to 4
Bits for service functions	5 to 8
Bits from tributaries	9 to 264
	Set III
Justification control bits C_{j2} (see Note)	1 to 4
Spare bits	5 to 8
Bits from tributaries	9 to 264
	Set IV
Justification control bits C_{j3} (see Note)	1 to 4
Bits from tributaries available for negative justification	5 to 8
Bits from tributaries available for positive justification	9 to 12
Bits from tributaries	12 to 264
Frame length	1056 bits
Frame duration	125 μs
Bits per tributary	256 bits
Maximum justification rate per tributary	8 kbit/s

Note – C_{jn} indicates *n*th justification control bit of the *j*th tributary.

10 Fault conditions and consequent actions

10.1 The digital multiplex equipment should detect the following fault conditions:

10.1.1 Failure of power supply.

10.1.2 Loss of incoming signal at 2048 kbit/s at the input of the multiplexer.

Note – When using separate circuits for the digital signal and the timing signal, loss of either or both should constitute loss of the incoming signal.

10.1.3 Loss of the incoming signal at 8448 kbit/s at the input of the demultiplexer.

Note 1 – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

Note 2 – When using separate circuits for the digital signal and the timing signal, loss of either or both should constitute loss of the incoming signal.

10.1.4 Loss of frame alignment.

10.1.5 Alarm indication received from the remote multiplex equipment at the 8448 kbit/s input of the demultiplexer (see § 10.2.2).

10.2 *Consequent actions*

After detection of a fault condition appropriate actions should be taken as specified in Table 2/G.745. The consequent actions are as follows:

10.2.1 Prompt maintenance alarm indication generated to designate that the performance is below acceptable standards and maintenance attention is required locally. When detecting the AIS at the 8448 kbit/s input of the demultiplexer, the prompt maintenance alarm indication associated with loss of frame alignment should be prohibited (see Note 1 below).

Note – The location and provision of any visual and/or audible alarm activated by this prompt maintenance alarm indication is left to the discretion of each Administration.

10.2.2 Alarm indication to the remote multiplex equipment generated by changing from the state 0 to the state 1 bit 7 of set III at the 8448 kbit/s output of the multiplexer.

10.2.3 AIS (see Note 2 below) applied to all the four 2048 kbit/s tributary outputs from the demultiplexer.

10.2.4 AIS (see Note 2 below) applied to the 8448 kbit/s output of the multiplexer.

10.2.5 AIS (see Note 2 below) applied to the time slots of the 8448 kbit/s signal at the multiplexer output corresponding to the relevant 2048 kbit/s tributary.

Note 1 – The bit rate of the AIS at the output of the corresponding demultiplexer should be as specified for the tributaries. The method of achieving this is under study.

Note 2 – The equivalent binary content of the AIS at 2048 kbit/s and 8448 kbit/s is a continuous stream of binary 1s.

TABLE 2/G.745

Fault conditions and consequent actions

Equipment part	Fault condition (see § 10.1)	Consequent actions (see § 10.2)				
		Prompt maintenance alarm indication generated	Alarm indication to the remote multiplexer generated	AIS applied		
				To all the tributaries	To the composite signal	To the relevant time slots of the composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes, si practicable	Yes, si practicable	Yes, si practicable	
Multiplexer only	Loss of incoming signal on a tributary	Yes				Yes
Demultiplexer only	Loss of incoming signal at 8448 kbit/s	Yes	Yes	Yes		
	Loss of frame alignment	Yes	Yes	Yes		
	AIS received from the remote multiplexer					

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

CHARACTERISTICS OF SECOND ORDER PCM MULTIPLEX EQUIPMENT OPERATING AT 6312 kbit/s

(Malaga-Torremolinos, 1984)

1 General characteristics

1.1 *Fundamental characteristics*

The encoding law used is the μ-law as specified in Recommendation G.711. The sampling rate, load capacity and the code are also specified in that Recommendation.

The number of quantized values is 255. Two character signals are reserved for zero value (11111111 and 01111111).

In some networks the all 0 character signal (00000000) is eliminated to avoid loss of timing information to the digital line, resulting in 254 quantized values.

1.2 *Bit rate*

The nominal bit rate is 6312 kbit/s. The tolerance on this rate is ± 30 parts per million (ppm).

1.3 *Timing signal*

It should be possible to derive the transmitting timing signal of a PCM multiplex equipment from an internal source, from the incoming digital signal and also from an external source.

2 Frame structure

Refer to §§ 3.2.1 and 3.2.2 of Recommendation G.704 for frame structure and use of derived channel time slots.

3 Loss and recovery of frame alignment

The strategy for the loss and recovery of frame alignment should be according to Rec. G.706, § 3.1.

4 Fault conditions and consequent actions

4.1 *Fault conditions*

The PCM multiplex equipment should detect the following conditions:

4.1.1 Failure of power supply.

4.1.2 Loss of incoming signals at 6312 kbit/s.

4.1.3 Loss of frame alignment.

4.1.4 Alarm indication received from the remote PCM multiplex equipment.

4.2 *Consequent actions*

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 1/G.746. The consequent actions are as follows:

4.2.1 A service alarm indication should be generated to signify that the service provided by the PCM multiplex is no longer available. This indication should be forwarded to the switching and/or signalling equipment depending upon the arrangement provided.

TABLE 1/G.746

Fault conditions and consequent actions for the PCM multiplex equipment

Equipment part	Fault condition	Consequent actions			
		Service alarm indication generated	Prompt maintenance alarm indication generated	Alarm indication to the remote end generated	Transmission suppressed at the analogue outputs
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes	Yes (if practicable)	Optional
Demultiplexer only	Loss of incoming signals at 6312 kbit/s	Yes	Yes	Yes	Yes
	Loss of frame alignment	Yes	Yes	Yes	Yes
	Alarm indication received from the remote end	Optional	Yes		Optional

Note 1 – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 2 – Indications of additional fault conditions, such as codec failure and excessive bit errors, are left to the discretion of individual Administrations.

4.2.2 The service alarm described in § 4.2.1 above should be used to automatically remove the associated circuits from service and to restore them to service when frame alignment has been recovered.

Note – The removal of the associated circuits described in § 4.2.2 above should be done in such a way that the circuits are not needlessly removed in the case of a brief isolated loss of frame alignment but are removed in the case of a permanent or intermittent loss of frame alignment.

It is also important to minimize the impact of signalling errors which may occur during periods of loss of frame alignment. These functions should be provided in the PCM multiplex equipment or in the switching/signalling equipment.

4.2.3 A prompt maintenance alarm indication should be generated to signify that performance is below acceptable standards and maintenance attention is required locally.

4.2.4 An alarm indication to the remote end should be generated by forcing bit a to the value 1.

4.2.5 Transmission should be suppressed at the analogue outputs.

4.2.6 *Rapid indication of loss of frame alignment*

An indication should be given to the Signalling System No. 6 equipment (digital version) when the PCM multiplex equipment (local end only) detects a loss of frame alignment. The average time to detect and give an indication of random bits in the frame alignment signal bit positions should not be greater than 3 ms. This indication will serve the same function as that provided by the data carrier failure alarm in the analogue version (see Recommendation Q.275 [1]).

5 Signalling

5.1 *Signalling arrangement*

Refer to § 3.2.3 of Recommendation G.704.

5.2 *Loss of multiframe alignment in case of channel associated signalling*

Loss of multiframe alignment is assumed to have taken place when loss of frame alignment occurs.

6 Interfaces

Analogue: Refer to Recommendations G.712, G.713 and G.714.

Digital: Refer to Recommendation G.703.

Reference

[1] CCITT Recommendation *Data channel failure detection*, Vol. VI, Rec. Q.275.

Recommendation G.747

SECOND ORDER DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 6312 kbit/s AND MULTIPLEXING THREE TRIBUTARIES AT 2048 kbit/s

(Melbourne, 1988)

1 General

The digital multiplex equipment described in this Recommendation is intended for use between networks using different digital hierarchies as specified in Recommendations G.702 and G.802.

2 Bit rate

The bit rates of the tributary and multiplex signals should be 2048 kbit/s ± 50 ppm and 6312 kbit/s ± 30 ppm, respectively, as specified in Recommendation G.703.

3 Frame structure

Table 1/G.747 gives the recommended 6312 kbit/s multiplexing frame structure.

4 Loss and recovery of frame alignment and consequent action

Loss of frame alignment should be assumed to have taken place when four consecutive frame alignment signals have been incorrectly received in their predicted positions.

When frame alignment is assumed to be lost, the frame alignment device should decide that such alignment has effectively been recovered when it detects the presence of three consecutive correct frame alignment signals.

The frame alignment device, having detected the appeareance of a single correct frame alignment signal, should begin a new search for the frame alignment signal when it detects the absence of the frame alignment signal in one of the two following frames.

Note – As it is not strictly necessary to specify the detailed frame alignment strategy, any suitable frame alignment strategy may be used provided the performance achieved is at least as efficient in all respects as that obtained by the above frame alignment strategy.

5 Multiplexing and justification methods

Cyclic bit interleaving in the tributary numbering order and positive justification are recommended.

The justification control signal should be distributed and use the C_{ji}-bits ($j = 1, 2, 3$; $i = 1, 2, 3$) (see Note 5 to Table 1/G.747).

Positive justification should be indicated by the justification control signal 111 and no justification by the signal 000. Majority decision is recommended.

Table 1/G.747 gives the maximum justification rate per tributary and the nominal justification ratio.

TABLE 1/G.747

6312 kbit/s multiplexing frame structure

Nominal tributary bit rate (kbit/s)	2048
Number of tributaries	3
Frame structure	Bit number
	Set I
Frame alignment signal (111010000)	1 to 9
Bits from tributaries	10 to 168
	Set II
Alarm indication to the remote multiplex equipment (Note 1)	1
Parity bit (Notes 2 and 3)	2
Bit reserved for future use (Note 4)	3
Bits from tributaries	4 to 168
	Set III
Justification control bits C_{j1} (Note 5)	1 to 3
Bits from tributaries	4 to 168
	Set IV
Justification control bits C_{j2} (Note 5)	1 to 3
Bits from tributaries	4 to 168
	Set V
Justification control bits C_{j3} (Note 5)	1 to 3
Bits from tributaries available for justification	4 to 6
Bits from tributaries	7 to 168
Frame length	840 bits
Bits per tributary in a frame	273 bits
Maximum justification rate per tributary	7.5 kbit/s
Nominal justification ratio	0.453

Note 1 – See § 10.2.1.

Note 2 – The parity bit = 1 if the number of marks in all tributary bits including the bits in the justifiable time-slots in the preceding frame is odd; the parity bit = 0 if the number of marks in all tributary bits including the bits in the justifiable time-slots in the preceding frame is even.

Note 3 – The implementation and the use of this parity bit procedure are for further study.

Note 4 – This bit should be set to 1 when not used.

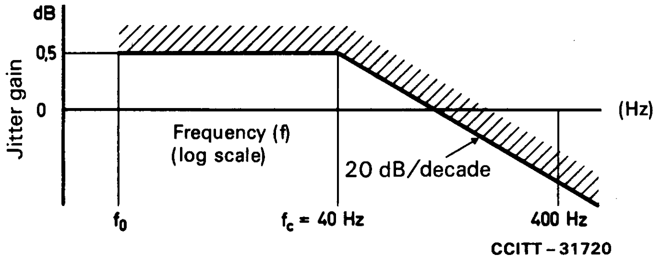
Note 5 – C_{ji} ($j = 1, 2, 3$; $i = 1, 2, 3$) indicates the ith justification control bit of the jth tributary.

6 jitter

6.1 *Muldex jitter transfer characteristic*

A 2048 kbit/s signal, modulated by sinusoidal jitter, should be subject to a muldex jitter transfer characteristic within the gain/frequency limits given in Figure 1/G.747. The equivalent binary content of the test signal should be 1000.

Note – In addition, the need to specify a demultiplexer tributary jitter transfer characteristic from the 6312 kbit/s demultiplexer input to the 2048 kbit/s demultiplexer output is for further study.



Note – The frequency f_0 should be as low as possible, taking into account the limitations of measuring equipment. In any case, f_0 should be no greater than 10 Hz. The selective measurement method should be used.

FIGURE 1/G.747

Muldex jitter transfer characteristic

6.2 *Output jitter*

6.2.1 *Tributary output jitter*

With no jitter applied to the input ports of the multiplexer and with the multiplexer directly connected to the demultiplexer, the peak-to-peak jitter at the tributary output port should not exceed 0.2 UI over a measurement interval of one minute in the frequency range from f_0 to 100 kHz (see Note 1).

When measured with an instrument incorporating a bandpass filter having a lower cutoff frequency of 18 kHz, a roll-off of 20 dB/decade and an upper limit of 100 kHz, the peak-to-peak output jitter should not exceed 0.05 UI when measured over a one minute interval (see Note 2).

Note 1 - The frequency f_0 should be as low as possible, taking into account the limitations of measurement equipment. In any case f_0 should be no greater than 10 Hz.

Note 2 – For interfaces meeting the national high Q option, detailed in Recommendation G.823, the lower cutoff frequency for the above measurement should be 700 Hz.

6.2.2 *Multiplexer output jitter*

The peak-to-peak jitter at the 6312 kbit/s output port should not exceed 0.05 UI when it is measured over a one minute interval within the frequency range from f_1 = 10 Hz to f_4 = 60 kHz.

6.3 *Input jitter*

6.3.1 *Tributary input jitter*

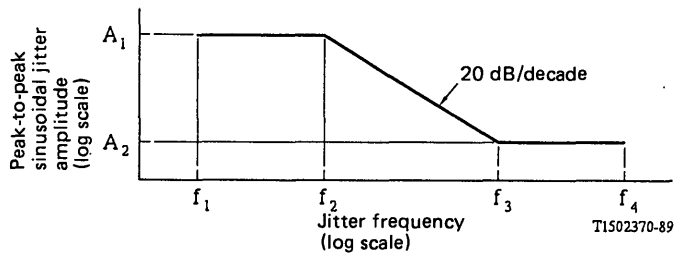
The 2048 kbit/s input port should be capable of accommodating levels of input jitter up to the limits given in Rec. G.823.

6.3.2 *Demultiplexer input jitter*

The 6312 kbit/s input port should be capable of accommodating levels of input jitter up to the limits given in Figure 2/G.747.

Note 1 – Current Recommendation G.703 does not refer to the jitter tolerated at the digital distribution frame at 6312 kbit/s nor at the input port of equipment connected to this distribution frame.

Note 2 – The jitter accommodation requirement should be met when the jittered input signal is composed of the multiplexed tributary signals having any value of jitter allowed for the 2048 kbit/s.



Peak-to-peak sinusoidal jitter amplitude		Frequency			
A_1 (UI)	A_2 (UI)	f_1 (Hz)	f_2 (Hz)	f_3 (kHz)	f_4 (kHz)
5.0	0.15	10	120	4	60

FIGURE 2/G.747

Lower limit of maximum tolerable sinusoidal input jitter at 6312 kbit/s

7 Digital interfaces

The digital interfaces at 2048 kbit/s and 6312 kbit/s should be in accordance with Recommendation G.703.

8 Timing signal

If it is economically feasible, it may be desirable to be able to derive the multiplexing timing signal from an external source as well as from an internal source.

9 Service digits

Three bits per frame are available for service functions (see Table 1/G.747): bit 1 of Set II is used to transmit an alarm indication to the remote multiplex equipment when specific fault conditions are detected in the multiplex equipment (see § 10 below); bit 2 of Set II may be used for a parity check; bit 3 of Set II is reserved for future use.

10 Fault conditions and consequent actions

10.1 *Fault conditions*

10.1.1 The digital multiplex equipment should detect the following fault conditions:

1) failure of power supply;
2) loss of an incoming 2048 kbit/s tributary signal at a multiplexer input port;
3) loss of an incoming 6312 kbit/s multiplex signal at a demultiplexer input port;
4) loss of frame alignment signal at a demultiplexer input port;
5) detection of an alarm indication received from the remote multiplex equipment at a demultiplexer input port;
6) detection of alarm indication signal (AIS) at a demultiplexer input port.

Note 1 – The equivalent binary content of the AIS at 2048 and 6312 kbit/s should be a continuous stream of binary 1s (marks) as recommended in Recommendation M.20.

Note 2 – Some current 44 736/6312 kbit/s demultiplexers do not issue a 6312 kbit/s AIS. Thus no detection can take place in that case.

Note 3 – The strategy for detecting the presence of the AIS should be such that the AIS is detectable even in the presence of an error ratio of $1 \cdot 10^{-3}$. However, a signal with all bits except the frame alignment signal in the state of 1 should not be mistaken as an AIS.

10.1.2 The need to monitor the degradation of the incoming 6312 kbit/s signal for the purpose of end-to-end error performance monitoring of the 6132 kbit/s digital block as well as the procedure for detecting such degradation, are for further study.

10.2 *Consequent actions*

Further to the detection of a fault condition, the appropriate actions should be taken as specified in Table 2/G.747.

Note 1 – The concept and definition of prompt maintenance alarm indication is given in Recommendation M.20.

Note 2 – When the alarm indication signal (AIS) is detected at the input of the demultiplexer, the prompt maintenance alarm indication associated with loss of frame alignment should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 2/G.747 with the fault condition.

10.2.1 Alarm indication to the remote multiplex equipment should be generated by changing bit 1 of Set II (see Table 1/G.747) from the state 0 to the state 1.

10.2.2 AIS should be applied to the following as specified in Table 2/G.747.

- all three 2048 kbit/s tributary outputs from the demultiplexer;
- 6312 kbit/s output of the multiplexer;
- the time slots of the 6312 kbit/s signal at the ouptput of the multiplexer, corresponding to the relevant 2048 kbit/s tributary.

TABLE 2/G.747

Fault conditions and consequent actions

Equipment part	Fault condition (see § 10.1)	Consequent actions (see § 10.2)				
		Prompt maintenance alarm indication generated	Alarm indication to the remote multiplex equipment generated	AIS applied		
				To all the tributaries	To the composite signal	To the relevant time slots of the composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes		Yes, if practicable	Yes, if practicable	
Multiplexer only	Loss of incoming signal on a tributary	Yes				Yes
Demultiplexer only	Loss of incoming signal at 6312 kbit/s	Yes	Yes	Yes		
	Loss of frame alignment	Yes	Yes	Yes		
	Alarm indication received from the remote multiplex equipment					

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

7.5 Principal characteristics of higher order multiplex equipments

Recommendation G.751

DIGITAL MULTIPLEX EQUIPMENTS OPERATING AT THE THIRD ORDER BIT RATE OF 34 368 kbit/s AND THE FOURTH ORDER BIT RATE OF 139 264 kbit/s AND USING POSITIVE JUSTIFICATION

(Geneva, 1976; further amended)

1 General characteristics

1.1 There should be a 4th-order bit rate of 139 264 kbit/s in the digital hierarchy which is based on the 2nd-order bit rate of 8448 kbit/s.

There should be two methods of achieving the 4th-order bit rate:

Method 1 – by using a 3rd-order bit rate of 34 368 kbit/s in the digital hierarchy.

Method 2 – by directly multiplexing sixteen digital signals at 8448 kbit/s.

The digital signals at the bit rate of 139 264 kbit/s obtained by these two methods should be identical.

1.2 The existence of the above two methods implies that the use of the bit rate of 34 368 kbit/s should not be imposed on an Administration that does not wish to realize the corresponding equipment.

1.3 In accordance with the above two methods, the following realizations of digital multiplex equipments using positive justification are recommended:

Method 1 – Realization by separate digital multiplex equipments: one type which operates at 34 368 kbit/s and multiplexes four digital signals at 8448 kbit/s; the other type which operates at 139 264 kbit/s and multiplexes four digital signals at 34 368 kbit/s.

The multiplexing for the 34 368 kbit/s digital multiplex equipment is recommended in § 1.4 below, while further specification of this equipment is given in § 2 below.

The multiplexing for the 139 264 kbit/s digital multiplex equipment is recommended in § 1.5 below, while further specification of this equipment is given in § 3 below.

Method 2 – Realization by a single digital multiplex equipment which operates at 139 264 kbit/s and multiplexes sixteen digital signals at 8448 kbit/s.

The digital multiplexing for the 139 264 kbit/s bit rate should be achieved by multiplexing, in accordance with § 1.5 below, four digital signals at 34 368 kbit/s, each of which is obtained by multiplexing, in accordance with § 1.4 below, four digital signals at 8448 kbit/s. Further specification of this equipment is given in § 4 below.

1.4 *Multiplexing four digital signals at 8448 kbit/s*

1.4.1 *Bit rate*

The nominal bit rate should be 34 368 kbit/s.

The tolerance on that rate should be ± 20 parts per million (ppm).

1.4.2 *Frame structure*

Table 1/G.751 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the bunched frame alignment signal.

TABLE 1/G.751

34 368 kbit/s multiplexing frame structure

Tributary bit rate (kbit/s)	8448
Number of tributaries	4
Frame structure	Bit number
	Set I
Frame alignment signal (1111010000)	1 to 10
Alarm indication to the remote digital multiplex equipment	11
Bit reserved for national use	12
Bits from tributaries	13 to 384
	Set II
Justification service bits C_{j1} (see Note)	1 to 4
Bits from tributaries	5 to 384
	Set III
Justification service bits C_{j2} (see Note)	1 to 4
Bits from tributaries	5 to 384
	Set IV
Justification service bit C_{j3} (see Note)	1 to 4
Bits from tributaire available for justification	5 to 8
Bits from tributaries	9 to 384
Frame length	1536 bits
Bits per tributary	378 bits
Maximum justification rate per tributary	22 375 kbit/s
Nominal justification ratio	0.436

Note – C_{jn} indicates the *n*th justification service bit of the *j*th tributary.

1.4.3 *Loss and recovery of frame alignment*

Loss of frame alignment should be assumed to have taken place when four consecutive frame alignment signals have been incorrectly received in their predicted positions.

When frame alignment is assumed to be lost, the frame alignment device should decide that such alignment has effectively been recovered when it detects the presence of three consecutive frame alignment signals.

The frame alignment device having detected the appearance of a single correct frame alignment signal, should begin a new search for the frame alignment signal when it detects the absence of the frame alignment signal in one of the two following frames.

Note – As it is not strictly necessary to specify the detailed frame alignment strategy, any suitable frame alignment strategy may be used provided the performance achieved is at least as efficient in all respects as that obtained by the above frame alignment strategy.

1.4.4 *Multiplexing method*

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended. The justification control signal should be distributed and use the C_{jn}-bits (n = 1, 2, 3, see Table 1/G.751). Positive justification should be indicated by the signal 111, no justification by the signal 000. Majority decision is recommended.

Table 1/G.751 gives the maximum justification rate per tributary and the nominal justification ratio.

1.4.5 *Service digits*

Two bits per frame are available for service functions. Bit 11 of Set I is used to transmit an alarm indication to the remote multiplex equipment when specific fault conditions are detected in the multiplex equipment (see §§ 2.5 and 4.5 below). Bit 12 of Set I is reserved for national use. On a digital path crossing the border, this bit is fixed at 1.

1.5 *Multiplexing four digital signals at 34 368 kbit/s*

1.5.1 *Bit rate*

The nominal bit rate should be 139 264 kbit/s. The tolerance on that rate should be ± 15 parts per million (ppm).

1.5.2 *Frame structure*

Table 2/G.751 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the bunched frame alignment signal.

1.5.3 *Loss and recovery of frame alignment*

Loss of frame alignment should be assumed to have taken place when four consecutive frame alignment signals have been incorrectly received in their predicted positions.

When frame alignment is assumed to be lost, the frame alignment device should decide that such alignment has effectively been recovered when it detects the presence of three consecutive frame alignment signals.

The frame alignment device having detected the appearance of a single correct frame alignment signal, should begin a new search for the frame alignment signal when it detects the absence of the frame alignment signal in one of the two following frames.

Note – As it is not strictly necessary to specify the detailed frame alignment strategy, any suitable frame alignment strategy may be used provided the performance achieved is at least as efficient in all respects as that obtained by the above frame alignment strategy.

1.5.4 *Multiplexing method*

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended. The justification control signal should be distributed and use the C_{jn}-bits (n = 1, 2, 3, 4, 5, see Table 2/G.751). Positive justification should be indicated by the signal 11111, no justification by the signal 00000. Majority decision is recommended.

Table 2/G.751 gives the minimum justification rate per tributary and the nominal justification ratio.

TABLE 2/G.751

139 264 kbit/s multiplexing frame structure

Tributary bit rate (kbit/s)	34 368
Number of tributaries	4
Frame structure	Bit number
	Set I
Frame alignment signal (111110100000)	1 to 12
Alarm indication to the remote digital multiplex equipment	13
Bits reserved for national use	14 to 16
Bits from tributaries	17 to 488
	Sets II to V
Justification service bits C_{jn} (n = 1 to 4) (see Note)	1 to 4
Bits from tributaries	5 to 488
	Set VI
Justification service bits C_{j5} (see Note)	1 to 4
Bits from tributaries available for justification	5 to 8
Bits from tributaries	9 to 488
Frame length	2928 bits
Bits per tributary	723 bits
Maximum justification rate per tributary	47 563 bit/s approx.
Nominal justification ratio	0.419

Note – C_{jn} indicates the nth justification service bit of the jth tributary.

1.5.5 *Service digits*

Four bits per frame are available for service functions. Bit 13 of Set I is used to transmit an alarm indication to the remote multiplex equipment when specific fault conditions are detected in the multiplex equipment (see §§ 3.5 and 4.5 below). Bits 14 to 16 of Set I are reserved for national use. On a digital path crossing the border, these bits are fixed at 1.

2 Digital multiplex equipment operating at 34 368 kbit/s and multiplexing four tributaries at 8448 kbit/s

2.1 *Multiplexing*

The multiplexing for the 34 368 kbit/s bit rate should be in accordance with § 1.4.

2.2 *Digital interfaces*

The digital interfaces at 8448 kbit/s and 34 368 kbit/s should be in accordance with Recommendation G.703.

2.3 *Jitter*

2.3.1 *Jitter transfer characteristic*

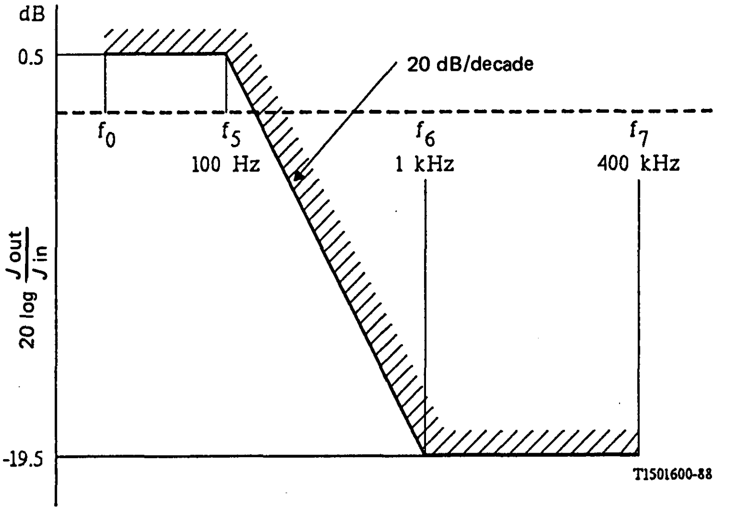
An 8448 kbit/s signal, modulated by sinusoidal jitter, should be subject to a muldex jitter transfer characteristic within the gain/frequency limits given in Figure 1/G.751. The equivalent binary content of the test signal should be 1000.

2.3.2 *Tributary output jitter*

The peak-to-peak jitter at a tributary output in the absence of input jitter should not exceed 0.25 UI when measured in the frequency range up to 400 kHz.

When measured with an instrument incorporating a bandpass filter having a lower cutoff frequency of 3 kHz, a rolloff of 20 dB/decade and an upper limit of 400 kHz, the peak-to-peak output jitter should not exceed 0.05 UI with a probability of 99.9% during a measurement period of 10 s.

Note – For interfaces meeting the national low Q option detailed in Recommendation G.703, the lower cutoff frequency for the above measurement should be 80 kHz.



Note 1 – The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 – To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

Note 3 – The need to tolerate spurious responses greater than – 19.5 dB in the frequency range f_6 to f_7 is for further study.

FIGURE 1/G.751

2.3.3 *Multiplex signal output jitter*

In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 34 368 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from f_1 = 100 Hz to f_4 = 800 kHz.

2.4 *Timing signal*

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal source.

2.5 *Fault conditions, and consequent actions*

2.5.1 *Fault conditions*

The digital multiplex equipment should detect the following fault conditions:

2.5.1.1 Failure of power supply.

2.5.1.2 Loss of an incoming signal at 8448 kbit/s at the input of the multiplexer.

Note – Where separate circuits are used for the digital signal and the timing signal then loss of either or both should constitute loss of the incoming signal.

2.5.1.3 Loss of the incoming signal at 34 368 kbit/s at the input of the demultiplexer.

Note – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

2.5.1.4 Loss of frame alignment.

2.5.1.5 Alarm indication received from the remote multiplex equipment at the 34 368 kbit/s input of the demultiplexer (see § 2.5.2.2 below).

2.5.2 *Consequent actions*

Further to detection of a fault condition, actions should be taken as specified by Table 3/G.751. The consequent actions are as follows:

2.5.2.1 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the Alarm Indication Signal (AIS) (see Note 2 under § 2.5.2.5) at 34 368 kbit/s is detected at the input of the demultiplexer, the prompt maintenance alarm indication associated with loss of frame alignment should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 3/G.751 with the fault condition.

Note – The location and provision of any visual and/or audible alarm activated by this maintenance alarm indication is left to the discretion of each Administration.

2.5.2.2 Alarm indication to the remote multiplex equipment generated by changing from the state 0 to the state 1 bit 11 of Set I at the 34 368 kbit/s output of the multiplexer.

2.5.2.3 AIS (see Notes 1 and 2 below) applied to all four 8448 kbit/s tributary outputs from the demultiplexer.

2.5.2.4 AIS (see Notes 1 and 2 below) applied to the 34 368 kbit/s output of the multiplexer.

2.5.2.5 AIS (see Note 2 below) applied to time slots of the 34 368 kbit/s signal at the output of the multiplexer, corresponding to the relevant 8448 kbit/s tributary.

The method of transmitting the AIS at the output port of the multiplexer in time slots corresponding to a faulty input tributary should be such that the status of the justification control digits is controlled so as to ensure that the AIS is within the tolerance specified for that tributary.

Note 1 – The bit rate of the AIS at the output of the multiplexer equipment or at the output of the demultiplexer equipment should be in accordance with the interface specifications.

Note 2 – The equivalent binary content of the AIS (AIS) at 8448 kbit/s and 34 368 kbit/s is nominally a continuous stream of 1s. The strategy for detecting the presence of the AIS should be such that the AIS is detectable even in the presence of an error ratio $1 \cdot 10^{-3}$. However a signal with all bits except the frame alignment signal in the 1 state, should not be mistaken as an AIS.

2.5.3 *Time requirements*

The fault detection and the application of the consequent actions given in §§ 2.5.2.2 to 2.5.2.5, including the detection of AIS, should be completed within a time limit of 1 ms.

TABLE 3/G.751

Fault conditions and consequent actions

Equipment part	Fault condition (see §§ 2.5.1 or 3.5.1)	Consequent actions (see §§ 2.5.2 or 3.5.2)				
		Prompt maintenance alarm indication generated	Alarm indication to the remote multiplex equipment generated	AIS applied		
				To all the tributaries	To the composite signal	To the relevant time slots of the composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes		Yes, if practicable	Yes, if practicable	
Multiplexer only	Loss of incoming signal on a tributary	Yes				Yes
Demultiplexer only	Loss of incoming signal	Yes	Yes	Yes		
	Loss of frame alignment	Yes	Yes	Yes		
	Alarm indication received from the remote multiplex equipment					

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

3 Digital multiplex equipment operating at 139 264 kbit/s and multiplexing four tributaries at 34 368 kbit/s

3.1 *Multiplexing*

The multiplexing for the 139 264 kbit/s bit rate should be in accordance with § 1.5 above.

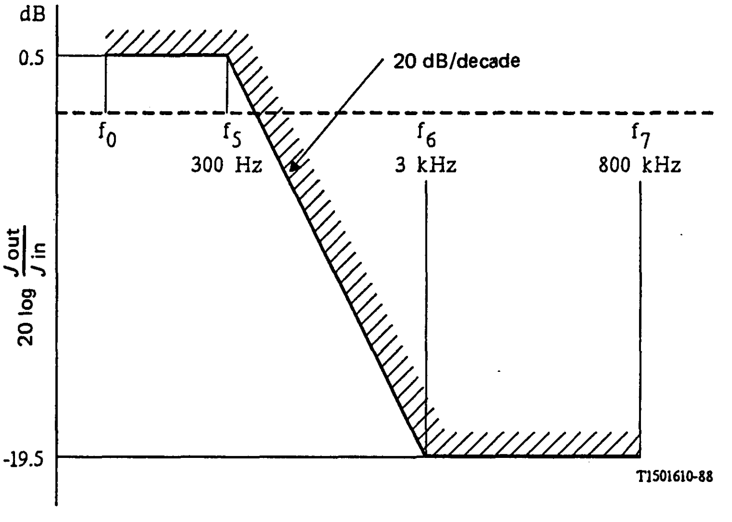
3.2 *Digital interfaces*

The digital interfaces at 34 368 kbit/s and 139 264 kbit/s should be in accordance with Recommendation G.703.

3.3 *Jitter*

3.3.1 *Jitter transfer characteristic*

A 34 368 kbit/s signal, modulated by sinusoidal jitter, should be subject to a muldex jitter transfer characteristic within the gain/frequency limits given in Figure 2/G.751. The equivalent binary content of the test signal should be 1000.



Note 1 – The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 – To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

Note 3 – The need to tolerate spurious responses greater than –19.5 dB in the frequency range f_6 to f_7 is for further study.

FIGURE 2/G.751

3.3.2 *Tributary output jitter*

The peak-to-peak jitter at a tributary output in the absence of input jitter should not exceed 0.3 UI when measured in the frequency range up to 800 kHz.

When measured with an instrument incorporating a bandpass filter having a lower cutoff frequency of 10 kHz, a rolloff of 20 dB/decade and an upper limit of 800 kHz, the peak-to-peak output jitter should not exceed 0.05 UI with a probability of 99.9% during a measurement period of 10 s.

3.3.3 *Multiplex signal output jitter*

In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 139 264 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from f_1 = 200 Hz to f_4 = 3500 kHz.

3.4 *Timing signal*

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from internal source.

3.5 *Fault conditions and consequent actions*

3.5.1 *Fault conditions*

The digital multiplex equipment should detect the following fault conditions:

3.5.1.1 Failure of power supply.

3.5.1.2 Loss of an incoming signal at 34 368 kbit/s at the input of the multiplexer.

3.5.1.3 Loss of the incoming signal at 139 264 kbit/s at the input of the demultiplexer.

Note – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

3.5.1.4 Loss of frame alignment.

3.5.1.5 Alarm indication received from the remote multiplex equipment at the 139 264 kbit/s input of the demultiplexer (see § 3.5.2.2 below).

3.5.2 *Consequent actions*

Further to detection of a fault condition actions should be taken as specified by Table 3/G.751. The consequent actions are as follows:

3.5.2.1 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the Alarm Indication Signal (AIS) (see Note 2 below) at 139 264 kbit/s is detected at the input to the demultiplexer, the prompt maintenance alarm indication associated with loss of frame alignment should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 3/G.751 with the fault condition.

3.5.2.2 Alarm indication to the remote multiplex equipment generated by changing from the state 0 to the state 1 bit 13 of Set I at the 139 264 kbit/s output of the multiplexer.

3.5.2.3 AIS (see Notes 1 and 2 below) applied to all four 34 368 kbit/s tributary outputs from the demultiplexer.

3.5.2.4 AIS (see Notes 1 and 2 below) applied to the 139 264 kbit/s output of the multiplexer.

3.5.2.5 AIS (see Note 2 below) applied to time slots of the 139 264 kbit/s signal at the output of the multiplexer corresponding to the relevant 34 368 kbit/s tributary.

The method of transmitting the AIS at the output port of the multiplexer in time slots corresponding to a faulty input tributary should be such that the status of the justification control digits is controlled so as to ensure that the AIS is within the tolerance specified for the tributary.

Note 1 – The bit rate of the AIS at the output of the multiplexer equipment or at the output of the demultiplexer equipment should be in accordance with the interface specifications.

Note 2 – The equivalent binary content of the AIS at 34 368 kbit/s and 139 264 kbit/s is nominally a continuous stream of 1s. The strategy for detecting the presence of the AIS should be such that the AIS is detectable even in the presence of an error ratio $1 \cdot 10^{-3}$. However a signal, with all bits except the frame alignment signal in the 1 state, should not be mistaken for an AIS.

3.5.3 *Time requirements*

The fault detection and the application of the consequent actions given in §§ 3.5.2.2 to 3.5.2.5, including the detection of AIS, should be completed within a time limit of 1 ms.

4 Digital multiplex equipment operating at 139 264 kbit/s and multiplexing sixteen tributaries at 8448 kbit/s

4.1 *Multiplexing*

The multiplexing for the 139 264 kbit/s bit rate should be achieved by multiplexing, in accordance with § 1.5 above, four digital signals at 34 368 kbit/s, each of which is obtained by multiplexing, in accordance with § 1.4 above, four digital signals at 8448 kbit/s.

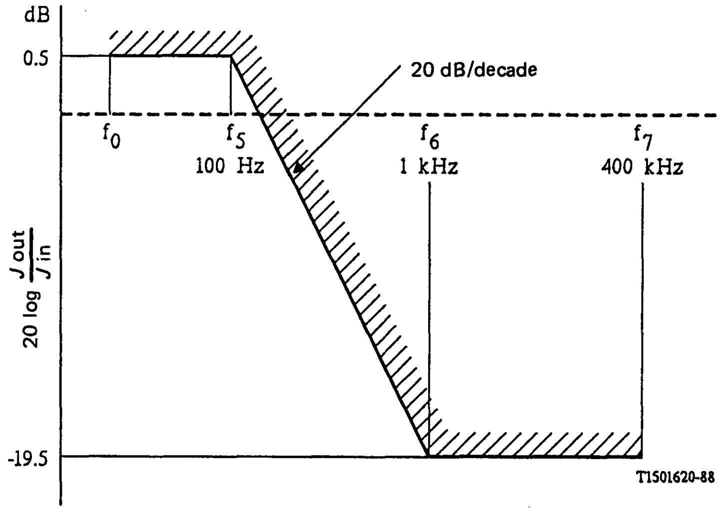
4.2 *Digital interfaces*

The digital interfaces at 8448 kbit/s and 139 264 kbit/s should be in accordance with Recommendation G.703.

4.3 *Jitter*

4.3.1 *Jitter transfer characteristic*

A 8448 kbit/s signal, modulated by sinusoidal jitter, should be subject to a muldex jitter transfer characteristic within the gain/frequency limits given in Figure 3/G.751. The equivalent binary content of the test signal should be 1000.



Note 1 — The frequency f_0 should be less than 20 Hz and as low as possible (e.g. 10 Hz), taking into account the limitations of measuring equipment.

Note 2 — To achieve accurate measurements, the use of a selective method is recommended with a bandwidth sufficiently small referred to the relevant measurement frequency, but not wider than 40 Hz.

Note 3 — The need to tolerate spurious responses greater than −19.5 dB in the frequency range f_6 to f_7 is for further study.

FIGURE 3/G.751

4.3.2 *Tributary output jitter*

The peak-to-peak jitter at a tributary output in the absence of input jitter should not exceed 0.35 UI when measured in the frequency range up to 400 kHz.

When measured with an instrument incorporating a bandpass filter having a lower cutoff frequency of 3 kHz, a rolloff of 20 dB/decade and an upper limit of 400 kHz, the peak-to-peak output jitter should not exceed 0.05 UI with a probability of 99.9% during a measurement period of 10 s.

Note — For interfaces meeting the national low Q option, detailed in Recommendation G.703, the lower cutoff frequency for the above measurement should be 80 kHz.

4.3.3 *Multiplex signal output jitter*

In the case where the transmitting timing signal is derived from an internal oscillator, the peak-to-peak jitter at the 139 264 kbit/s output should not exceed 0.05 UI when it is measured within the frequency range from f_1 = 100 Hz to f_4 = 3500 kHz.

4.4 *Timing signal*

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal source.

4.5 *Fault conditions and consequent actions*

4.5.1 *Fault conditions*

The digital multiplex equipment should detect the following fault conditions:

4.5.1.1 Failure of power supply.

4.5.1.2 Loss of an incoming signal at 8448 kbit/s at the input of the multiplexer.

Note – Where separate circuits are used for the digital signal and the timing signal then loss of either or both should constitute loss of the incoming signal.

4.5.1.3 Loss of the incoming signal at 139 264 kbit/s at the input of the demultiplexer.

Note – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

4.5.1.4 Loss of frame alignment of the signal at 139 264 kbit/s at the input of the demultiplexer.

4.5.1.5 Loss of frame alignment of a signal at 34 368 kbit/s within the demultiplexer.

4.5.1.6 Alarm indication received from the remote multiplex equipment at the 139 264 kbit/s input of the demultiplexer (see § 4.5.2.2 below).

4.5.1.7 Alarm indication received from the remote multiplex equipment on a signal at 34 368 kbit/s within the demultiplexer (see § 4.5.2.3 below).

4.5.2 *Consequent actions*

Further to detection of a fault condition, actions should be taken as specified by Table 4/G.751. The consequent actions are as follows:

4.5.2.1 Prompt maintenance alarm indication generated to signify that performance is below acceptable standards and maintenance attention is required locally. When the Alarm Indication Signal (AIS) (see Note 2 below) at 139 264 kbit/s or 34 368 kbit/s is detected by the demultiplexer, the prompt maintenance alarm indication associated with the corresponding loss of frame alignment should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 4/G.751 with the fault condition.

Note – The location and provision of any visual and/or audible alarms activated by the maintenance alarm indication is left to the discretion of each Administration.

4.5.2.2 Alarm indication on the 139 264 kbit/s signal to the remote multiplex equipment generated by changing from the state 0 to the state 1 bit 13 of Set I at the 139 264 kbit/s output of the multiplexer.

4.5.2.3 Alarm indication on a 34 368 kbit/s signal to the remote multiplex equipment generated by changing from the state 0 to the state 1 bit 11 of Set I on the 34 368 kbit/s signal into the multiplexer.

4.5.2.4 AIS (see Notes 1 and 2 below) applied to all sixteen 8448 kbit/s tributary outputs from the demultiplexer.

4.5.2.5 AIS (see Notes 1 and 2 below) applied to all four 8448 kbit/s relevant tributary outputs from the demultiplexer.

4.5.2.6 AIS (see Notes 1 and 2 below) applied to the 139 264 kbit/s output of the multiplexer.

4.5.2.7 AIS (see Note 2 below) applied to the time slot of the 139 264 kbit/s at the output of the multiplexer, corresponding to the relevant 8448 kbit/s tributary.

The method of transmitting the AIS at the output port of the multiplexer in time slots corresponding to a faulty input tributary, should be such that the status of the justification control digits is controlled so as to ensure that the AIS is within the tolerance specified for that tributary.

Note 1 – The bit rate of the AIS at the output of the multiplexer equipment or at the output of the demultiplexer equipment should be in accordance with the interface specifications.

Note 2 – The equivalent binary content of the AIS at 8448 kbit/s, 34 368 kbit/s and 139 264 kbit/s is nominally a continuous stream of 1s. The strategy for detecting the presence of the AIS should be such that the AIS is detectable even in the presence of an error ratio $1 \cdot 10^{-3}$. However a signal with all bits except the frame alignment signal in the 1 state, should not be mistaken for an AIS.

4.5.3 *Time requirements*

The fault detection and the application of the consequent actions given in §§ 4.5.2.2 to 4.5.2.7, including the detection of AIS, should be completed within a time limit of 1 ms.

TABLE 4/G.751

Fault conditions and consequent actions

Equipment part	Fault condition (see § 4.5.1)	Consequent actions (see § 4.5.2)						
		Prompt maintenance alarm indication generated	Alarm indication on the 139 264 kbit/s signal to the remote multiplex equipment generated	Alarm indication on a 34 368 kbit/s signal to the remote multiplex equipment generated	AIS applied			
					To all the 16 tributaries at 8448 kbit/s at the output of the demultiplexer	To the 4 relevant tributaries at 8448 kbit/s at the output of the demultiplexer	To the composite signal at 139 264 kbit/s at the output of the multiplexer	To the relevant time slot of the composite signal
Multiplexer and demultiplexer	Loss of power supply	Yes			Yes, if practicable		Yes, if practicable	
Multiplexer only	Loss of incoming signal on a tributary	Yes						Yes
Demultiplexer only	Loss of incoming signal at 139 264-kbit/s	Yes	Yes		Yes			
	Loss of frame alignment on the 139 264 kbit/s signal	Yes	Yes		Yes			
	Alarm indication received from the remote multiplex equipment on the 139 264 kbit/s signal							
	Loss of frame alignment on a 34 368 kbit/s signal	Yes		Yes		Yes		
	Alarm indication received from the remote multiplex equipment on a 34 368-kbit/s signal							

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

CHARACTERISTICS OF DIGITAL MULTIPLEX EQUIPMENTS BASED ON A SECOND ORDER BIT RATE OF 6312 kbit/s AND USING POSITIVE JUSTIFICATION

(Geneva, 1976; amended at Geneva, 1980)

The CCITT,

considering

(a) that various third- and higher-order multiplex equipments exist due to the differing characteristics of networks and signal sources in those networks;

(b) that, although studies will continue with the aim of reducing the differences between various systems, the existing situation cannot be changed in the near future;

recommends the following

(1) when countries using 1544 kbit/s primary multiplex equipments, such as the PCM multiplex equipment according to Recommendation G.733 and second-order multiplex using 6312 kbit/s according to Recommendations G.743 and G.746, are planning digital paths requiring interconnection at higher bit rates they should, when practical, utilize third-order bit rates of either 32 064 kbit/s or 44 736 kbit/s. When countries using 32 064 kbit/s third-order multiplex equipments are planning digital paths requiring interconnection at higher bit rates, they should, when practical, utilize the fourth-order bit rate of 97 728 kbit/s.

For Figure 1/G.752 refer to Figure 1/G.702 for the basic multiplex arrangements recommended for Administrations using 1544 kbit/s primary multiplex equipment. The bit rates of terrestrial systems should accommodate multiples of 1544 kbit/s. Whenever practical, the bit rate should also accommodate a multiple of 6312 kbit/s, either 32 064 or 44 736 kbit/s, and 97 728 kbit/s;

(2) the characteristics of the third-order multiplex equipments using positive justification is given in § 1, below;

(3) the characteristics of the fourth-order multiplex equipments using positive justification is given in § 2 below.

1 Third-order digital multiplex equipment based on second-order bit rate of 6312 kbit/s and using positive justification

1.1 *General*

The third-order digital multiplex equipment using positive justification described below, is intended for use on digital paths and between countries using 1544 kbit/s and 6312 kbit/s primary and secondary multiplex equipments.

A bit rate of either 32 064 kbit/s or 44 736 kbit/s is recommended to allow for the efficient and economical coding of wideband signals in the networks of Administrations using primary systems according to Recommendations G.733 and G.743. For instance for a 300 voice-circuit mastergroup (Recommendation G.233 [1]) 32 064 kbit/s is appropriate, while for a 600 voice-circuit mastergroup 44 736 kbit/s coding is appropriate.

1.2 *Third-order digital multiplex equipment operating at 32 064 kbit/s*

1.2.1 *Bit rate*

The nominal bit rate should be 32 064 kbit/s. The tolerance on that rate should be ± 10 parts per million (ppm).

1.2.2 *Frame structure*

Table 1/G.752 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the frame alignment signal.

TABLE 1/G.752

32 064 kbit/s multiplexing frame structure

Tributary bit rate (kbit/s)	6312
Number of tributaries	5
Frame structure	Bit number
	Set I
Bits for frame alignment signal (see Note 1)	1 to 5
Bits from tributaries	6 to 320
	Set II
C_{j1} (j = 1 to 5) for justification control signal (see Note 2)	1 to 5
Bits from tributaries	6 to 320
	Set III
C_{j2} (j = 1 to 5) for justification control signal (see Note 2)	1 to 5
Bits from tributaries	6 to 320
	Set IV
Bits for frame alignment signal (see Note 3)	1 to 5
Bits from tributaries	6 to 320
	Set V
C_{j3} (j = 1 to 5) for justification control signal (see Note 2)	1 to 5
Bits from tributaries	6 to 320
	Set VI
Auxiliary bits H_n (n = 1, 2, 3, 4, 5) (see Note 4)	1 to 5
Bits from tributaries	6 to 320
Frame length	1 920 bits
Bits per tributary (including justification)	378 bits
Maximum justification rate per tributary	16 700 bit/s
Nominal justification ratio	0.036

Note 1 – The frame alignment signal is a 11010 pattern.

Note 2 – C_{jn} indicates the nth justification control bit of the jth tributary (j = 1 to 5).

Note 3 – The frame alignment signal is a 00101 pattern.

Note 4 – H_5 is used for transmitting failure information from the receive end to the transmit end.

Note 5 – The bit available for the justification of each tributary is the first slot of the tributary in set VI.

1.2.3 *Loss and recovery of frame alignment and consequent action*

The frame alignment recovery time should not exceed 8 ms. The signal to be applied to the tributaries during the out-of-frame alignment time should be studied.

1.2.4 *Multiplexing method*

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended.

The justification control signal should be distributed and the C_{jn}-bits should be used ($n = 1, 2, 3$, see Table 1/G.752).

Positive justification should be indicated by the signal 111, no justification by the signal 000. Majority decision is recommended.

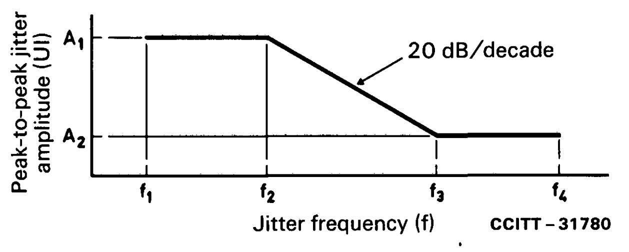
Table 1/G.752 gives the maximum justification rate per tributary and the nominal justification ratio.

1.2.5 *Jitter*

1.2.5.1 *Specifications at the input ports*

The digital signal presented at the input ports shall be as defined in Recommendation G.703 modified by the transmission characteristic of the interconnecting cable. The input ports shall be able to tolerate a digital signal with these electrical characteristics but modified by sinusoidal jitter up to the limits specified by the amplitude frequency relationship in Figure 2/G.752. The equivalent binary content of the signal, with jitter modulation, applied to the inputs shall be a pseudo-random bit sequence of length $2^{15} - 1$.

Note – The signal with jitter modulation applied to the demultiplexer input shall contain the bits necessary for framing and justification in addition to information bits.



Input	A_1 (UI)	A_2 (UI)	f_1 (Hz)	f_2 (kHz)	f_3 (kHz)	f_4 (kHz)
6312 kbit/s	1	0.05	60	1.6	32	160
32 064 kbit/s (provisional)	5	0.05	60	1.6	160	800

UI Unit interval

FIGURE 2/G.752

Lower limit of maximum tolerable input jitter

1.2.5.2 *Multiplex signal output jitter*

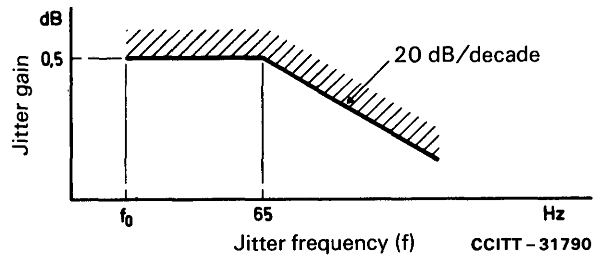
The jitter at the 32 064 kbit/s output of the multiplexer should not exceed 0.01 UI rms.

1.2.5.3 *Demultiplexer output jitter with no multiplexer or demultiplexer input jitter*

The peak-to-peak jitter at a tributary output of the demultiplexer with no jitter at the inputs should not exceed 0.2 UI.

1.2.5.4 *Demultiplexer jitter transfer characteristic*

A 6312 kbit/s signal, modulated by sinusoidal jitter, should be subject to a demultiplexer jitter transfer characteristic within the gain/frequency limits given in Figure 3/G.752.



Note – The frequency f_0 should be as low as possible taking into account the limitations of measuring equipment.

FIGURE 3/G.752

Demultiplexer transfer characteristic

1.2.6 *Digital interface*

The digital interfaces at 6312 kbit/s and 32 064 kbit/s should be in accordance with Recommendation G.703.

1.2.7 *Timing signal*

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal source.

1.2.8 *Service digits*

The service digits are reserved for national use.

1.3 *Third-order digital multiplex operating at 44 736 kbit/s*

1.3.1 *Bit rate*

The nominal bit rate should be 44 736 kbit/s. The tolerance on that rate should be ± 20 parts per million (ppm).

1.3.2 *Frame structure* (see Table 2/G.752).

1.3.3 *Loss and recovery of frame and multiframe alignment and consequent action*

The frame alignment recovery time should not exceed 2.5 ms. The signal to be applied to the tributaries during the out-of-frame alignment time should be studied.

Once frame alignment is established, multiframe alignment should be recovered in less than 250 μs.

1.3.4 *Multiplexing method*

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended.

The justification control signal should be distributed and the C_{jn}-bits should be used (n = 1, 2, 3, see Table 2/G.752).

Positive justification should be indicated by the signal 111, no justification by the signal 000. Majority decision is recommended.

Table 2/G.752 gives the maximum justification rate per tributary and the nominal justification ratio.

TABLE 2/G.752

44 736-kbit/s multiplexing frame structure

Tributary bit rate (kbit/s)	6312
Number of tributaries	7
Frame structure (see Note 1)	Bit number
	Set I
Bit for multiframe alignment signal (M_j) (see Note 1)	1
Bits from tributaries	2 to 85
	Set II
1st bit for frame alignment signal (F_{11}) (see Note 2)	1
Bits from tributaries	2 to 85
	Set III
1st bit for justification control signal (C_{j1})	1
Bits from tributaries	2 to 85
	Set IV
2nd bit for frame alignment signal (F_0)	1
Bits from tributaries	2 to 85
	Set V
2nd bit for justification control signal (C_{j2})	1
Bits from tributaries	2 to 85
	Set VI
3rd bit for frame alignment signal (F_0)	1
Bits from tributaries	2 to 85
	Set VII
3rd bit for justification control signal (C_{j3})	1
Bits from tributaries	2 to 85
	Set VIII
4th bit for frame alignment signal (F_{12})	1
Bits from tributaries (see Note 3)	2 to 85
Frame length	680 bits
Multiframe length	4760 bits
Bits per tributary per multiframe (including justification)	672 bits
Maximum justification rate per tributary	9398 bit/s
Nominal justification ratio	0.390

Note 1 – This frame is repeated 7 times to form a multiframe with frames designated j = 1, 2, 3, 4, 5, 6, 7. The multiframe alignment signal is an XXPP010 pattern where X is a bit assigned to service function, and P is the parity bit for the preceding multiframe (i.e. from M_1 to M_7). P = 1 if the number of marks in all tributary bits in the preceding multiframe is odd, P = 0 if the number of marks in all tributary bits in the preceding multiframe is even. Note that the two X bits are identical in any multiframe, as are the two P bits.

Note 2 – The frame alignment signal is $F_0 = 0$ and $F_{11} = F_{12} = 1$.

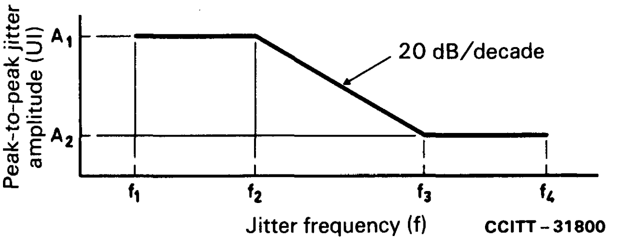
Note 3 – The bit available for the justification of tributary j is the first slot of tributary j following F_{12} in the jth frame.

1.3.5 *Jitter*

1.3.5.1 *Specifications at the input ports*

The digital signal presented at the input ports shall be as defined in Recommendation G.703 modified by the transmission characteristic of the interconnecting cable. The input ports shall be able to tolerate a digital signal with these electrical characteristics but modified by sinusoidal jitter up to the limits specified by the amplitude frequency relationship in Figure 4/G.752. The equivalent binary content of the signal, with jitter modulation, applied to the inputs shall be a pseudo-random bit sequence of length $2^{15} - 1$.

Note – The signal with jitter modulation applied to the demultiplexer input shall contain the bits necessary for framing and justification in addition to information bits.



Input	A_1 (UI)	A_2 (UI)	f_1 (Hz)	f_2 (kHz)	f_3 (kHz)	f_4 (kHz)
6312 kbit/s	2	0.05	10	0.6	24	120
44 736 kbit/s	14	0.05	10	3.2	900	4500

UI Unit interval

FIGURE 4/G.752

Lower limit of maximum tolerable input jitter

1.3.5.2 *Multiplex signal output jitter*

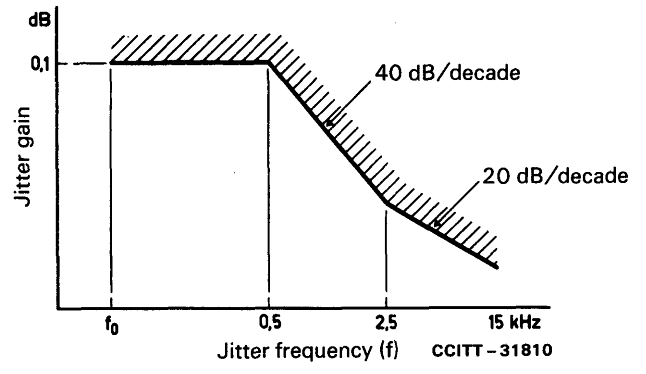
The jitter at the 44 736 kbit/s multiplexer output should not exceed 0.01 UI rms.

1.3.5.3 *Demultiplexer output jitter with no multiplexer or demultiplexer input jitter*

With no jitter at the input to the multiplexer and demultiplexer, the jitter at the demultiplexer output should not exceed 1/5 UI peak-to-peak.

1.3.5.4 *Demultiplexer jitter transfer characteristic*

The gain of the jitter transfer characteristic should not exceed the limits given in Figure 5/G.752.



Note – The frequency f_0 should be as low as possible taking into account the limitations of measuring equipment.

FIGURE 5/G.752

Demultiplexer transfer characteristic

1.3.6 *Digital interfaces*

The digital interfaces at 6312 kbit/s and 44 736 kbit/s should be in accordance with Recommendation G.703.

1.3.7 *Timing signal*

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal source.

1.3.8 *Service digits*

The service digits are reserved for national use.

2 Fourth-order multiplex equipment operating at 97 728 kbit/s

2.1 *Bit rate*

The nominal bit rate should be 97 728 kbit/s. The tolerance on that rate should be ± 10 parts per million (ppm).

2.2 *Frame structure*

Table 3/G.752 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the frame alignment signal.

2.3 *Loss and recovery of frame alignment and consequent action*

The mean frame alignment recovery time should not exceed 1 ms.

The signal to be applied to the tributaries during the out-of-frame alignment time should be all 1s pattern.

2.4 *Multiplexing method*

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended.

The justification control signal should be distributed and the C_{jn}-bits should be used (n = 1, 2, 3, see Table 3/G.752).

Positive justification should be indicated by the signal 111, no justification by the signal 000. Majority decision is recommended.

Table 3/G.752 gives the maximum justification rate per tributary and the nominal justification ratio.

TABLE 3/G.752

97 728 kbit/s multiplexing frame structure

Tributary bit rate (kbit/s)	32 064
Number of tributaries	3
Frame structure	Bit number
	Set I
Frame alignment signal (110)	1 to 3
Bits from tributaries	4 to 192
	Set II
Justification control bits C_{j1} (see Note 1)	1 to 3
Bits from tributaries	4 to 192
	Set III
Justification control bit C_{j2} (see Note 1)	1 to 3
Bits from tributaries	4 to 192
	Set IV
Frame alignment signal (001)	1 to 3
Bits from tributaries	4 to 192
	Set V
Justification control bits C_{j3} (see Note 1)	1 to 3
Bits from tributaries	4 to 192
	Set VI
Auxiliary bits H_n (n = 1, 2, 3) (see Note 2)	1 to 3
Bits from tributaries	4 to 192
Frame length	1 152 bits
Bits per tributary per frame (including justification)	378 bits
Maximum justification rate per tributary	84 833 bit/s
Nominal justification ratio	0.035

Note 1 – C_{jn} indicates the nth justification bit of the jth tributary (j = 1, 2, 3).

Note 2 – This signal is H_1 H_2 H_3 pattern where H_1 is the parity bit for the preceding frame, and H_2 is a bit reserved for national use, and H_3 is a bit to transmit the failure information from the receiving end to the transmitting end.

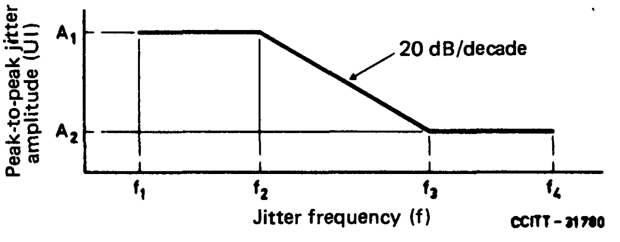
Note 3 – The bit available for justification of tributary j is the first slot of tributary j following H_n.

2.5 *Jitter*

2.5.1 *Specifications at the input ports*

The digital signal presented at the input ports shall be as defined in Recommendation G.703 modified by the transmission characteristic of the interconnecting cable. The input ports shall be able to tolerate a digital signal with these electrical characteristics but modified by sinusoidal jitter up to the limits specified by the amplitude frequency relationship in Figure 6/G.752. The equivalent binary content of the signal, with jitter modulation, applied to the inputs shall be a pseudo-random bit sequence of length $2^{15} - 1$.

Note – The signal with jitter modulation applied to the demultiplexer input shall contain the bits necessary for framing and justification in addition to information bits.



Input	A_1 (UI)	A_2 (UI)	f_1 (Hz)	f_2 (kHz)	f_3 (kHz)	f_4 (kHz)
32 064 kbit/s	2	0.2	10	0.8	8	400
97 728 kbit/s	6	0.1	10	5.5	325	1000

UI Unit interval

FIGURE 6/G.752

Lower limit of maximum tolerable input jitter (provisional)

2.5.2 *Multiplex signal output jitter*

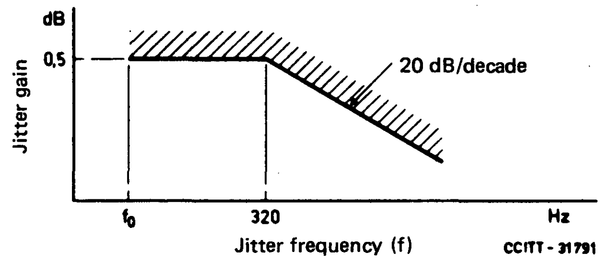
The jitter at the 97 728 kbit/s output of the multiplexer should not exceed 0.01 UI rms.

2.5.3 *Demultiplexer output jitter with no multiplexer or demultiplexer input jitter*

The peak-to-peak jitter at a tributary output of the demultiplexer with no jitter at the inputs should not exceed 0.25 UI.

2.5.4 *Demultiplexer jitter transfer characteristic*

A 32 064 kbit/s signal, modulated by sinusoidal jitter, should be subject to a demultiplexer jitter transfer characteristic within the gain/frequency limits given in Figure 7/G.752.



Note – The frequency f_0 should be as low as possible taking into account the limitations of measuring equipement.

FIGURE 7/G.752

Demultiplexer transfer characteristic

2.6 *Digital interface*

The digital interfaces at 32 064 kbit/s and 97 728 kbit/s should be in accordance with Recommendation G.703.

2.7 *Service digits*

The service digits are reserved for national use.

Reference

[1] CCITT Recommendation *Recommendations concerning translating equipments*, Vol. III, Rec. G.233.

Recommendation G.753

THIRD ORDER DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 34 368 kbit/s AND USING POSITIVE/ZERO/NEGATIVE JUSTIFICATION

(Geneva, 1980, further amended)

1 General

The third order digital multiplex system with positive/zero/negative pulse justification as given below is intended for digital connection between countries having the same type of justification using any second order digital systems at 8448 kbit/s.

2 Bit rate

The nominal bit rate should be 34 368 kbit/s. The tolerance on that rate should not be more than ± 20 parts per million (ppm).

3 Frame structure

Table 1/G.753 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the bunched frame alignment signal.

TABLE 1/G.753

34 368-kbit/s multiplexing frame structure using positive/zero/negative justification

Tributary bit rate (kbit/s)	8448
Number of tributaries	4
Frame structure	Bit number
	Set I
Frame alignment signal (111110100000)	1 to 12
Bits from the secondary tributaries	13 to 716
	Set II
Justification control bits (C_{j1})	1 to 4
Bits for service functions	5 to 8
Justification control bits (C_{j2})	9 to 12
Bits from the secondary tributaries	13 to 716
	Set III
Justification control bits (C_{j3})	1 to 4
Bits reserved for national use	5 to 8
Bits from tributaries available for negative justification	9 to 12
Bits from tributaries available for positive justification	13 to 16
Bits from the tributaries	17 to 716
Frame length	2148 bits
Frame duration	62.5 µs
Bits per tributary	528
Maximum justification rate per tributary	16 kbit/s

Note – C_{jn} indicates the nth justification control pulse of the jth tributary.

4 Loss and recovery of frame alignment and consequent actions

The frame alignment system should be adaptive to the error ratio in the line link. Until frame alignment is restored the frame alignment system should retain its position. A new search for the frame alignment signal should be undertaken when three or more consecutive frame alignment signals have been incorrectly received in their positions.

Frame alignment is considered to have been recovered when more than two consecutive frame alignment signals have been correctly received in their predicted positions.

5 Multiplexing method

Cyclic bit interleaving in the tributary numbering order and positive-negative justification with two-command control are recommended. The justification control signal should be distributed and use C_{jn}-bits (n = 1, 2, 3 see Table 1/G.753). Correction of one error in a command is possible.

Positive justification should be indicated by the signal 111, transmitted in each of two consecutive frames; negative justification should be indicated by the signal 000, transmitted in each of two consecutive frames, and no justification by the signal 111 in one frame followed by 000 in the next frame.

Digit time slots 9, 10, 11, 12 (Set III) are used for information carrying bits (for negative justification), and digit time slots 13, 14, 15, 16 in Set III when it is necessary are used for no information carrying bits (for positive justification) for the tributaries 1, 2, 3, 4.

Besides, when information from tributaries 1, 2, 3 and 4 is not transmitted, bits 9, 10, 11 and 12 in Set III are available for transmitting information concerning the type of justification (positive or negative) in frames containing commands of positive justification control and intermediate amount of jitter in frames containing commands of negative justification.

Table 1/G.753 gives maximum justification rate per tributary.

6 Jitter

The amount of jitter that should be tolerated at the input of the multiplexer and the demultiplexer should be according to 3.1.1/G.823. The amount of jitter at the output of the multiplexer and the demultiplexer should be studied and specified.

7 Digital interface

The interface at the nominal bit rate 34 368 kbit/s is under study.

8 Timing signal

The clock should be able to be controlled by an external source.

9 Service digits

Some spare bits per frame are available for service functions (bits 5, 6 and 8 in Set II) for national and international use. Bits 5 and 6 in Set II are available for a digital service channel (using 32 kbit/s Adaptive Delta Modulation) and bit 8 in Set II is available for ringing up a digital service channel.

10 Fault conditions and consequent actions

10.1 The digital multiplex equipment should detect the following fault conditions:

10.1.1 Failure of power supply.

10.1.2 Loss of the incoming signal at 8448 kbit/s at the input of the multiplexer.

Note – When using separate circuits for the digital signal and the timing signal, loss of either or both of them should constitute loss of the incoming signal.

10.1.3 Loss of the incoming signal at 34 368 kbit/s at the input of the demultiplexer.

Note – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

10.1.4 Loss of frame alignment.

10.1.5 Alarm indication received from the remote multiplex equipment at the 34 368 kbit/s input of the demultiplexer (see § 10.2.2 below).

10.2 *Consequent actions*

After detecting a fault condition, appropriate actions should be taken as specified in Table 2/G.753. The consequent actions are as follows:

10.2.1 Prompt maintenance alarm indication generated to signify that the performance is below acceptable standards and maintenance attention is required locally. When detecting the Alarm Indication Signal (AIS) at the 34 368 kbit/s input of the demultiplexer the prompt maintenance alarm indication associated with loss of frame alignment should be inhibited (see Note 1 below).

Note – The location and provision of any visual and/or audible alarm activated by this prompt maintenance alarm indication is left to the discretion of each Administration.

10.2.2 Alarm indication to the remote multiplex equipment generated by changing from the state 0 to the state 1 bit 7 of Set II at the 34 368 kbit/s output of the multiplexer.

10.2.3 AIS (see Note 2 below) applied to all four outputs of the 8448 kbit/s tributary outputs from the demultiplexer.

10.2.4 AIS (see Note 2 below) applied to the 34 368 kbit/s output of the multiplexer.

10.2.5 AIS (see Note 2 below) applied to the time slots of the 34 368 kbit/s signal at the multiplexer output corresponding to the relevant 8448 kbit/s tributary.

Note 1 – The bit rate of the AIS at the output of the corresponding demultiplexer should be as specified for the tributaries. The method of achieving this is under study.

Note 2 – The equivalent binary content of the AIS at 8448 kbit/s and 34 368 kbit/s is a continuous stream of binary 1s.

TABLE 2/G.753

Fault conditions and consequent action

Equipment part	Fault conditions (see § 10.1)	Consequent actions (see § 10.2)				
		Prompt maintenance alarm indication generated	Alarm indication to the remote multiplexer generated	AIS applied		
				To all tributaries	To the composite signal	To the relevent time slots of the composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes	Yes, if practicable	Yes, if practicable	Yes, if practicable	
Multiplexer only	Loss of incoming signal on a tributary	Yes				Yes
Demultiplexer only	Loss of incoming signal at 34 368 kbit/s	Yes	Yes	Yes		
	Loss of frame alignment	Yes	Yes	Yes		
	AIS received from the remote multiplexer					

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

FOURTH ORDER DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 139 264 kbit/s AND USING POSITIVE/ZERO/NEGATIVE JUSTIFICATION

(Geneva, 1980; further amended)

1 General

The fourth order digital multiplex system with positive/zero/negative pulse justification as given below is intended for use on digital connection between countries having the same type of justification using any third order digital systems at 34 368 kbit/s.

2 Bit rate

The nominal bit rate should be 139 264 kbit/s. The tolerance on that rate should not be more than ± 15 parts per million (ppm).

3 Frame structure

Table 1/G.754 gives:

- the tributary bit rate and the number of tributaries;
- the number of bits per frame;
- the bit numbering scheme;
- the bit assignment;
- the bunched frame alignment signal.

TABLE 1/G.754

139 264-kbit/s multiplexing frame structure using positive/zero/negative justification

Tributary bit rate (kbit/s)	34 368
Number of tributaries	4
Frame structure	Bit number
	Set I
Frame alignment signal	1 to 10
Bits for service functions	11 to 12
Bits from tributaries	13 to 544
	Set II
Justification control bits (C_{j1})	1 to 4
Bits from tributaries	5 to 544
	Set III
Justification control bit (C_{j2})	1 to 4
Bits from tributaries	5 to 544
	Set IV
Justification control bit (C_{j3})	1 to 4
Bits from tributaries available for negative justification	5 to 8
Bits from tributaries available for positive justification	9 to 12
Bits from tributaries	13 to 544
Frame length	2176 bits
Frame duration	15.625 μs
Bits per tributaries	537
Maximum justification rate per tributary	64 kbit/s

Note – C_{jn} indicates the *n*th justification control bit of the *j*th tributary.

4 Loss and recovery of frame alignment and consequent action

The frame alignment system should be adaptive to the error rate in the line link. Until frame alignment is restored the frame alignment system should retain its position. A new search for the frame alignment signal should be undertaken when three and more consecutive frame alignment signals have been incorrectly received in their position.

Frame alignment is considered to have been recovered when more than two consecutive frame alignment signals have been correctly received in their predicted positions.

5 Multiplexing method

Cyclic bit interleaving in the tributary numbering order and positive-negative justification with two-command control are recommended. The justification control signal should be distributed and use C_{jn}-bits ($n = 1$, 2, 3 see Table 1/G.754). Correction of one symbol error in a command is possible.

Positive justification should be indicated by the signal 111, transmitted in each of two consecutive frames; negative justification should be indicated by the signal 000, transmitted in each of two consecutive frames, and no justification by the signal 111 in one frame followed by 000 in the next frame.

Digit time slots 5, 6, 7, 8 (Set IV) are used for information carrying bits (for negative justification), and digit time slots 9, 10, 11, 12 in Set IV, when it is necessary, are used for no information carrying bits (for positive justification) for the tributaries 1, 2, 3, 4.

Besides, when information from tributaries 1, 2, 3 and 4 is not transmitted, bits 5, 6, 7 and 8 in Set IV are available for transmitting information concerning the type of justification (positive or negative) in frames containing commands of positive justification control and intermediate amount of jitter in frames containing commands of negative justification.

Table 1/G.754 gives maximum justification rate per each third order tributary.

6 Jitter

The amount of jitter that should be accepted at the inputs of the demultiplexer and multiplexer and should be at the output of the demultiplexer is under study.

7 Digital interface

The interface at the nominal bit rates 34 368 kbit/s and 139 264 kbit/s is under study.

8 Timing signal

The clock should be able to be controlled by an external source.

9 Service functions

Some spare bits per frame are available for service functions (bits 11 and 12 in Set I) for national and international use. Bit 11 in Set I is available for a digital service channel (using 32 kbit/s Adaptive Delta Modulation) and bit 12 is available for ringing up a digital service channel.

10 Fault conditions and consequent actions

10.1 The digital multiplex equipment should detect the following fault conditions:

10.1.1 Failure of power supply.

10.1.2 Loss of the incoming signal at 34 368 kbit/s at the input of the multiplexer.

10.1.3 Loss of the incoming signal at 139 264 kbit/s at the input of the demultiplexer.

Note – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.

10.1.4 Loss of frame alignment.

10.1.5 Alarm indication received from the remote multiplex equipment at the 139 264 kbit/s input of the demultiplexer (see § 10.2.2 below).

10.2 *Consequent actions*

After detection of a fault condition appropriate actions should be taken as specified in the Table 2/G.754. The consequent actions are as follows:

10.2.1 Prompt maintenance alarm indication generated to signify that the performance is below acceptable standards and maintenance attention is required locally. When detecting the Alarm Indication Signal (AIS) at the 139 264 kbit/s input of the demultiplexer the prompt maintenance alarm indication associated with loss of frame alignment should be inhibited (see Note 1 below).

Note – The location and provision of any visual and/or audible alarm activated by this prompt maintenance alarm indication is left to the discretion of each Administration.

10.2.2 Alarm indication to the remote multiplex equipment generated by changing from the state 0 to the state 1 bit 12 of Set I at the 139 264 kbit/s output of the multiplexer.

10.2.3 AIS (see Note 2 below) applied to all the four outputs of the 34 368 kbit/s tributary outputs from the demultiplexer.

10.2.4 AIS (see Note 2 below) applied to the 139 264 kbit/s output of the multiplexer.

10.2.5 AIS (see Note 2 below) applied to the time slots of the 139 264 kbit/s signal at the multiplexer output corresponding to the relevant 34 368 kbit/s tributary.

Note 1 – The bit rate of the AIS at the output of the corresponding demultiplexer should be as specified for the tributaries. The method of achieving this is under study.

Note 2 – The equivalent binary content of the AIS at 34 368 kbit/s and 139 264 kbit/s is a continuous stream of binary 1s.

TABLE 2/G.754

Fault conditions and consequent actions

<table>
<tr><th rowspan="3">Equipment part</th><th rowspan="3">Fault condition (see § 10.1)</th><th colspan="5">Consequent actions (see § 10.2)</th></tr>
<tr><th rowspan="2">Prompt maintenance alarm indication generated</th><th rowspan="2">Alarm indication to the remote multiplexer generated</th><th colspan="3">AIS applied</th></tr>
<tr><th>To all tributaries</th><th>To the composite signal</th><th>To the relevant time slots of the composite signal</th></tr>
<tr><td>Multiplexer and demultiplexer</td><td>Failure of power supply</td><td>Yes</td><td>Yes, if practicable</td><td>Yes, if practicable</td><td>Yes, if practicable</td><td></td></tr>
<tr><td>Multiplexer only</td><td>Loss of incoming signal on a tributary</td><td>Yes</td><td></td><td></td><td></td><td>Yes</td></tr>
<tr><td rowspan="3">Demultiplexer only</td><td>Loss of incoming signal at 139 264 kbit/s</td><td>Yes</td><td>Yes</td><td>Yes</td><td></td><td></td></tr>
<tr><td>Loss of frame alignment</td><td>Yes</td><td>Yes</td><td>Yes</td><td></td><td></td></tr>
<tr><td>AIS received from the remote multiplexer</td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 139 264 KBIT/S AND MULTIPLEXING THREE TRIBUTARIES AT 44 736 KBIT/S

(Melbourne, 1988)

1 General

The digital multiplex equipment described in this Recommendation is intended for use between networks using different digital hiararchies as specified in Recommendations G.702 and G.802.

2 Bit rate

The bit rates of the tributary and multiplex signals should be 44 736 kbit/s ± 20 ppm and 139 264 kbit/s ± 15 ppm, respectively, as specified in Recommendation G.703.

3 Frame structure

Table 1/G.755 gives the recommended 139 264 kbit/s multiplexing frame structure.

4 Loss and recovery of frame alignment and consequent action

Loss of frame alignment should be assumed to have taken place when four consecutive frame alignment signals have been incorrectly received in their predicted positions.

When frame alignment is assumed to be lost, the frame alignment device should decide that such alignment has effectively been recovered when it detects the presence of three consecutive correct frame alignment signals.

The frame alignment device, having detected the appearance of a single correct frame alignment signal, should begin a new search for the frame alignment signal when it detects the absence of the frame alignment signal in one of the two following frames.

Note – As it is not strictly necessary to specify the detailed frame alignment strategy, any suitable frame alignment strategy may be used provided the performance achieved is at least as efficient in all respects as that obtained by the above frame alignment strategy.

5 Multiplexing and justification methods

Cyclic bit interleaving in the tributary numbering order and positive justification are recommended.

The justification control signal should be distributed and use the C_{ji}-bits (j = 1, 2, 3; i = 1, 2, 3, 4, 5) (see Note 6 to Table 1/G.755).

Positive justification should be indicated by the justification control signal 11111 and no justification by the signal 00000. Majority decision is recommended.

Table 1/G.755 gives the maximum justification rate per tributary and the nominal justification ratio.

6 Jitter

6.1 *Demultiplexer triburaty jitter transfer characteristic*

The demultiplexer 44 736 kbit/s tributary jitter transfer characteristic should meet the gain/frequency limits given in Figure 1/G.755. The equivalent binary content of the test signal used should result in a tributary output signal of 1000.

TABLE 1/G.755

139 264 kbit/s multiplexing frame structure

Nominal tributary bit rate (kbit/s)	44 736
Number of tributaries	3
Frame structure	Bit number
	Set I
Frame alignment signal (111110100000)	1 to 12
Bits from tributaries	13 to 159
	Set II
Justification control bits C_{j1} (Note 1)	1 to 3
Bits from tributaries	4 to 159
	Set III
Justification control bits C_{j2} (Note 1)	1 to 3
Bits from tributaries	4 to 159
	Set IV
Justification control bits C_{j3} (Note 1)	1 to 3
Alarm indication to the remote multiplex equipment (Note 2)	4
Parity bit (Notes 3, 4 and 5)	5
Bits reserved for future use (Note 6)	6 to 9
Bits from tributaries	10 to 159
	Set V
Justification control bits C_{j4} (Note 1)	1 to 3
Bits from tributaries	4 to 159
	Set VI
Justification control bits C_{j5} (Note 1)	1 to 3
Bits from tributaries available for justification	4 to 6
Bits from tributaries	7 to 159
Frame length	954 bits
Bits per tributary in a frame	307 bits
Maximum justification rate per tributary	146 kbit/s
Nominal justification ratio	0.545

Note 1 – C_{ji} (j = 1, 2, 3; i = 1, 2, 3, 4, 5) indicates the ith justification control bit of the jth tributary.

Note 2 – See § 10.2.1.

Note 3 – The parity bit = 1 if the number of marks in all tributary bits including the bits in the justifiable time-slots in the preceding frame is odd; the parity bit = 0 if the number of marks in all tributary bits including the bits in the justifiable time-slots in the preceding frame is even.

Note 4 – It is recognized that existing multiplex equipment installed prior to adoption of this Recommendation does not insert the parity bit.

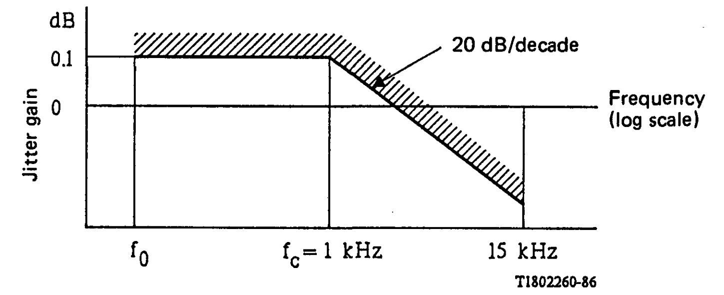
Note 5 – The implementation and the use of this parity bit procedure are for further study.

Note 6 – These bits should be set to 1 when not used.

Note 1 – This characteristic is usually measured between the high speed and low speed interfaces of the demultiplexer and the measurements are taken in unit intervals. It is then necessary to introduce a correction factor to account for the difference in the size of unit intervals.

Note 2 – In addition, the need to specify a muldex jitter transfer characteristic is for further study.

Note 3 – It is recognized that the existing multiplex equipment designed prior to the adoption of this Recommendation might need tributary test signals incorporating the 44 736 kbit/s frame structure defined in Recommendation G.572.



Note – The frequency f_0 should be as low as possible, taking into account the limitations of measuring equipment. In any case f_0 should be no greater than 10 Hz. The selective measurement method should be used.

FIGURE 1/G.755

Demultiplexer tributary jitter transfer characteristic

6.2 *Output jitter*

6.2.1 *Tributary output jitter*

With no jitter applied to the input ports of the multiplexer and with the multiplexer directly connected to the demultiplexer, the peak-to-peak jitter at the tributary output port should not exceed 0.3 UI when measured over a one minute interval within the frequency range from $f_1 = 10$ Hz to $f_4 = 400$ Hz.

When measured with an instrument incorporating a bandpass filter having a lower cutoff frequency of $f_3 = 60$ kHz, a roll-off of 20 dB/decade and an upper limit of $f_4 = 400$ kHz, the peak-to-peak output jitter should not exceed 0.05 UI when it is measured over a one minute interval.

6.2.2 *Multiplexer output jitter*

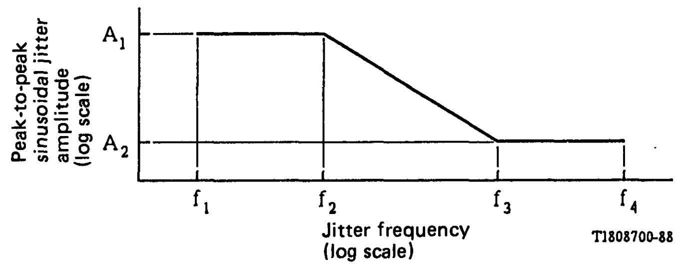
The peak-to-peak jitter at the 139 264 kbit/s output port should not exceed 0.05 UI when it is measured over a one minute interval within the frequency range from 200 Hz to 3500 kHz.

6.3 *Input jitter*

6.3.1 *Tributary input jitter*

The 44 736 kbit/s input port should be capable of accommodating levels of input jitter up to the limits given in Figure 2/G.755.

Note – Current Recommendation G.703 does not refer to the jitter tolerated at the digital distribution frame at 44 736 kbit/s nor at the input port of equipment connected to this distribution frame.



Peak-to-peak sinusoidal jitter amplitude		Frequency			
A_1 (UI)	A_2 (UI)	f_1 (Hz)	f_2 (Hz)	f_3 (kHz)	f_4 (kHz)
5.0	0.1	10	2.3	60	400

FIGURE 2/G.755

Lower limit of maximum tolerable sinusoidal input jitter at 44 736 kbit/s

6.3.2 *Demultiplexer input jitter*

The 139 264 kbit/s input port should be capable of accommodating levels of input jitter up to the limits given in Recommendation G.823.

Note – The jitter accommodation requirement should be met when the jittered input signal is composed of the multiplexed tributary signals having any value of jitter allowed for the 44 736 kbit/s level.

7 Digital interfaces

The digital interfaces at 44 736 kbit/s and 139 264 kbit/s should be in accordance with Recommendation G.703.

8 Timing signal

If it is economically feasible, it may be desirable to be able to derive the multiplexing timing signal from an external source as well as from an internal source.

9 Service digits

Six bits per frame are available for service functions (see Table 1/G.755): bit 4 of Set IV is used to transmit an alarm indication to the remote multiplex equipment when specific fault conditions are detected in the multiplex equipment when specific fault conditions are detected in the multiplex equipment (see § 10 below); bit 5 of Set IV may be used for a parity check; bits 6 to 9 of Set IV are reserved for further use.

10 Fault conditions and consequent actions

10.1 *Fault conditions*

10.1.1 The digital multiplex equipment should detect the following fault conditions:

1) failure of power supply;
2) loss of an incoming 44 736 kbit/s tributary signal at a multiplexer input port;
3) loss of an incoming 139 264 kbit/s multiplex signal at a demultiplexer input port;

   Note – The detection of this fault condition is required only when it does not result in an indication of loss of frame alignment.
4) loss of frame alignment signal at a demultiplexer input port;
5) detection of an alarm indication received from the remote multiplex equipment at a demultiplexer input port;
6) detection of alarm indication signal (AIS) at a demultiplexer input port.

Note 1 – The equivalent binary content of the AIS at 139 264 kbit/s should be a continuous stream of binary 1s (marks) as recommended in Recommendation M.20.

Note 2 – The strategy for detecting the presence of the AIS should be such that the AIS is detectable even in the presence of an error ratio of $1 \cdot 10^{-3}$. However, a signal with all bits except the frame alignment signal in the state of 1 should not be mistaken as an AIS.

10.1.2 The need to monitor the degradation of the incoming 139 264 kbit/s signal for the purpose of end-to-end error performance monitoring of the 139 264 kbit/s digital block, as well as the procedure for detecting such degradation are for further study.

10.2 *Consequent actions*

Further to the detection of a fault condition, the appropriate actions should be taken as specified in Table 2/G.755.

Note 1 – The concept and definition of prompt maintenance alarm indication is given in Recommendation M.20.

Note 2 – When the alarm indication signal (AIS) is detected at the input of the demultiplexer, the prompt maintenance alarm indication associated with loss of frame alignment should be inhibited, while the rest of the consequent actions are in accordance with those associated in Table 2/G.755 with the fault condition.

10.2.1 Alarm indication to the remote multiplex equipment should be generated by changing bit 4 of Set IV (see Table 1/G.755) from the state 0 to the state 1.

10.2.2 AIS should be applied to the following as specified in Table 2/G.755:

- all three 44 736 kbit/s tributary outputs from the demultiplexer;
- 139 264 kbit/s output of the multiplexer;
- the time slots of the 139 264 kbit/s signal at the output of the multiplexer, corresponding to the relevant 44 736 kbit/s tributary.

Note – The equivalent binary content of the AIS at 44 736 kbit/s is a signal with a valid frame alignment signal, parity and justification control bits as defined in Table 2/G.752, with the tributary bits being set to a 1010 ... sequence, starting with a binary 1 after each frame alignment, multi-frame alignment and justification control bit, and with all justification control bits being set to binary 0.

TABLE 2/G.755

Fault conditions and consequent actions

Equipment part	Fault condition (see § 10.1)	Consequent actions (see § 10.2)				
		Prompt maintenance alarm indication generated	Alarm indication to the remote multiplex equipment generated	AIS applied		
				To all the tributaries	To the composite signal	To the relevant time slots of the composite signal
Multiplexer and demultiplexer	Failure of power supply	Yes		Yes, if practicable	Yes, if practicable	
Multiplexer only	Loss of incoming signal on a tributary	Yes				Yes
Demultiplexer only	Loss of incoming signal at 139 264 kbit/s	Yes	Yes	Yes		
	Loss of frame alignment	Yes	Yes	Yes		
	Alarm indication received from the remote multiplex equipment					

Note – A *Yes* in the table signifies that a certain action should be taken as a consequence of the relevant fault condition. An *open space* in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

7.6 Principal characteristics of transcoder and digital circuit multiplication equipments

Recommendation G.761

GENERAL CHARACTERISTICS OF A 60-CHANNEL TRANSCODER EQUIPMENT

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

1 General

The 60-channel transcoder implements a conversion between two 30-channel 2048 kbit/s PCM streams and one 60-channel 2048 kbit/s ADPCM stream. In the 30-channel 2048 kbit/s streams, the telephone signals are coded using 64 kbit/s A-law PCM as specified in Recommendation G.711. In the 60-channel 2048 kbit/s stream, the telephone signals are coded using 32 kbit/s ADPCM as specified in Recommendation G.721. Figure 1/G.761 indicates the nomenclature used for the three different signal ports A, B and C.

Note 1 – Administrations should take into account the guidance given in Recommendation G.721 concerning the use and transmission performance of 32 kbit/s ADPCM .

Note 2 – It should be noted that the transcoder equipment described in this Recommendation has a limited capability of transparently transmitting 64 kbit/s data channels and this should be taken into account in the planning of networks which are likely to evolve into an ISDN (see § 3.8).

This Recommendation is divided into two parts:

- § 2 contains the interface requirements associated with the port C. These requirements are not only applicable to the 60-channel transcoder equipment, but could be applied, in the future, to other equipment such as a 60-channel multiplex terminal, a 60-channel terminating unit at a TDM switch, or a TDMA terminal. In these latter cases, the A and B interfaces would be virtual. As well as point-to-point operation, account has been taken of multi-destination operation in TDMA applications.
- § 3 contains the requirements which are specific to a 60-channel transcoder equipment realization.

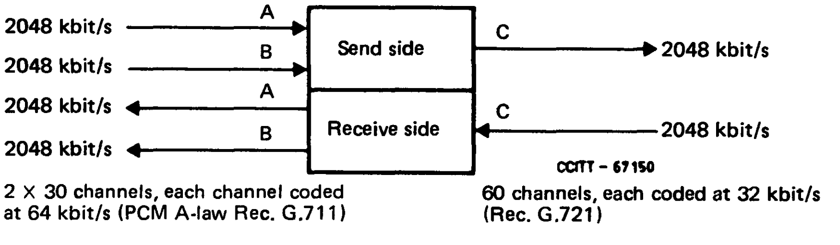


FIGURE 1/G.761

60-channel transcoder ports

2 Characteristics of a 2048 kbit/s signal organized in 64 kbit/s and/or 32 kbit/s time slots (port C)

2.1 *Interface C*

The electrical characteristics of the 2048 kbit/s interface are in accordance with Recommendation G.703, § 6.

2.2 *Frame structure*

The frame structure is in accordance with Recommendation G.704, § 2.3, with bit 1 of time slot 0 used for the cyclic redundancy check (CRC) procedure.

Time slots 1 to 15 and 17 to 31 each corresponds to:

- either two 4-bit samples of telephone signals coded using 32 kbit/s ADPCM originating from the same incoming PCM stream (A or B); the bit ordering of the 32 kbit/s signals is such that the 4-bit words are transmitted in bit order starting with bit 1 (see §§ 4.2.2 and 4.2.3 of Recommendation G.721). Bits 1 to 4 correspond to the first 32 kbit/s signal and bits 5 to 8 correspond to the second 32 kbit/s signal;
- or a digital signal at 64 kbit/s.

Where stream C is transmitting 60 telephone signals, the numbering of the channels and the correspondence between the 64 kbit/s PCM channels in streams A and B and the 32 kbit/s ADPCM channels in stream C are given in Table 1/G.761.

TABLE 1/G.761

Organization of 2048 kbit/s frame for 60-channels at 32 kbit/s (stream C)

8-bit time slot number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bits 1-4 of channel	–	1A	1B	3A	3B	5A	5B	7A	7B	9A	9B	11A	11B	13A	13B	15A
Bits 5-8 of channel	–	2A	2B	4A	4B	6A	6B	8A	8B	10A	10B	12A	12B	14A	14B	16A

8-bits time slot number	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Bits 1-4 of channel	Note 2	15B	17A	17B	19A	19B	21A	21B	23A	23B	25A	25B	27A	27B	29A	29B
Bits 5-8 of channel	Note 2	16B	18A	18B	20A	20B	22A	22B	24A	24B	26A	26B	28A	28B	30A	30B

Note 1 – The organization of the frame has been chosen to facilitate the direct time slot transfer described in § 3.8.

Note 2 – TS16 is foreseen for signalling but speech channels can be transmitted when necessary. These are numbered 31A and 31B respectively for Bits 1-4 and Bits 5-8 (see § 2.5).

Note 3 – The numbering of the channels from 1 to 30 and the correspondence with the time slots in PCM stream A (respectively B) are given in Recommendation G.735, § 2.

2.3 *Allocation of bits in time slot 0*

The allocation of the bits in time slot 0 is given in Recommendation G.704, § 2.3, with bit 1 of time slot 0 used for the cyclic redundancy check procedure.

Bits 3 to 8 in TS0 of those frames not containing the frame alignment signal are used to transmit:

- alarm indications associated with PCM streams A or B (see §§ 2.6.2 and 2.6.3 dealing with alarm indications);
- spare bits associated with PCM streams A or B (see § 3.3).

2.4 *Frame alignment and CRC procedures*

The strategy for loss and recovery of frame alignment and CRC multiframe alignment is given in Recommendation G.706, § 4.

2.5 *Allocation of bits in TS16*

TS16 can be used:

- either for signalling purposes; namely channel associated signalling (see § 2.5.1) and common channel signalling (see § 2.5.2);
- or, as envisaged in § 5.1 of Recommendation G.704, for the transmission of telephone signals; in this case two samples of telephone signals each coded with 4 bits. Used in this way, stream C can transmit up to 62 telephone signals. Bits 1 to 4 and 5 to 8 of stream C will correspond to 64 kbit/s PCM signals transmitted in TS16 of PCM streams A and B respectively.

2.5.1 *Channel associated signalling*

The allocation of bits in TS16 will depend on the number of signalling bits per channel.

2.5.1.1 *Two or less signalling bits per channel*

This applies to the digital version of Signalling System R2 (see Recommendation Q.421) specified for international applications. This also applies to a number of national signalling systems.

TS16 is organized in multiframes. Each multiframe contains 16 consecutive frames, numbered from 0 to 15. The multiframe repetition frequency is 500 Hz.

2.5.1.1.1 *Allocation of bits in TS16 frame 0*

Table 2/G.761 indicates the content of TS16 frame 0.

Bits 1 to 4 are fixed at 0 and constitute the multiframe alignment signal.

Bits 5 and 8 are used to indicate "AIS in TS16" of PCM streams A and B (see § 2.6.5).

Bits 6 and 7 are used to transmit the remote alarm indications associated with the multiframe of PCM streams A and B (see § 2.6.6).

TABLE 2/G.761

Content of TS16 frame 0

Bit number							
1	2	3	4	5	6	7	8
0	0	0	0	X_5	X_6	X_7	X_8

2.5.1.1.2 *Allocation of bits in TS16 frames 1 to 15*

Table 3/G.761 indicates the content of TS16 in frames 1 to 15.

This allocation of bits provides each 32 kbit/s channel with two signalling channels at 500 bit/s nominated "a" and "b" as defined in Recommendation G.704, § 5.1.3.2.2.

To minimize the risks of simulation of the multiframe alignment signal, special processing of certain signalling bits is carried out as described in § 2.5.1.1.3.

In the case of direct transfer of some 64 kbit/s time slots of PCM streams A or B, the four bits of TS16 associated with the transferred time slots will be transparently transmitted and allocated in accordance with Table 7/G.704. They will not be subject to the special processing described in § 2.5.1.1.3. The four bits of time slot 16 associated with each of the time slots not used in PCM streams A and B because of the direct transfer will be restituted by the transcoder with the following values:

a = 0; b = 1; and d = 1, in conformity with Table 9/G.704.

The signalling distortion of any signalling channel will not be greater than ± 2 ms.

TABLE 3/G.761

Content of TS16 frames 1 to 15

Time slot 16 bit number	1 2	3 4	5 6	7 8
Signalling	Channel a b	Channel a b	Channel a b	Channel a b
Frame 1	1A	2A	15B	16B
Frame 2	1B	2B	17A	18A
Frame 3	3A	4A	17B	18B
Frame 4	3B	4B	19A	20A
Frame 5	5A	6A	19B	20B
Frame 6	5B	6B	21A	22A
Frame 7	7A	8A	21B	22B
Frame 8	7B	8B	23A	24A
Frame 9	9A	10A	23B	24B
Frame 10	9B	10B	25A	26A
Frame 11	11A	12A	25B	26B
Frame 12	11B	12B	27A	28A
Frame 13	13A	14A	27B	28B
Frame 14	13B	14B	29A	30A
Frame 15	15A	16A	29B	30B

Note – The organization of the multiframe ensures consistency with the frame and multiframe organization of Recommendation G.704, § 5.1.3 and allows the possibility of the mixed use in stream C of 32 kbit/s and 64 kbit/s channels with their associated signalling.

2.5.1.1.3 *Special processing of signalling bits*

The signalling bits to be transmitted in bit 2 (respectively 4, 6 and 8) of TS16 (frames 1 to 15) are calculated from B_{n-1}, B_{n-2}, B_{n-3}, b_{n-1} and b_n in accordance with Table 4/G.761 where:

i) b_n is the signalling bit before processing;

ii) B_n is the signalling bit after processing, and

iii) the subscripts $n-3$, $n-2$, and $n-1$ relate to previous signalling bits pertaining to the same telephone channel; more specifically, if b_n is a bit with a given number (2, 4, 6 or 8) in any time slot 16 of frames 1 to 15, then b_{n-1} is the bit with the same number, one multiframe earlier.

Note 1 – It follows from the above that there are 60 individual and independent processing operations at the same time.

The reverse processing (after transmission) is in accordance with Table 5/G.761. The reverse processed value $\hat{b}_n$ is deduced from the successive received bits B_{n-3}, B_{n-2}, B_{n-1}, B_n and from the previous value $\hat{b}_{n-1}$. In the absence of transmission errors in stream C, $\hat{b}_n = b_n$ and there is no increase in signalling distortion. When this is not so, the error multiplication factor lies between 2 and 4.

When, in the case of fault conditions on multiframe A or B (see Table 9/G.761), the signalling bits need to be forced to state 1, this should be implemented on the unprocessed signalling channels (i.e. before the special processing at the send end or after the reverse processing at the receive end). This does not apply to the cases of "partial AIS stream A (B)" considered in § 2.6.2 where the AIS is all 1s, unprocessed.

2.5.1.1.4 *Loss and recovery of multiframe alignment*

The multiframe alignment should be assumed to have been lost when two consecutive multiframe alignment signals have been received in error.

The multiframe alignment should be assumed to have been recovered following detection of an all-zero 4-bit word formed by the first four bits of a time slot 16 and an all-zero 4-bit word one multiframe period later.

2.5.1.2 *More than two signalling bits per channel*

See § 3.8.

2.5.2 *Common channel signalling*

TS16 of stream C can be used for common channel signalling. In this case, its content corresponds, without any modification, to that of TS16 of either PCM stream A or PCM stream B. It should be noted that the simultaneous transfer of TS16 from both streams A and B is not envisaged in this case.

Time slot 16 of PCM stream B (or A) not used because of the direct transfer of time slot 16 of PCM stream A (or B) in time slot 16 of the PCM stream C will be restituted by the transcoder in the form of an all-0s signal or an all-1s signal.

2.6 *Alarm indications*

The following alarm indications can be transmitted in stream C.

2.6.1 *AIS stream C*

This means that a fault, common to the 60 channel has been detected in the send side "AIS stream C" is transmitted as an all ones configuration in stream C.

2.6.2 *AIS stream A (respectively B)*

This means that a fault, common to the 30 channels of stream A (respectively B), has been detected in the send side.

For the send side, the following applies:

When "AIS stream A" and "AIS stream B" are present simultaneously, then "AIS stream C" should be transmitted.

When "AIS stream A" (respectively B) is present, but not "AIS stream B" (respectively A), then the informaiton bits and the signalling bits associated with stream B (respectively A) should be transmitted normally and an all ones configuration should be transmitted in the time slots associated with stream A (respectively B) in stream C and the corresponding bits in TS16. In addition, bit 7 (respectively 8) of TS0 not containing the frame alignment signal in stream C should be set to 1 to indicate the "AIS stream A" (respectively B) (see Table 6/G.761). This configuration in stream C is nominated "partial AIS stream A" (respectively "partial AIS stream B").

For the receive side, the following applies:

Partial AIS stream A (respectively B) will be considered as being present if bit 7 (respectively bit 8) is detected at state 1 on three consecutive occasions.

Partial AIS stream A (respectively B) will be considered as having ceased if bit 7 (respectively 8) is detected at state 0 on three consecutive occasions.

TABLE 4/G.761

Processing of signalling bits (send side)

Input	State				Output
b_n	b_{n-1}	B_{n-3}	B_{n-2}	B_{n-1}	B_n
0	0	0	0	0	1
0	1	0	0	0	0
0	0 or 1	0	0	1	0
0	0 or 1	0	1	0	1
0	0 or 1	0	1	1	0
0	1	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	1	1	1	1	0
1	1	0	0	0	1
1	0	0	0	0	0
1	0 or 1	0	0	1	1
1	0 or 1	0	1	0	0
1	0 or 1	0	1	1	1
1	1	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	0
1	1	1	1	1	1

Note – Other states may be possible, just after powering-on, which may be avoided by careful design.

TABLE 5/G.761

Processing of signalling bits (receive side)

Input	State				Output
B_n	B_{n-3}	B_{n-2}	B_{n-1}	$\hat{B}_{n-1}$	$\hat{B}_n$
0	0	0	0	0	1
0	0	0	0	1	0
1	0	0	0	0	0
1	0	0	0	1	1
0	0	0	1	0 or 1	0
1	0	0	1	0 or 1	1
0	0	1	0	0 or 1	1
1	0	1	0	0 or 1	0
0	0	1	1	0 or 1	0
1	0	1	1	0 or 1	1
0	1	0	0	1	0
1	1	0	0	1	1
0	1	0	1	0	1
1	1	0	1	0	0
0	1	1	0	0	1
1	1	1	0	0	0
0	1	1	1	1	0
1	1	1	1	1	1

Note – Other states may be possible, just after powering-on, which may be avoided by careful design.

TABLE 6/G.761

Use of bits 7 and 8 of TS0 not containing the frame alignment signal in stream C

Bit number	7	8	Meaning
States	1	0	AIS stream A
	0	1	AIS stream B
	0	0	Normal
	1	1	Indicates that the safeguarding option (see § 3.10) is being used

2.6.3 *Alarm indication to the remote end for stream A (respectively B)*

In the send side, bit 3 of TS0, not containing the frame alignment signal of stream A (respectively B) should be transferred to bit 3 (respectively 4) of the corresponding TS0 of stream C.

In the receive side, bit 3 (respectively 4) of TS0 not containing the frame alignment signal of stream C should be transferred to bit 3 of the corresponding TS0 of stream A (respectively B).

2.6.4 *AIS in TS16 of stream C*

For channel associated signalling, this means that a fault condition, common to the signalling information associated with all 60 channels of stream C has been detected in the send side. "AIS in TS16 of stream C" is transmitted as an all ones configuration in TS16.

2.6.5 *AIS in TS16 stream A (respectively B)*

For channel associated signalling, this means that a fault, common to the 30 channels of stream A (respectively B), has been detected in the send side.

For the send side, the following applies:

When "AIS in TS16 stream A" and "AIS in TS16 in stream B" are present simultaneously, then "AIS in TS16 of stream C" should be transmitted. When "AIS in TS16 stream A" (respectively B) is present, but not "AIS in TS16 stream B" (respectively A), then the signalling information of stream B (respectively A) should be transmitted normally, and the signalling bits of TS16 of stream C associated with stream A (respectively B) should be transmitted as an all ones configuration. In addition, bit 5 (respectively 8) of TS16 frame 0 should be set to 1 to indicate "AIS in TS16 stream A" (respectively B).

For the receive side, the following applies:

AIS in TS16 stream A (respectively B) will be considered as being present if bit 5 (respectively 8) of TS16 frame 0 is detected at state 1 on two consecutive occasions.

AIS in TS16 stream A (respectively B) will be considered as having ceased if bit 5 (respectively 8) is detected at state 0 on two consecutive occasions.

2.6.6 *Remote alarm in TS16 of stream A (respectively B)*

For channel associated signalling, this means that a loss of multiframe alignment in stream A (respectively B) has been detected in the opposite direction of transmission.

Bit 6 (respectively 7) of TS16 frame 0 of stream C should be put to 1 to transmit this remote alarm indication associated with stream A (respectively B).

The simultaneous presence of bits 6 and 7 (of TS16 frame 0 of stream C) in state 1 indicates a remote alarm associated with the signalling information of the 60 channels.

3 Other characteristics of the 60 channel transcoder equipment

3.1 *Interfaces A and B*

The electrical characteristics of the two interfaces A and B are in accordance with Recommendation G.703, § 6.

3.2 *Frame structure of streams A and B*

The frame structure of the 2048 kbit/s streams A and B is given in Recommendation G.704, § 2.3, with bit 1 of time slot 0 used for the CRC procedure. The strategy for loss and recovery of frame alignment and CRC multiframe alignment are given in Recommendation G.706, § 4.

As indicated in Recommendation G.704, § 5.1, TS16 of streams A and B can be used for the transmission of telephone signals, if not used for signalling purposes, providing two supplementary channels nominated 31A and 31B respectively. (See Table 1/G.761.)

3.3 *Transparent transfer of bits of time slot 0 not containing the frame alignment signal*

The transcoder equipment should be capable of providing the following two options, the choice between these to be made by the individual Administration or by mutual agreement of the Administrations concerned:

a) bit 4 of time slot 0 not containing the frame alignment signal of streams A and B should be transparently transmitted in stream C using bits 5 and 6 respectively of time slot 0 not containing the frame alignment signal of stream C;

b) bit 5 should be transmitted in a corresponding way using bits 5 and 6 respectively of stream C.

3.4 *Multiframe structure in TS16 of streams A and B*

When used for channel associated signalling, TS16 of streams A and B is organized in multiframes as defined in Recommendation G.704, § 5.1.3. The definition of the alarm indications and the criteria for multiframe alignment loss and recovery are given in Recommendation G.735.

3.5 *Absolute delay*

The overall absolute delay introduced by a pair of interconnected transcoders (i.e. PCM to PCM) should be less than 500 microseconds for any of the 32 kbit/s channels and for any of the transparently transferred 64 kbit/s channels.

In the case of channel associated signalling, the overall delay introduced by a pair of interconnected transcoders (i.e. PCM to PCM) should be less than 3 milliseconds for any of the signalling channels.

3.6 *Synchronization*

3.6.1 *Send side*

So that the equipment may be inserted into a plesiochronous network, or into a synchronous network operating in degraded conditions, both PCM ports A and B at the send side should be provided with frame and multiframe resynchronizing devices, which initiate controlled sample slips (i.e. sample repetitions or deletions) as required.

It should be possible to synchronize the sending side to any one of the following:

- timing signal associated with incoming PCM stream A;
- timing signal associated with incoming PCM stream B;
- timing signal associated with incoming stream C;
- external 2048 kHz timing signal (see Recommendation G.703, § 10).

In the case of synchronization failure, the consequent action is a prompt maintenance alarm (see Table 8/G.761).

Note – Synchronization failure is assumed in case of a fault condition (see Note 2 to Table 8/G.761) on the incoming signal being used for synchronization.

3.6.2 *Receive side*

The receiving side should be synchronized to the timing signal associated with incoming stream C.

Note – The organization of the network should be such that controlled sample slips are avoided in normal operating conditions. This can lead to the need to synchronize the sending side to the receiving side in remote 30 channel PCM terminals. In circumstances where slips are unavoidable, they will affect both 32 kbit/s channels and directly transferred 64 kbit/s channels.

3.7 *Jitter*

The basic jitter requirements at interfaces are covered by the requirements of §§ 2.1 and 3.1.

When the sending side of the transcoder is synchronized to the incoming PCM stream A or B, and provided both streams A and B are synchronized to each other, slips should not occur when sinusoidal jitter having an amplitude lower then the maximum tolerable input jitter (see Figure 2/G.823) is present at one or both the input ports A and B.

Jitter transfer characteristics between various signal ports are under study.

3.8 *Direct time slot transfer*

It should be possible to manually programme the transcoder to transfer transparently at least two time slots from each of the two incoming PCM streams A and B into stream C.

For national applications, it is sometimes necessary to use more than two signalling bits per channel. In such cases, time slot 16 from PCM streams A and B should be transferred to/from time slots 16 and 17 respectively of stream C. The special processing of signalling bits as described in § 2.5.1.1.3 will not be required.

To be compatible with Recommendation G.735, § 2, at least TS6 and TS22 of each PCM stream A and B should be transferable. The positions of these time slots in the stream C frame are given below:

- TS6 of PCM stream A into TS5 of stream C;
- TS6 of PCM stream B into TS6 of stream C;
- TS22 of PCM stream A into TS22 of stream C;
- TS22 of PCM stream B into TS23 of stream C.

In the case of the transfer of more than two time slots, Table 7/G.761 indicates the allocation up to the maximum possible, taking account of the priority ordering given in Recommendation G.735, § 2.

If (n) 64 kbit/s time slots of PCM stream A (respectively B) are transferred transparently through the transcoder, then the transmission capabilities of PCM stream A (respectively B) will be limited to $(30-2n)$ channels. More precisely, with the frame structure of stream C given in § 2.2:

- when TS6 is transferred transparently, channel 5 of the same PCM stream cannot be used;
- when TS22 is transferred transparently, channel 22 of the same PCM stream cannot be used.

In the case of direct transfer, the transcoder will restitute the binary mark sequence corresponding to amplitude 1 for coding law A (see Recommendation G.712, § 4.3), in the non-usable time slot of PCM output streams A and B.

Note 1 – The need to transmit transparently more than two time slots per incoming PCM stream is under study.

Note 2 – The possibility of remotely controlling the choice of the time slots which are to be transmitted transparently is under study.

Note 3 – The octet sequence integrity is maintained by the transcoder in the case of direct transfer of several time slots at 64 kbit/s.

3.9 *In-service monitoring*

When the PCM to ADPCM and/or the ADPCM to PCM processing functions are multiplexed for 60 channels, in-service monitoring of these processing functions should be provided. This in-service monitoring should be implemented in such a way that it it possible to distinguish between failures affecting the send and receive sides separately.

Since no PCM (respectively ADPCM) signals are transmitted in TS0, the in-service monitoring can be implemented by inserting test signals into extra channels corresponding to TS0 of PCM streams A and B.

3.10 *Safeguarding of one PCM stream A or B*

As an option, safeguarding of one PCM tributary can be provided automatically, or otherwise, when a failure of the transcoder digital processing parts, or of the transcoder power supplies, have been detected. In this case the nominated PCM stream, A or B, should, for both directions of transmission, be made to bypass the transcoder and be connected to the transmission link in place of the normal stream C signal.

The simultaneous presence at state 1 of bits 7 and 8 of TS0 not containing the frame alignment signal in stream C on three consecutive occasions is used to indicate to the remote transcoder that the downstream transcoder has been switched to the safeguarding mode. When the safeguarding option is provided automatically, the procedure for the exchange of information between the two transcoders when switching to and from the safeguarding mode is under study.

Note 1 – The choice of the PCM stream (A or B) which will be safeguarded is made when the equipment is installed. It should be the same at both ends of the transmission link.

Note 2 – The use of the safeguarding facility can result in two 2048 kbit/s interfaces in cascade. It is then necessary to ensure, when installing the transcoder, that the combined attenuation of the station cabling at 1024 kHz on both sides of the transcoder is not greater than the maximum attenuation allowed by the equipment connected to the transcoder.

Note 3 – Before using the safeguarding facility, it should be checked that the bits 7 and 8 of TS0 not containing the frame alignment signal of the PCM stream to be safeguarded are in the idle state 1 as specified in Recommendation G.704, § 3.3.1.3.

3.11 *Fault conditions and consequent actions*

3.11.1 *Without safeguarding*

The fault conditions associated with the frames of streams A, B and C and the consequent actions, when the safeguarding option is not used, are given in Table 8/G.761.

When channel associated signalling is used, the fault conditions associated with the multiframes of streams A, B and C and their consequent actions are given in Table 9/G.761.

3.11.2 *With safeguarding*

When the safeguarding option is provided, Tables 8/G.761 and 9/G.761 must be used, with the exception of the fault condition "transcoder failure" of Table 8/G.761. Instead, the fault conditions and consequent actions given in Table 10/G.761 must be used, with reference to Figure 2/G.761.

TABLE 7/G.761

Order of priority for the transfer of 64 kbit/s time slots from streams A or B to stream C

Time slot in stream A	Time slot in stream B	Time slot in stream C
6		5
	6	6
22		22
	22	23
14		13
	14	14
30		30
	30	31
2		1
	2	2
18		18
	18	19
10		9
	10	10
26		26
	26	27
4		3
	4	4
20		20
	20	21
12		11
	12	12
28		28
	28	29
8		7
	8	8
24		24
	24	25
17 (Note 1)		15
	17 (Note 1)	17 (Note 2)

Note 1 – This time slot does not comply with the normal priority ordering given in Recommendation G.735, § 2.

Note 2 – Time slot 17 of stream C will not be available for direct transfer of time slot 17 of stream B when the PCM streams employ time slot 16 channel associated signalling with more than two signalling bits per channel (see § 2.5.1.2).

TABLE 8/G.761

Fault conditions on frames A, B and C and consequent actions without safeguarding

Consequent actions / Fault conditions	Prompt maintenance alarm indication	Bit 3 TS0 not containing the FAS stream		TS0 not containing the FAS stream C		Stream C – Apply into bits in TSI-31 associated with stream		AIS applied to stream		AIS applied to stream	TS0 not containing the FAS stream C	
		A	B	bit 3	bit 4	A (Note 2)	B (Note 3)	A	B	C	bit 7	bit 8
PCM stream A (Note 1)	Yes (Note 4)					11 . . . 11					1	
PCM stream B (Note 1)	Yes (Note 4)						11 . . . 11					1
PCM streams A and B (Note 1)	Yes (Note 4)									Yes		
Stream C (Note 1)	Yes (Note 4)							Yes	Yes			
TS0 stream A bit 3 to 1 (Note 6)				1								
TS0 stream B bit 3 to 1 (Note 6)					1							
TS0 stream C bit 3 to 1 (Note 6)		1										
TS0 stream C bit 4 to 1 (Note 6)			1									

TABLE 8/G.761 *(cont.)*

Consequent actions / Fault conditions	Prompt maintenance alarm indication	Bit 3 TS0 not containing the FAS stream		TS0 not containing the FAS stream C		Stream C – Apply into bits in TS1-31 associated with stream		AIS applied to stream		AIS applied to stream	TS0 not containing the FAS stream C	
		A	B	bit 3	bit 4	A (Note 2)	B (Note 3)	A	B	C	bit 7	bit 8
TS0 stream C bit 7 to 1								Yes				
TS0 stream C bit 8 to 1									Yes			
Transcoder failure, send side (Note 5)	Yes									Yes		
Transcoder failure, receive side (Note 5)	Yes							Yes	Yes			
Power supply failure	Yes							Yes if possible	Yes if possible	Yes if possible		
Synchronization failure of the sending side	Yes											

Note 1 – The fault conditions associated with streams A, B and C are: loss of signal, loss of frame alignment, error ratio greater than 10^{-3} as defined in Recommendation G.735, § 4.1.

Note 2 – Only in time slots and signalling bits associated with PCM stream A (both for 32 and 64 kbit/s channels).

Note 3 – Only in time slots and signalling bits associated with PCM stream B (both for 32 and 64 kbit/s channels).

Note 4 – The prompt maintenance alarm indication must be inhibited if the AIS is detected at the corresponding port.

Note 5 – The fault condition "transcoder failure" is detected by the in-service monitoring unit. The transcoder is equipped with such a unit if the digital signal processing is time-multiplexed between the 60-channels.

Note 6 – These fault conditions are not detected by the transcoder. The indications pass transparently through the transcoder (see § 2.6.3).

TABLE 9/G.761

Fault conditions on multiframes A, B and C and consequent actions

Consequent actions / Fault conditions	Prompt maintenance alarm indication	TS 16 frame 0 bit 6		TS 16 frame 0 stream C		TS 16 stream C frames 1-15		AIS TS 16		AIS TS 16	TS 16 frame 0 stream C	
		A	B	6	7	A (Note 2)	B (Note 3)	A	B	C	bit 5	bit 8
Multiframe A (Note 1)	Yes (Note 4)					1111					1	
Multiframe B (Note 1)	Yes (Note 4)						1111					1
Multiframe A and B (Note 1)	Yes (Note 4)									Yes		
Multiframe C (Note 1)	Yes (Note 4)							Yes	Yes			
Bit 6 TS 16 frame 0 stream A to 1 (Note 5)				1								
Bit 6 TS 16 frame 0 stream B to 1 (Note 5)					1							
Bit 6 TS 16 frame 0 stream C to 1 (Note 5)		1										
Bit 7 TS 16 frame 0 stream C to 1 (Note 5)			1									
Bit 5 TS 16 frame 0 stream C to 1								Yes				
Bit 8 TS 16 frame 0 stream C to 1									Yes			

Note 1 – The fault condition associated with the three multiframes is the loss of multiframe alignment.

Note 2 – Only in signalling bits associated with PCM stream A. The 1111.... bits are processed in accordance with § 2.5.1.1.3 and Tables 4/G.761 and 5/G.761.

Note 3 – Only in signalling bits associated with PCM stream B. The 1111.... bits are processed in accordance with § 2.5.1.1.3 and Tables 4/G.761 and 5/G.761.

Note 4 – The prompt maintenance alarm indication must be inhibited if the AIS in TS16 is detected at the corresponding port.

Note 5 – These fault conditions are not detected by the transcoder. The indications pass transparently through the transcoder (see § 2.6.6).

TABLE 10/G.761

Fault conditions and consequent actions when implementing the safeguarding option

Fault conditions / Consequent actions	Switching to the safeguarding mode		AIS in PCM stream not safeguarded	
	at (1)	at (2)	at (1)	at (2)
Transcoder failure at (1)	Yes		Yes if possible	Yes
Power supply failure at (1)	Yes		Yes if possible	Yes
TS0 stream C from (1) to (2) bits 7 and 8 in state 1		Yes		Yes

Note – The transcoder designations (1) and (2) are indicated in Figure 2/G.761.

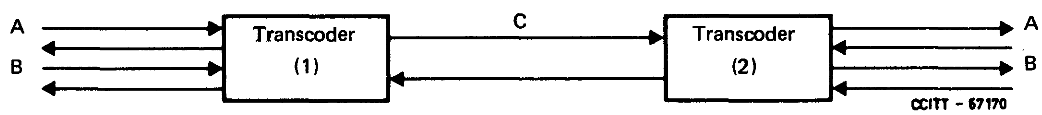


FIGURE 2/G.761

Use of 2 transcoders in a point-to-point link

Recommendation G.762

GENERAL CHARACTERISTICS OF A 48-CHANNEL TRANSCODER EQUIPMENT

(Melbourne, 1988)

1 General

The 48-channel transcoder provides for the conversion between two 24-channel 1544 kbit/s PCM streams and one 48-channel 1544 kbit/s ADPCM stream. In the 24-channel 1544 kbit/s streams, the voice-frequency signals are coded at 64 kbit/s according to the PCM μ-law defined in Recommendation G.711. In the 48-channel 1544 kbit/s stream, the voice-frequency signals are coded at 32 kbit/s according to the ADPCM encoding law defined in Recommendation G.721.

Figure 1/G.762 represents the nomenclature used for the three different signal ports X, Y and Z.

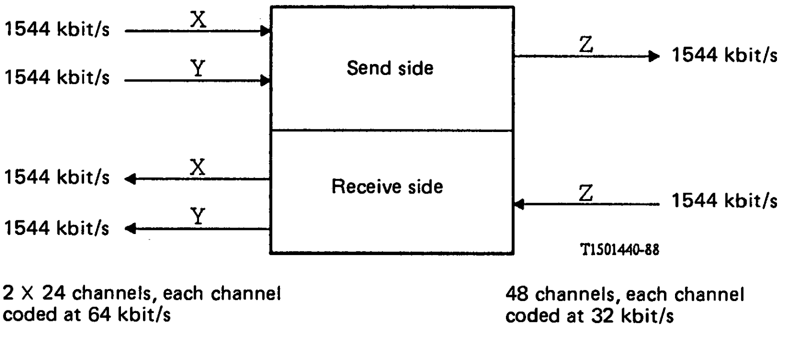


FIGURE 1/G.762

48-channel transcoder ports

The 1544 kbit/s stream associated with port Z can be partitioned into four independent 384 kbit/s entities defined as time slot groupings. Each 384 kbit/s time slot grouping consists of twelve 32 kbit/s time slots which can be used to transport up to 12 voice-frequency channels or 11 voice-frequency channels plus their channel associated a-b-c-d signalling information. Therefore, the 1544 kbit/s stream associated with port Z will have a maximum channel capacity of between 44 and 48 voice-frequency channels.

Note 1 – Administrations should take into account the guidance given in Recommendation G.721 concerning the use and transmission performance of 32 kbit/s ADPCM.

Note 2 – It should be noted that the transcoder equipment described in this Recommendation has a limited capability of transparently transporting 64 kbit/s data channels and this should be taken into account in the planning of networks which are likely to evolve into an ISDN (see § 4.4).

This Recommendation is divided into three parts:

– Paragraph 2 contains the interface requirements associated with port Z;

– Paragraph 3 contains the interface requirements associated with ports X and Y;

– Paragraph 4 contains the requirements which are specific to a 48-channel transcoder equipment realization.

2 Characteristics of a 1544 kbit/s signal organized in 32 kbit/s and/or 64 kbit/s time slots (port Z)

2.1 *Interface Z*

The electrical characteristics of the 1544 kbit/s interface are in accordance with § 2 of Recommendation G.703.

2.2 *Frame structure*

2.2.1 *Frame structure at 1544 kbit/s*

Refer to § 3.2.1 of Recommendation G.704 for the frame structure and use of derived channel time slots.

2.2.2 *Frame structure at 384 kbit/s*

Refer to § 3.2.3 of Recommendation G.704 for the frame structure at 384 kbit/s.

2.3 *Loss and recovery of frame and multiframe alignment*

2.3.1 *Loss and recovery of 1544 kbit/s frame and multiframe alignment*

The criteria for loss and recovery of the frame alignment and multiframe alignment signal for port Z are in accordance with § 2.1 of Recommendation G.706 for the 24-frame multiframe and for the 12-frame multiframe.

2.3.2 *Loss and recovery of delta channel multiframe alignment*

The criteria for loss and recovery of the signalling grouping channel multiframe alignment signal are in accordance with § 3.2.6 of Recommendation G.704.

2.4 *Signalling*

Refer to § 3.2.4 of Recommendation G.704 for signalling in the 384 kbit/s stream.

3 Characteristics of ports X and Y

3.1 *Interfaces X and Y*

The electrical characteristics of the 1544 kbit/s interface are in accordance with § 2 of Recommendation G.703.

3.2 *Frame structure*

Refer to § 2.1 of Recommendation G.704 for the frame structure and use of derived channel time slots.

3.3 *Loss and recovery of 1544 kbit/s frame and multiframe alignment*

The criteria for loss and recovery of the frame alignment and multiframe alignment signal for ports X and Y are in accordance with § 2.1 of Recommendation G.706 for the 24-frame alignment and for the 12-frame multiframe.

3.4 *Signalling*

Refer to § 3.1.3 of Recommendation G.704 and § 4.3 below.

4 Other characteristics of the 48-channel transcoder equipment

4.1 *48-channel frame structure*

In the case where streams X and Y are each carrying 24 voice-frequency signals and no channel-associated signalling information is present, stream Z will transmit the full complement of 48 channels. Table 1/G.762 shows the correspondence between the 64 kbit/s PCM channels in streams X and Y and the 32 kbit/s ADPCM channels in stream Z. Time slots 1-12 correspond to channels 1-12 from PCM stream X coded with 4 bits. Time slots 13-24 correspond to channels 13-24 from PCM stream X coded with 4 bits. Time slots 25-36 correspond to channels 1-12 from PCM stream Y coded with 4 bits. Time slots 37-48 correspond to channels 13-24 from PCM stream Y coded with 4 bits.

TABLE 1/G.762

Organization of the 1544 kbit/s frame for up to 48 channels at 32 kbit/s in stream Z

4 bit time slot of stream Z	1	2	3	4	5	6	7	8	9	10	11	12	Time slot Grouping 1
8 bit channel of stream X	1X	2X	3X	4X	5X	6X	7X	8X	9X	10X	11X	12X or SGC	
4 bit time slot of stream Z	13	14	15	16	17	18	19	20	21	22	23	24	Time slot Grouping 2
8 bit channel of stream X	13X	14X	15X	16X	17X	18X	19X	20X	21X	22X	23X	24X or SGC	
4 bit time slot of stream Z	25	26	27	28	29	30	31	32	33	34	35	36	Time slot Grouping 3
8 bit channel of stream Y	1Y	2Y	3Y	4Y	5Y	6Y	7Y	8Y	9Y	10Y	11Y	12Y or SGC	
4 bit time slot of stream Z	37	38	39	40	41	42	43	44	45	46	47	48	Time slot Grouping 4
8 bit channel of stream Y	13Y	14Y	15Y	16Y	17Y	18Y	19Y	20Y	21Y	22Y	23Y	24Y or SGC	

The signalling grouping channels for time slot groupings 1-4, when present in stream Z, occupy time slots 12, 24, 36 and 48 respectively. As shown in Table 2/G.762, the channel capacity for stream X (respectively Y) is reduced by one for each time slot grouping associated with stream X (respectively Y) configured with a signalling grouping channel. Selection of the time slot grouping format to include the signalling grouping channel (SGC) is made on a per-time slot grouping basis, independent of the other time slot groupings associated with stream X or Y.

TABLE 2/G.762

Unused channels in streams X and Y when the signalling grouping channel is present in a time slot grouping

Signalling grouping channel present	Unused channel
Time slot grouping 1	Channel 12 in stream X
Time slot grouping 2	Channel 24 in stream X
Time slot grouping 3	Channel 12 in stream Y
Time slot grouping 4	Channel 24 in stream Y

4.1.1 *Unused channels*

As explained in § 4.1, the presence of a signalling grouping channel in a time slot grouping causes a given channel in stream X or Y to be configured as unused.

The unused channels on the receive side of streams X and Y should have their data and signalling bits conditioned in a way that is compatible with downstream equipment.

The unused channels on the send side of streams X and Y are not processed.

4.2 *Selection of 1544 kbit/s multiframe formats*

Selection of either the 24-frame or 12-frame multiframe format at ports X, Y or Z is independent of the multiframe frame formats selected at the other ports.

4.3 *Signalling*

4.3.1 *Common-channel signalling*

A channel being used to convey common-channel signalling information in stream X or Y will not undergo the transcoding function. The signalling channel will be transmitted transparently in stream Z at the 64 kbit/s rate, as can other channels from streams X and Y in accordance with § 4.4.

4.3.2 *Channel-associated signalling*

Refer to Table 1/G.762 and Table 7/G.704 for the association of channel associated a-b-c-d signalling bits between streams X and Y and the signalling grouping channels in stream Z.

4.4 *Direct time slot transfer*

It should be possible to select and pass through 64 kbit/s channels from streams X and Y transparently into stream Z. Furthermore, it should be possible to pass through at least one 64 kbit/s channel in each time slot grouping stream Z.

The priority for selecting which time slots from streams X and Y should be directly transferred and their placement into stream Z is for further study.

4.4.1 *Channel-associated signalling in 64 kbit/s pass-through time slots*

The transcoder should allow for selection of reinsertion or no reinsertion of channel-associated signalling bits into the receive side of streams X and Y for channels which are passed-through transparently at 64 kbit/s.

4.4.2 *Conditioning of unused channels*

When 64 kbit/s channels from stream X (respectively Y) are transferred transparently into stream Z, the transmission capacity of PCM stream X (respectively Y) is reduced. The unused channels in stream X (respectively Y) should be conditioned as described in § 4.1.1.

4.5 *Signalling grouping channel alarm indications*

When signalling grouping channel frame alignment is lost (as per § 3.2.6 of Recommendation G.704), updating of the channel-associated signalling bits on the receive side of streams X and Y should be inhibited for the affected channels until frame alignment is regained.

A time slot grouping alarm is declared when the signalling grouping channel multiframe alignment signal is lost for 2 to 3 seconds.

When signalling grouping channel multiframe alignment is declared (as per § 3.2.6 of Recommendation G.704), updating of the channel-associated signalling bits on the receive side of streams X and Y will be enabled.

The time slot grouping alarm is released when signalling grouping channel multiframe alignment has been reacquired for 10 to 20 seconds.

On the send side, M_1 is set to 1 to transmit a time slot grouping alarm to the remote end when the near end is in time slot grouping alarm. On the receive side, a remote time slot grouping alarm is declared when M_1 has been set for 335 to 1000 milliseconds. Remote time slot grouping alarm is released when M_1 has been reset for 20 to 1000 milliseconds.

On the send side, M_2 is used to indicate a 1544 kbit/s alarm or a 1544 kbit/s AIS has been received on port X (time slot groupings 1 or 2) or port Y (time slot groupings 3 or 4). On the receive side, a signalling grouping channel AIS alarm is declared when M_2 has been set for 335 to 1000 milliseconds. Signalling grouping channel AIS is released when M_2 has been reset for 20 to 1000 milliseconds.

On the send side, M_3 is used to indicate a remote 1544 kbit/s alarm has been received on port X (time slot groupings 1 or 2) or port Y (time slot groupings 3 or 4). On the receive side, a remote signalling grouping channel AIS alarm is declared when M_3 has been set for 335 to 1000 milliseconds. Signalling grouping channel remote AIS alarm is released when M_3 has been reset for 20 to 1000 milliseconds.

4.6 *Fault conditions and consequent actions*

4.6.1 *1544 kbit/s fault conditions associated with stream Z*

A summary of the 1544 kbit/s fault conditions associated with the receive side of stream Z and the consequent actions are listed in Table 3/G.762.

The transcoder shall detect the following 1544 kbit/s fault conditions associated with stream Z:

i) loss of incoming signals at 1544 kbit/s;

ii) loss of 1544 kbit/s frame alignment;

iii) 1544 kbit/s alarm indication signal (AIS) received;

iv) 1544 kbit/s alarm indication received from the remote end.

4.6.2 *Consequent actions associated with stream Z*

Upon detection of 1544 kbit/s fault conditions in stream Z, appropriate actions should be taken which are in accordance with § 3.2 of Recommendation G.733. In addition, the following consequent actions should be taken as indicated in Table 3/G.762:

i) declare a 1544 kbit/s alarm on the receive side of port Z;

ii) send a 1544 kbit/s alarm indication to the remote end on the send side of port Z in accordance with § 4.2.4 of Recommendation G.733;

iii) send a 1544 kbit/s alarm indication signal (AIS) on the receive side of streams X and Y. The AIS consists of an all-1s signal in all channels including the framing bit;

iv) declare 1544 kbit/s AIS on the receive side of port Z;

v) declare a remote 1544 kbit/s alarm on the receive side of port Z;

vi) send a 1544 kbit/s alarm indication to the remote end on the receive side of streams X and Y in accordance with § 4.2.4 of Recommendation G.733.

TABLE 3/G.762

1544 kbit/s fault conditions associated with stream Z and consequent actions

Fault conditions \ Consequent actions	Declare 1544 kbit/s alarm on Z	Send 1544 kbit/s alarm indication to remote end on Z	Send 1544 kbit/s AIS on X and Y	Declare 1544 kbit/s AIS on Z	Declare remote 1544 kbit/s alarm on Z	Send 1544 kbit/s alarm indication to remote end on X and Y
Loss of incoming signal at 1544 kbit/s	Yes	Yes	Yes			
Loss of 1544 kbit/s frame alignment	Yes	Yes	Yes			
1544 kbit/s AIS received		Yes	Yes	Yes		
1544 kbit/s alarm indication received from remote end					Yes	Yes

4.6.3 *Fault conditions associated with the signalling grouping channel*

A summary of the signalling grouping channel fault conditions associated with the receive side of stream Z and the consequent actions are listed in Table 4/G.762.

The transcoder shall detect the following signalling grouping channel fault conditions associated with stream Z:

i) loss of signalling grouping channel multiframe alignment on a single time slot grouping associated with port X or a single time slot grouping associated with port Y;

ii) loss of signalling grouping channel multiframe alignment on both time slot groupings associated with port X or both time slot groupings associated with port Y;

iii) remote time slot grouping alarm indication (M_1) received from the remote end on a single time slot grouping associated with port X or a single time slot grouping associated with port Y;

iv) remote time slot grouping alarm indication (M_1) received from the remote end on both time slot groupings associated with port X or both time slot groupings associated with port Y;

v) signalling grouping channel AIS (M_2) received from the remote end on a single time slot grouping associated with port X or a single time slot grouping associated with port Y;

vi) signalling grouping channel AIS (M_2) received from the remote end on both time slot groupings associated with port X or both time slot groupings associated with port Y;

vii) remote signalling grouping channel AIS (M_3) received from the remote end on a single time slot grouping associated with port X or a single time slot grouping associated with port Y;

viii) remote signalling grouping channel AIS (M_3) received from the remote end on both time slot groupings associated with port X or both time slot groupings associated with port Y.

4.6.4 *Consequent actions associated with the signalling grouping channel*

Upon detection of signalling grouping channel fault conditions in stream Z, the following consequent actions shall be taken as indicated in Table 4/G.762:

i) declare time slot grouping alarm on the associated time slot grouping;

ii) send a time slot grouping alarm indication to the remote end by forcing the M_1 bit within the affected signalling grouping channel to 1;

iii) condition the data in the affected channels on the receive side of streams X or Y to provide a signal that is compatible with downstream equipment;

iv) condition the channel-associated signalling bits in affected channels on the receive side of streams X or Y to provide a signal that is compatible with downstream equipment. An example for most signalling types would be universal trunk conditioning where the signalling bits should be forced to the idle state for 2 to 3 seconds, and then conditioned to simulate the channel seized condition;

v) send a 1544 kbit/s AIS on the receive side of stream X (for time slot groupings 1 and 2) or stream Y (for time slot groupings 3 and 4). The AIS consists of an all 1s signal in all channels including the framing bit;

vi) declare a remote time slot grouping alarm condition on the associated time slot grouping to indicate the reception of a remote time slot grouping alarm indication in the M_1 bit of the affected signalling grouping channel;

vii) send a 1544 kbit/s alarm indication to the remote end on the receive side of stream X (for time slot groupings 1 and 2) and stream Y (for time slot groupings 3 and 4);

viii) declare a signalling grouping channel AIS condition on the associated time slot grouping to indicate the reception of a signalling grouping channel AIS indication in the M_2 bit of the affected signalling grouping channel;

ix) declare a remote signalling grouping channel AIS condition on the associated time slot grouping to indicate the reception of a remote signalling grouping channel AIS indication in the M_3 bit of the affected signalling grouping channel.

4.6.5 *Fault conditions associated with streams X and Y*

A summary of the fault conditions associated with the frames of streams X and Y and the consequent actions are listed in Table 5/G.762.

The transcoder shall detect the following fault conditions associated with streams X and Y:

i) loss of incoming signals at 1544 kbit/s;

ii) loss of 1544 kbit/s frame alignment;

iii) 1544 kbit/s AIS received from remote end;

iv) 1544 kbit/s alarm indication received from the remote end.

4.6.6 *Consequent actions associated with streams X and Y*

Upon detection of the 1544 kbit/s fault conditions associated with streams X and Y, the following consequent actions shall be taken in Table 5/G.762:

i) declare 1544 kbit/s alarm on the send side of port X and Y;

ii) send a 1544 kbit/s alarm indication to the remote end on the receive side of streams X and Y in accordance with § 4.2.4 of Recommendation G.733;

iii) send a signalling grouping channel AIS to the remote end by forcing the M_2 bit within the affected signalling grouping channel(s) to 1;

iv) condition the affected channels on the send side of stream Z to provide a signal in all channels that is compatible with downstream equipment;

v) declare 1544 kbit/s AIS on the send side of port X or Y;

vi) declare remote 1544 kbit/s alarm on the send side of port X or Y;

vii) send a signalling grouping channel AIS to the remote en by forcing the M_3 bit within the affected signalling grouping channel(s) to a 1.

TABLE 4/G.762

Signalling grouping channel fault conditions associated with stream Z and consequent actions

Consequent actions / Fault conditions	Declare time slot grouping alarm	Send time slot grouping alarm indication to remote end	Condition affected channels on X or Y	Condition signalling in affected channels on X or Y	Send 1544 kbit/s AIS on X or Y	Declare remote time slot grouping alarm	Send 1544 kbit/s alarm indication to remote end on X or Y	Declare signalling grouping channel AIS	Declare remote signalling grouping channel AIS
Loss of signalling grouping channel multiframe alignment (single time slot grouping)	Yes	Yes	Yes	Yes					
Loss of signalling grouping channel multiframe alignment (time slot grouping pair)	Yes	Yes			Yes				
Remote time slot grouping alarm indication received (single time slot grouping)			Yes	Yes		Yes			
Remote time slot grouping alarm indication received (time slot grouping pair)						Yes	Yes		

TABLE 4/G.762 *(cont.)*

Consequent actions / Fault conditions	Declare time slot grouping alarm	Send time slot grouping alarm indication to remote end	Condition affected channels on X or Y	Condition signalling in affected channels on X or Y	Send 1544 kbit/s AIS on X or Y	Declare remote time slot grouping alarm	Send 1544 kbit/s alarm indication to remote end on X or Y	Declare signalling grouping channel AIS	Declare remote signalling grouping channel AIS
Signalling grouping channel AIS received (single time slot grouping)			Yes	Yes				Yes	
Signalling grouping channel AIS received (time slot grouping pair)					Yes			Yes	
Remote signalling grouping channel AIS received (single time slot grouping)			Yes	Yes					Yes
Remote signalling grouping channel AIS received (time slot grouping pair)							Yes		Yes

TABLE 5/G.762

1544 kbit/s fault conditions associated with streams X and Y and consequent actions

Consequent actions / Fault conditions	Declare 1544 kbit/s alarm	Send 1544 kbit/s alarm indication to remote end	Send signalling grouping channel AIS	Condition affected channels in stream Z	Declare 1544 kbit/s AIS	Declare remote 1544 kbit/s alarm	Send signalling grouping channel AIS indication to remote end
Loss of incoming signal at 1544 kbit/s	Yes	Yes	Yes	Yes			
Loss of 1544 kbit/s frame alignment	Yes	Yes	Yes	Yes			
1544 kbit/s AIS received		Yes	Yes	Yes	Yes		
1544 kbit/s alarm received from remote end						Yes	Yes

4.7 *Synchronization*

It should be possible to currently synchronize the outgoing streams of ports X, Y and Z to any one of the following:

- timing signal associated with incoming PCM stream X;
- timing signal associated with incoming PCM stream Y;
- timing signal associated with incoming stream Z;
- internal 1544 kbit/s timing signal.

4.8 *Absolute delay*

The overall absolute delay introduced by a single transcoder in either direction (PCM to ADPCM or ADPCM to PCM) should be no greater than 750 microseconds for any of the 48 channels.

When a 64kbit/s signal is transparently transferred through a single transcoder, the absolute delay introduced should be no greater than 750 microseconds in either direction. Frame integrity should be maintained for adjacent 64 kbit/s channels (i.e. equal delay).

In the case of channel associated signalling, the overall delay introduced by a single transcoder should be no greater than 5.0 milliseconds.

4.9 *Jitter*

For further study.

Recommendation G.763

DIGITAL CIRCUIT MULTIPLICATION EQUIPMENT USING 32 KBIT/S ADPCM AND DIGITAL SPEECH INTERPOLATION

(Melbourne, 1988)

1 General

1.1 *Scope*

This Recommendation is intended as an introduction to digital circuit multiplication equipment and systems, and as a base document for the specification of Digital Circuit Multiplication Equipment (DCME) and Digital Circuit Multiplication Systems (DCMS).

Essential facilities, interface conditions and overall performance requirements are given. Requirements for full compatibility and interoperability are under study (see Supplemnent N° 31 at the end of this fascicle).

1.2 *Attributes*

Digital circuit multiplication equipment is utilized as a means of augmenting the capacity of digital transmission systems operating between several International Switching Centers (ISCs). DCME has all of the following attributes:

- digital speech interpolation (DSI);
- low rate encoding (LRE);
- dynamic load control (DLC) arrangement in association with interfacing;
- capability to accommodate the following types of bearer service requirements:
  - i) speech,
  - ii) 3.1 kHz audio (data and speech),
  - iii) 64 kbit/s unrestricted (transparent),
  - iv) alternate speech/64 kbit/s unrestricted.

The link between two DCMEs is generally one where a highly efficient traffic carrying capability is required, e.g., a long-distance link.

1.3 *Application*

This Recommendation is applicable to the design of digital circuit multiplication equipment intended for, but not limited to, use in an international digital circuit. Freedom is permitted in design details which are not covered in this Recommendation (see Note).

Note – Several additional items yet to be fully considered include the evaluation of:

- instantaneous 2-bit speech encoding on overloads (to avoid clipping), and voice-band data rate discrimination (to permit rates less than or equal to 4800 bit/s to be coded at 32 kbit/s only and to increase bearer channel efficiency).
- silence elimination techniques (to permit saving of bearer channel capacity during the inactive periods of half-duplex voice-band data calls).

2 Definitions relating to digital circuit multiplication equipment

2.1 digital circuit multiplication equipment (DCME)

A general class of equipment which permits concentration of a number of 64 kbit/s PCM encoded input trunk channels on a reduced number of transmission channels (see § 2.7).

2.2 digital circuit multiplication system (DCMS)

A telecommunications network comprised of two or more DCME terminals where each DCME terminal contains a transmit unit and a receive unit.

2.3 low rate encoding (LRE)

A voice-band signal encoding method, e.g. adaptive differential pulse code modulation (ADPCM), which results in a bit rate less than 64 kbit/s, e.g. 40 kbit/s, 32 kbit/s, or 24 kbit/s.

Note – Conversion between speech signals encoded in PCM at 64 kbit/s and those encoded in ADPCM must be carried out by means of transcoding processes given in Recommendations G.721 and G.723.

2.4 variable bit rate (VBR)

The capability of the encoding algorithm to dynamically switch between 32 and 24 kbit/s for speech traffic under control of the DCME.

2.5 digital speech interpolation (DSI)

A process which, when used in the transmit unit of a DCME, causes a trunk channel (see § 2.9) to be connected to a bearer channel (see § 2.8) only when activity is actually present on the trunk channel. Thus, by exploiting the probability of the speech activity factor (see § 2.14) of trunk channels being less than 1.0, enables the traffic from a number of trunk channels to be concentrated and carried by a lesser number of time-shared bearer channels. The signals carried by a bearer channel, therefore, represent interleaved bursts of speech signals derived from a number of different trunk channels.

Note – A process complementary to DSI is required in the receive unit of a DCME, i.e, assignment of the interleaved bursts to their appropriate trunk channels.

2.6 DCME frame

A time interval, the beginning of which is identified by a «unique word» in the control channel. The DCME frame need not coincide with the multiframes defined in Recommendation G.704. The format specification of the DCME frame includes channel boundaries and bit position significance.

2.7 transmission channel

A 64 kbit/s time slot within a DCME frame.

2.8 bearer channel (BC)

A bearer channel is a unidirectional, digital, transmission path from the transmit unit of one DCME to the receive unit of a second associated DCME and which is used to carry concentrated traffic between the two DCMEs.

Note 1 – A number of bearer channels in each direction of transmission form the both-way link required between two DCMEs. This link may be, for example, a 2048 kbit/s system.

Note 2 – A bearer channel may have any of the following instantaneous bit rates: 24, 32, 40 and 64 kbit/s.

2.9 trunk channel (TC)

A unidirectional, digital transmission path (generally short distance) used for carrying traffic and which connects a DCME to other equipment, e.g. an International Switching Centre (ISC). Two such trunk channels (transmit and receive) are needed by 4-wire telephone circuits and constitute a trunk circuit.

Note 1 – Signals carried by a trunk channel will be transmitted at a bit rate of 64 kbit/s.

Note 2 – A number of trunk channels in each direction of transmission are required between a DCME and, for instance, an ISC. These trunk channels may be carried by a number of 1544 of 2048 kbit/s systems.

2.10 assignment message

The message specifying the interconnections required between trunk channels and bearer channels.

2.11 assignment map

A record, held in a memory of a DCME, of the interconnections required between trunk channels and bearer channels. This record is dynamically uptated in real time in accordance with the traffic demands made on the DCME.

2.12 control channel

A unidirectional transmission path from the transmit unit of one DCME to the receive unit of one or more associated DCMEs and which is dedicated primarily to carrying channel assignment messages. In addition, the control channel transmits other messages such as idle noise levels, dynamic load control, and alarm messages.

Note – An alternative name for «control channel» is «assignment channel».

2.13 ensemble activity

The ratio of the time active signals and their corresponding hangover time and front-end delay occupy the trunk channels, to the total measuring time, averaged over the total number of trunk channels included in the measurement.

2.14 speech activity factor

The radio of the time speech signals with their corresponding hangover time and front-end delay occupy a trunk channel, to the total measuring time, averaged over the total number of trunk channels carrying speach.

2.15 voice band data ratio

The radio of the number of trunk channels carrying voice-band data signals to the total number of trunk channels averaged over a fixed interval of time.

2.16 64 kbit/s unrestricted digital data ratio

The radio of the number of trunk channels carrying 64 kbit/s unrestricted digital data signals, to the total number of trunk channels averaged over a fixed interval of time.

2.17 **DCME overload (mode)**

The condition when the number of input trunk channels instantaneously active carrying speech exceeds the number of 32 kbit/s channels available for interpolation.

2.18 **overload channels**

The additional bearer channel capacity which is generated using variable bit rate (VBR) encoding to minimize or eliminate DSI competitive clipping.

2.19 **average bits per sample**

The average number of encoding bits per sample computed over a given time window for the ensemble of active interpolated bearer channels within a given interpolated pool. Only bearer channels carrying speech are included in this calculation.

2.20 **transmission overload**

The condition when the average bits per sample goes beyond the value set in accordance with speech quality requirements.

2.21 **freeze-out**

The condition when a trunk channel becomes active and cannot immediately be assigned to a bearer channel, due to lack of available transmission capacity.

2.22 **freeze-out fraction (FOF)**

The ratio of the total time that the individual channels experience the freeze-out condition to the total time of the active intervals and their corresponding hangover times and front-end delays, for all trunks over a fixed interval of time, e.g. one minute.

2.23 **interpolation gain (IG)**

The trunk channel multiplication ratio which is achieved through DSI. The IG is the ratio of the number of trunk channels to the number of DCME bearer channels where the same signal encoding rate is used for trunk and bearer channels. The achievable gain depends on the ensemble activity and the system size.

2.24 **transcoding gain (TG)**

The transmission channel multiplication ratio which is achieved through LRE, which effectively creates a number of low rate encoded bearer channels which is greater than the number of available transmission channels. When only a transcoding process conforming to Recommendation G.721 (i.e 32 kbit/s ADPCM) is used, the TG will equal 2. When no transcoding is used the TG will equal 1. When overload channels are created the TG will be greater than 2.

2.25 **DCME gain (DCMG)**

The trunk channel transmission multiplication ratio, which is achieved through application of DCME, including LRE and DSI. Hence DCMG = TG · IG.

2.26 **clique**

A set of bearer channels which are associated with a set of trunk channels and which are independent in operation and control from other bearer channels. The set of trunk channels is directed to a single destination.

Note – An alternate term for clique is «bundle».

2.27 **multi-clique mode**

A DCME operational mode in which more than one clique is used when each clique is associated with a different destination.

2.28 **multi-destination mode**

A DCME operational mode where traffic is exchanged between more than two (2) corresponding DCMEs simultaneously and trunk channel traffic is interpolated over a pool of available bearer channels for all destinations having traffic in the pool. The transmit trunk channels are designated to receive trunk channels at corresponding locations.

3 Tutorial

3.1 *Use of digital circuit multiplication system (DCMS)*

DCMS provides the means to reduce the cost of long distance transmission by making use of the combination of Digital Speech Interpolation (DSI) and Low Rate Encoding (LRE) techniques.

DSI is used to concentrate a number of input channels (generally referred to as trunk channels) onto a smaller number of output channels (generally referred to as bearer channels). It does this by connecting a trunk channel to a bearer channel only for the period that the trunk channel is active, i.e. is carrying a burst of speech or voice-band data. Since in average conversations one direction of transmission is active for only 30 to 40 per cent of the time, if the number of trunks is large the statistics of the speech and silence distributions will permit a significantly smaller number of bearer channels (bearer channel pool) to be used. Control information must also be passed between the terminals to ensure that bearer and trunk channel assignments at each end remain synchronized.

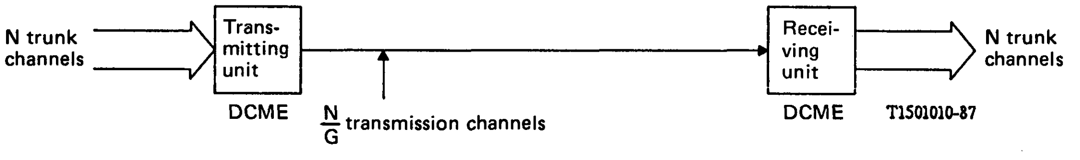
LRE uses digital filtering techniques to construct an estimate of the waveform at both the encoder and the decoder. Since the actual information rate of speech is much lower than the channel Nyquist rate, the link used between the LRE encoder and the decoder can operate at a rate which is dependent mainly on the quality of the models and the permissible amount of transmission degradation. The CCITT has standardized in Recommendations G.721 and G.723 a type of LRE known as ADPCM, the performance of which has been extensively characterized.

The simplest way to use DCMS is in the single destination mode as shown in Figure 1/G.763. This mode of operation, is most economic for the largest routes. For smaller routes there are two options:

- operation in multi-clique mode;
- operation in multi-destination mode.

Operation in multi-clique mode, see Figure 2/G.763, divides the bearer channels into a number of blocks or «cliques», each associated with a different route. There is a fixed boundary between cliques, and trunk/bearer channel assignments are generally carried in a control channel within the clique that they refer to. This limits the dynamic processing of received channels to those which are contained in the wanted clique; selection of the wanted clique channels can be done using a simple static digital switch without reference to the assignment information. With a 2048 kbit/s bearer system in multi-clique DCMS, the statistics of the DSI are unpromising with more than three routes.

Operation in multi-destination mode, see Figure 3/G.763, permits any bearer channel to be associated with any trunk channel of any of a number of different routes. There is no segregation of routes on the bearer, and therefore at the receive terminal it is impossible to select the wanted channels without reference to the assignment information. Multi-destination mode is economic for very small routes via satellite, but practical difficulties limit the number of routes which is desirable to have on a single DCMS.



G Digital circuit multiplication gain (DCMG)

FIGURE 1/G.763

Point-to-point mode
(only one direction shown)

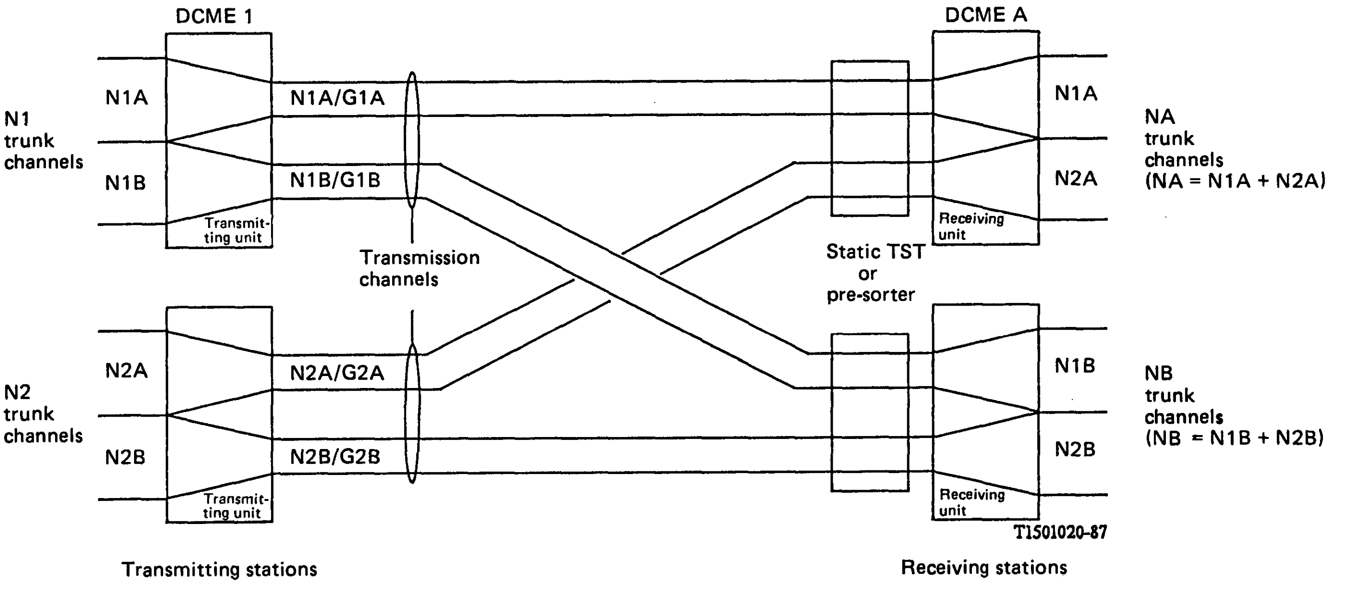


FIGURE 2/G.763

Multi-clique mode
(only one direction shown)

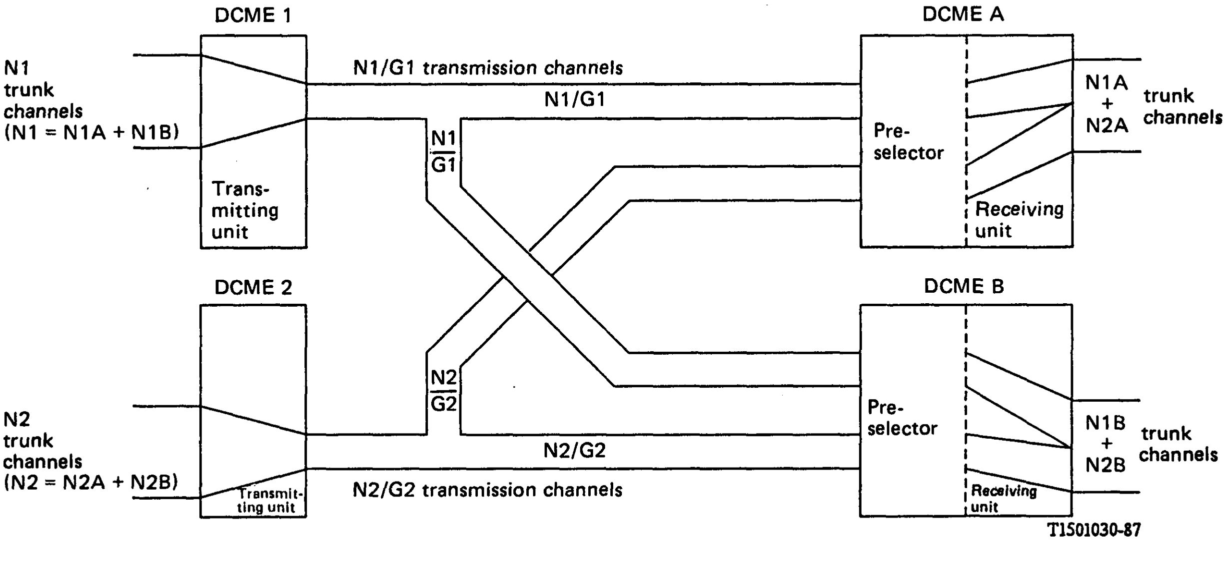


FIGURE 3/G.763

Multi-destination mode
(only one direction shown)

3.2 *Location*

Location of DCME depends on its use. Equipment used in single destination mode or in multi-clique mode can in general be located at the:

- ISC,
- earth station,
- cable head,

without significant restrictions.

Equipment used in the multi-clique mode will typically be located at the ISC so that the advantages of DCMG can be extended over the national section.

Equipment used in the multi-destination mode will typically be located at the earth station or cable head. The reason for this is that whereas in multi-clique mode the number of receive bearer channels at the DCME terminal is approximately equal to the number of transmit bearer channels, in multi-destination mode the number of receive bearer channels at the DCME terminal is the number of transmit bearer channels multiplied by the number of destinations. It therefore may be uneconomic to provide sufficient transmission capacity between the earth station and the ISC to permit location of multi-destination DCME at an ISC.

3.3 *Transmission requirements*

DCMS is usually required to carry any traffic which can be carried on ordinary General Switched Telephone Network (GSTN) connections. That includes voice-band data using V-series GSTN modems and facsimile calls following Recommendations T.4 and T.30 and using V.29 modems. In addition, in the ISDN, 64 kbit/s unrestricted on-demand digital data and alternate speech/64 kbit/s unrestricted bearer services must be carried.

DCMS are primarily designed to maximize the efficiency of speech transmission. Use with voice-band data especially at high rates, presents problems. These problems are mainly due to the difficulty for 32 kbit/s ADPCM to encode voice-band data waveforms.

3.4 *DCME gain (DCMG)*

The gain of DCME is the input trunk channel transmission multiplication ratio, which is achieved through application of DCME, including LRE and DSI (for a specified speech quality at a certain level of bearer channel activity). The maximum available gain depends on:

- number of trunk channels;
- number of bearer channels;
- trunk channel occupancy;
- speech activity;
- voice-band data traffic;
- ratio of half duplex to full duplex voice-band data;
- type of signalling;
- 64 kbit/s traffic;
- minimum acceptable speech quality;
- dynamic load control threshold.

Of these, the factor which has the greatest significance is the percentage of 64 kbit/s digital data traffic. This is because a trunk channel carrying 64 kbit/s traffic requires two 32 kbit/s bearer channels to be removed from the pool of channels available to the DSI process.

The percentage of voice-band data typically varies between 5 and 30 per cent, depending on the route. It is not unusual for a route to show more than a 2:1 variation, depending on time of day, with peaks which may or may not coincide for speech and voice-band data.

The type of signalling system used on the route can significantly affect the gain. Continuously compelled signalling systems hold channels active for undesirably long periods. In the case of Signalling System R2 digital signalling via a DCMS used on a satellite, the channel might be active for 5 to 14 seconds (Signalling System R2 also requires capacity for line signalling).

The measured speech activity depends on the characteristics of the activity detector. It is usual to assume an activity of 35 to 40 per cent. Outside of the route busy hour the occupancy of the trunk channels by traffic will be lower than during the route busy hour. The effect of this is to reduce the activity measured by the activity detector to about 27 per cent outside the route busy hour, whereas it will be close to the speech activity factor, i.e. about 40 per cent, during the route busy hour.

The speech quality is governed by two main factors: the LRE rate, and the amount of speech lost while a newly active trunk channel is awaiting connection to a bearer channel. If there are a great many newly active trunk channels in competition, the beginning of a burst of speech is more likely to be «clipped» of «frozen out» than if relatively few trunk channels are active.

The speech quality of a DCME in a network with external echo control devices may be affected by clipping introduced by echo control devices and by a possible noise contrast effect. In particular when echo suppressors or echo cancellers are used on low noise circuits, suppression of the far end noise may be objectionable due to noise contrast. Possible means of eliminating this problem are use of echo control devices which insert idle line noise at the appropriate level during suppression periods, or insertion of idle line noise at the DCME during the relevant period when the echo control device is integrated in the DCME.

When commissioning a new DCMS, observations should be made of the type and characteristics of the traffic which will use it. It is unwise to rely solely on customer complaints to indicate when a system is poorly dimensioned since interactions between the DCMS and echo control [1)] may obscure the true problem. Furthermore the consquence of trying to concentrate too may trunk channels onto too few bearers may be simply to increase the calling rate and to reduce the call holding time. This may result in greatly reduced quality, especially where continuously compelled signalling systems are used, and in levels of trunk channel activity far above what was envisaged in the original system dimensioning.

Two possible criteria for acceptable speech performance are: an average of 3.7 bits per sample and les than two per cent probability of clipping exceeding 50 ms, or alternatively less than 0.5 per cent of speech lost due to clipping.

Using the above criteria, approximations have been derived that relate the percentage of voice-band data and the number of trunk channels to the gain of a DCME using 30 bearer channels. These approximations are intended for use in initial system dimensioning and are as follows:

$G = 0.42 + 0.73 (\log_e T)$ for less than 7% voice-band data,

$G = -1.15 + \log_e T$ for less than 15% voice-band data,

where

G Gain

T Number of trunk channels.

These simple approximations are only valid for between 30 and 150 trunk channels with a channel activity of 37 per cent. If operation with fewer bearer channels is envisaged, then the approximations given above will tend to overestimate the achievable gain and this must be taken into account. If a more accurate representation is required, it will be necessary to carry out a first order Markov chain analysis referred to in the literature on DSI [1], [2], [3].

3.5 *ISDN bearer services*

DCMS are generally required to carry the full range of ISDN bearer services which can be provided on a 64 kbit/s channel as specified in Recommendation I.231. These are:

– circuit mode 64 kbit/s unrestricted, 8 kHz structured bearer service category.

  This category may be used among other things for speech, multiple sub-rate information streams multiplexed by the user, or for transparent access to an X.25 public network.

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1) The highest speech quality is obtained when echo cancellers conforming to Recommendation G.165 are used for echo control. However echo suppressors conforming to Recommendation G.164 and G.161 may be used.

- circuit mode 64 kbit/s, 8 kHz structured bearer service category, usable for speech information transfer.

  This is broadly similar to the preceding category, but with different access protocols.

- circuit mode 64 kbit/s, 8 kHz structured bearer service category, usable for 3.1 kHz audio information transfer.

  This bearer service provides the transfer of 3.1 kHz bandwith audio information, for example voice-band data via modems, Group I, II and III facsimile information, and speech.

- circuit mode alternate speech/64 kbit/s unrestricted 8 kHz structured bearer service category.

  This service is similar to both the unrestricted and speech 64 kbit/s circuit-mode bearer services, but provides for the alternate transfer of either voice or unrestricted digital information at 64 kbit/s within the same call.

3.6 *Restoration of services*

For most applications, the loss of traffic under failure conditions would be such that the installation of a single pair of terminals on a route would be insufficient without a means of rapid changeover to spare equipment in the event of failure. This means that DCME is often used in a cluster of *n* active terminals and one standby terminal to be loaded with the configuration information of the failed terminal. Other automatic fallback modes may be considered.

Failure of the transmission system between DCME terminals can be handled by normal transmission system restoration procedures. Failure of the transmission systems entering the DCME terminals from the exchanges may result in a wide range of different alarm conditions being experienced, particularly where a multi-destination DCME terminal serves more than one exchange and more than one route. It is desirable to limit the generation of alarm conditions to the channels which have actually failed.

3.7 *Control of transmission overload*

A reduction in the number of bearer channels available to the interpolation process can occur due to high activity of voice-band and 64 kbit/s data services or statistical variations in the ensemble input speech activity. This can lead to overload, where the number of instantaneously active trunk channels exceeds the number of available bearer channels. Action is then required to safeguard speech quality. There are four possible solutions:

- The system can be dimensioned so that with the maximum anticipated short-term trunk channel activities there is negligible probability of violating the speech quality criteria. This employs the DCMS very inefficiently outside the busy hour.

- A multi-destination system can be made to carry routes with widely different busy hours, so that although the trunk channels might have relatively low non-busy hour occupancy, the bearer channels would always be well loaded.

- Signals can be sent from the DCME to the exchange to busy-out part of the route when the quality criteria are violated. This is known as Dynamic Load Control (DLC), and can be an effective control method. However, it cannot be retroactive and it is slow to take effect. Furthermore, care must be taken to ensure that when circuits are returned to service the increase in bearer channel activity is not sufficient to result in the immediate reapplication of DLC.

- The signal-to-quantization performance can be traded against the clipping of speech burst. By using variable rate ADPCM algorithms, it is possible to quantize to three, rather than four, bits on individual speech channels on a pseudo-cyclic basis for a given number of samples. In this way the system can be given a gradual degradation characteristic, rather than a sudden overloading.

Practical DCMS are likely to require some or all of these techniques to be used.

3.8 *Control channel*

Because the assignment of trunk channels to bearer channels is continually changing , it is necessary to provide a control information channel between the transmit and the receive units to ensure that their assignment maps correspond. This channel carries information for assignments, changes of coding rates, message refreshments, 64 kbit/s channel allocations and other system and management messages. It should be carried in a permanently allocated time slot which includes forward error correction, so that transmission errors do not cause the transmit and receive assignment maps to go out of step.

4 DCME functions

This Recommendation is applicable to DCME designs in both directions of transmission.

The purpose of DCME is to provide maximum effective use of transmission facilities in the digital operating environment, using DSI and LRE techniques. At a minimum, the DCME functions shall include:

- interpolation of speech signals (DSI);
- transcoding of 64 kbit/s PCM to ADPCM (LRE) when applicable;
- the means to carry the ISDN bearer services given in § 4.4;
- one or more of the following operating modes:
  - i) point-to-point,
  - ii) multi-clique,
  - iii) multi-destination;
- speech detection;
- voice-band data detection;
- a means for transmit detection and receive injection of background noise;
- the means to accommodate non-interpolated preassigned traffic;
- a means for interterminal communication (control channel);
- a means for exchanging signals with an ISC for purposes of ISDN bearer services involving 64 kbit/s unrestricted taffic, DLC, and alarms;
- time slot interchange;
- the ability to support the signalling systems identified in § 4.12.

4.1 *Digital speech interpolation*

The DCME shall incorporate digital speech interpolation (DSI) techniques to achieve a reduction in the composite transmission rate of the 64 kbit/s trunk channels.

4.2 *DCME low rate encoding algorithm*

The DCME shall operate with a nominal low rate encoding gain of 2:1 through the use of adaptive differential pulse code modulation (ADPCM) techniques. The DCME shall incorporate the algorithms defined in Recommendation G.721 and G.723. These algorithms include provisions for transcoding the 64 kbit/s PCM input signal to 24 kbit/s ADPCM during overload conditions, to 32 kbit/s ADPCM during normal operation, and to 40 kbit/s for voice-band data.

4.3 *DCME gain*

The DCME shall combine digital speech interpolation and low rate encoding techniques to achieve a reduction in the composite transmission rate of the 64 kbit/s trunk channels.

4.4 *DCME bearer services*

The DCME shall respond to the following ISDN bearer service requests from its associated ISCs:

a) speech;

b) 3.1 kHz audio (data and speech);

c) 64 kbit/s unrestricted.

4.5 *Operational modes*

The following three modes of operation are described:

a) point-to-point;
b) multi-clique; and
c) multi-destination.

4.5.1 *Point-to-point mode* (see Figure 1/G.763)

The transmit side DCME concentrates *N* trunk channels at 64 kbit/s into *N/G* transmission channels. The transmission channels represent a number of time shared variable bit rate (bearer) channels which are grouped into a primary rate multiplex format.

At the receive side, the receiving DCME simply demultiplexes the primary-rate format and reconstitutes the *N* trunk channels from the *N/G* transmission channels.

4.5.2 *Multi-clique mode* (see Figure 2/G.763)

In this mode the pool of bearer channels is subdivided into two or three independant pools (cliques) of fixed capacity, each pool corresponding to an individual destination While the aggregate bearer bit rates for both the transmit side and the receive side are equal, the DCMG of each clique may be different, since this gain is a function of the number of input channels, routed within each clique.

It is desirable to limit the number of cliques within a primary-rate bearer to two or three. Figure 2/G.763 indicates one from of this approach in which the primary-rate bearer circuit is assumed to be available to each of the DCM nodes, but each node has the capability of preselecting the traffic that is intended for it.

4.5.3 *Multi-destination mode* (see Figure 3/G.763)

In this mode, the input trunk channels are interpolated over a common pool of bearer channels, regardless of their destination. The input trunk channels are destination preassigned so that they may be routed to the appropriate destination in accordance with the assignment channel messages. This operational mode permits higher DCM gains that the multi-clique mode, but its usefulness is limited if the DCME is located at the ISC.

4.6 *Activity detector*

4.6.1 *Purpose*

The purpose of the activity detector is to recognize when a valid signal is applied to the input of the DCME, which results in a request for an available bearer channel for transmission of the valid signal. The activity detector must:

a) detect low-level activity on a quiet input trunk channel;
b) reject high-level noise on an input trunk channel;
c) avoid introducing front end clipping on signals;
d) minimize false operation on impulse noise;
e) avoid clipping during a signalling sequence;
f) avoid clipping on facsimile messages during page changes.

4.6.2. *Activity detector characteristics* (under study)

The activity detector characteristics are based upon the assumption that the frequency response of the transmission channel up to the input of the activity detector is ± 0.5 dB with respect to 1020 Hz over the frequency band from 300 to 3400 Hz, and that the level of any single audio frequency, measured selectively on an idle channel, should not exceed −50 dBm0.

4.6.2.1 *Operating threshold and operation time for variable threshold*

The transmit activity detector threshold shall automatically adjust relative to the average power of Gaussian noise band limited between 300 to 3400 Hz.

The threshold and operate time of the transmit activity detector may operate in a manner which is equivalent to an activity detector with the characteristics given below (see note).

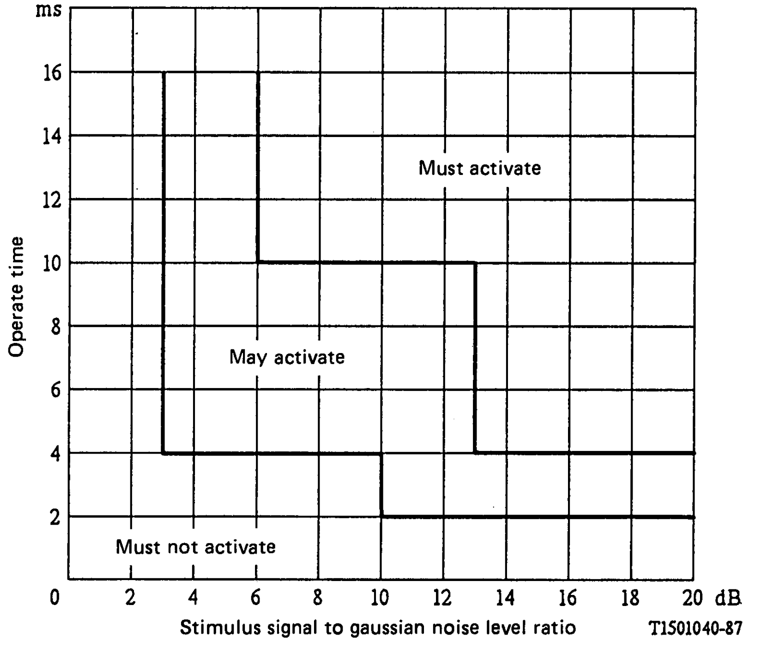
Note – All parameter values are provisional and under study.

Average signal power	*Operate time*
< -40 dBm0	OFF
$\geqslant -40$ dBm0, $\leqslant -30$ dBm0	Figure 4/G.763
> -30dBm0	2 ms $< t <$ 4 ms

The operate time requirements will be satisfied while permitting tolerances on the average signal power of any stimulus signal in the frequency band at boundary conditions as follows:

-40 dBm0	$\pm$ 1.5 dB
-30 dBm0	$\pm$ 1.0 dB

The rate of change of the transmit activity detector adaptive threshold will be between 2.5 dB/s and 20.0 dB/s.



Note 1 – Mask applicable to stimulus signals which are ≥ -40 dBm0, but ≤ -30 dBm0.
Note 2 – Stimulus signal to be 1020 Hz sinusoid.

FIGURE 4/G.763

Transmit activity detector operate threshold mask

4.6.2.2 *Interaction of the transmit activity detector with echo control devices*

The threshold of the transmit activity detector shall not adapt to Gaussian noise level variations which are due to the actions of echo suppressors or echo cancellers. This may be accomplished by any means which is functionally equivalent to providing an inhibit signal from a receive activity detector when activity is present in the receive channel.

4.6.2.3 *Hangover time*

The permissible hangover time as a function of stimulus signal duration shall be within the mask shown in Figure 5/G.763 for Signalling System No. 5 and within the mask shown in Figure 6/G.763 for Signalling Systems No. 6, 7 and R2D.

It shall be possible to select the required type of hangover time mask. For voice-band data, the hangover time should be extended so that it is sufficiently long to bridge FAX page changes. This time may be as long as 14 s.

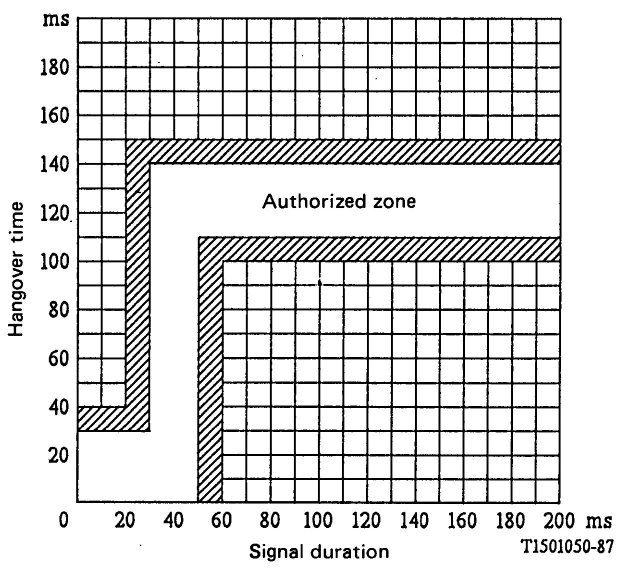


FIGURE 5/G.763

Hangover time mask for Signalling System No. 5

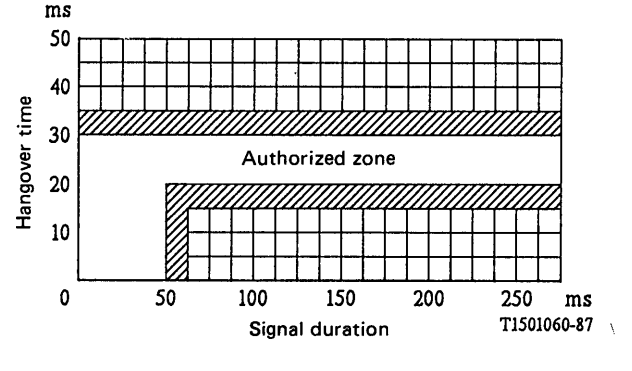


FIGURE 6/G.763

Hangover time mask for Signalling Systems No. 6 , 7 and R2D

4.7 *Data/speech discrimination*

4.7.1 *Purpose*

The DCME data detector shall be capable of discriminating between voice-band data and speech. This discrimination is necessary in order to assign the voice-band data signal to a non-overloaded bearer channel and to eliminate or minimize front end clipping of the data signal.

4.7.2 *Data/speech discrimination characteristics*

Most of the V-Series modems use the 2100 Hz disabling tone for the purpose of disabling echo control devices. The 2100 Hz echo control disabling signal shall be used to identify those input trunk channels where the active signal is in-band data originating from 2-wire PSTN data modems. Upon detecting the 2100 Hz disabling tone with or without phase reversal (see Recommendation V.25), a particular call shall be designated as data through the DCME.

4.8 *Control channel*

The control channel shall include provisions for accommodating the following categories of inter DCME-terminal messages:

- trunk-to-bearer assignment;
- idle noise level;
- dynamic load control;
- alarm information;
- self diagnostic information;
- signal classification.

In addition, the control channel shall include DCME frame synchronization and the messages shall be protected against bit errors occurring on the bearer channel.

A dedicated 32 kbit/s channel shall be used; however, the precise format and operation is under study.

4.9 *Communication to the ISC*

The DCME shall communicate with the ISC in accordance with Recommendation Q.50.

4.9.1 *Dynamic load control (DLC)*

The DCME shall generate dynamic load control messages for the following two categories of traffic:

a) speech and 3.1 kHz audio, and

b) 64 kbit/s unrestricted.

The DCME shall provide a dynamic load control signal which may be sent to the local and distant telephone switching centres to limit the traffic load presented to the DCME during overload conditions. The dynamic load control signal is activated by monitoring load parameters for the interpolated speech and the 64 kbit/s unrestricted channels.

Overload conditions should be indicated by the average number of bits per sample calculated for each clique. When the value falls below a particular, previously set threshold level, the DLC message should be generated at the DCME. DLC messages shall be sent back to the local ISC(s), and the distant DCME shall be informed through the control channel. The distant DCME shall interpret and appropriately convey the DLC information to its associated ISC(s).

The DLC condition shall be reset automatically when the average number of bits per sample exceeds a second, previously set threshold.

4.9.2 *Dynamic load control activation/deactivation criteria*

Speech and 3.1 kHz audio dynamic load control activation messages shall be generated when the average number of bits per sample drops below a preset threshold.

The 64 kbit/s unrestricted dynamic load control activation messages shall be generated when:

a) the measured number of assigned 64 kbit/s unrestricted channels exceeds a preset threshold, or

b) the speech and 3.1 kHz audio dynamic load control has been activated, or

c) the speech and 3.1 kHz audio dynamic load control is expected to be activated due to an increase of one additional channel in the 64 kbit/s unrestricted traffic loading.

Dynamic load control activation shall occur immediately upon satisfying the threshold criteria. Dynamic load control deactivation messages shall be generated when the average number of bits per sample exceeds a preset threshold or the number of 64 kbit/s unrestricted channels falls below a preset threshold. If the 64 kbit/s dynamic load control is not active, 64 kbit/s unrestricted channel requests shall not be refused. Dynamic load control deactivation shall not occur earlier than a programmable interval which has a minimum of 10 s.

4.9.3 *Establishment and release of 64 kbit/s unrestricted class connections*

The DCME shall establish/release 64 kbit/s unrestricted duplex connections under control of the seizing/releasing ISC as part of the call set-up/clearing process between exchanges. Dedicated seizure/select and release messages and the associated acknowledgement messages are exchanged between the DCME and the ISC as defined in Recommendation Q.50.

Subject to the capability of the ISC, this process is usable for performing the in-call modifications between the DCMEs during alternate speech/64 kbit/s unrestricted type calls.

Upon reception of a seizure/select message from the ISC for a trunk, the DCME shall perform the necessary internal checks, including the 64 kbit/s unrestricted dynamic load control status, for the accommodation of this call and an acknowledgement (positive or negative) message shall be returned as soon as possible to the calling ISC. The calling end DCME shall initiate the establishment of the unrestricted 64 kbit/s forward connection to the called end DCME using a special identifier in the assignment message. The called end DCME, upon receipt of this message, shall automatically initiate the establishment of the unrestricted 64 kbit/s return connection. Failure to complete the establishment of a 64 kbit/s circuit between DCMEs shall be reported to the ISC as soon as this has been detected internally. This reporting shall be in the form of an out-of-service message.

Upon receipt of a release message from the calling ISC, the releasing end DCME shall initiate the release of the unrestricted 64 kbit/s forward connection, and the opposite end DCME shall automatically initiate the release of the unrestricted 64 kbit/s return connection. Upon completion of this process, a positive release acknowledgement message shall be returned to the releasing ISC. Failure to complete the release shall be reported to the releasing ISC using the out-of-service message and the DCME shall put the trunk in a blocked condition.

After manual or automatic removal of any failure condition, the DCME shall put the trunk in an idle condition and send a back-in-service message to the ISC.

A calling end DCME shall detect a release initiated by the opposite end (non-controlling) ISC by the reception of a disconnect message in the control channel. This abnormal release shall be recognized as a dual seizure situation being resolved between the ISCs. The detecting DCME shall first complete the release normally and immediately attempt to re-establish the released 64 kbit/s unrestricted duplex connection between the DCMEs.

4.10 *Trunk channel idle noise level detection and injection*

The DCME transmit unit shall measure the trunk channel idle noise level and forward this information to the corresponding DCME receive unit, which shall insert the appropriate idle level noise within the receive output speech channel during silent intervals following disconection of the bearer channel. The idle level noise shall not be inserted on 64 kbit/s unrestricted channels.

4.11 *Time slot interchange (TSI)*

The DCME shall include a time slot interchange capability on the trunk side interface so that a given time slot at the transmit unit can be assigned to any time slot on the receive unit.

4.12 *Signalling transmission*

The DCME shall support the following signalling systems:

- Signalling System No. 5
- Signalling System No. 6 (both analogue and digital versions)
- Signalling System No. 7
- Signalling System R1 under study (Note 1)
- Signalling System R2 (Note 2)

Signalling detection is under study.

Note 1 – Signalling System R1 may be supported, but a special signalling interface will be required.

Note 2 – Transmission of R2D line signalling in the control channel is recommended.

4.13 *Voice-band data transmission*

Once a voice-band data call is recognized by the DCME, the DCME system shall not introduce any degradation to the voice-band data block error rate performance beyond that normally encountered by a single encoding of the ADPCM codec used inthe DCME for voice-band data tansmission.

4.14 *Echo protection*

The DCME shall not activate transmission in the transmit direction as the result of receive signals. Such activation increases the apparent speech activity factor and reduces the DCME gain. Therefore, echo in the transmit signal resulting from the receive signal must be removed, but this echo control function is not required to be a part of the DCME.

A network echo control device meeting or exceeding the requirements of Recommendations G.165, G.164 or G.161 is required on all trunk channels carrying speech serviced by a DCME[2])

4.15 *Bearer channel preassignment*

The DCME shall permit trunk channels to be preassigned to bearer channels. The 64 kbit/s trunk channels may be preassigned to any of the following:

- channels subject to 32 kbit/s ADPCM,
- channels subject to 40 kbit/s ADPCM,
- channels transmitted using 64 kbit/s.

5 Interfaces

The transmission interface to the international switching centre (ISC) or national transmission medium (trunk side) shall be at the primary hierarchical rates of either 2048 kbit/s or 1544 kbit/s. The transmission interface to the national or international transmission medium (bearer side) shall be at either 2048 kbit/s or 1544 kbit/s. The data rates on the trunk and bearer sides are normally the same.

In the case of interworking between the 1544 kbit/s and 2048 kbit/s hierarchies on the same DCMS, it is recommended in Recommendation G.802 that the bearer system should be 2048 kbit/s. Nevertheless, there may be operational difficulties with such interworking depending on whether the DCME is Type 1, where the DCME cannot communicate with the ISC, or Type 2, where it can, as defined in Recommendation Q.50.

5.1 *Transmission interface; trunk side*

5.1.1 *Trunk side interface at 2048 kbit/s*

a) The electrical characteristics shall comply with Recommendation G.703. The test load impedance shall be either 75 Ω unbalanced or 120 Ω balanced depending on the user requirement.

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2) The French Administration has indicated that improved echo suppressor performance, superior to Recommendations G.164 and G.161, can be achieved by incorporating an echo suppressor within the DCME, because advantage can be taken of the more sophisticated speech detection incorporating a delay line to reduce break-in and double-talk clipping.

b) The frame structure shall comply with Recommendation G.704.

c) The encoding law for voice frequency signals shall conform to the A-law system described in Recommendation G.711.

5.1.2 *Trunk side interface at 1544 kbit/s*

a) The electrical characteristic shall comply with Recommendation G.703. The line code adopted shall be either AMI or B8ZS depending on the user requirement.

b) The frame stucture shall comply with Recommendation G.704. The multiframe size shall be either 24 frames or 12 frames depending on the user requirement.

c) The encoding law for voice frequency signals shall conform to the μ-law system described in Recommendation G.711.

5.2 *Transmission interface: bearer side*

5.2.1 *Bearer side interface at 2048 kbit/s*

5.2.1.1 *Electrical characteristics*

The electrical characteristics shall comply with Recommendation G.703. The test load impedance shall be either 75 Ω unbalanced or 120 Ω balanced depending on the user requirement.

5.2.1.2 *Bearer frame structure*

The bearer frame structure shall comply with Recommendation G.704. Time slot 0 shall be used as recommended in Recommendation G.704 and time slots 1 to 31 shall carry control channels and traffic according to the DCME frame structure.

5.2.2 *Bearer side interface at 1544 kbit/s*

5.2.2.1 *Electrical characteristics*

The electrical characteristics shall comply with Recommendation G.703. The test load impedance shall be 100 Ω resistive.

5.2.2.2 *Bearer frame structure*

The bearer frame structure shall comply with Recommendation G.704.

Provisions shall be included in the bearer frame structure to accomodate control channels and traffic according to the DCME frame structure.

The 193rd bit shall be used for frame synchronization as recommended in Recommendation G.704.

5.3 *Control interfaces to switching equipment (at the ISC)*

The choice of interface is considered to be a national matter and left for each Administration to define within the constraints of their transmission facilities and ICSs.

The control interface to the switching equipment is dependent on the capability of the ISC and the facilities between the ISC and the DCME (see Recommendation Q.50).

5.4 *Man-machine interface*

The DCME shall contain a system command structure which serves as a menu-driven interface between internal functions and the system operator. Typically two RS 232C/V24 ports are necessary to provide operator access to the equipment: one for a display terminal and one for a printer.

5.5 *Operations function interface(s)*

5.5.1 *Trunk side operation at 2048 kbit/s or 1544 kbit/s*

The utilization of spare bits for monitoring and error protection shall be in accordance with Recommendations G.704 and G.706.

Details covering the use of the above in an equipment specification are under study.

5.5.2 *Bearer side*

5.5.2.1 *Single destination mode*

The utilization of spare bits for monitoring and error protection is under study.

5.5.2.2 *Multi-clique or multi-destination mode*

The utilization of spare bits for monitoring and error protection is under study.

5.6 *Local alarms interface (provisional)*

The DCME must present alarms to the local entity according to the user's requirement. The choice of the physical/electrical interface is to be decided by the individual Administration. In the case of individual voltage-free loop alarms, the categories of alarm in Recommendation G.803 should be included. In the case of a serial alarm interface, it is recommended to provide as a minimum the following signals:

a) initial occurrence of an alarm in the monitored DCME;

b) initial ocurrence of a clear in the monitored DCME;

c) receipt of a data request from the local entity;

d) initial system power-on.

Note – The inclusion of Telecommunications Management Network (TMN) protocols and interface requirements in future DCME Recommendations is planned.

5.7 *External clock interface*

5.7.1 *DCME working with 2048 kbit/s transmission interfaces*

The external clock interface shall comply with Recommendation G.703, § 10.3. The test load impedance shall be either 75 Ω unbalanced or 120 Ω balanced depending on the user requirement.

5.7.2 *DCME working with 1544 kbit/s transmission interfaces*

The timing normally derived from an incoming digital link at 1544 kbit/s complying with Recommendation G.703, § 2. Where required an external clock interface may be provided.

6 Timing synchronization

6.1 *General*

Timing synchronization of DCME can be achieved in many ways and care should therefore be taken in any implementation to ensure that the configuration adopted is correct.

6.1.1 *Reference clock*

The DCME reference clock shall be derived from a source which meets the requirement of Recommendation G.811. For networks that entail one international destination, loop timing can be used as an alternative at one end of the link. The need for an internal reference clock for use under failure conditions is for further study.

6.1.2 *Plesiochronous slips*

The slip rate shall not exceed the requirements of Recommendation G.822. Controlled slips at 2048 kbit/s on the trunk side shall be 2 frames, controlled slips at 1544 kbit/s and on the bearer side require further study.

6.1.3 *Buffer sizes and locations*

Table 1/G.763 indicates suitable buffer sizes and locations for the 2048 kbit/s hierarchy for the various synchronization options which are detailed in Appendix I. A table for the 1544 kbit/s hierarchy is under study.

TABLE 1/G.763

Synchronization type (Note 1)	Buffer size (Note 2)	Slip size (Note 3)	Location (Note 4)	Figure No. of Appendix I
No buffering				
Asynchronous	No buffer	–	–	I-1/G.763
Synchronous	No buffer	–	–	I-2/G.763, I-12/G.763, I-15/G.763
Synchronous analogue-to-digital	No buffer	–	–	I-5/G.763
Plesiochronous buffering				
Asynchronous	0.5 ms	2 frames	Trunk side	I-3/G.763
Synchronous	0.5 ms	2 frames	Bearer side	I-4/G.763, I-13/G.763, I-16/G.763
Plesiochronous/doppler buffering				
Synchronous	1.7 ms	2 frames	Bearer side	I-6/G.763, I-11/G.763, I-14/G.763, I-17/G.763, I-19/G.763
Synchronous	2.4 and 1.7 ms		Bearer side and trunk side	I-7/G.763
Asynchronous	1.7 ms	2 frames	Trunk side	I-9/G.763
Synchronous	2.4 and 1.7 ms		Trunk side and bearer side	I-8/G.763
Synchronous	1.7 ms	2 frames	Trunk side	I-10/G.763, I-18/G.763

Note 1 – Asynchronous refers to the case where the transmit unit and receive unit of the same DCME terminal are deriving their timing from different clock sources.

Note 2 – Buffer sizes are derived from the following:

– single doppler with plesiochronous buffer: $(0.6 \text{ ms} \times 2) + 0.5 = 1.7$ ms;

– double doppler buffer: $1.2 \text{ ms} \times 2 = 2.4$ ms;

– plesiochronous buffer for 2 PCM (2048 kbit/s) frames: 0.5 ms.

The doppler buffer size used is an example for a specific satellite. These buffer sizes may need to be adjusted taking into account the orbital parameters of the satellite in use.

Note 3 – The slip size of 2 PCM frames is based upon the requirement in the 2048 kbit/s frame to maintain frame alignment.

Note 4 – In general it is preferable to avoid placing the plesiochronous slip buffers on the bearer side of the DCME to minimize disruptions caused by slips. This may not be possible under all circumstances.

6.1.4 *Terminal synchronization*

The DCME terminal shall be capable of deriving its timings from any of the incoming digital links or from an external clock. When the synchronization is derived from the trunk receive side, it is recommended that a fallback trunk receive synchronization source is allocated in the event of the primary channel receiving an alarm condition indicating a received line signal failure, loss of frame alignment, AIS or receive BER $\geqslant 10^{-3}$. Switching between primary and fallback sources shall be automatic.

7 Performance

7.1 *Speech performance*

Recommendation P.84[3] describes a subjective test method for comparing the performance of DCME systems against suitable reference conditions for carefully defined input signals. Recommendation P.84 consists of listening tests and is the recommended source of information about subjective testing of DCME. These tests are a first step and do not preclude the need for conversational tests.

It is recommended that a fixed delay be inserted in the transmit speech path to reduce the probability of front end clipping. This delay compensates for activity detection time and DCME assignment message connection delay. The delay should be such as to assure that the main speech spurt clipping is less than 5 ms.

7.2 *Voice-band data performance*

Paragraph 2.3 refers to Recommendation G.721 (32 kbit/s ADPCM algorithms) and to Recommendation G.723 (24 kbit/s and 40 kbit/s algorithms derived from Recommendation G.721), which have been selected for use in DCME. Extensive testing has demonstrated satisfactory voice-band data performance for the 40 kbit/s algorithm specified in Recommendation G.723 for a voice-band data rate of 9600 bit/s.

Voice-band data at rates greater than 9600 bit/s may be satisfactorily transmitted, but in any event a 64 kbit/s unrestricted channel can be selected through the DCME which will accommodate voice-band data rates at 14400 bit/s.

8 System management functions

8.1 *Transmission facilities*

Each terminal should monitor each incoming digital link for the following conditions or parameters and store separate cumulative counts of each type of event as required by users:

- AIS, remote alarm indication;
- loss of incoming signal, loss of frame alignment, reframe rate;
- severely errored seconds;
- degraded minutes;
- slips, slip rate.

8.2 *Terminal traffic handling performance*

The DCMS terminals shall monitor and store records of the various parameters needed to evaluate the traffic handling performance being provided.

8.2.1 *Measurement of statistics* (see Table 2/G.763)

Measurements and calculations, other than for BER, shall be done only on non-preassigned trunk channels which are defined in the configuration data. The DLC-on ratio for voice/voice-band data and the DLC-on ratio for 64 kbit/s unrestricted traffic shall be obtained separately for each destination. All other parameters shall be obtained separately for each transmit pool.

The measurements of each parameter shall be made over Statistics Time Interval (STI) determined by the operator. Each statistic shall be calculated once every update interval (e.g. 30s), with the accumulated data from every sampled DCME frame (e.g. each 10th frame) over the previous averaging period (e.g. 1 min). The average over the STI shall be the average of the values calculated each update interval during the STI within the range from 10 min to 60 min (in 10 min steps).

The definitions of the Quality of Service and offered traffic statistics are given in Appendix II.

During the STI, the average BER shall be calculated at the end of each 1 minute interval, the voice freezeout excess shall be calculated from the 1 min values of voice queue freezeout fraction and the BER excess shall be calculated from the 1 min values of average BER.

[3] The specifications in Rec. P.84 are subject to future enhancement and therefore should be regarded as provisional.

The summary statistics calculated at the end of the STI shall be output to a statistics data file on a secure storage medium (e.g. non-volatile RAM, hard disk. etc.).

TABLE 2/G.763

DCME management statistics

Service to be measured	Quality of service statistics	Offered traffic statistics
Voice	(1) Bits per sample (2) Voice queue freezeout fraction (3) Voice freezeout excess	(4) Voice activity ratio (5) DLC voice-on ratio
Data	(6) Data queue freezeout fraction	(7) Data activity ratio
64 kbit/s on demand	(8) 64 kbit/s failed seizures ratio	(9) 64 kbit/s connected ratio (10) 64 kbit/s DLC-on ratio
All services	(11) Average BER (12) BER excess (13) Severely errored seconds (14) Degraded minutes	

Note – Statistics (1) to (4) and (6) to (9) shall be calculated separately for each transmit pool.

Statistics (5) and (10) shall be calculated separately for each destination.

Statistics (11) and (12) shall be calculated separately for each receive control channel.

Statistics (13) and (14) shall be calculated separately for each incoming digital link according to Recommendation G.821.

8.3 *Synchronizer*

The state of synchronization of each primary group interface, the selected clock source, and the times of any failures or changes of clock source should be monitored.

8.4 *Communication links*

The condition of all communication links should be monitored to detect failures as far as practicable, including:

- control channels;
- ISC-DCME interface;
- man-machine interface.

8.5 *Reports*

The terminal should:

a) at operator defined intervals, or when set parameters have been exceeded, or as a worst 15-minutes report for any 24 hours period, file operator selected parameters from those monitored and stored, including header information such as terminal identification, date, and measurement period covered by the file;

b) compare selected parameters, status or measurements with predetermined conditions;

c) upon detection that predetermined conditions have been met or exceeded for a given period of time, take the necessary action(s) which may include:

   1) filing of an anomaly report;
   2) transmission of alarm signals;
   3) block all new calls due to failure;
   4) switch to standby, if available;
   5) total shut down of the terminal.

8.6 *System configuration*

The terminal shall include a non-volatile back-up memory containing a copy of the latest configuration of the DCME, for use in failure situations. A non-working spare copy should also be provided to allow changes in configuration to be made without impact upon service security. In cases where cluster operation of terminals is used to provide additional service security, means must be provided for the standby terminal to adopt the configuration of the working terminal which it is intended to replace.

The configuration information shall include details of trunk side interface channel connections, modes of operation of any preassigned channels, any restrictions in force to any destination or on any block of circuits (e.g. limit on the number of 64 kbit/s calls).

8.7 *Failure strategy*

Upon detection of conditions affecting the service, the DCME shall take the appropriate actions to protect existing traffic, such as switching to fallback timing sources or fallback units where redundancy is provided, transmission of DLC signals, disconnection of failed circuits, transmission of any appropriate alarm conditions.

9 Maintenance functions and alarms

9.1 *Maintenance functions*

The DCME should provide the following maintenance functions:

a) facilities for disabling (terminal out-of-service test):
   – digital speech interpolation;
   – low rate encoding (ADPCM);
   – variable bit rate coding;

b) facilities for providing fixed connections of specific trunk channels to specific bearer channels, at 32 kbit/s without interpolation, 40 kbit/s without interpolation and 64 kbit/s interpolation;

c) facilities for protected monitoring points (under study).

9.2 *DCME alarm conditions*

Alarm conditions and the appropriate consequent actions are defined as follows:

9.2.1 *Normal traffic carrying operating conditions*

The following shall apply when the DCME is carrying traffic, when no digital links are exhibiting fault conditions and when the DCME is also not exhibiting a fault condition:

a) the absence of alarm indications on the DCME terminal shall indicate a normal condition;

b) the means used on the DCME terminal to indicate operating modes or to provide routine information shall be of such form, colour or type that they cannot be confused with alarm conditions.

9.2.2 *Time delay*

Optionally, a time delay, selectable up to three seconds maximum, shall be provided before alarms are initiated or indications are transmitted in fault conditions categories A, B, C and/or D of Table 3/G.763, as appropriate.

9.2.3 *Fault conditions and consequent actions*

Table 3/G.763 shows various fault conditions and consequent actions which are externally observable.

TABLE 3/G.763

Consequent actions

Fault condition		Alarm (Note 4)	Apply to bearer side, towards distant terminal (Note 5)	Apply to trunk side of own network (Note 5)	Other action
A	Failure of incoming 1.5- or 2-Mbit/s trunk from own network (Note 1) (See conditions G, E)	Prompt	Message in control channel to indicate which 64 kbit/s trunks are affected	AIRE in affected trunk	Management report [a)]
B	Failure of bearer from distant end (Note 1) (See condition F)	Prompt	Remote alarm messge in control channel and AIRE	AIS in all affected trunks	Management report [a)]
C	AIS in incoming 1.5- or 2-Mbit/s trunk from own network (See conditions G, E)		Message in control channel to indicate which 64 kbit/s trunks are affected	AIRE in affected trunk	Managements report [a)]
D	AIS in bearer from distant end (See condition F)		Remote alarm in control channel and AIRE	AIS in all affected trunks	
E	Remote alarm indication in incoming 1.5- or 2-Mbit/s trunk from own network (See conditions A, C)		Message in control channel to indicate which 64 kbit/s trunks are affected		Management report [a)]
F	Remote alarm message in control channel and AIRE (Note 2) (See conditions B, D)			Extend remote alarm indication in all appropriate trunks (optional)	
G	Message in control channel of bearer to indicate failure or AIS in a 1.5- or 2-Mbit/s trunk incoming from distant end (See conditions A, C)			All "1s" in affected 64 kbit/s trunks and "out of service" code via an ISC to DCME link	
H	Timing source failure	Prompt if unprotected deferred if protected			Management report [a)] and switch to fall back source when available

	Fault condition	Alarm (Note 4)	Apply to bearer side, towards distant terminal (Note 5)	Apply to trunk side of own network (Note 5)	Other action
J	DCME failure (not power failure, but self-test routine)	Prompt is deferred depending upon nature of failure	AIS, if necessary, dependent upon nature of failure (for prompt alarms only)	AIS, if necessary, upon nature of failure (for prompt alarms only)	Management report [a]
K	DCME power failure	Prompt when service affecting, deferred otherwise	AIS if possible when service affecting	AIS if possible when service affecting	Management report [a] if possible
L	Speech performance degraded (Note 3)	Prompt or deferred, depending upon level of degradation			– Management report [a] – Apply DLC or STM as appropriate via the ISC DCME link
M	1.5- or 2-Mbit/s trunk BER between 10^{-6} and 10^{-3}	Deferred			Management report [a]
N	Bearer BER between 10^{-6} and 10^{-3}	Deferred	Message in control channel to distant end		Management report [a]
O	Receive message in control channel for BER between 10^{-6} and 10^{-3}	Deferred			Management report [a]
P	Control channel error rate exceeds threshold (under study)	Prompt	Remote alarm message in control channel and AIRE	AIS in all affected trunks	Management report [a]

[a] Denotes management report, printout or information storage for maintenance.

STM Synchronous transfer module
AIS Alarm indication signal
AIRE Alarm indication to remote end

Note 1 – The fault conditions are loss of incoming signal, loss of frame alignment or a bit error ratio greater than 10^{-3} as defined in Recommendations G.737, § 4.1, and G.734, § 3.1 for 2048 and 1544 kbit/s digital links, respectively.

Note 2 – "Fault condition" is a network condition. DCME should optionally pass on the condition transparently for recognition and action by own network.

Note 3 – The following conditions must exist before the alarm for speech performance degradation operates:

a) Deferred alarm: the average number of encoding bits per sample, as defined in Appendix II, is less than a present threshold determined by subjective criteria (for further study) for a period "x" seconds (to be determined);

b) Prompt alarm: the "voice queue freezeout fraction" exceeds a selectable threshold (value under study). The possibility of additionnaly using "voice freezeout excess" and/or measuring the length of freezeout instances is also under study.

Note 4 – Recommendation G.803 defines the alarm categories.

Note 5 – The DCME shall not cause any indeterminate or unknown conditions when AIS is injected into its network, either on the trunk or the bearer side of the DCME.

APPENDIX I

(to Recommendation G.763)

Timing synchronization

The following figures provide a number of examples of Doppler and plesiochronous slip buffer placements for a variety of network synchronization schemes. In the figures it is assumed that all buffers will derive their write clocks from the input bit stream.

The following drawing convention is used:

...... Timing path

_____ Traffic path.

I.1 *Point-to-point operation*

I.1.1 *Terrestrial operation within a national network*

Figures I-1/G.763 and I-2/G.763 show methods of DCME terminal synchronization for operation within a national network.

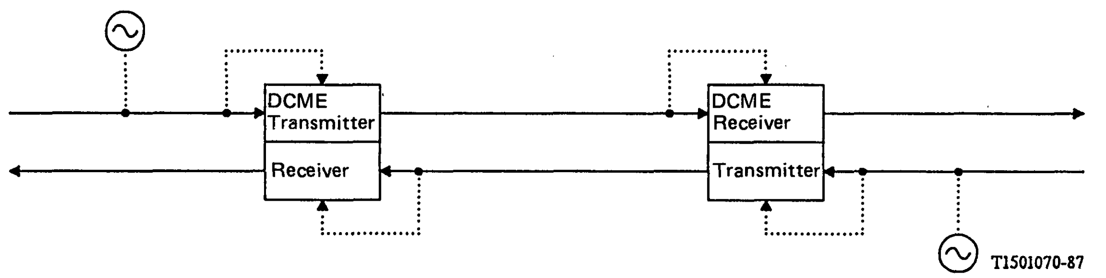


FIGURE I-1/G.763

DCME synchronous (independent) operation (in a single asynchronous network)

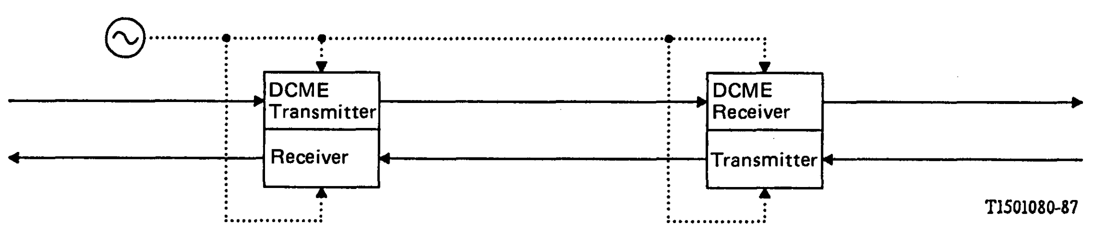


FIGURE I-2/G.763

DCME synchronous operation (in a single synchronous network)

I.1.2 *Terrestrial operation between national networks*

Figures I-3/G.763, I.4/G.763 and I.5/G.763 show methods of terminal synchronization for operation between national networks via terrestrial networks. Plesiochronous buffers are required for networks as shown in Figures I-3/G.763 and I-4/G.763. Figure I-5/G.763 utilizes loop timing and therefore does not require plesiochronous buffering.

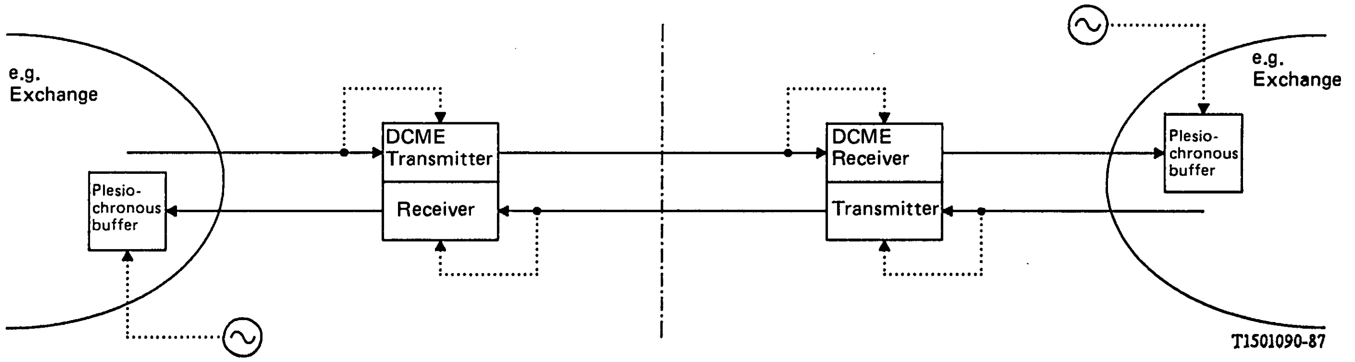


FIGURE I-3/G.763

DCME synchronous (independent) operation
(between two plesiochronous networks)

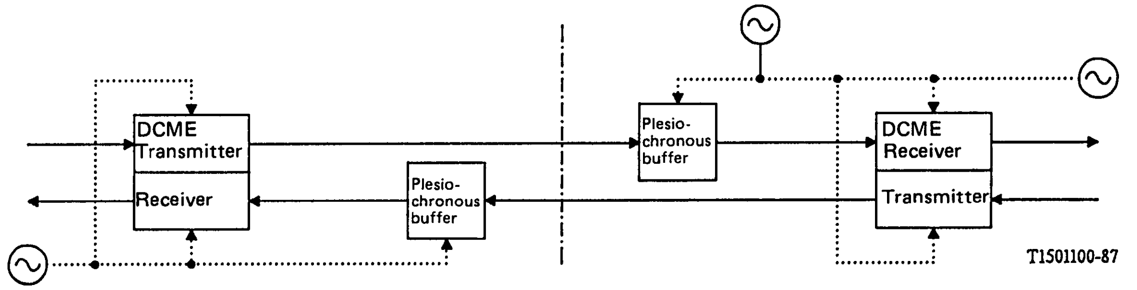


FIGURE I-4/G.763

DCME buffered plesiochronous operation
(between two plesiochronous networks)

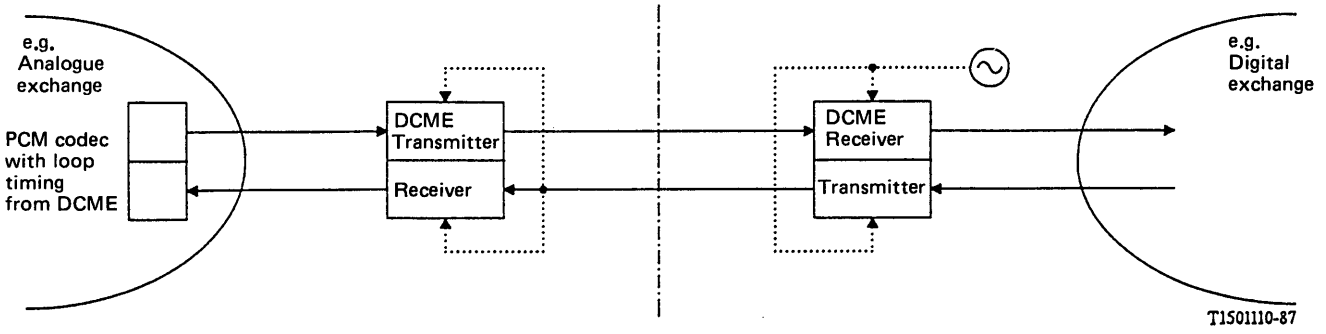


FIGURE I-5/G.763

DCME synchronous loop operation
(between analogue and digital networks)

I.1.3 *Satellite operation between national networks based upon continuous digital carrier type services*

Figures I-6/G.763 to I-9/G.763 show methods of terminal synchronization for operation between national networks over a satellite link based upon anynchronous continuous digital carrier type services. Figure I-6/G.763 introduces controlled slips between the DCMEs which are limited to in 70 days if G.811 clocks are available in both networks. Figures I-7/G.763, I-8/G.763 and I-9/G.763 permit slip free operation between the DCMEs.

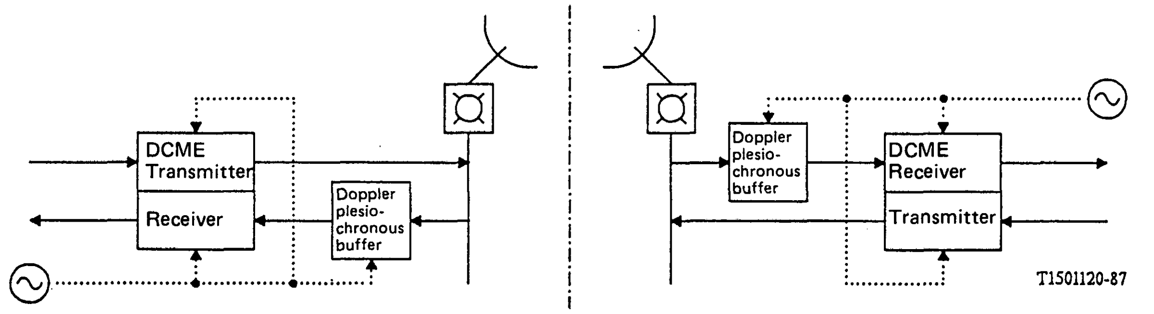


FIGURE I-6/G.763

DCME buffered plesiochronous operation (between two plesiochronous networks)

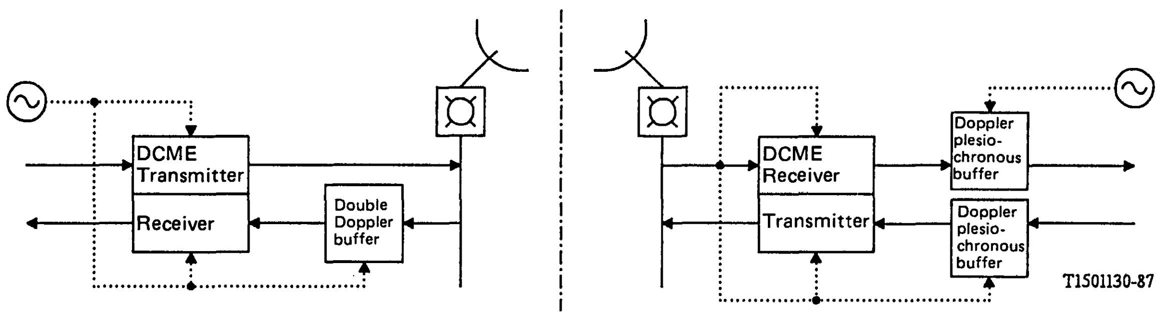


FIGURE I-7/G.763

DCME synchronous loop operation (between two plesiochronous networks)

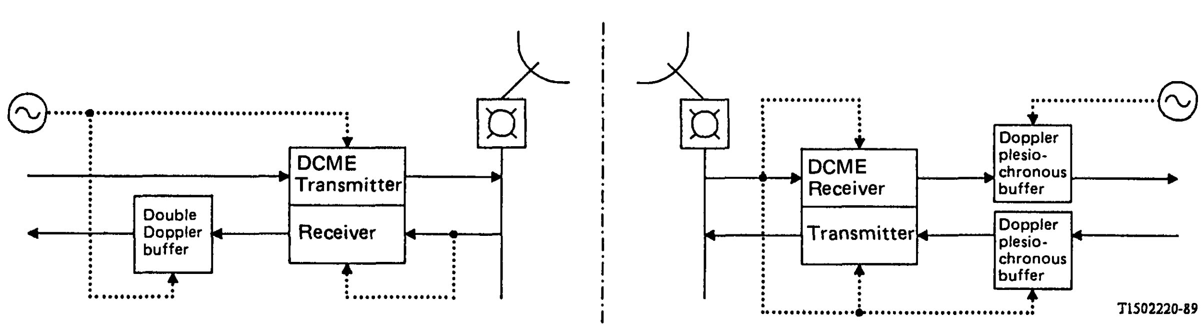


FIGURE I-8/G.763

DCME synchronous loop operation (between two plesiochronous networks)

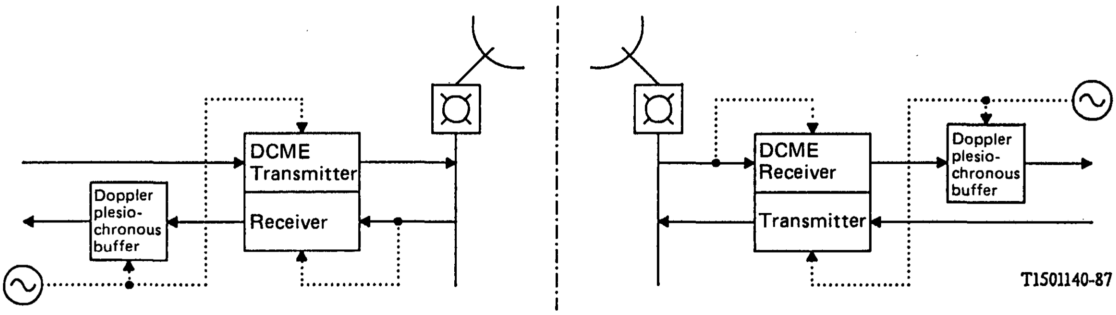


FIGURE I-9/G.763

DCME synchronous (independent) operation
(between two plesiochronous networks)

I.1.4 *Satellite operation between national networks based upon TDMA-Type services*

Figures I-10/G.763 and I-11/G.763 show a method of CDME terminal synchronization for operation between national networks over a satellite link based on TDMA-type services. An appropriate interface is provided in the TDMA terminal to permit interfacing the DCME with and without multi-clique operation over a primary multiplex port. Figure I-10/G.763 permits slip free operation between the DCMEs.

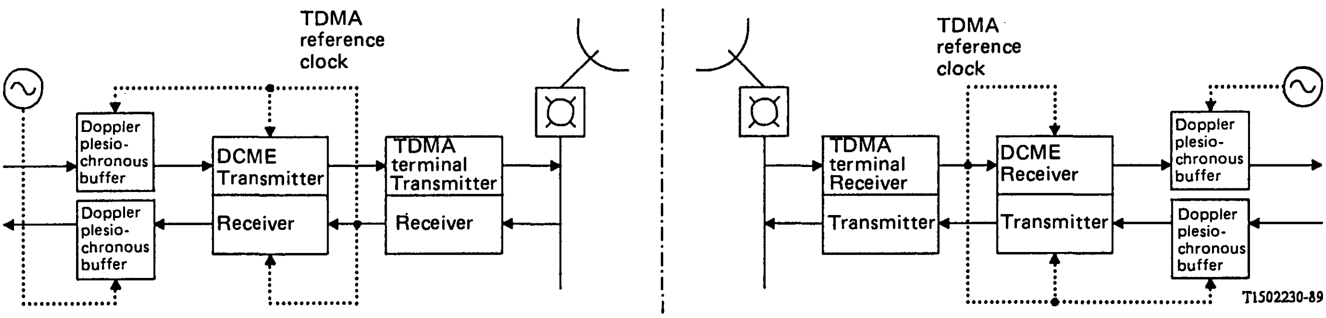


FIGURE I-10/G.763

DCME synchronous operation
(between two plesiochronous networks)

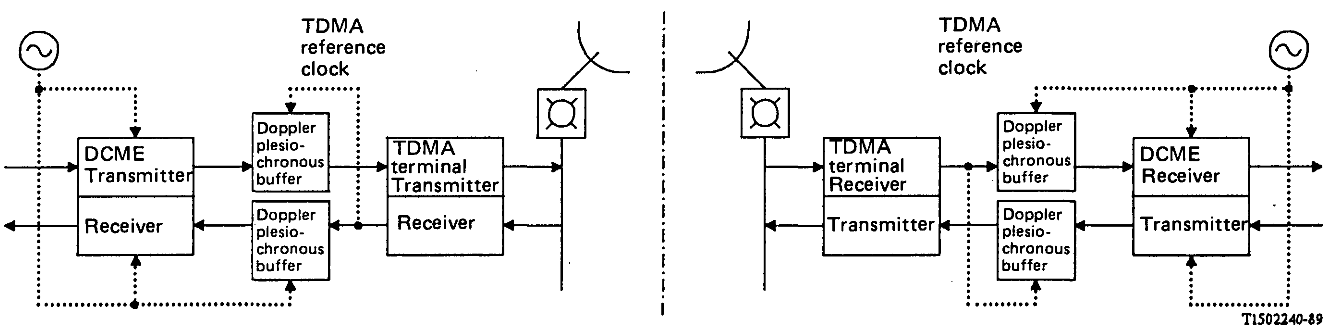


FIGURE I-11/G.763

DCME buffered plesiochronous operation
(between two plesiochronous networks)

I.2 *Multi-clique operation*

I.2.1 *Terrestrial operation within a national network*

Figure I-12/G.763 shows a method of DCME terminal syncrhonization for operation within a national network. The cross-connect function provides a means of assembling the received multi-clique pools onto a single primary multiplex.

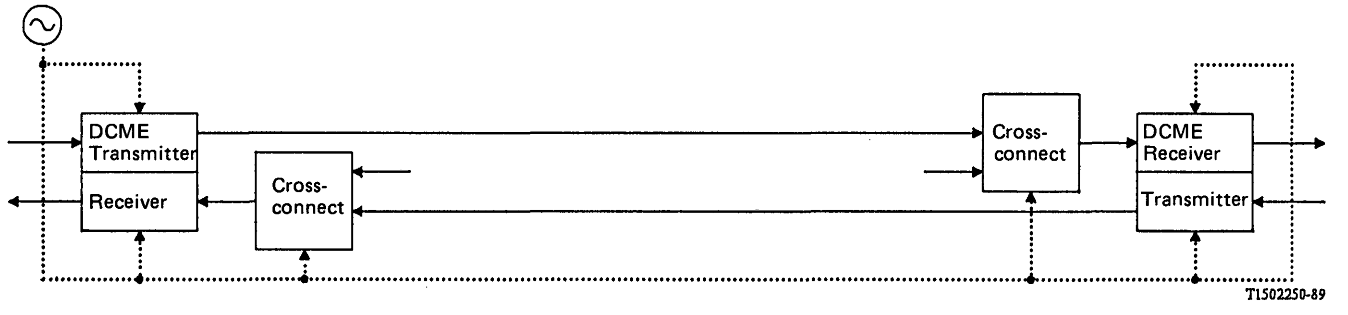


FIGURE I-12/G.763

DCME synchronous operation
(in a single synchronous network)

I.2.2 *Terrestrial operation between national networks*

Figure I-13/G.763 shows a method of DCME terminal synchronization for operation between national networks via terrestrial facilities. Plesiochronous buffers are required to resolve timing differences between the various plesiochronous networks. Due to the multiple source nature of the multi-clique configuration, the plesiochronous buffers must be placed before the cross-connect function.

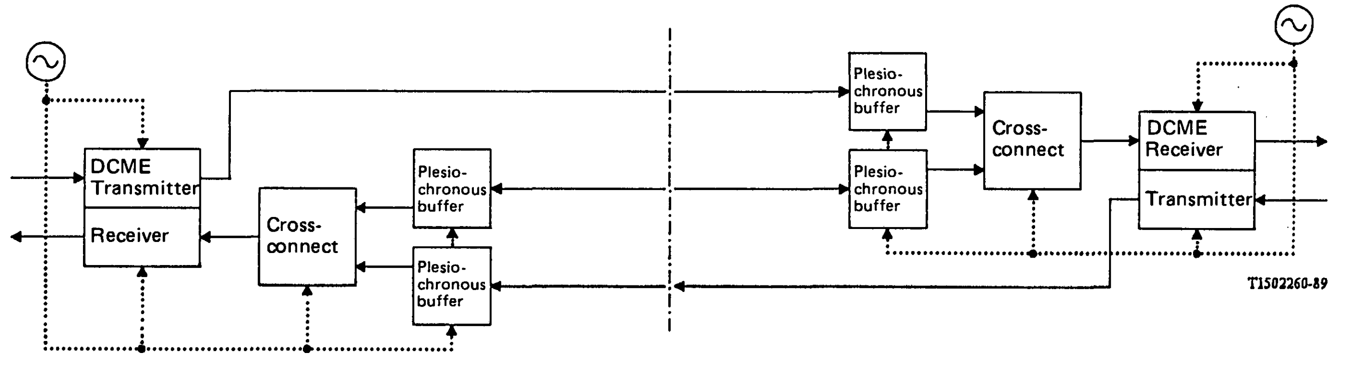


FIGURE I-13/G.763

DCME buffered plesiochronous operation
(between two plesiochronous networks)

I.2.3 *Satellite operation between national networks based upon continuous carrier type services*

Figure I-14/G.763 shows a method of DCME terminal synchronization for operation between national networks based on continuous digital satellite carriers. Plesiochronous/Doppler buffers are required to resolve timing differences between the various plesiochronous networks and to remove satellite induced Doppler shifts on the received data streams. Due to the multiple source nature of the multi-clique configuration, the plesiochronous/ Doppler buffers must be placed before the cross-connect function.

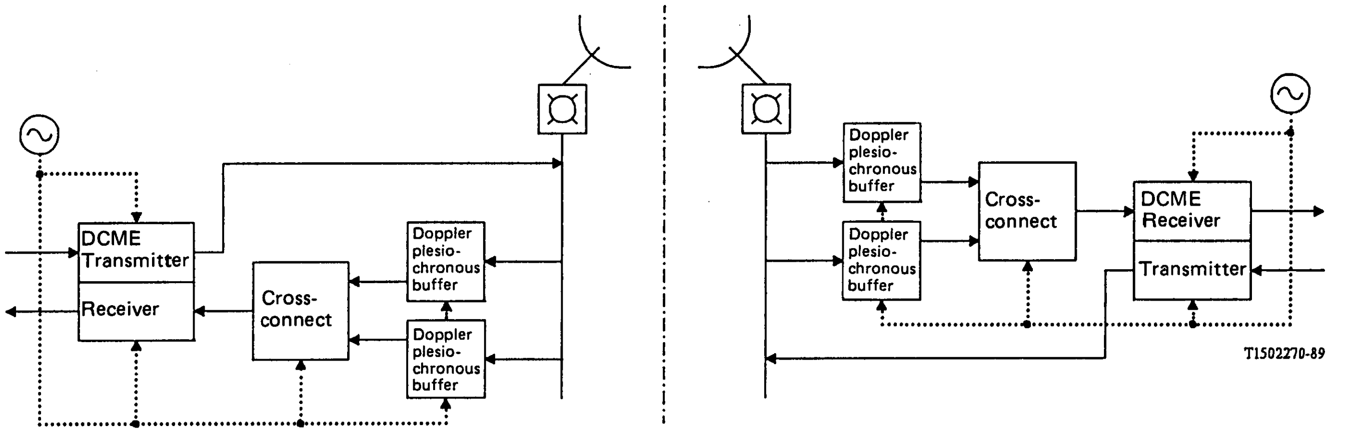


FIGURE I-14/G.763

DCME buffered plesiochronous operation
(between two plesiochronous networks)

I.3 *Multi-destination operation*

I.3.1 *Terrestrial operation within a national network*

Figure I-15/G.763 shows a method of DCME terminal synchronization for operation within a national network. The received data streams are assumed to originate from mutually synchronized sources.

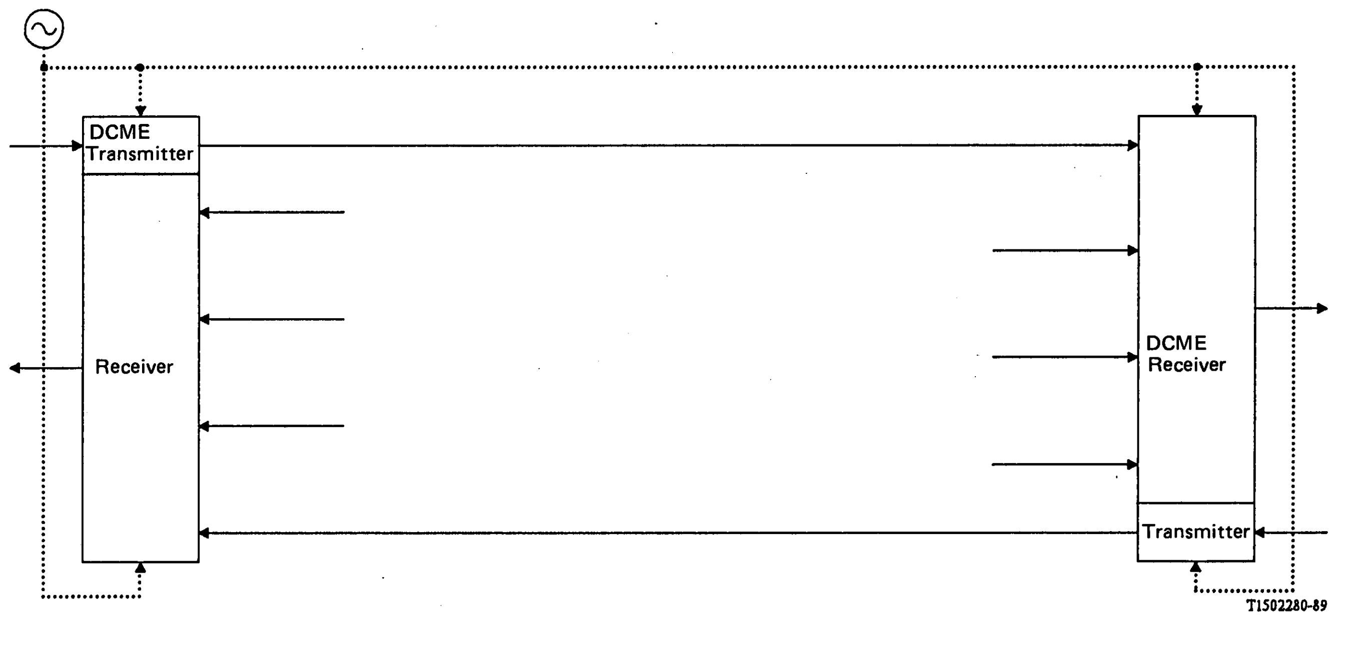


FIGURE I-15/G.763

DCME synchronous operation
(in a single synchronous network)

I.3.2 *Terrestrial operation between national networks*

Figure I-16/G.763 shows a method of DCME terminal synchronization for operation between national networks via terrestrial facilities. Plesiochronous buffers are required to resolve timing differences between the various plesiochronous networks. Due to the multiple source nature of the multi-destination configuration, the plesiochronous buffers must be placed before the DCME receive function.

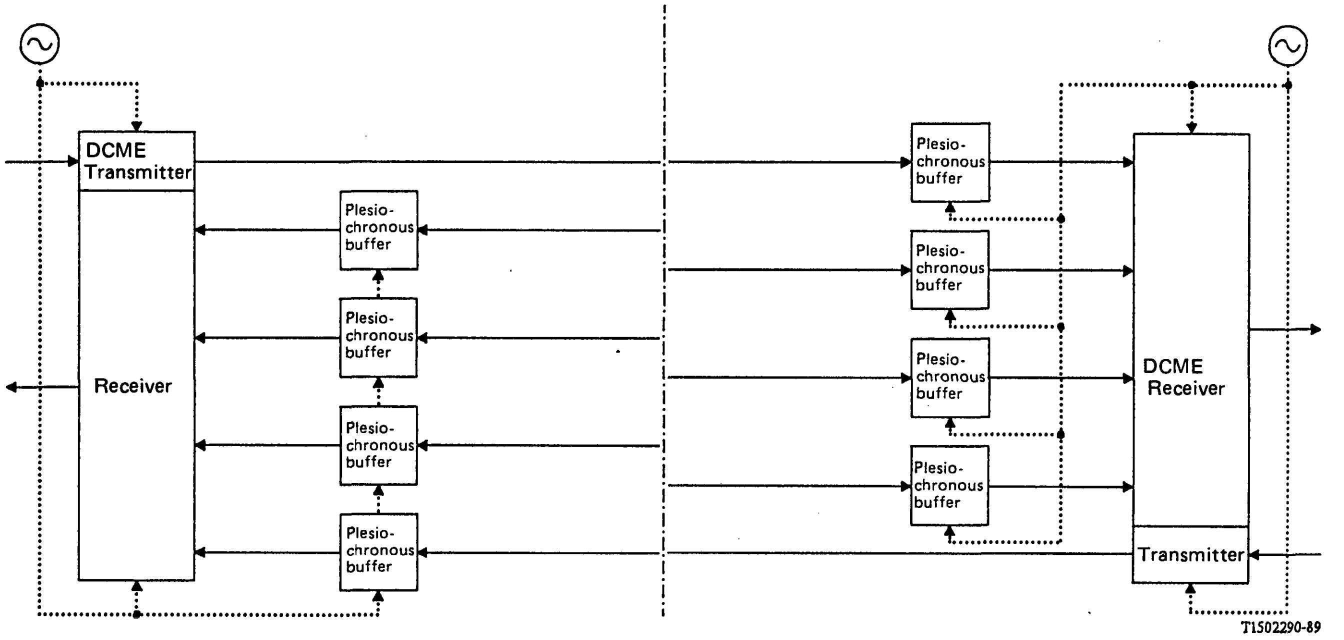


FIGURE I-16/G.763

DCME buffered plesiochronous operation (between two plesiochronous networks)

I.3.3 *Satellite operation between national networks based upon contiuous carrier type services*

Figure I-17/G.763 shows a method of DCME terminal synchronization for operation between national networks based on continuous digital satellite carriers. Plesiochronous/Doppler buffers are required to resolve timing differences between the plesiochronous networks and to remove satellite induced Doppler shifts on the received data streams. Due to the multiple source nature of the receive signals in the multi-destination configuration, the plesiochronous/Doppler buffers must be placed before the DCME receiver.

I.3.4 *Satellite operation between national networks based upon TDMA-type services*

Figures I-18/G.763 and I-19/G.763 show a method of DCME terminal synchronization for operation between national networks over a satellite link based on TDMA-type services. An appropriate interface is provided in the TDMA terminal to permit interfacing the DCME over a primary multiplex port. Figure I-18/G.763 permits slip free operation between the DCMEs.

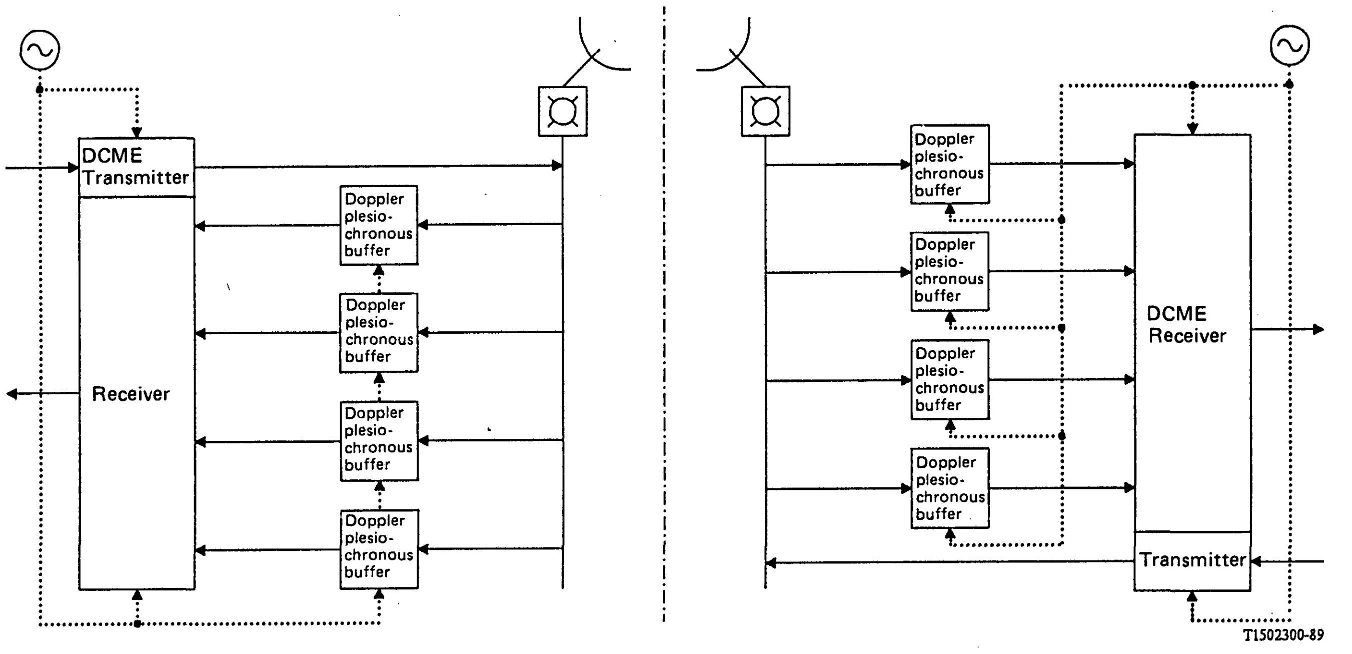


FIGURE I-17/G.763

DCME buffered plesiochronous operation
(between two plesiochronous networks)

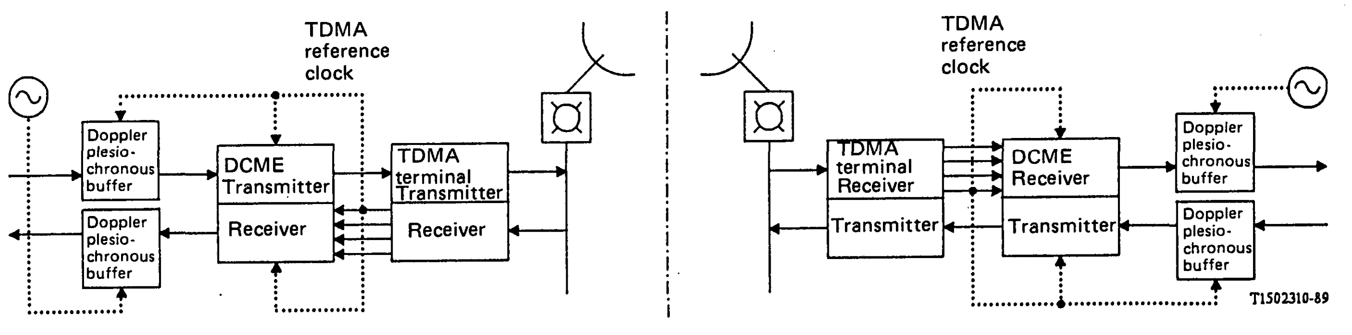


FIGURE I-18/G.763

DCME synchronous operation
(between two plesiochronous networks)

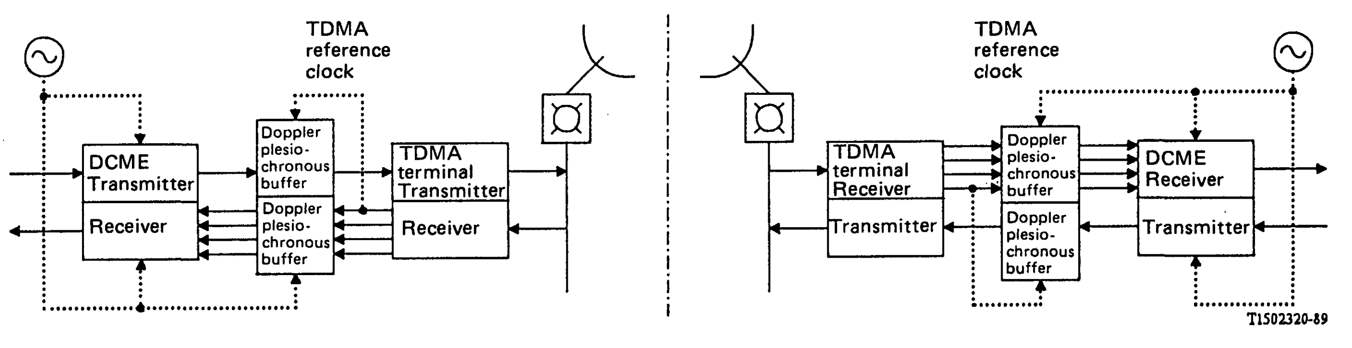


FIGURE I-19/G.763

DCME buffered plesiochronous operation
(between two plesiochronous networks)

APPENDIX II

(to Recommendation G.763)

Channel state classification and system management statistics

The purpose of this Appendix is to provide sufficient information to clearly define the system management statistics identified in Table 2/G.763.

Note – It is important that the voice and data performance are measured separately for the following reasons:

- The effect of freezeout and clipping is different on voice calls and data calls.
- The DCME process gives priority to assigning activity classed as data and hence the freezeout figures for the data queue should always be less that the corresponding freezeout figure for the voice queue.

II.1 *Channel state classifications*

The following channel states are defined in order to clarify their specific meaning in the definitions of the system management statistics.

II.1.1 *Trunk channel (TC) classification*

The following trunk channel states are defined:

a) *Transparent* – The channel is engaged in the transmission of an unrestricted 64 kbit/s call;

b) *Voice-active* – The channel is classified as voice by the data/speech discriminator and it is declared active by the activity detector;

c) *Voice-inactive* – The channel is classified as voice by the data speech discriminator and the channel is declared inactive by the activity detector;

d) *Data-active* – The channel is classified as data by the data/speech discriminator and it is declared active by the activity detector;

e) *Data-inactive* – The channel is classified as data by the data/speech discriminator and it is declared inactive by the activity detector;

f) *Signalling-active* – Signalling is detected in this channel by the signalling detector (under study) and the channel is declared active by the activity detector.

II.1.2 *Bearer channel (BC) classification*

The following bearer channel states are defined:

a) *Voice* – The connected trunk channel carries a voice signal or in-band signalling;

b) *Data* – The connected trunk channel carries a data signal;

c) *Transparent* – The connected trunk channel carries a transparent call;

d) *Disconnected* – No trunk channel is connected to this bearer channel;

e) *Voice-available* – The bearer channel is connected to a voice trunk channel, but could be used for a different assignement;

f) *Data-available* – The bearer channel is connected to a data trunk channel, but could be used for a different assignment;

g) *Pre-assigned* – The bearer channel is permanently assigned to a trunk channel;

h) *Bank* (provisional) – This 4-bit bearer channel can be used to obtain the LSBs of up to four data channels.

II.2 *System management statistics*

In the following definitions, N is the number of sampled DCME frames in the averaging period.

II.2.1 **bits/sample for voice**

The average number of encoding bits per sample for all TCs used for voice. The average should be calculated to two decimal places.

$$\text{Bits/sample for voice} = \frac{\sum_N \text{No. of bits within the BC used for voice}}{\sum_N \text{No. of non-preassigned TCs classified other than transparent, data or inactive}}$$

II.2.2 **voice queue freezeout fraction (Voice FOF)**

The ratio of competitive clip duration to voice spurt duration. The fraction may be determined as the ratio of the number of non-preassigned TCs classified as voice-active but not connected, to the total number of non-preassigned TCs classified as voice-active connected plus not connected. The ratio should be expressed as a percentage to three decimal places.

$$\text{Voice FOF} = \frac{\sum_N \text{No. of non-preassigned TCs classified as voice-active but not connected}}{\sum_N \text{Total No. of non-preassigned TCs classified as voice-active (i.e. not connected + connected)}} \times 100$$

The number of TCs classified as voice-active and connected includes those within the hangover time. The voice spurt duration is taken to include hangover.

II.2.3 **voice freezeout excess**

Percentage of time voice FOF exceeds 0.5% when averaged over 1 minute. The percentage should be calculated to two decimal places. [For statistic time interval (STI) see § 8.2.1.]

$$\text{Voice FOF excess} = \frac{\text{No. of 1 min. periods in STI in which voice FOF} > 0.5\%}{\text{No. of 1 min. periods in STI}} \times 100$$

II.2.4 **voice activity ratio**

The ratio of the number of non-preassigned TCs which are classified as voice-active to the total number of non-preassigned TCs. The ratio is expressed as a percentage, to the nearest integer.

$$\text{Voice activity ratio} = \frac{\sum_N \text{No. of non-preassigned voice-active TCs}}{\text{No. of non-preassigned TCs} \times N} \times 100$$

The voice activity ratio includes hangover time.

II.2.5 **DLC voice-on ratio**

The ratio of the number of frame during which DLC for voice/voiceband data (V/VBD) is ON, to the total number of frames. The ratio is expressed as a percentage, to the nearest integer.

$$\text{DLC voice-on ratio} = \frac{\text{No. of sampled DCME frames with DLC ON for V/VBD}}{N} \times 100$$

II.2.6 **data queue freezeout fraction (Data FOF)**

The ratio of the number of non-preassigned TCs classified as data-active but not connected, to the total number of non-preassigned TCs classified as data-active (i.e. connected + not connected). The ratio should be expressed as a percentage to three decimal places.

$$\text{Data FOF} = \frac{\sum_N \text{No. of non-preassigned TCs classified as data-active but not connected}}{\sum_N \text{Total No. of non-preassigned TCs classified as data-active (i.e. not connected + connected)}} \times 100$$

The number of TCs classified as data-active connected includes those within the hangover time.

II.2.7 **data activity ratio**

The ratio of the number of non-preassigned TCs which are classified as data-active, to the total number of non-preassigned TCs. The ratio is expressed as a percentage to the nearest interger.

$$\text{Data activity ratio} = \frac{\sum_N \text{No. of non-preassigned data-active TCs}}{\text{No. of non-preassigned TCs} \times N} \times 100$$

The data activity ratio includes hangover time.

II.2.8 **64 kbit/s failed seizures ratio**

The percentage of 64 kbit/s on demand seizure (S64) attempts that receive a 64 kbit/s negative acknowledgment (S64 NACK) from the DCME, given as an integer.

$$\text{64 kbit/s FSR} = \frac{\text{Count of S64 signals received in STI}}{\text{Count of S64 NACK signals sent in STI}} \times 100$$

II.2.9 **64 kbit/s connected ratio**

The ratio of the number of non-preassigned TCs which are classified as 64 kbit/s connect-called plus 64 kbit/s connect-calling, to the total number of non-preassigned TCs. The ratio is expressed as a percentage to the nearest integer.

$$\text{64 kbit/s connected ratio} = \frac{\sum\limits_{N} \begin{array}{l}\text{No. of non-preassigned 64 kbit/s TCs}\\ \text{connect-called and -calling}\end{array}}{\text{No. of non-preassigned TCs} \times N} \times 100$$

The data activity ratio includes hangover time.

II.2.10 **64 kbit/s DLC – on ratio**

The ratio of the number of frames during which DLC for 64 kbit/s unrestricted is ON, to the total number of frames. The ratio is expressed as a percentage to the nearest integer.

$$\text{64 kbit/s DLC-on ratio} = \frac{\begin{array}{l}\text{No. of sampled DCME frames with DLC}\\ \text{for 64 kbit/s ON}\end{array}}{N} \times 100$$

II.2.11 **average BER**

The average BER, as measured on the receive control channel.

$$\text{Average BER} = \frac{\text{Count of No. of bit errors identified in the control channel}}{\text{Count of total No. of bits received in the control channel}} \times 100$$

II.2.12 **BER excess**

The percentage of time that the average BER exceeds $1 \cdot 10^{-3}$ when averaged over 1 minute. The value is given as an integer.

$$\text{BER excess} = \frac{\text{No. of 1 min periods in STI in which BER} > 1 \cdot 10^{-3}}{\text{No. of 1 min periods in STI}} \times 100$$

II.2.13 **severely errored seconds ratio**

See Recommendation G.821.

II.2.14 **degraded minutes ratio**

See Recommendation G.821.

References

[1] KOU (K.Y.), O'NEAL (J.B.), NILSON (A.A.): Computations of DSI (TASI) overload as a function of the traffic offered, *IEEE Trans. on Communications,* Vol. COM – 33, No. 2, Feb. 1985.

[2] BRADY (P.T.): A model for generating on-off speech patterns in 2-way conversation, *Bell System Technical Journal,* page 2445 *et seq.*, Sep. 1969.

[3] Special Issue on bit rate reduction and speech interpolation, Guest Editors M.R. Aaron and N.S. Jayant, *IEEE trans. on Communications* Vol. COM 30 No. 4, April 1982.

7.7 Operations, administration and maintenance features of transmission equipment

Recommendation G.771

Q-INTERFACES AND ASSOCIATED PROTOCOLS FOR TRANSMISSION EQUIPMENT IN THE TELECOMMUNICATIONS MANAGEMENT NETWORK (TMN)

(Melbourne, 1988)

1 Introduction

1.1 *Scope*

This Recommendation defines the Q_1 and Q_2 interfaces and associated protocols required to connect transmission equipment to a TMN as defined in Recommendation M.30. Although primarily intended for use on transmission equipment, these interfaces may be used in other applications when appropriate.

A limited set of protocol suites is defined, from which an Administration may select those appropriate to their needs. Guidance is given on a suitable selection process. The set of protocol suites does not yet include a protocol suite capable of interworking with ISDN.

1.2 *Telecommunication management network*

A telecommunications management network (TMN) provides the means to transport and process information related to network operations, administration and maintenance. General principles of the TMN are described in Recommendation M.30. Figure 1/G.771 shows an example of the physical architecture for a TMN.

2 References

Recommendation M.30 – General principles of a TMN

Recommendation X.200 – Reference model of OSI for CCITT applications

Recommendation Q.513 – Interfaces for operations, administration and maintenance

3 Definitions

3.1 *Definitions associated with the TMN architecture*

Definitions of terms relative to the TMN architecture are defined in Recommendation M.30.

3.2 *Additional definitions*

3.2.1 **application messages**

Application messages are the messages flowing on the local communication network (LCN) and the data communication network (DCN) to meet the needs of TMN application functions.

3.2.2 **application message characteristics**

Application message characteristics are the application message attributes and information contents of the application messages.

3.2.3 **application message attributes**

Application message attributes are the attributes that characterize the requirements of communication functions for application messages in the LCN and DCN.

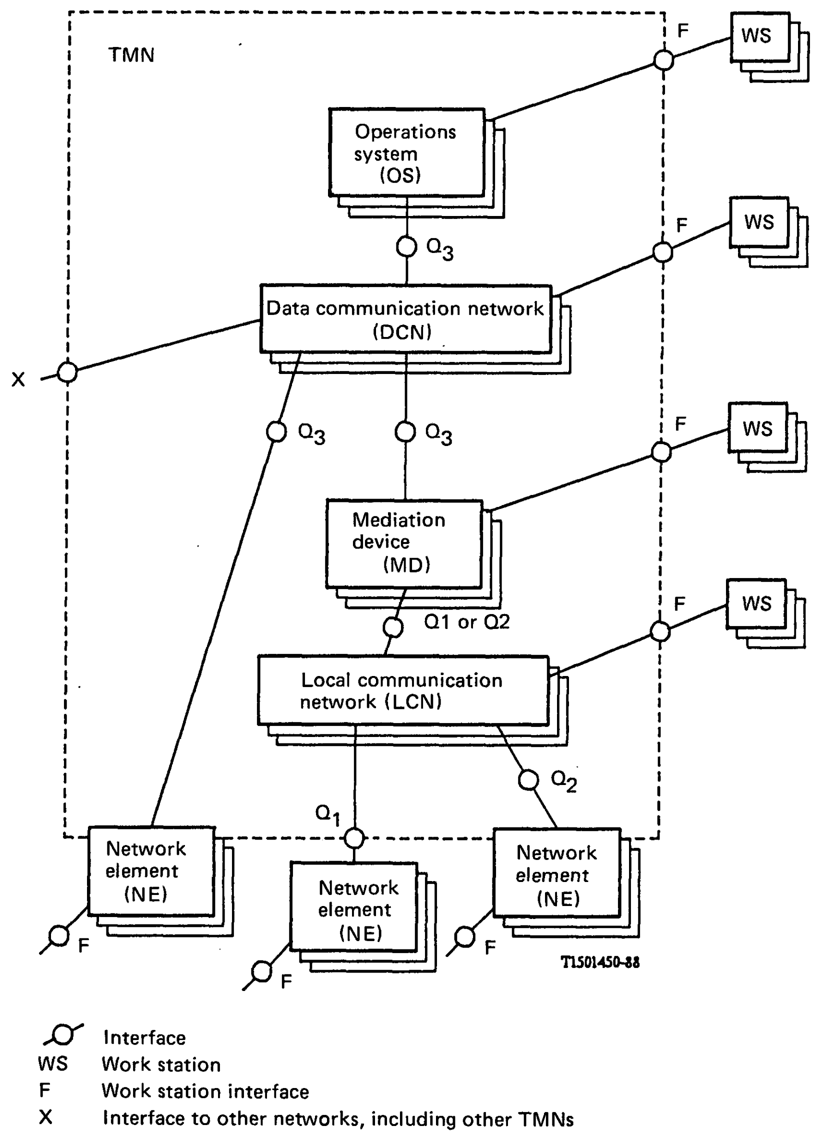


FIGURE 1/G.771

A generalized physical architecture for a telecommunications management network (TMN)

3.2.4 **application message information contents**

Application message information contents provide the structure and the meaning of application messages in the LCN and in the DCN.

3.2.5 **physical configuration attributes**

Physical configuration attributes are those characteristics related to the physical configuration of the LCN and the DCN.

3.2.6 **protocol selection attributes**

Protocol selection attributes are those characteristics of protocol suites related to their ability to meet the communication needs of application messages in the LCN and the DCN.

4 Q-interfaces

4.1 *Purpose*

The Q-interfaces provide for the interconnection of network elements (NEs), operations systems (OSs) and mediation devices (MDs) through the DCN and/or LCN. The purpose of an interface specification is to assure compatibility of devices interconnected, to accomplish a given TMN application function independent of the type of device or of the supplier.

The main purpose of the messages flowing over the Q-interfaces is to facilitate information exchange between network element functions and operation system functions. It is the task of the mediation function to extract or map the information from the one to the other. A list of mediation functions is given in Recommendation M.30. The definition of mediation devices requires further study.

The message transfer via the Q-interface requires the use of protocols. This Recommendation specifies a limited set of protocols, based on the 7 layer OSI model, which take into consideration the division of functions, interface attributes and economics.

4.2 *General physical characteristics of Q-interfaces*

The Q-interfaces are used for all communications within the TMN. (Annex A provides some examples.) A physical Q-interface appears at, or as close as possible to, a device. A device is a physical implementation of a function.

The DCN is used for communications between central operations systems and distributed telecommunications centres. It interfaces at the Q_3 standard interface (see Recommendation Q.513).

The highest level of MDs and OSs are implemented using the Q_3 interface. For practical reasons, an NE incorporating mediation functions may be provided with a Q_3 interface to communicate directly with OSs using the DCN.

The LCN connects at Q_1 and Q_2 standard interfaces as defined in this Recommendation. When operational or economic factors dictate, the LCN may also connect remote NEs to local MDs or to local NEs which incorporate mediation functions.

NEs containing no mediation functions are connected to MDs using the Q_1 interface. NEs containing some mediation functions are connected to MDs using the Q_2 interface. The Q_2 interface is also used for the connection between different MDs.

The Q-interfaces may also be used with Q-interface adapters for connecting the equipment with non-standardized M-interfaces, as specified in Recommendation M.30. Examples of using Q-interface adapters are provided in Annex A.

4.3 *General protocol characteristics*

The characteristics of the protocols associated with the Q-interfaces depend upon the functions to be performed. The need for two families of protocols, based on the 7 layer OSI model have been identified. The PQ(dcn) family, associated with Q_3 interface, is more complex than the PQ(lcn) family, associated with Q_1 and Q_2 interfaces which are capable of a more limited set of functions. Within the PQ(lcn) family, the protocol suites associated with the Q_1 interface will generally be simpler than those associated with Q_2.

Physical configuration attributes characterize the physical configuration of a set of MDs and NEs in a given implementation, and are important factors in the selection of protocol suites of the PQ(lcn) family of protocols.

Some LCN physical configuration attributes are provided in Annex B.

5 PQ(lcn) family of protocol suites

5.1 *Purpose*

The purpose of the PQ(lcn) family of protocol suites is to enable efficient communications to take place between mediation devices and network elements, and/or between mediation devices across the Q_1 and Q_2 interfaces within the telecommunication management network.

5.2 *Description of the family*

The family of PQ(lcn) protocol suites consists of a limited number of members. Each family member is a particular protocol suite and is distinguishable from other family members by protocol attributes defined in § 5.3.4.

A protocol suite consists of OSI layers 1-7. Not all layers of the OSI model have to be provided for the PQ(lcn) family of protocol suites.

5.3 *Guide to protocol suite selection*

5.3.1 *Purpose*

The purpose of this section is to define the process and to provide the information that is necessary to allow the selection of protocol suites from the sets of the PQ(lcn) family of protocols provided in § 5.4.

5.3.2 *PQ(lcn) protocol suite selection process*

The following steps are involved in an iterative manner to select the protocol suites that will satisfy user needs:

i) identify TMN application functions that will be carried by the LCN, as per Recommendation M.30;

ii) identify the distribution of mediation functions;

iii) identify the physical configuration attributes of the LCN;

iv) define the TMN application messages to be carried on the LCN;

v) prepare individual TMN application message characteristics which meet the needs of the TMN application functions. These are the characteristics of application messages that are to be carried on the LCN, on the basis of a set of application message characteristics provided in § 5.3.3;

vi) analyze both the physical configuration attributes and the individual application message characteristics in order to associate these with protocol selection attributes provided in § 5.3.4;

vii) select appropriate protocol suites which meet the needs of TMN application functions by associating the protocol selection attributes with members of the PQ(lcn) family of protocol suites.

Note – Figure 2/G.771 pictures the steps vi) and vii) of the selection process above. It should be noted that the application message characteristics pose requirements on the services provided at the application layer, which is the collective view of the services provided at all layers, whereas the protocol selection attributes are given for each OSI layer individually.

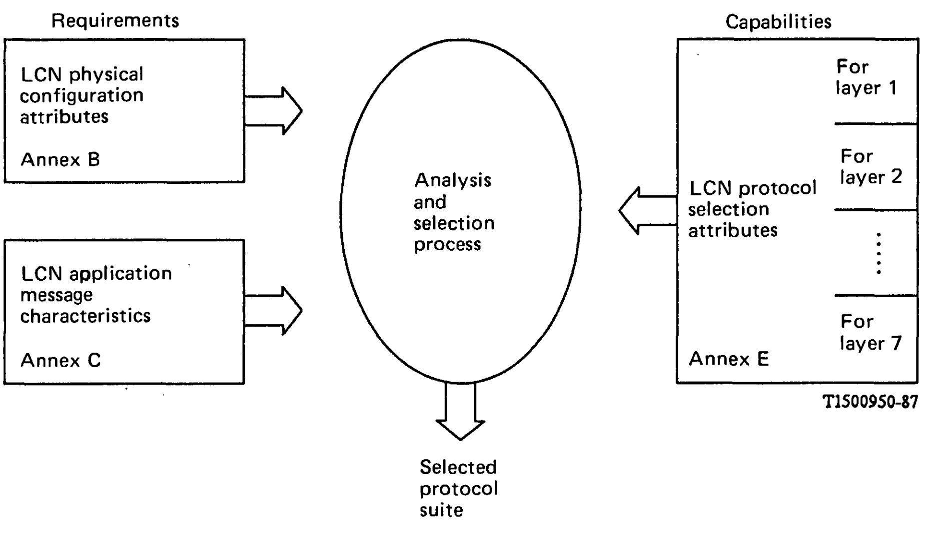


FIGURE 2/G.771

LCN protocol suite selection process

5.3.3 *TMN application message characteristics*

There are two types of characteristics that must be considered in the evaluation of application messages:

- application message attributes;
- application message information contents.

Annex C provides a list of possible LCN application message characteristics that can be applied to application messages.

Annex D provides an example of application messages profile characterization.

The values and names associated with application message characteristics in the LCN must be consistent with the values and names associated with overall TMN application message characteristics.

5.3.4 *LCN protocol selection attributes*

Annex E provides some LCN protocol selection attributes.

5.4 *Protocol suites*

This section defines the protocol suites to be used to support Q_1 and Q_2 interfaces and lists the protocol selection attribute values for each protocol suite.

5.4.1 *Protocol selection attribute values*

A table identifying the protocol selection attributes for each of the protocol suites defined in this Recommendation will be provided when protocol suites are included in the PQ(lcn) family.

Table F-5/G.771 provides an example of such a table for candidate protocol suites.

5.4.2 *Protocol suite definitions*

Several proposed candidate protocol suites can be found in Annex F. The choice of candidates for this section is under study.

ANNEX A

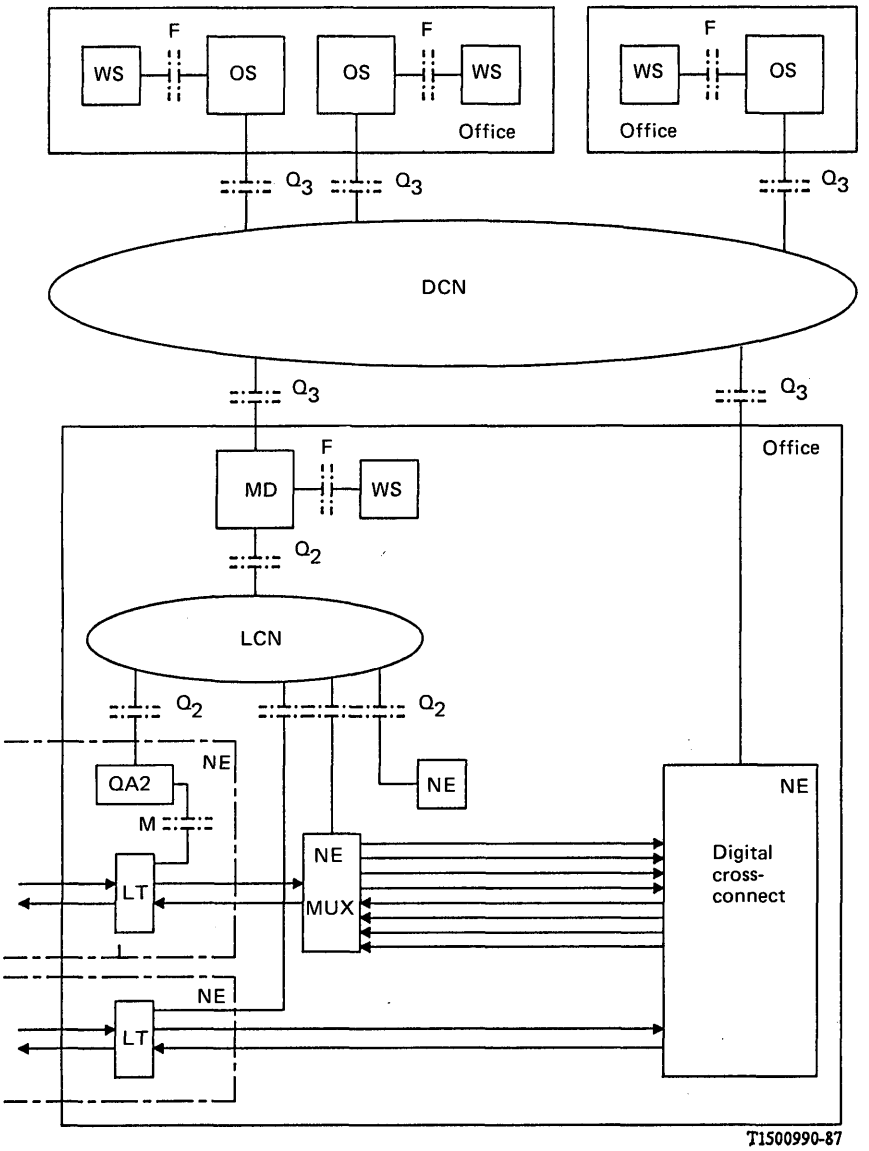
(to Recommendation G.771)

Examples of physical implementations using TMN architecture

The following are some of the equipments covered by Recommendation G.771:

- transmission terminals (multiplexers, digital cross-connects, channel translation equipments, etc.);
- digital and analogue transmission systems (via metallic and fibre cables, via radio and satellite, etc.);
- associated support systems (test modules, power supply systems, building alarm systems, fault location systems, etc.).

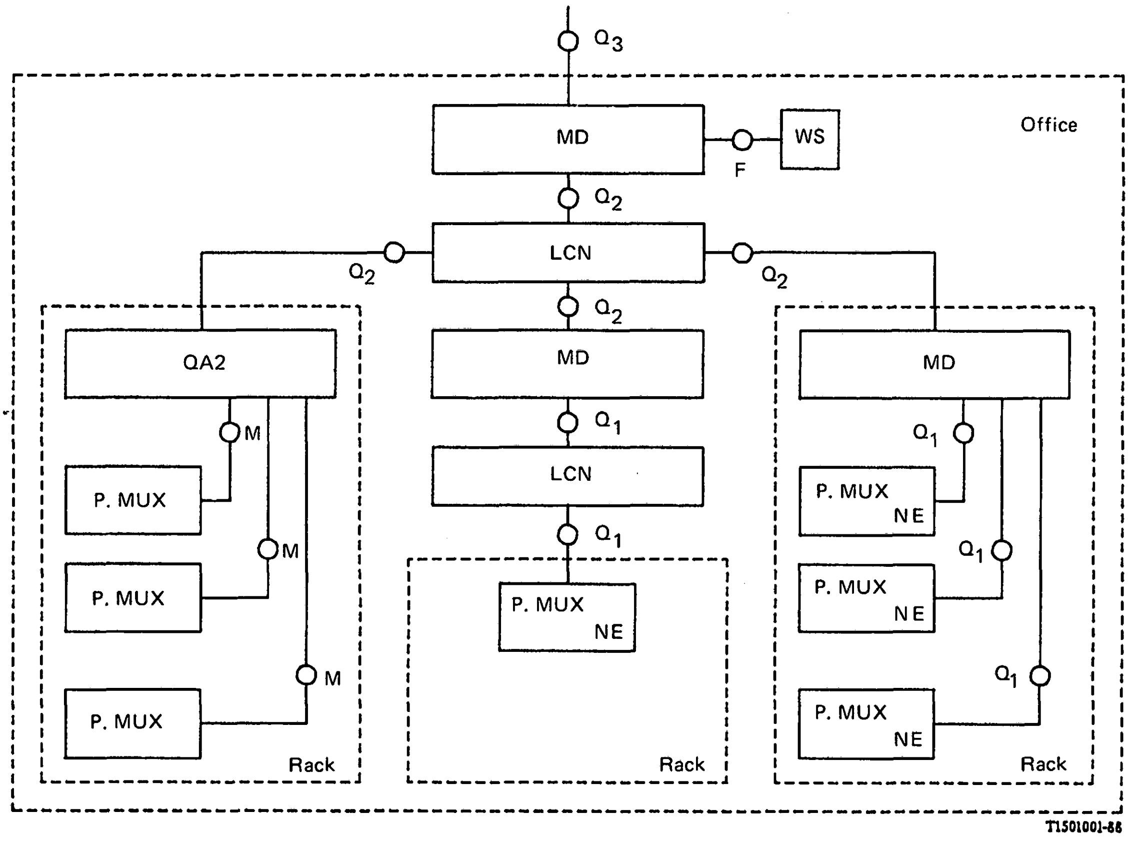
Examples of physical implementations using TMN architecture are shown in the following figures, A-1/G.771 and A-2/G.771.



OS Operation system
DCN Data communication network
MD Mediation device
NE Network element
WS Work station
Q, F Standardized interface
LT Line terminal
MUX Muldex
M Non-standardized maintenance interface
QA2 Q-interface adaptor 2
LCN Local communications network

FIGURE A-1/G.771

An example of physical TMN implementation



NE	Network element
P. MUX	Primary muldex
MD	Mediation device
M	Non-standardized maintenance interface
QA2	Q-interface adaptor 2
WS	Work station
Q, F	Standard interfaces

FIGURE A-2/G.771

An example of physical office implementation

ANNEX B

(to Recommendation G.771)

LCN physical configuration attributes

The LCN physical configuration attributes represent the requirements an Administration imposes on the configuration of the whole of the particular LCN to be designed. In the PQ(lcn) protocol suite selection process (§ 5.3.2), the LCN physical configuration attributes will not only influence the choice of PQ(lcn) protocol suite, but also determine the type and quantity of mediation devices needed.

During the design of the LCN the Administration may also consider the number of ports per configuration and the number of such configurations that can be served by a particular mediation device that implements the selected protocol suite. Together with the distribution of network elements over space and the extent of cascading the mediation devices, this leads to the layout of the LCN. However, such mediation device design characteristics are beyond the scope of this Recommendation.

Some LCN physical configuration attributes are:

B.1 *Number of NE ports*

Specifies how many network element local communication ports are to be served by an LCN (including mediation devices).

Descriptor: (ports)	small	≤ 32
	medium	$> 32, \leq 256$
	large	$> 256, \leq 2048$
	very large	> 2048

B.2 *Configuration*

Specifies the configuration to be used for the LCN.

Descriptor: star;
bus;
ring.

B.3 *Number of ports per configuration*

Specifies how many ports are to be interconnected within a single configuration (star, bus or ring) of the LCN.

For a star configuration, count the number of branches since one port per branch is implicitly assumed. For master-slave protocol suites for the bus or ring configuration, the master is excluded from the count of ports per configuration.

Descriptor: (ports)	small	≤ 8
	medium	$> 8, \leq 32$
	large	$> 32, \leq 128$
	very large	> 128

B.4 *Communication distance*

Specifies the distance to be bridged within the LCN.

Descriptor: (metres)	very short	≤ 10
	short	$> 10, \leq 100$
	medium	$> 100, \leq 1000$
	long	> 1000

B.5 *Communication environment*

Descriptor: within-rack;
on the same floor;
in-building;
out of building.

B.6 The need to provide further attributes is for further study.

ANNEX C

(to Recommendation G.771)

LCN application message characteristics

C.1 *Application message attributes*

C.1.1 *Communication pattern*

Response – subordinate node only answers questions and executes explicit commands.

Autonomous – subordinate node can also provide the master with other information (e.g. when polled).

Peer – subordinate node can also communicate with other subordinate nodes.

C.1.2 *Data quantity*

Amount of data transferred. General criteria of 4096 octets and 256 octets can be used as descriptor.

Descriptor: (octets)	low	≤ 256
	medium	$> 256, \leq 4096$
	large	> 4096

C.1.3 *Frequency*

Describes how often the message instance is expected to use the LCN.

Descriptor: (transactions per day)	seldom	≤ 1
	periodic	$> 1, \leq 1440$
	often	> 1440

C.1.4 *Delay*

Defines the amount of delay that can be accepted in LCN communication. Delay here does not include mediation processing time.

Descriptor: (seconds)	short	≤ 1
	medium	$> 1, \leq 10$
	long	> 10

C.1.5 *Multiple responses*

Denotes that there can be more than one response to a request from the same source.

Descriptor: single, multiple.

C.1.6 *Priority*

States the order of importance, or priority associated with a message.

Descriptor: yes, no.

C.1.7 *Receipt confirmation*

Critical messages communicated from one system may require confirmation that the peer system is in receipt of that specific data.

Descriptor: yes, no.

C.1.8 *Reliability*

Describes whether information can be lost or affected by transmission in the LCN.

Descriptor: (error)	low:	no requirement;
	medium:	infrequent;
	high:	none.

C.1.9 *Phase commit*

Required if a series of actions must be carried out in a coordinated manner by one or more NEs under supervision of MD.

Descriptor: yes, no.

C.1.10 *Availability*

The amount of isolation that can be tolerated from impairments in the LCN.

Descriptor: (%)	low	> 85
	medium	> 95
	high	> 99.5

C.1.11 *Data organization*

Describes whether the information is organized in files and the type of data organization associated.

Descriptor: (data organization) yes, no.

C.2 *Applications message information content*

The list below provides types of data elements that are common across operations functions. As such they will allow a structure to be provided for the information contained in specific messages and thus be eventually mapped into a notation associated with the LCN protocol.

The common data elements described below may not all be needed for every individual LCN nor will they necessarily be organized in the order given below.

C.2.1 *Type of message*

Refers to the mode of interaction and not the specific operation functions invoked by the message.

Example: message type (report, command, etc.).

C.2.2 *Type of resource*

Refers to the general network entity which is being managed.

Examples: fibre optic system; model X.

C.2.3 *Instance of resource*

Refers to the specific instance of the NE which is being managed, such as model X, number Y.

C.2.4 *Date/time*

May or may not be applicable.

C.2.5 *Name of the message*

Refers to the specific operation being performed.

Examples: equipment alarm report; equipment control command; facility performance report.

C.2.6 *Resource sub-entity*

Refers to the detailed resource sub-entity targeted by the operation.

Examples: fibre optic transmitter; primary rate circuit.

C.2.7 *Resource sub-entity instance*

Identification of the particular instance of the resource sub-entity.

Example: fibre optic transmitter No. 5.

C.2.8 *Message parameters*

Refers to data elements that are specific to the message name.

Examples: major or minor; error-free seconds.

C.2.9 *Result parameters*

These are the data elements that represent the values that, where applicable, will be associated with message parameters or other data elements.

Example: 100 error-free seconds.

C.2.10 *Error message type*

Category of reply to unsuccessful information exchange attempt.

Example: invalid alarm type.

C.2.11 *Error message parameters*

Parameters that may accompany error message types.

C.2.12 *Multiple response names*

This data element is a combination of other data elements in the situation where a specific message is part of a suitable response chain, for example, where individual messages must be referred to an initiating message.

C.2.13 *Multiple response parameters*

Output data elements associated with multiple response names.

ANNEX D

(to Recommendation G.771)

Examples of application message profile characterization

Example of fibre optic transmission system

Major Alarm Report

APPLICATION MESSAGE ATTRIBUTES:

1.	INITIATOR	______ NE ______
2.	DATA QUANTITY	______ Low ______
3.	FREQUENCY	______ Seldom ______
4.	DELAY	______ High ______
5.	MULTIPLE RESPONSES	______ Not applicable ______
6.	PRIORITY	______ Yes ______
7.	RECEIPT CONFIRMATION	______ ? ______
8.	RELIABILITY	______ High ______
9.	PHASE COMMIT	______ Not applicable ______
10.	AVAILABILITY	______ High ______
11.	DATA ORGANIZATION	______ Not applicable ______

APPLICATION MESSAGE INFORMATION CONTENT:

1.	TYPE OF MESSAGE	______ Report ______
2.	TYPE OF RESOURCE	______ Fibre optic transmission system XYZ ____
3.	INSTANCE OF RESOURCE	______ Unit number N ______
4.	DATE/TIME	______ YYYY/MM/DD __ HR/MIN/SEC __
5.	NAME OF MESSAGE	______ Equipment alarm report ______
6.	RESOURCE SUB-ENTITY	______ Transmit unit ______
7.	RESOURCE SUB-ENTITY INSTANCE	______ Channel number M ______
8.	MESSAGE PARAMETER	______ Laser failure ______
9.	RESULT PARAMETERS	______ Not applicable ______
10.	ERROR MESSAGE TYPE	______ Not applicable ______
11.	ERROR MESSAGE PARAMETERS	______ Not applicable ______
12.	MULTIPLE RESPONSE NAMES	______ Not applicable ______
13.	MULTIPLE RESPONSE PARAMETERS	______ Not applicable ______

ANNEX E

(to Recommendation G.771)

LCN protocol selection attributes

These LCN protocol selection attributes summarize the capabilities of the individual PQ(lcn) protocol suites for use in the LCN protocol suite selection process described in § 5.3.2.

Note – Abbreviations are given for each allowed attribute value as a key to Table F-5/G.771, which groups all the candidate selection attribute values.

The protocol selection attributes are:

a) At layer 1:

Configuration	S: star; B: bus; R: ring
Number of ports per configuration (ports)	S: small $\leqslant 8$ M: medium $> 8, \leqslant 32$ L: large $> 32, \leqslant 128$ VL: very large > 128
Physical medium	SP: screened pair; TP: twisted pair; CP: coaxial pair; OF: optical fibre; O: other
Transmission mode	S: synchronous; AS: asynchronous; HD: half duplex; FD: full duplex
Operating speed (bits per second)	1200; 2400; 4800; 9600; 19 200; 64 000; 128 000; 1 000 000
Communication distance (metres)	VS: very short $\leqslant 10$ S: short $> 10, \leqslant 100$ M: medium $> 100, \leqslant 1000$ L: long > 1000
Communication environment	WR: within-rack; OF: on the same floor; IB: in-building; OB: out of building
Availability (%)	L: low M: medium H: high (L, M, H: under study)

b) At layer 2:

Data link connection	CO: connection oriented CL: connection-less
Data link initiator	M: master; AP: all participants
Data link address size (addresses)	S: small $\leqslant 8$ M: medium $> 8, \leqslant 32$ L: large $> 32, \leqslant 128$ VL: very large > 128
Receipt confirmation	Y: yes; N: no
Maximum frame size (octets)	S: small $\leqslant 256$ M: medium $> 256, \leqslant 4096$ L: large > 4096
Max. frame frequency per port (frames per second)	L: low $\leqslant 1/60$ M: medium $> 1/60, \leqslant 1$ H: high > 1

Max. frame transmit delay (seconds)	S: short ⩽ 0.1 M: medium > 0.1, ⩽ 1 L: long > 1
Error detection	N: none; P: parity, CS: checksum (n); CRC: cyclic redundancy check (n)
Hamming distance	1; 2; 3; 4; n
Error recovery	N: none; R: repetition; C: correction

c) At layer 3:

LCN network size (ports)	S: small ⩽ 32 M: medium > 32, ⩽ 256 L: large > 256, ⩽ 2048 VL: very large > 2048
Routing	Y: yes; N: no
(Un) packing	Y: yes; N: no
Connections	N: none; P: permanent; SW: switched
Priority	Y: yes; N: no

d) The other layers are for further study.

ANNEX F

(to Recommendation G.771)

Proposed candidate protocol suites

This annex contains the candidate protocol suites currently under consideration for selection as members of the PQ(lcn) family of protocol suites. The description of the individual protocol suites is of varying completeness, but each description is limited to the specification of the lower two or three OSI layers. For a complete protocol suite specification, higher layers must be defined; however, the available information is provided here to guide hardware decisions. The completion of the descriptions and the selection is for further study.

Candidate protocol suite No. 3 has the widest support, but no candidate protocol suite has yet been subjected to a formal selection process by CCITT.

Each candidate protocol suite is described in the following sections. Following the descriptions is a summary section which contains in Table F-5/G.771 the candidate protocol selection attribute values (see Annex E). Differences of the values in Table F-5/G.771 indicate differences in capabilities which may affect the suitability of individual candidates for particular application areas.

Some initial applications are indicated for each candidate protocol suite. However, the range of applications appropriate to these suites has not been thoroughly examined.

F.1 *Candidate protocol suite No. 1 (CPS 1)*

Initial application:

Alarm surveillance, performance monitoring and configuration control of NEs found in reasonably large numbers in the telecommunications network (e.g. muldex, line transmission terminal).

F.1.1 *OSI layer 1*

F.1.1.1 *Configuration*

One serial bus connects up to 30 nodes.

Configurations with more than 30 nodes can be realized by a hierarchical structure of several serial buses.

Such a hierarchical structure is characterized by a high throughput with a low transmission rate per bus.

F.1.1.2 *Communication environment*

The serial bus configuration shall be used only for in-building application.

F.1.1.3 *Physical connection*

One balanced, screened pair with a maximum length of 500 metres.

F.1.1.4 *Electrical requirements*

Each bus interface shall be in accordance with Recommendation V.11 multipoint interconnections [1, 3, 14, and 23].

Each bus shall be terminated by resistors in accordance with [23].

Each receiver shall present a maximum of one unit load to the bus, as defined in [23].

F.1.1.5 *Line code*

The line code shall be NRZ (non-return to zero).

F.1.1.6 *Speed*

The bit rate shall be 19.2 kbit/s.

The bit rate tolerance shall be ± 1%.

F.1.1.7 *Transmission mode*

The transmission mode shall be half duplex, asynchronous.

F.1.2 *OSI layer 2*

Asynchronous, byte oriented protocol according to [15].

F.1.2.1 *Transmission frame format*

The transmission frame format shall be in accordance with [15 (i)].

F.1.2.2 *Link transmission procedure*

The link transmission procedure shall be in accordance with [15 (ii)].

All standard transmission frames specified in [15] shall be used (frame with variable length, frame with fixed length and single character).

The operation mode shall be: master/slave, cyclical polling.

F.1.2.3 *Addressing*

The addresses 1 to 30 of the 256 possible addresses shall be used for cyclical polling.

The address 255 shall be used for broadcasting (one message to all nodes).

F.1.2.4 *Window size*

The window size is fixed to one.

F.1.3 *Higher layers*

Under study.

F.2 *Candidate protocol suite No. 2 (CPS 2)*

Initial application:

Alarm surveillance, performance monitoring, testing commands and response, and configuration control of NEs including cross-connect equipment, can be applied to both NEs found in reasonably large numbers in the telephone network (e.g., muldex, line transmission terminal) and to high capability NEs found in limited numbers in the telecommunications network (e.g. cross-connect).

F.2.1 *OSI layer 1*

F.2.1.1 *Configuration*: Bus.

F.2.1.2 *Line speed*: 1 Mbit/s.

F.2.1.3 *Medium*: Screened pair.

F.2.1.4 *Electrical requirement*: Recommendation V.11 interface with pulse transformer.

F.2.1.5 *Line code*: CMI.

F.2.2 *OSI layer 2*

F.2.2.1 *Frame format*

Frame components:

- flag,
- destination address: 2 octets,
- source address: 2 octets,
- control: 1 octet,
- logical link control (LLC) data: variable length (maximum 512 octets),
- frame check sequence: CRC 16,
- flag.

F.2.2.2 *Media access control*

The media access control discipline known as carrier sense multiple access (CSMA) is used [12, 18].

F.2.2.3 *Logical link control layer*

Acknowledged connectionless mode protocol specification to be specified in [11, 17] is used.

F.2.3 *Upper layers*

Under study.

F.3 *Candidate protocol suite No. 3 (CPS 3)*

Initial application:

Alarm surveillance, performance monitoring, and configuration control of NEs found in reasonably large numbers in the telecommunications network (e.g. muldex, line transmission terminals).

F.3.1 *OSI layer 1*

F.3.1.1 *Physical characteristics*

F.3.1.1.1 *Configuration*

Serial bus operation in accordance with [14] (ring configuration under study).

Use of full or half-duplex operation shall be determined by the Administration.

F.3.1.1.2 *Transmission pairs*

Two screened balanced pairs, one pair for each direction of transmission.

Note – Two Administrations have proposed using each of the pairs in half-duplex mode to provide additional bus security without additional wiring. Certain additional requirements relating to bus occupancy may then be necessary for correct operation in this mode.

F.3.1.1.3 *Bus security*

Where additional bus security is required, bus duplication or output driver protection resistors may be considered.

Note – Where duplicated buses are employed, no deliberate transmission should take place on both buses at the same time, and the functioning of one bus shall not be prejudiced by continuous noise or unintentional transmissions on the other.

F.3.1.1.4 *Connector*

The Administration shall specify the connector type.

F.3.1.2 *Electrical characteristics*

F.3.1.2.1 *Static and dynamic characteristics*

Static and dynamic characteristics of each bus connection shall be in accordance with [14].

F.3.1.2.2 *Bus termination*

Each bus end shall be terminated by resistors (120 ohms +10%, −0%) in accordance with [14].

F.3.1.2.3 *Load connection*

Each receiver shall present a maximum of one unit load, as defined in [14], to the bus. The number of load connections is limited to 32.

F.3.1.2.4 *Bit rate*

The bit rate shall be 19.2 or 64 kbit/s. A bit rate of 128 kbit/s may be necessary in some applications. The bit rate tolerance shall be ± 1%.

F.3.1.2.5 *Turn-off time*

A transmitting station shall put its generator in the high impedance state within 1 ms from the end of the last bit of the final closing flag.

Note – The need to reduce this time for bit rates above 19.2 kbit/s is under study.

F.3.1.2.6 *Preamble*

Following the enabling of the generator, an implementation dependant preamble of no more than 4 bit times is allowed. No assumption as to the state of the bus during this preamble is allowed.

F.3.1.3 *Line code*

The line code shall be NRZ1.

Clock extraction by the remaining station is assumed.

F.3.1.3.1 *Principle*

Each transition [14] shall represent a ZERO, and no transition shall represent a ONE bit.

F.3.1.3.2 *Lock-in process*

For clock extraction, a lock-in sequence of either one octet of ZEROES or one or two flags in accordance with [6], shall be sent immediately prior to the beginning of the opening flag of the frame to be transmitted and immediately following the preamble of § F.3.1.2.6 (if implemented).

F.3.1.4 *Extended mode*

Where an extended mode capability is required (e.g., using a modem) the requirements of §§ F.3.1.1 to F.3.1.3 shall apply with the following exceptions:

F.3.1.4.1 *Configuration – full duplex*

F.3.1.4.2 *Connector*

The connector shall conform to [16]. Appropriate signal leads are to be provided for modem control in accordance with Recommendation V.24 [2], [22]. See Table F-1/G.771.

F.3.1.4.3 *Electrical requirements*

Data set control leads shall conform to Recommendation V.24 [2], [22].

F.3.1.4.4 *Line code*

NRZ line code shall be employed. A separate clock distribution shall be provided.

F.3.1.4.5 *Speed*

The bit rate shall be 9.6 or 64 kbit/s. Lower speed, e.g. 1.2, 2.4 and 4.8 kbit/s, may be necessary in some applications.

F.3.2 *OSI layer 2*

The data link protocol is synchronous HDLC type.

F.3.2.1 *HDLC frame structure*

The HDLC frame structure shall conform to [6] (frame structure).

F.3.2.1.1 *Addressing field*

The addressing field shall be one octet.

F.3.2.1.2 *Information field*

The information field in any HDLC frame shall be an integral number of octets.

Information field octets shall be sent with the least significant bit first.

Maximum information field lengths of 128 and 256 octets shall be supported.

A maximum information field length of 512 octets may be necessary in some applications.

F.3.2.2 *Addressing*

The secondary station shall be capable of being assigned any address in the range 1 to 254.

F.3.2.2.1 *All-station address*

The address field pattern "11111111" is defined as the all-station address.

F.3.2.2.2 *No station address*

The address field pattern "00000000" is defined as the no-station address.

The no-station address shall never be assigned to a secondary station.

F.3.2.2.3 *Group address*

Not used.

F.3.2.3 *HDLC procedure*

The HDLC procedure is defined by [7].

F.3.2.3.1 *Commands and responses*

The following HDLC commands and responses must be supported:

a) commands:
   - SNRM: set normal response mode;
   - DISC: disconnect;

b) commands or responses:
   - I: information;
   - RR: receive ready;
   - RNR: receive not ready;

c) responses:
   - FRMR: frame reject;
   - UA: unnumbered acknowledgement;
   - DM: disconnected mode.

F.3.2.3.2 *Modes*

Two modes are selected:

- one operational mode: normal response mode (NRM);
- one non-operational mode: normal disconnected mode (NDM).

F.3.2.4 *Class of procedure*

The Unbalanced operation Normal response mode Class (UNC) as defined by [9] shall be implemented.

F.3.2.4.1 *HDLC optional functions*

The following HDLC optional functions shall be implemented:

a) unnumbered information (option No. 4):
   - command UI;
   - response UI;

b) data link test (option No. 12):
   - command TEST;
   - response TEST.

F.3.2.5 *Other parameters of OSI layer 2*

F.3.2.5.1 *Window size*

The window size is fixed to 1.

3.2.5.2 *Waiting-time before a repetition*

In the case of no-reply or lost-reply, the primary station shall provide a waiting-time function.

The waiting-time before a repetition has to be greater than the duration of the longest frame to be sent by the primary station, added with the response-time of the secondary station and the duration of the longest frame to be sent by the secondary station.

F.3.2.5.3 *Number of repetitions*

In the situation of § F.3.2.5.2, the maximum number of repetitions before detecting a no-reply or a lost-reply condition is fixed at 5 (6 requests).

F.3.2.5.4 *Response time*

The secondary station shall commence the opening flag of its response not later than 5 ms after the end of the closing flag of the frame sent from the primary station.

Note – The need to reduce this time for bit rates above 19.2 kbit/s is under study.

F.3.3 *Higher layers*

Under study.

TABLE F-1/G.771

Pin description of 24-pin connector [16]

Pin	V.24 circuit	Description	Notes
1	101	Protective ground	1
13	102	Signal ground	
2	103	Send data A-wire	
14	103	Send data B-wire	
11	104	Receive Data A-wire	
23	104	Receive Data B-wire	
3	105	Request to Send A-wire	2
15	105	Request to Send B-wire	2
7	106	Clear to Send A-wire	2
19	106	Clear to Send B-wire	2
8	107	Data Mode A-wire	2
20	107	Data Mode B-wire	2
9	109	Receiver Ready A-wire	2
21	109	Receiver Ready B-wire	2
6	114	Send Timing A-wire (DCE to DTE)	
18	114	Send Timing B-wire (DCE to DTE)	
10	115	Receive Timing A-wire (DCE to DTE)	
22	115	Receive Timing B-wire (DCE to DTE)	

Note 1 – Equipment: removable strap to frame ground.
Cable: connected to shield.

Note 2 – These circuits are optional for connection to an embedded operations channel or modem and are not used for connections to a multipoint bus.

Note 3 – Circuits are grouped by function: ground, data, control and timing.

Provision should be made at each interface point on a multipoint bus for the continuation of the interface to the next network element.

Provision shall be made for the termination of the lines in their characteristics impedance (typically, 120 ohms, resistive), should the equipment be at one of a multipoint bus.

For further information, see [2], [16], [22], [23].

F.4 *Candidate protocol suite No. 4 (CPS 4)*

Initial application:

Alarm surveillance, performance monitoring, testing on specific NEs found in limited numbers in the telecommunications network (e.g. muldex, line transmission equipment).

F.4.1 *Layer 1*

- Electrical characteristics in accordance with Recommendations V.24 and V.28 [20];
- Configuration: star;
- Physical connection: ISO 2110 (25 pin) (see Table F-2/G.771);
- Transmission mode: duplex, interface type D;
- Operating speed: 1200, 2400, 4800 and 9600 bit/s (user option);
- Shield: ground strap to frame (user option).

TABLE F-2/G.771

ISO 2110 pin description

Pin	V.24 circuit	Description	Notes
1	101	Protective ground	1
7	102	Signal ground	2
2	103	Transmitted data	2
3	104	Received data	2
4	105	Request to Send	2
5	106	Clear to Send	2
6	107	Data Set Ready	2
20	108.2	Data Terminal Ready	3
22	125	Ring indicator	3
8	109	Received Line Signal Detector	2
24	113	Transmitter Signal Element Timing (DTE to DCE)	4
15	114	Transmitter Signal Element Timing (DCE to DTE)	5
17	115	Receiver Signal Element Timing (DCE to DTE)	5

Note 1 – Equipment: removable strap to frame ground.
Cable: connected to shield.

Note 2 – Basic interchange circuits, all systems.

Note 3 – Additional interchange circuits required for switched service.

Note 4 – Circuit DA (CCITT 113) is not used in OS/NE interfaces.

Note 5 – Additional interchange circuits required for synchronous channel.

Note 6 – Duplex, interface type D.

Circuits are grouped by function: ground, data, control and timing.

For further information, see [2], [3], [5], [19].

F.4.2 *Layer 2*

It is mandatory that the data link layer conform to LAPB as defined in Recommendation X.25 [4]. In addition, provision shall be made for connection between data terminal equipments (OSs and NEs) without an intervening packet switched network. The interface shall conform to [8].

The link layer specification that follows applies to all cases.

F.4.2.1 *Equipment type during link set-up and reset*

When a packet switched network is used to connect the NE and OS, they each are designated Data Terminal Equipment (DTE) and the network acts as a Data Circuit-Terminating Equipment (DCE). When a dedicated or dial-up link is provided, other means must be used to supply the DCE role.

At level 1, the modems will provide the DCE interface, supplying bit synchronization.

At the link level, the procedures specified in [8] are followed. The NE or OS must be able to start the set-up or reset of the link (a DCE function in Recommendation X.25) as well as to respond to a start from the connecting equipment (a DTE function in Recommendation X.25). In addition, provision must be made for assignment of the A/B addresses. This mandatory option is to be field-settable and stored in non-volatile memory. Equipment which meets this requirement is compatible with connection to either a DCE or remote DTE.

F.4.2.2 *Window*

Modulo 8 operation shall be used. The window for unacknowledged frames is to be optional between 1 and 7 frames. Typical values are 7 and 2.

F.4.2.3 *User information*

The user information is to be arranged in an integral number of octets.

The maximum length of the user information shall be user settable, consistent with the range of values for the N1 parameter as shown in Table F-3/G.771. Maximum information field lengths that shall be supported are 131 and 259 octets with 515 octets optional. These values provide for three packet header octets and maximum length of packet data units of 128, 256 and 512 octets respectively.

F.4.2.4 *Other frame parameters*

Certain other frame parameters shall be set by the user to be consistent with the bit rate, frame size and characteristics of the connecting network. The NE design should be sufficiently flexible to accommodate parameter sets for diverse networks, both as order options and later reconfigurations. The range of parameters is shown in Table F-3/G.771. These options, like those of the physical layer, are to be set at installation, changeable by the user, and non-volatile.

F.4.3 *Other layers*

No layer 3 is planned for this suite.

Layers 4-7 are under study.

F.5 *Candidate protocol suite No. 5 (CPS 5)*

Initial application:

All management of high capability NEs found in limited numbers in the telecommunications network (e.g. digital cross-connect).

F.5.1 *Layer 1*

– Electrical characteristics in accordance with Recommendations V.24 and V.28 [20];
– Configuration: star;
– Physical connection: ISO 2110 (25 pin) (see Table F-2/G.771);
– Transmission mode: duplex, interface type D;
– Operating speed: 1200, 2400, 4800 and 9600 bit/s (user option);
– Shield: ground strap to frame (user option).

TABLE F-3/G.771

LAPB data link layer attributes

LAPB Protocol Octet aligned			
Single link procedure (SLP)	Range	Default values (Note 1)	Units
K – I-Frames window:	1 to 7	7	
T1 – Waiting acknowledgement (Retry) timer:	2 to 20	3	seconds
T2 – Response delay timer	0.3		seconds
T3 – Disconnect time	Note 2		
T4 – No activity timer	4 to 120	20	seconds
N1 – Bits per I-Frame, excluding flags	1080, 2104	1080	bits
N2 – Retransmission count	2 to 16	7	
A/B address assignment	Selectable by the user		

Note 1 – The default values shall be part of a vendor's offering. That is, unless otherwise specified by the user, the default parameters shall be the initial values supplied. They can be subsequently changed by the user within the specified range.

Note 2 – The value of time T3, the disconnect timer, is not critical for successful interworking of OSs and NEs. Therefore no value is specified.

F.5.2 *Layer 2*

It is mandatory that the data link layer conform to LAPB as defined in Recommendation X.25 [4]. In addition, provision shall be made for connection between data terminal equipments (OSs and NEs) without an intervening packet switched network. The interface shall conform to [8].

The link layer specification that follow applies to all cases.

F.5.2.1 *Equipment type during link set-up and reset*

When a packet switched network is used to connect the NE and OS, they each are designated data terminal equipment (DTE) and the network acts as a data circuit-terminating equipment (DCE). When a dedicated or dial-up link is provided, other means must be used to supply the DCE role.

At level 1, the modems will provide the DCE interface, supplying bit synchronization.

At the link level, the procedures specified in [8] are followed. The NE or OS must be able to start the set-up or reset of the link (a DCE function in Recommendation X.25) as well as to respond to a start from the connecting equipment (a DTE function in Recommendation X.25). In addition, provision must be made for assignment of the A/B addresses. This mandatory option is to be field-settable and stored in non-volatile memory. Equipment which meets this requirement is compatible with connection to either a DCE or remote DTE.

F.5.2.2 *Window*

Modulo 8 operation shall be used. The window for unacknowledged frames is to be optional between 1 and 7 frames. Typical values are 7 and 2.

F.5.2.3 *User information*

The user information is to be arranged in an integral number of octets. In other words, the data is to be structured in 8 bit bytes.

The maximum length of the user information shall be user settable, consistent with the range of values for the N1 parameter as shown in Table F-3/G.771. Maximum information field lengths that shall be supported are 131 and 259 octets with 515 octets optional. These values provide for three packet header octets and maximum length of packet data units of 128, 256 and 512 octets, respectively.

F.5.2.4 *Other frame parameters*

Certain other frame parameters shall be set by the user to be consistent with the bit rate, frame size and characteristics of the connecting network. The NE design should be sufficiently flexible to accommodate parameter sets for diverse networks, both as order options and later reconfigurations. The range of parameters is shown in Table F-3/G.771. These options, like those of the physical layer, are to be set at installation, changeable by the user, and non-volatile.

F.5.3 *Layer 3*

It is mandatory that the packet layer conform to Recommendation X.25. In addition the packet layer must provide for connection of data terminal equipment (OSs and NEs) without an intervening packet network; the required interface for this purpose conforms to [10]. In addition, the provisions of [13] shall apply.

The attributes which must be supported are summarized in Table F-4/G.771. Note in particular that this table shows the different attributes needed to support PVCs (the X.25/PVC procedures) and SVCs (the X.25/SVC procedures).

F.5.3.1 *Equipment type during restart*

When the packet level X.25 interface is used, automatic selection of the DCE/DTE role during restart is required, as specified in [10].

F.5.3.2 *Other features and parameters*

The packet layer attributes are summarized in Table F-4/G.771.

F.5.4 *Higher layers*

Under study.

F.6 *Candidate protocol suite No. 6 (CPS 6)*

Initial application:

Alarm surveillance, performance monitoring and configuration control of NEs found in reasonably large numbers in the telecommunications network (e.g. muldex, line transmission terminal).

F.6.1 *Interface characteristics*

F.6.1.1 *General characteristics*

- Network topology: "loop" (a variety of a ring chain configuration);
- Serial data transmission;
- Master-slave principle;
- Maximum number of slaves: 30;
- Transmission medium: one balanced screened pair (with the possibility of providing bypasses of faulty sections of the "loop" and slaves);
- Maximum connection length between two connected slaves: 1000 m.

TABLE F-4/G.771

X.25 packet layer attributes

Attributes	Range (Notes 1, 2)	Default values (Note 3)	Units
Permanent virtual circuits			
Packet size	128, 256, 512 optional	128	octets
Window size	1-7	2	
Interrupt packets	optional		
Switched virtual circuits			
Flow control parameter negotiation			
Packet size	128, 256, 512 optional	128	octets
Window size	1-7	2	
Throughput class negotiation			
Bit rate	1200, 2400, 4800, 9600	2400	bit/s
Expedited data negotiation			
Closed user group			
Closed user group selection			
Basic format	2		decimal digits
Fast select	128		octets
Fast select acceptance			
Hunt group			
Transit delay selection and indication			
Calling address extension			
Called address extension			
Minimum throughput class negotiation			
End-to-end transit delay negotiation			

Note 1 – The ranges specified for negotiated parameters in no way affect the normal negotiation rules specified in the international standards.

Note 2 – The attributes which are not marked optional are mandatory.

Note 3 – The default values shall be part of a vendor's offering. That is, unless otherwise specified by the user, the default parameters shall be the initial values supplied. They can be subsequently changed by the user within the specified range.

F.6.1.2 *Layer 1 of the ISO-OSI reference model* (physical layer)

– Electrical characteristics in accordance with Recommendations V.11 and V.24 [1], [2], [21];

– Transmission method: asynchronous;

– Mode of operation of the slave: duplex;

– Transmission rate: $\leqslant$ 19 200 bit/s.

F.6.1.3 Further layers are under study.

TABLE F-5/G.771

Candidate protocol selection attribute values

Attribute	CPS 1	CPS 2	CPS 3	CPS 4	CPS 5	CPS 6
Layer 1						
Configuration	B	B	B,R [a]	S	S	R
No. of ports per configuration	M	VL	M	M	M	M
Physical medium	SP	SP	SP	SP	SP	SP
Transmission mode	AS-HD	S-FD	S-HD,FD	S-FD	S-FD	AS-HD
Operating speed (bit/s)	19 200	1 000 000	19 200 64 000 128 000	1200 9600	1200 9600	⩽ 19 200
Communication distance	M	M	M(L)	M(L)	M(L)	M
Communication environment	IB	IB	IB(OB)	IB(OB)	IB(OB)	IB
Availability [a]						
Layer 2						
Data link connection	CO	CL	CO	CO	CO	CO
Data link initiator	M	AP	M	AP	AP	M
Data link address size	M	VL	VL	S	S	[a]
Receipt confirmation	Y	Y	Y	Y	Y	Y
Max. frame size	S	M	S,M	S,M	S,M	S
Max. frame frequency per port	H	H	H	H	H	M
Max. frame transmit delay	M	S	M	S,M	S,M	S
Error detection	P+CS8	CRC16	CRC16	CRC16	CRC16	CRC
Hamming distance	4					
Error recovery	R	R	R	R	R	R
Layer 3						
LCN network size					VL	
Routing					Y	
(Un) packing					Y	
Connections					P,SW	
Priority					Y	
Higher layers [a]						

[a] Under study.

Note – An explanation of the abbreviations used in this Annex is given in Annex E.

References

[1] CCITT Recommendation *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communication*, Vol. VIII, Rec. V.11.

[2] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment*, Vol. VIII, Rec. V.24.

[3] CCITT Recommendation *Electrical characteristics for unbalanced double-current interchange circuits*, Vol. VIII, Rec. V.28.

[4] CCITT Recommendation *Interface between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE) for terminals operating in the packet mode and connected to public data networks by dedicated circuit*, Vol. VIII, Rec. X.25.

[5] ISO 2110 *Data communications – 25-pin DTE/DCE interface connector and pin assignments.*

[6] ISO 3309 *Data communications – High-level data link control procedures – Frame structure.*

[7] ISO 4335 *Data communications – High-level data link control procedures – Consolidation of elements of procedures.*

[8] ISO 7776 *Data communications – High-level data link control procedures – Description of the X.25 LAPB-compatible DTE data link procedures.*

[9] ISO 7809 *Data communications – High-level data link control procedures – Consolidation of classes of procedures.*

[10] ISO 8208 *Information Processing Systems – X.25 packet level protocol for data terminal equipment.*

[11] ISO 8802.2 *Information Processing Systems – Local area networks – Part 2: Logical link control.*

[12] ISO 8802.3 *Information Processing Systems – Local area networks – Part 3: Carrier sense multiple access with collision detection.*

[13] ISO 8878 *Data communications – Use of X.25 to provide the OSI connection-mode network service.*

[14] ISO DIS 8482 *Data communications – Twisted pair multipoint interconnections.* Compatible with Rec. V.11 and Reference 23.

[15] IEC TC 57 Part 5
(i) IEC TC 57 Part 5-1. Format FT 1.2
(ii) IEC TC 57 Part 5-2.

[16] IEEE STD 488 *Standard digital interface for programmable instrumentation.*

[17] IEEE STD 802.2 *Local area networks – Logical link control.*

[18] IEEE STD 802.3 *Local area networks – Carrier sense multiple access/collision detection.*

[19] EIA-232-C *Interface between Data Terminal Equipment and Data Communications Equipment employing serial binary data interchange.*

[20] EIA-232-D *Interface between Data Terminal Equipment and Data Circuit-Terminating Equipment employing serial binary data interchange.*

[21] EIA-422 *Electrical characteristics of balanced voltage digital interface circuits.*

[22] EIA-449 *General purpose 37-position and 9-position interface for Data Terminal Equipment and Data Circuit-Terminating Equipment employing serial binary data interchange.*

[23] EIA-485 *Electrical characteristics of generators and receivers for use in balanced digital multipoint systems.*

DIGITAL PROTECTED MONITORING POINTS

(Melbourne, 1988)

Note – The detailed requirements contained in this Recommendation are applicable to the 2048 kbit/s hierarchy. The application of the principles defined in this Recommendation to the 1544 kbit/s hierarchy is for further study.

1 Definition

A **protected monitoring point (PMP)** provides a digital interface at which it is possible to monitor the transmitted signal and to make measurements with suitable test equipments [1].

2 Location

The possible locations for protected monitoring points can be:

a) at the output ports of an equipment;

b) in the signal path between equipments.

Some examples are shown in Figure 1/G.772.

3 Electrical characteristics of the protected monitoring point

Note – The reference for all parameters associated with protected monitoring points shall be the relevant output interface as defined in Recommendation G.703 [2] (see Figures 1/G.772 and 2/G.772).

3.1 *Impedance*

The load impedance presented by the test equipment at the protected monitoring point is the nominal impedance for the corresponding transmission path interface as defined in Recommendation G.703.

3.2 *Attenuation*

The attenuation between the transmission path interface and the protected monitoring point, when the impedance presented by the test and measuring equipment connected to the protected monitoring point is equal to the nominal impedance for the relevant interface as defined in Recommendation G.703, shall be $A \pm 1$ dB for all frequencies in the range 2.5% to 150% of the nominal bit rate at the interface (see Figure 2/G.772).

Different values may be necessary at different nominal bit rates.

The value of A is under study.

The digital signal level presented at the transmission path interface of the protected monitoring point shall be as defined in Recommendation G.703 but modified by the characteristics of the interconnecting cable. The attenuation of the cable shall be assumed to follow a $\sqrt{f}$ law and the loss X at a frequency equal to half the nominal bit rate is given below:

$0 \leqslant X \leqslant 3$ dB for 64 kbit/s

$0 \leqslant X \leqslant 6$ dB for 2 and 8 Mbit/s

$0 \leqslant X \leqslant 12$ dB for 34 and 140 Mbit/s.

Note – For a protected monitoring point device at an equipment output port, as described in Figure 1a/G.772, the value of X is 0 dB.

3.3 *Protection of the PMP device*

3.3.1 The protection of the protected monitoring point device against electrostatic discharges shall accord with the requirements of Recommendation K.21 [3] and IEC Publication 801-2 [4].

3.3.2 No damage shall result from the application of any load impedance, including short and open circuits, to the protected monitoring point.

3.3.3 The protection against the inadvertent application of voltages to the protected monitoring point is under study.

4 Electrical characteristics of the transmission path interface

Note – The reference for all parameters associated with the transmission path interface shall be the relevant output interface as defined in Recommendation G.703.

4.1 *Impedance*

The transmission path interface shall have the nominal impedance as defined in Recommendation G.703 for the relevant bit rate output interface.

4.2 *Return loss*

With the transmission path interface terminated with its nominal impedance, the return loss shall comply with the requirements defined in Recommendation G.703 for the relevant bit rate output interface. This shall apply with any value of load impedance, including short and open circuits, applied to the protected monitoring point.

4.3 *Attenuation*

The attenuation in the transmission path, when the transmission path interface is terminated in its nominal impedance, shall be less than Y dB (see Figure 2/G.772) for all frequencies in the range 2.5% to 150% of the nominal bit rate, when the protected monitoring point is terminated in any load impedance, including short and open circuit.

The value of Y is for further study; 1 dB has already been proposed.

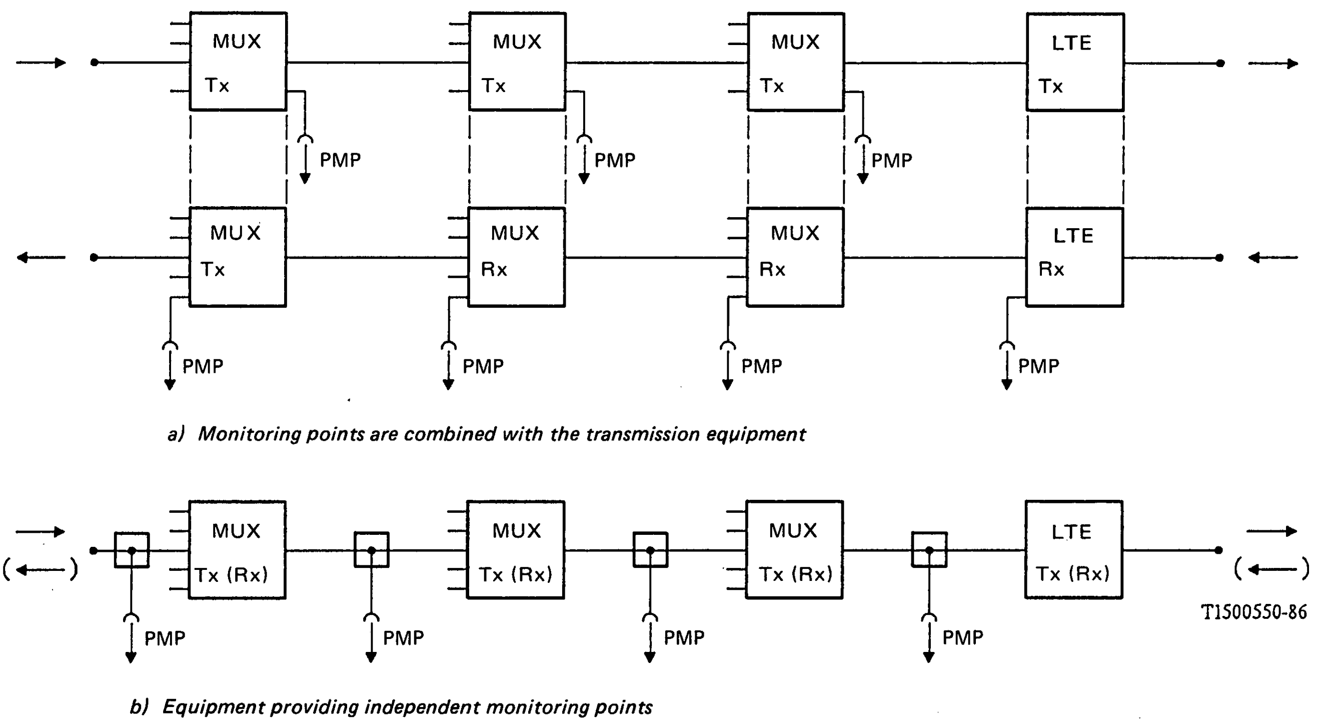
4.4 *Impact of the protected monitoring point on the maximum cable length*

The introduction of a protected monitoring point as described in Figure 1b with an attenuation of Y dB will effectively reduce the maximum attenuation allowed for in Recommendation G.703 by Y dB.

4.5 *Protection of the transmitted signal*

Under study.

The degree of protection shall be specified in terms of an X% variation in the pulse mask of the signal on the transmission path when the protected monitoring point is terminated in any impedance including short and open circuit.



Tx Transit side
Rx Receive side
PMP Protected monitoring point
MUX Multiplex equipment
LTE Line terminal equipment

FIGURE 1/G.772

Examples for the implementation of monitoring points

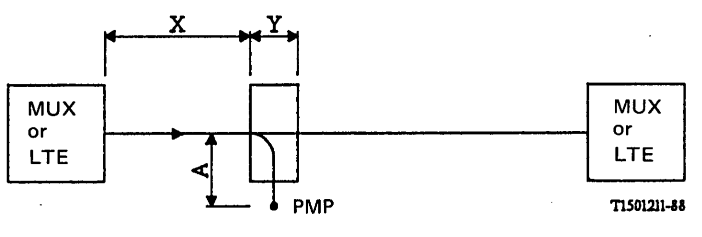


FIGURE 2/G.772

Definition of A, X and Y

References

[1] CCITT Recommendation *Maintenance terminology and definitions,* Vol. IV, Rec. M.60.

[2] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces,* Vol. III, Rec. G.703.

[3] CCITT Recommendation *Resistability of subscribers terminals to overvoltages and overcurrents,* Vol. IX, Rec. K.21.

[4] IEC Publication 801-2 *Prescriptions relatives aux décharges électrostatiques.*

7.9 Other terminal equipments

Recommendation G.791

GENERAL CONSIDERATIONS ON TRANSMULTIPLEXING EQUIPMENTS

(Geneva, 1980; further amended)

The CCITT,

considering

the advantages offered in some cases by direct through-connection (without voice-frequency interfaces) from FDM signals to TDM signals and vice versa,

recommends in such cases

(1) the use of the transmultiplexing equipment described in Definition 4020 of Recommendation G.701;

(2) Recommendation G.792 which contains the characteristics common to all transmultiplexing equipment;

(3) Recommendation G.793 which concerns 60-channel transmultiplexers providing 2048 kbit/s signals and using A-law encoding;

(4) Recommendation G.794 which concerns 24-channel transmultiplexers providing 1544 kbit/s signals and using μ-law encoding.

1 Complementary definitions

1.1 type P transmultiplexer (TMUX-P)

A transmultiplexing equipment in which the analogue interface is made up of several groups.

1.2 type S transmultiplexer (TMUX-S)

A transmultiplexing equipment in which the analogue interface is made up of one or more supergroups.

1.3 hierarchical transmultiplexer

A transmultiplexer in which the digital interfaces satisfy the provisions of Recommendations G.703 and G.704 and the analogue interfaces those of Recommendation G.233 [1].

1.4 transmultiplexer channel

A frequency band of 4000 Hz on the analogue side, corresponding to a bit rate of 64 kbit/s on the digital side, which permits the transmission of a signal limited to the telephone band 300-3400 Hz. Access may be gained to a given channel:

- either at the level of the time slot associated with the relevant channel of the TDM signal;
- or at the level of the frequency band (f_p, $f_p \pm 4000$ Hz) of the FDM signal, f_p being the virtual carrier frequency associated with the channel concerned. The + sign corresponds to the case of the base supergroup, the − sign to the case of the base group.

Note – Correspondence between out-of-band signalling on the analogue side and channel associated signalling on the digital side will be covered in the Recommendations specific to the various transmultiplexers.

2 Transmultiplexer application

The application on transmultiplexers for the interconnection of digital and analogue networks is illustrated in Supplement No. 28.

Reference

[1] CCITT Recommendation *Recommendations concerning translating equipments*, Vol. III, Rec. G.233.

Recommendation G.792

CHARACTERISTICS COMMON TO ALL TRANSMULTIPLEXING EQUIPMENTS

(Geneva, 1980; further amended)

The CCITT,

recommends

that the characteristics below be respected by all the transmultiplexing equipments defined in Recommendation G.791.

Recommendation O.133 contains information about test equipment. Account should be taken of the measurement accuracy provided by test equipment designed in accordance with that Recommendation.

The following specifications are based on ideal measuring equipment. Therefore, they do not include any margin for measurement errors.

To avoid level errors produced as a result of the use of test frequencies which are sub-multiples of the PCM sampling rate, the use of integer sub-multiples of 8 kHz should be avoided.

Where a nominal reference frequency of 1020 Hz is indicated (measurement of attenuation/frequency distortion and adjustment of relative levels), the actual frequency should be 1020, +2 to −7 Hz in accordance with Recommendation O.6 [18].

1 Coding law

Transmultiplexers should satisfy Recommendation G.711, § 3.

2 Sampling rate of PCM channels

The nominal sampling rate of PCM channels is $8000 \text{ Hz} \pm 50 \cdot 10^{-6}$ according to Recommendation G.711, § 2.

3 Amplitude limitation of PCM channels

In accordance with Recommendation G.711, § 4, the theoretical load capacity of PCM channel is +3.14 dBm0 for the A-law and +3.17 dBm0 for the μ-law.

4 Accuracy of the analogue virtual carriers

The analogue virtual carriers should satisfy the Recommendation cited in [1].

5 Saturation level at the input of the analogue group

The transmultiplexers should be able to accept at their analogue inputs, levels corresponding to the equivalent peak powers defined in Table 3/G.223 [5] (for example, +19 dBm0 for a group and +20.8 dBm0 for a supergroup).

Note – Attention is drawn to the possibility of using a transmultiplexer on the interpolated side of a digital speech interpolation (DSI) device. Given an interpolation rate of 2, this would lead to equivalent peak powers of 19.5 dBm0 for TMUX-P and 21.2 dBm0 for TMUX-S (see Table 3/G.223 [5]).

6 Methods of measuring quality in the audio band

The various possible methods of measuring quality characteristics in the audio band are indicated in Figure 1/G.792.

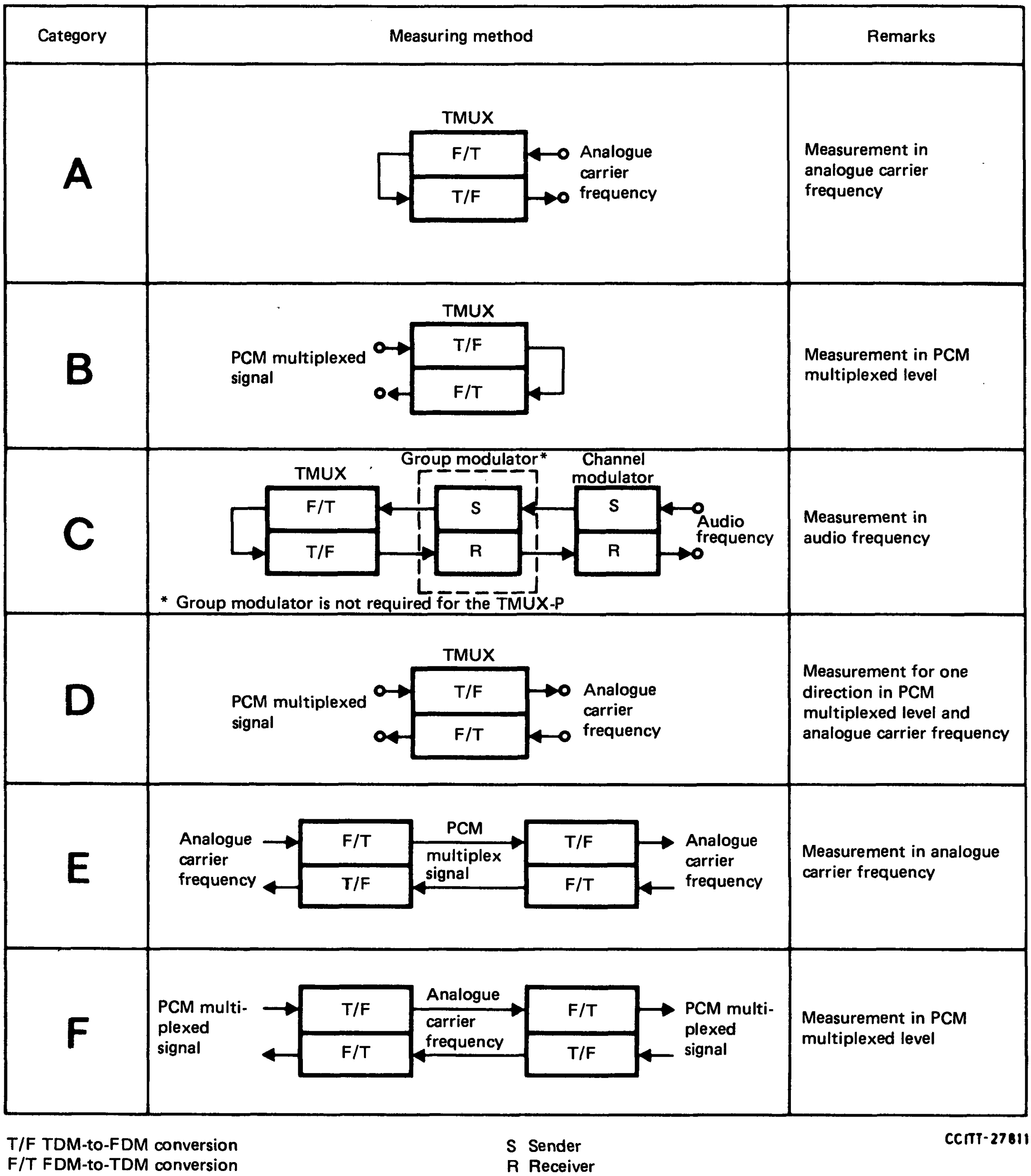


FIGURE 1/G.792

Block diagrams of measuring methods for transmultiplexers

When method B cannot be used because it requires digital signal generators and analyzers, which certain Administrations do not yet possess, method C can be used provisionally [looping of the digital ports, use of the terminals of auxiliary analogue channels (and possibly group modulators), assumption of the additivity of impairments and deduction of the impairments at the terminals of the channels (and possibly modulators) previously measured].

Method D corresponds in fact to four possible methods, depending on whether the emission of the test signal and its detection takes place on the analogue side or the digital side.

Methods E and F are used for crosstalk measurements.

For the sake of the convenience and precision of the measurements, it is desirable that the regulation, when included in the transmultiplexer, can be blocked with a gain equal to unity. The specifications in §§ 7 to 23 assume such blocking.

7 Attenuation distortion in the voice-frequency band as a function of frequency

The measuring method is method A.

The variation of the attenuation of each channel of a transmultiplexer as a function of frequency must remain within the limits of the mask in Figure 2/G.792. The level of emission is −10 dBm0; the reference frequency is 1020 Hz.

8 Group delay

8.1 *Absolute value of the group delay*

The measuring method is method A.

The absolute value of group delay defined as the minimum value of group delay in the speech band 300-3400 Hz should remain less than 3 ms for all the channels of a transmultiplexer.

Note – When the transmultiplexer is used for satellite digital communication at the earth station the minimum value of the group propagation time in the audiofrequency band may be increased from 3 ms to 6.5 ms. In all other cases, the value of 3 ms should be complied with.

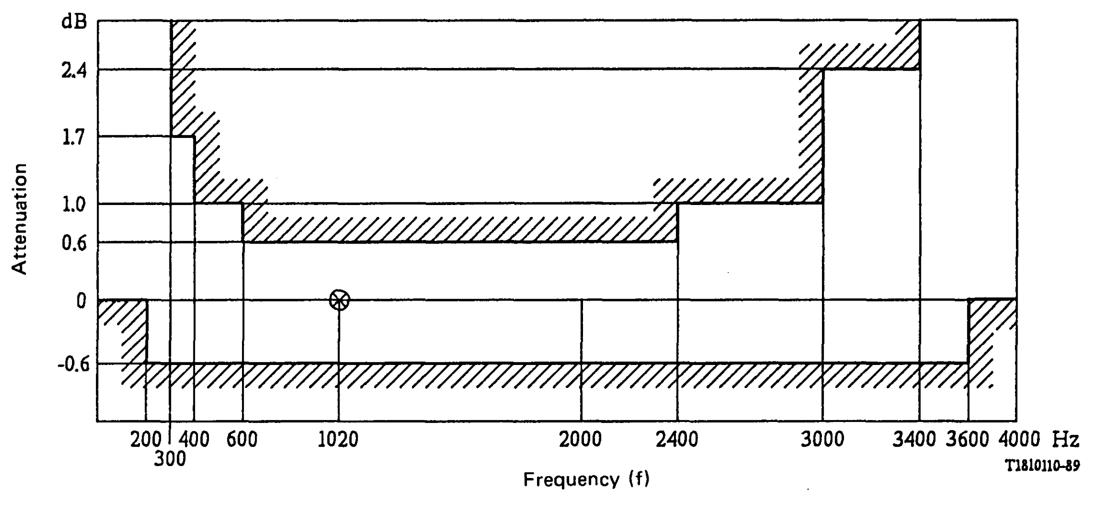


FIGURE 2/G.792

Attenuation distortion mask as a function of the frequency to be observed for all channels of a transmultiplexer

8.2 *Group-delay distortion*

The measuring method is method A.

The group-delay distortion should not exceed the limits of the mask in Figure 3/G.792.

The minimum group delay is taken as a reference; the power level at the input is 0 dBm0.

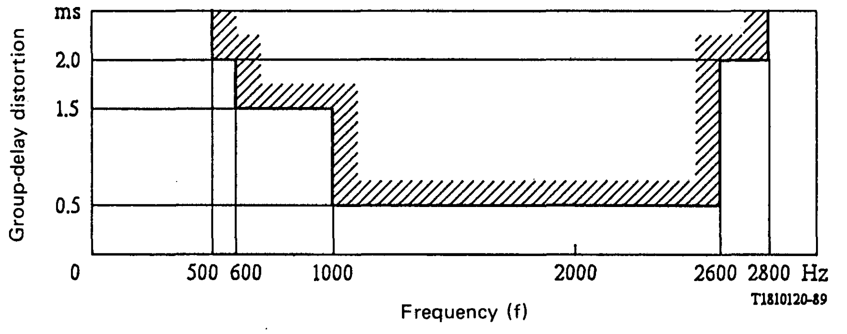


FIGURE 3/G.792

Mask of group-delay distortion as a function of frequency

9 Noise

9.1 *Idle channel noise, with all channels idle*

The measuring method is method B.

When a PCM signal corresponding to amplitude 0 for the μ-law and the number 1 for the A-law in all channels of the transmultiplexer is applied to the digital input of the transmultiplexer, the psophometric noise measured over any channel at the digital output should not exceed −65 dBm0p. The measurement is conducted in the presence of pilots.

9.2 *Channel noise, with all channels loaded except the one measured*

The measuring method is method A. In this case an intermodulation measuring set-up using the white noise method is employed, as described in the Recommendation cited in [6].

The level of emission of the noise signal being equal to the conventional load of the FDM signal considered (the Recommendation cited in [7]: 3.3 dBm0 for the group, 6.1 dBm0 for the supergroup), the noise measured in any given measuring slot should not exceed −62.5 dBm0p (i.e., −60 dBm0 in a 3100 Hz band).

The centre frequencies of the specified measuring slots (CCITT Recommendation G.230 [8] and CCIR Recommendation 482 [9]) applicable to the transmultiplexers are:

- for the base group: 70 and 98 kHz
- for the base supergroup: 394 and 534 kHz.

This measurement is carried out without emitting pilots or out-of-band signalling.

Note – Attention is drawn to the possibility of using a transmultiplexer on the interpolated side of a digital speech interpolation (DSI) device. Given an interpolation rate of 2, this would lead to conventional loads of 4.5 dBm0 for TMUX-P and 7.3 dBm0 for TMUX-S (see Table 2/G.223, [7]).

9.3 *Single frequency noise outside the band 300-3400 Hz*

The measuring method is B.

When a PCM signal corresponding to amplitude 0 for the μ-law and amplitude 1 for the A-law in all channels is applied to the digital input of the transmultiplexer, the noise over any frequency should not exceed −50 dBm0 with the exception of the frequency of 80 Hz where it should not exceed −40 dBm0.

9.4 *Idle noise in the PCM – FDM direction all channels idle*

The measuring method is method D. A PCM signal, amplitude 0 for the μ-law and 1 for the A-law is applied at the digital input of the transmultiplexer in all channels. The power of the noise measured at the analogue output in any channel must be less than −70 dBm0p.

Note – White noise is assumed, and to take account of the psophometric weighting, the measurement can be made in a band of 1740 Hz, centred on the odd multiples of 2 kHz. The measurement may be difficult in certain channels due to the presence of pilots.

10 Intermodulation

The measuring method is method A.

If two sine-wave signals of different frequencies f_1 and f_2 belonging to the band 300-3400 Hz of the channel considered, having no harmonic relation and of equivalent levels in the −4 to −21 dBm0 range, are applied simultaneously to the analogue ports of the transmultiplexer, there should be no intermodulation product of the type $2f_1 - f_2$ of a level higher than −35 dB with respect to the level of one of the two input signals.

11 Total distortion including quantizing distortion

The measuring method is method B (or provisionally method C).

If method B is used, the test signal is generated digitally and is therefore affected by theoretical quantizing distortion.

A choice between the two following methods is recommended:

Method 1

The signal-to-total distortion ratio measured according to method 1 described in § 8 of Recommendation G.712 should respect the mask of Figure 4/G.792. The mask is to be complied with by all channels of the transmultiplexer.

Method 2

With a sine-wave signal at a frequency between 700 and 1100 Hz or 350 and 550 Hz (e.g. 420 ± 20 Hz) (except for submultiples of 8 kHz) being applied in the channel concerned at the digital input of the transmultiplexer, the ratio of signal-to-total distortion power, measured with appropriate noise weighting (see the Recommendation cited in [10]), should be below the limits of the mask represented in Figure 5/G.792. The mask is to be complied with by all the channels of the transmultiplexer.

12 In-band spurious signals

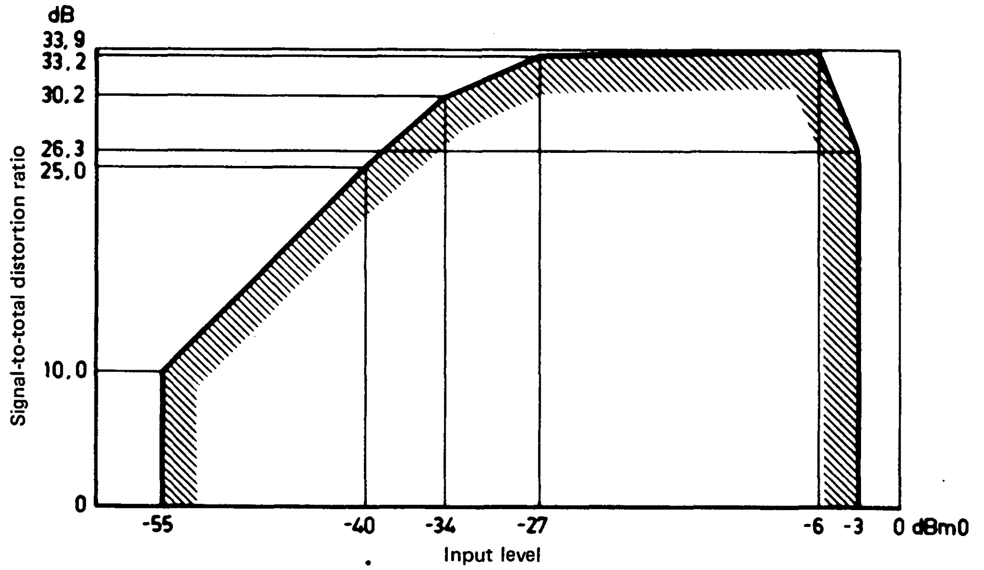
The measuring method is method A.

The transmultiplexers must meet the provisions of Recommendation G.712, § 9.

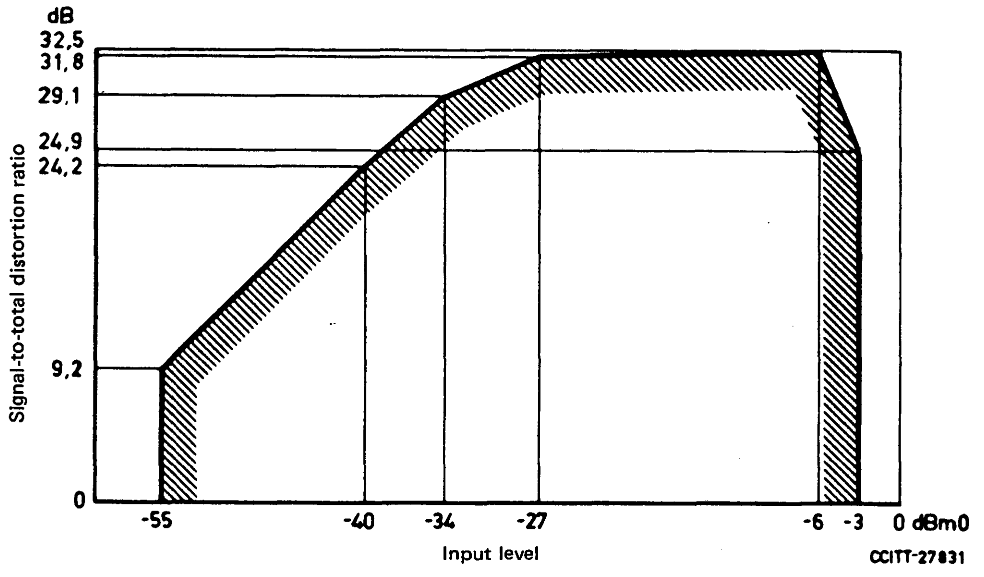
13 Variation of gain with the input level

The measuring method is method A, the pilots being present at the analogue input.

With a sine-wave signal at a frequency between 700 and 1100 Hz (except for submultiples of 8 kHz) and a level between −55 and +3 dBm0 being applied in the channel concerned at the analogue input of the transmultiplexer, the variation of gain with respect to its value for an input level of −10 dBm0 should remain between the limits of the mask shown in Figure 6/G.792. The mask is to be complied with by all channels of a transmultiplexer.



a) Method C



b) Method B

FIGURE 4/G.792

Signal-to-total distortion ratio as a function of the input level according to method 1 (Recommendation G.712, § 8)

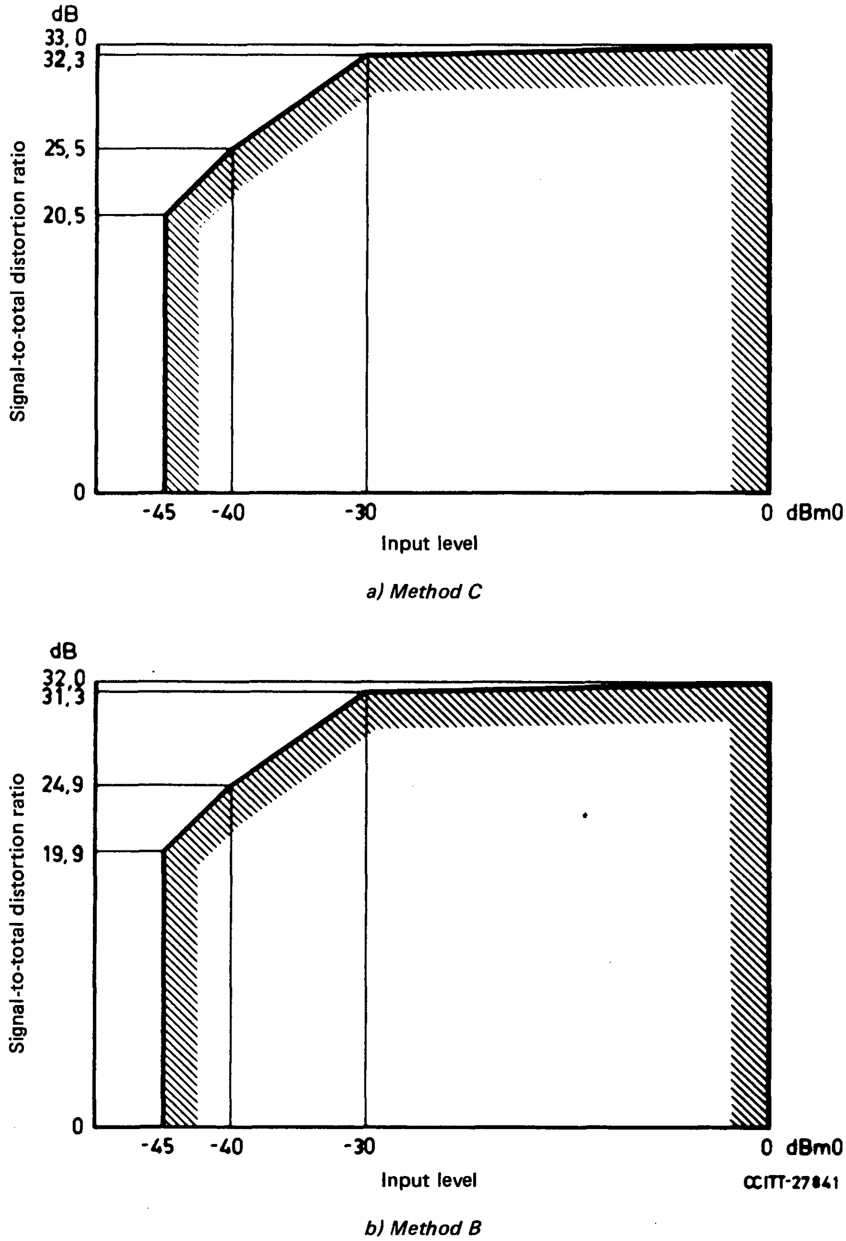


FIGURE 5/G.792

Signal-to-total distortion ratio as a function of the input level according to method 2 (Recommendation G.712, § 8)

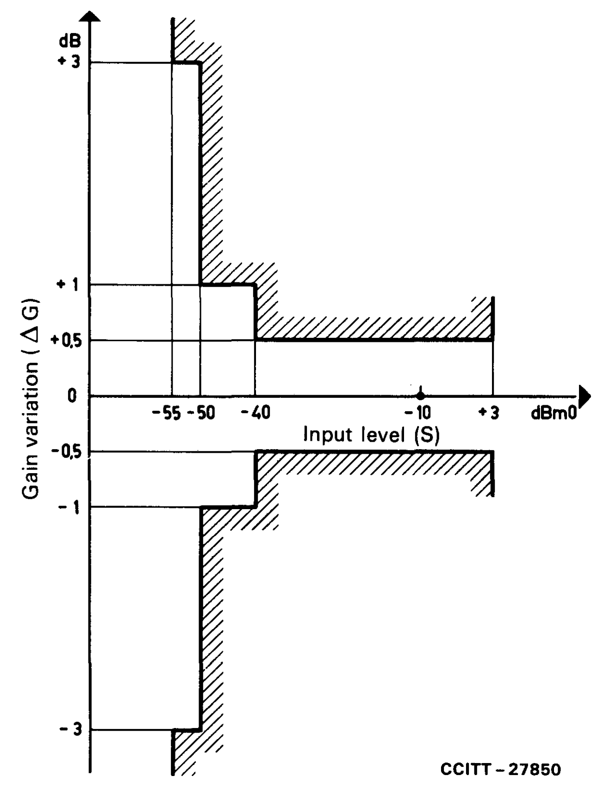


FIGURE 6/G.792

Gain variation as a function of input level S, Method 2 in Recommendation G.712, § 10 (sinusoidal test signal)

14 Crosstalk

For measuring crosstalk, two transmultiplexers must be connected back-to-back (methods E and F). There are two possible configurations and four possible measurements (see Figure 7/G.792):

- far-end crosstalk digital to digital (see Note 1)
- near-end crosstalk digital to digital (see Note 1)
- far-end crosstalk analogue to analogue
- near-end crosstalk analogue to analogue

14.1 *Intelligible crosstalk*

When a sine-wave signal between 700 and 1100 Hz and with a level of 0 dBm0 is injected in any channel on the digital or analogue side of the transmultiplexer, the crosstalk ratio between the signal channel and any other channel must be greater than 65 dB for any of the four crosstalk contributions identified above (see Note 2).

14.2 *Unintelligible crosstalk*

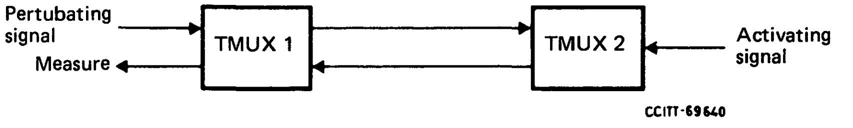
When a conventional telephone signal according to Recommendation G.227 [11], is injected in any channel on the digital or analogue side of the transmultiplexer, at a level of 0 dBm0, the level of crosstalk measured in any other channel for any of the four crosstalk contributions identified above must be below −60 dBm0p (see Note 3).

Note 1 – In this configuration, the two transmultiplexers are connected at the level of the analogue FDM signal and there will generally be a problem of level adaptation between the send and the receive sides. This can be solved with the use of attenuators or amplifiers of appropriate gain. Attention must be given on the risk of introduction of additional crosstalk in these complementary devices. It should be desirable to include the level adaptation facilities in the transmultiplexer itself.

Note 2 – In order to overcome fundamental gain enhancement effects associated with PCM encoders, which can mask the true crosstalk, measuring methods using activating signals based on those defined in Recommendation G.712 can be used.

Note 3 – Recognizing the difficulty of generating conventional telephone signals according to Recommendation G.227 in a suitable format for insertion into either the analogue or digital input to the transmultiplexer, it shall be adequate to demonstrate, via suitable single frequency crosstalk tests, that the intent of the above specification is met, without actually using a conventional telephone signal.

a) Far-end crosstalk measurement



b) Near-end crosstalk measurement

FIGURE 7/G.792

Measurements of crosstalk with methods E and F

15 Go-to-return crosstalk

For measuring go-to-return crosstalk, two transmultiplexers must be connected back-to-back (methods E and F). There are two possible configurations and two possible measurements (see Figure 7b/G.792):

– near-end crosstalk digital to digital (see Note 1 of § 14);

– near-end crosstalk analogue to analogue.

When a sine-wave signal between 300 and 3400 Hz and with a level of 0 dBm0 is injected in any channel on the digital or analogue side of the transmultiplexer, the crosstalk ratio between the signal channel and the associated return channel must be greater than 58 dB for each contribution identified above.

When using method F, a PCM signal corresponding to amplitude 0 for the μ-law and amplitude 1 for the A-law, should be inserted into the digital input of all return channels.

Note – Concerning the activating signal for method F, see Recommendation G.712, § 10.

16 Variation of the equivalent of the channels within the FDM assembly

Measuring method A.

When a test tone at the equivalent of 1020 Hz in any channel, and with a level of −10 dBm0 is applied to the analogue input of the transmultiplexer, the level measured at the analogue output of the transmultiplexer shall be within a tolerance of ± 1 dB of the level measured when that test tone is applied at the equivalent of 1020 Hz in the channel containing the reference pilot of the FDM assembly considered.

17 Adjustment of the relation between the coding law and the analogue level

Measuring method D.

To measure the correspondence between the coding laws and the analogue levels, the sequence of character signals from Table 5/G.711 for the A-law and from Table 6/G.711 for the μ-law may be applied periodically at the digital input of the transmultiplexer: the signal at the analogue output of the transmultiplexer should correspond to a sine-wave signal of frequency 1 kHz in the corresponding channel at a level between −0.5 and +0.5 dBm0.

Note – The use of another digital periodic sequence representing a nominal reference frequency of 1020 Hz at a nominal level of 0 dBmO is acceptable, provided that the theoretical level accuracy is better than ± 0.03 dB.

To check the load capacity of the PCM coder contained in the transmultiplexer, a sine-wave signal at a nominal frequency of 1020 Hz can be applied for any channel at the analogue input of the transmultiplexer. Initially the level of this signal is considerably below the load capacity, then it is raised gradually. Note is taken of the input level at which the character signal corresponding to the extreme quantization interval for positive and negative amplitudes first appears at the digital output in the channel considered. The load capacity is then taken to be equal to this input level, increased by 0.3 dB. The values obtained for the various channels should be between 2.64 and 3.64 dBm0 for the A-law and between 2.67 and 3.67 dBm0 for the μ-law.

18 Carrier leak at the analogue ports

Measuring method A, the analogue input of the transmultiplexer being looped to its nominal impedance.

The transmultiplexers should meet the provisions of the Recommendation cited in [12].

19 Protection against out-of-band signals at the analogue ports

19.1 *Out-of-band spurious signals at the analogue output*

The measuring method is C for the TMUX-P, range a) (see below), otherwise A. The test signal has a level of 0 dBm0. For the TMUX-P, range a), a signal according to Recommendation G.227 is used, otherwise a sine-wave signal (300 to 3400 Hz). The level of supurious signals outside the group or supergroup band (f_1 to f_2) at the analogue output should not exceed the following limits:

TMUX-P	a)	$f_1 > f_x > (f_1 - 4\text{ kHz})$ and $f_2 < f_x < (f_2 + 4\text{ kHz})$	$\leqslant -60$ dBm0p (Note 1)
	b)	$(f_1 - 4\text{ kHz}) > f_x > (f_1 - 12\text{ kHz})$ and $(f_2 + 4\text{ kHz}) < f_x < (f_2 + 12\text{ kHz})$	$\leqslant -70$ dBm0 (Note 2)
	c)	$f_x \leqslant (f_1 - 12\text{ kHz})$ and $f_x \geqslant (f_2 + 12\text{ kHz})$	$\leqslant -80$ dBm0
TMUX-S	a)	$f_x = f_1 - 4\text{ kHz}$ and $f_x = f_2 + 4\text{ kHz}$	$\leqslant -60$ dBm0 (Note 3)
	b)	$(f_1 - 8\text{ kHz}) > f_x > (f_1 - 20\text{ kHz})$ and $(f_2 + 8\text{ kHz}) < f_x < (f_2 + 20\text{ kHz})$	$\leqslant -70$ dBm0 (Note 2)
	c)	$f_x \leqslant (f_1 - 20\text{ kHz})$ and $f_x \geqslant (f_2 + 20\text{ kHz})$	$\leqslant -80$ dBm0

Note 1 – Telephony channels, pilots or additional test frequencies are possible in this frequency range.

Note 2 – Adjacent carrier-frequency sound-programme channels may begin in this range (with reduced requirements).

Note 3 – This range may contain pilots or additional measuring frequencies.

19.2 *Crosstalk due to out-of-band signals at the analogue input*

Measuring methods C and A, respectively (see § 19.1). With test signals as in § 19.1 in a channel of an adjacent FDM assembly, the level at the transmultiplexer output should not exceed the following limits:

TMUX-P	a)	$f_1 > f_x > (f_1 - 4\text{ kHz})$ and $f_2 < f_x < (f_2 + 4\text{ kHz})$	$\leqslant -60$ dBm0p (Note)
	b)	$f_x < (f_1 - 4\text{ kHz})$ and $f_x > (f_2 + 4\text{ kHz})$	$\leqslant -70$ dBm0 (Note)
TMUX-S	a)	$f_x = f_1 - 4\text{ kHz}$ and $f_x = f_2 + 4\text{ kHz}$	$\leqslant -50$ dBm0 (Note)
	b)	$f_x < (f_1 - 8\text{ kHz})$ and $f_x > (f_2 + 8\text{ kHz})$	$\leqslant -70$ dBm0 (Note)

Note – For this measurement, a low-level auxiliary signal is injected into the disturbed channel. The appropriate auxiliary signal is a sine-wave signal between −33 and −40 dBm0. The frequency and characteristics of the filter in the measuring equipment must be carefully selected to ensure that the auxiliary signal does not appreciably reduce the accuracy of the crosstalk measurement.

20 Protection and suppression of pilots

Measuring method D.

The transmultiplexers should meet the provisions of the Recommendation cited in [14].

21 Protection and suppression of out-of-band signalling

21.1 *Protection of the out-of-band signalling channel for transmultiplexers using signalling system R2*

Measuring method D.

When a transmultiplexer is capable of emitting out-of-band signalling waves at frequency 3825 Hz, it should meet the provisions of Recommendation Q.414 [15], Figure 6/Q.414 being replaced by Figure 7/G.792. The measuring method associated with the latter figure is recalled in Note 1.

Note 1 – The signalling channel must be protected at the sending end against disturbance from the associated and the adjacent channel.

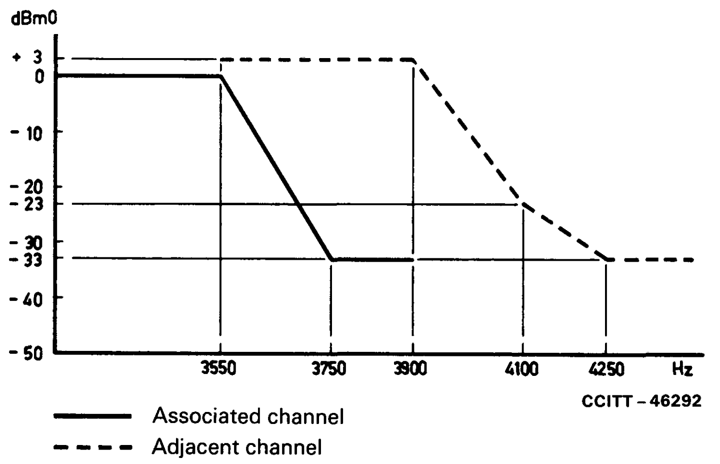
When a sine-wave at 0 dBm0 level is applied to the digital input of the associated channel, the level measured at the analogue output of the transmultiplexer must not exceed the levels shown in Figure 8/G.792.

When a sine-wave of frequency f is applied to the digital input of the adjacent channel, it produces two signals that appear on the frequency scale of Figure 8/G.792 as having the frequencies $(4000 + f)$ and $(4000 - f)$. The level of the $(4000 + f)$ signal measured at the analogue output of the transmultiplexer shall not be higher than −33 dBm0, when the sine-wave with frequency f is applied to the digital input of the adjacent channel at a level shown in Figure 8/G.792 for the frequency of $(4000 + f)$. The level of the $(4000 - f)$ signal, measured at the analogue output of the transmultiplexer, shall not be higher than −33 dBm0, when the sine-wave with frequency f is applied to the digital input of the adjacent channel at any level below the value shown in Figure 8/G.792 for the frequency $(4000 - f)$.

21.2 *Disturbance of telephone channels by out-of-band signalling frequency for transmultiplexers using signalling system R2*

The measuring method is method B or D.

Interference at 175 Hz and 3825 Hz should not exceed −53 dBm0 respectively −63 dBm0 when a continuous tone of 3825 Hz with a nominal level of −20 dBm0 is applied to all channels. These values correspond to a contribution to the channel noise in the order of −73 dBm0p (design objective).



Note – The frequency of the virtual carrier of the associated speech channel is the origin of the frequency scale (zero frequency).

FIGURE 8/G.792

Protection of the signalling channel at the sending end

21.3 *Other out-of-band signalling systems*

See Annex A.

22 Mutual interference between pilots and out-of-band signalling

The transmultiplexers capable of emitting and receiving out-of-band signalling should meet the provisions of the Recommendation cited in [17].

23 Short- and long-term variation of loss with time

The measuring method is A. When a sine-wave signal at level −10 dBm0 and at a nominal frequency of 1020 Hz is applied at the analogue input of the transmultiplexer, the level measured at the analogue output should not vary by more than ± 0.2 dB during 10 consecutive minutes of normal operation, more than ± 0.5 dB during 3 consecutive days nor by more than ± 1 dB for one year, allowing for the authorized variations of power supply, voltages and temperature.

ANNEX A

(to Recommendation G.792)

Out-of-band signalling systems using a burst-mode method

The possibility of such systems is mentioned in Annex A to Recommendation Q.21 and Annex B to Recommendation G.232. These annexes should be taken into consideration. When a transmultiplexer is capable of converting such systems, the following applies:

- Signalling frequency at the sending point: 3825 Hz ± 4 Hz.
- Send level of the signalling frequency: −5 dBm0 ± 1 dB.
- Protection of the out-of-band signalling channel: see Figure 8/G.792.
- Disturbance of telephone channels by the out-of-band signalling frequency: the measuring method is method B.
- Channel noise should not exceed −63 dBm0p in the call channel (continuous tone).
- In the adjacent channel (the closest to the signalling frequency) likewise −63 dBm0p burst or continuous tone.
- In every other channel −76 dBm0p burst or continuous tone.

Note 1 – Burst tones do not occur in the call channel after call set-up has taken place.

Note 2 – Burst rates are in the order of 10 to 25 Hz.

Note 3 – Charge metering pulses are of long duration, e.g. 150/450 ms and are evaluated as a continuous tone.

References

[1] CCITT Recommendation *Recommendations relating to the accuracy of carrier frequencies,* Vol. III, Rec. G.225, § 1.

[2] CCITT Recommendation *Pilots on groups, supergroups, etc.,* Vol. III, Rec. G.241, § 1.

[3] *Ibid.,* § 2.

[4] *Ibid.,* § 3.

[5] CCITT Recommendation *Assumptions for the calculation of noise on hypothetical reference circuits for telephony,* Vol. III, Rec. G.223, Table 3/G.223, § 6.

[6] CCITT Recommendation *Measurement of circuit noise in cable systems using a uniform-spectrum random noise loading,* Vol. III, Rec. G.228, §§ A.1, A.2.2.

[7] CCITT Recommendation *Assumptions for the calculation of noise on hypothetical reference circuits for telephony,* Vol. III, Rec. G.223, § 2.1.

[8] CCITT Recommendation *Measuring method and through-connection filters for noise produced by modulating equipment,* Vol. III, Rec. G.230.

[9] CCIR Recommendation *Measurement of performance by means of a signal of a uniform spectrum for systems using frequency-division multiplex telephony in the fixed satellite service,* Vol. IV, Rec. 482, ITU, Geneva, 1978.

[10] CCITT Recommendation *Assumptions for the calculation of noise on hypothetical reference circuits for telephony,* Vol. III, Rec. G.223, § 7.

[11] CCITT Recommendation *Conventional telephone signal,* Vol. III, Rec. G.227.

[12] CCITT Recommendation *12-channel terminal equipments,* Vol. III, Rec. G.232, §§ 5.1, 5.2.

[13] CCITT Recommendation *Through-connection of groups, supergroups, etc.,* Vol. III, Rec. G.242, § 1.

[14] CCITT Recommendation *12-channel terminal equipments,* Vol. III, Rec. G.232, §§ 12.1, 12.2 and Annex A.

[15] CCITT Recommendation *Signal sender,* Vol. VI, Rec. Q.414, Figure 6/Q.414.

[16] CCITT Recommendation *12-channel terminal equipments,* Vol. III, Rec. G.232.

[17] *Ibid.,* § 12.3 and Annex B.

[18] CCITT Recommendation *1020 Hz reference test frequency,* Vol. IV, Rec. O.6.

Recommendation G.793

CHARACTERISTICS OF 60-CHANNEL TRANSMULTIPLEXING EQUIPMENTS

(Geneva, 1980; further amended)

1 Introduction

The 60-channel transmultiplexer is a transmultiplexing equipment which satisfies Recommendations G.791 and G.792 and provides interconnection between two digital signals at 2048 kbit/s and an analogue supergroup (60-channel TMUX-S).

2 Digital interfaces

2.1 *Coding law*

The coding law used is A-law specified in Recommendation G.711.

2.2 *Interfaces*

The 2048-kbit/s interfaces satisfy Recommendation G.703, § 6.

2.3 *Frame structure*

The structure is specified in Recommendation G.704, § 3.3.1.

The strategy and the criteria for loss and recovery of frame alignment satisfy Recommendation G.706, § 4.1.

2.4 *Multiframe structure*

The multiframe structure of time slot 16 satisfies Recommendation G.704, § 3.3.3.

The strategy and the criteria for loss and recovery of multiframe alignment satisfy Recommendation G.732, § 5.2.

3 Analogue interfaces

3.1 *Ports*

The analogue interface consists of a 60-channel supergroup (band 312-552 kHz) which satisfies Recommendation G.233 [1].

The preferred signal levels at the supergroup distribution frame should be:

- for sending −36 dBr
- for receiving −30 dBr

The impedances are: 75 ohms (unbalanced).

3.2 *Pilots*

The 60-channel transmultiplexer should transmit the following pilots:

TMUX-S: A supergroup pilot with a frequency 411 920 Hz and a level of −20 dBm0,
one pilot per group with a level of −20 dBm0 and frequencies of:

Group 1: 335 920 Hz

Group 2: 383 920 Hz

Group 3: 431 920 Hz

Group 4: 479 920 Hz

Group 5: 527 920 Hz

The transfer of pilot alarms individually for each group in a supergroup and the consequence for the split channels of group 3 can be seen in Figure 1 of Supplement No. 32.

Other sets of pilots as recommended in Recommendation G.241 can be used. Special attention should be given to the compatibility of the set of pilots adopted with the out-of-band signalling system using a frequency at 3825 Hz.

The characteristics relating to the generation and transmission of these pilots are given in Recommendation G.241 [2].

3.3 *Pilot detection and regulation*

The transmultiplexer may or may not regulate levels on the basis of the levels of the group and supergroup pilots. If so, the transmultiplexer must meet the conditions of the Recommendation cited in [2]. Detection of the levels of the group pilots and or supergroup mentioned in § 3.2 should, however, be effected to ensure operation of the interruption control system (Recommendation Q.416 [3]), when R2 signalling is used.

4 Correspondence between analogue and digital channels

A fixed correspondence is established between the analogue and digital channels. The correspondence shown in Table 1/G.793 (which facilitates the transfer of alarms and results in a natural order of the channels on the analogue side) is recommended.

TABLE 1/G.793

PCM 1 channels 1 to 12	Group 1 312-360 kHz
PCM 1 channels 13 to 24	Group 2 360-408 kHz
PCM 1 channels 25 to 30	Group 3 408-432 kHz
PCM 2 channels 1 to 6	Group 3 432-456 kHz
PCM 2 channels 7 to 18	Group 4 456-504 kHz
PCM 2 channels 19 to 30	Group 5 504-552 kHz

Note – In national networks or by agreement between Administrations, other schemes of correspondence between analogue and digital channels may be used.

5 Plesiochronous operation of incoming PCM streams

Sixty-channel transmultiplexers should be able to accept two mutually plesiochronous incoming PCM streams within the limits laid down in Recommendation G.703 (bit rate 2048 kbit/s, $\pm 50 \cdot 10^{-6}$).

In the case of transmultiplexers with digital filtering, this means that the two input ports at 2048 kbit/s are fitted with frame aligners (jump or repetition of samples) and multiframe aligners for synchronizing the incoming PCM streams with the transmultiplexer clock. In order to avoid a major slip frequency, the two incoming PCM streams should be either synchronous with the transmultiplexer or plesiochronous with each other and with the transmultiplexer clock, so that Recommendation G.811 on the plesiochronous network is satisfied.

6 Synchronization of transmultiplexer

The transmultiplexer must produce virtual analogue carrier frequencies with the accuracy specified in Recommendation G.225 [4] ($\pm 10^{-7}$).

For this purpose, it is recommended:

a) either that the transmultiplexer should have an internal clock of sufficient accuracy;

b) or that the transmultiplexer should be synchronizable with an external signal which may be:

   1) a frequency (see Note 3) produced by a central FDM generator: 4, 12 or 124 kHz;

   2) or one of the incoming PCM streams which has sufficient accuracy (this may be the case, for example, when this PCM stream at 2048 kbit/s is produced by a TDM switching equipment). If both 2048-kbit/s streams are of sufficient accuracy, the use of PCM stream No. 1 is preferred. In most cases this avoids, at the digital filtering transmultiplexer input, the slipping phenomena which, when too frequent, cause high error rates on in-band data signals.

Note 1 – In the case of a digital filtering transmultiplexer, when synchronization on one of the incoming PCM streams is not possible, the remote digital terminal should have the sending side synchronized with the receiving side so as to avoid slipping at the transmultiplexer input.

Note 2 – In the case of external synchronization, transmultiplexers often have an internal oscillator locked to the external signal. If, upon loss of the external sync signal, this internal oscillator is allowed to continue to supply the clock for the outgoing digital signal (now in the free-running mode), then this oscillator should have a minimum free-running accuracy of 50×10^{-6}. This is intended to allow the distant end digital terminal to receive an adequate frequency for alarm purposes only, so as not to confuse maintenance and trouble-shooting activities. Also, a local alarm should be given in the event of a fault in the synchronization system or in the absence of the external synchronization signal (Tables 2/G.793, 3/G.793 and 2 of Supplement No. 32).

Note 3 – In the case where the transmultiplexer is to be used in a TDMA satellite application, the effect of the satellite Doppler frequency variation must be taken into account. This can be done in two ways:

- either, the TDMA terminal incorporates the Doppler buffer memories of appropriate capacity in the earth station to satellite direction. In this case, the two directions of the TMUX must be synchronized from one of the two 2048 kbit/s PCM streams transmitted by the TDMA receive terminal;
- or, the TDMA terminal does not incorporate Doppler buffers. In this case, the PCM to FDM direction of the TMUX may be synchronized from one of the two 2048 kbit/s streams transmitted by the TDMA receive terminal. In the FDM to PCM direction, the 2048 kbit/s streams transmitted by the TMUX must be made synchronous with the TDMA system transmit clock: this supposes that a synchronization signal (contradirectional with the data) is provided by the TDMA transmit terminal to the TMUX. In the case where the processing in a digital filtering transmultiplexer is made synchronously for the two directions, Doppler buffer memories of appropriate capacity must be incorporated in the PCM interfaces.

7 Signalling

Different kinds of signalling systems can be envisaged.

7.1 *In-band signalling*

The 60-channel transmultiplexer is transparent for channel-associated in-band signalling.

7.2 *Common channel signalling*

In the case when common channel signalling must be routed through the transmultiplexer, attention is drawn to the fact that the transmission capabilities of a channel in the transmultiplexer is limited to the band 300-3400 Hz (i.e. data rates corresponding to this frequency band). Information on signalling bit rates is given in § 2 of Recommendation Q.702.

In the opposite case, when common channel signalling is not routed through the TMUX, no special problems are recognized.

7.3 *Out-of-band signalling*

As regards Signalling System R2, signalling conversion between the analogue and digital versions of line signalling as recommended in Recommendation Q.430 is to be used in the case of international interconnection and should conform to the following specifications.

The transmultiplexer, or an additional equipment associated with it, converts the analogue version to the 2-bit digital version of the R2 line Signalling System, and vice versa. In all cases, the transmultiplexer should provide the following facilities for signalling:

a) *Analogue side*

1) recognition of the signalling frequency at 3825 Hz in accordance with Recommendation Q.415 [5];
2) transmission of the signalling frequency at 3825 Hz in accordance with Recommendation Q.414 [6];
3) supervision of group pilots (and supergroup pilots if necessary) in accordance with Recommendation Q.416 [3].

b) *Digital side*

1) extraction of signalling bits *a* and *b* of time slots 16 received in accordance with the Recommendation cited in [7];

2) insertion of appropriate signalling data in bits *a* and *b* of time slots 16 transmitted in accordance with the Recommendation cited in [7];

3) detection of PCM system faults.

The conversion between the analogue and digital versions of the R2 line Signalling System should be made in accordance with [8]. When the conversion is made in an external equipment, the transmultiplexer should supply the necessary ports.

For national networks, a method of using the analogue line signalling version on both analogue and digital transmission systems is described in Supplement No. 32.

8 Fault conditions and consequent action

8.1 *Principles of the action to be taken*

The principles governing the handling of alarms is as follows: The behaviour of a transmultiplexer vis-à-vis a 30-channel PCM multiplex should be the same as that of another 30-channel PCM multiplex. However, the transmultiplexer performs certain functions peculiar to digital multiplexing equipments such as the transmission of the Alarm Indication Signal (AIS). Vis-à-vis a group modulator, it should behave like another group modulator.

The principles of alarm transfer are described in Supplement No. 32 which also contains particular solution used in national networks.

8.2 *Digital version of R2 signalling system*

Table 2/G.793 summarizes the fault conditions and the consequent actions.

8.3 *In-band signalling and common channel signalling*

Table 3/G.793 summarizes the fault conditions and the consequent actions (see Note).

Note – The problem of per channel alarm transfer needs further study. For applications where the TMUX is used in TDMA configuration, Recommendation Q.33 should be considered [11].

TABLE 2/G.793

Fault conditions and consequent actions, applicable if Signalling System R2 is used (see Note 1)

	Fault conditions	Consequent actions						
		Prompt maintenance alarm indication generated	Alarm indication transmitted to the remote end		Blocking of faulty speech channels	Information to be taken into account in conversion	Transmission of alarms	
			Bit 3 0 to 1 (see Note 2)	Bit 6 time slot 16, frame 0 to 1 (see Note 2)			Pilot cut-out	AIS sent (see Note 2)
PCM alarms	Loss of signal Error ratio > 10^{-3} Loss of frame alignment (see Note 2)	Yes (see Note 3)	Yes		Yes PCM ⟶ FDM	a=b=1	(see Note 4)	
PCM alarms	Loss of multiframe alignment (see Note 2)	Yes (see Note 3)		Yes		a=b=1	(see Note 4)	
PCM alarms	Reception of bit 3, time slot 0 or bit 6, time slot 16, frame 0 (see Note 2)					a=b=1		
FDM alarms	Absence of the received group pilot (see Note 5)	Yes			Yes FDM ⟶ PCM	Absence of pilot		Yes (see Note 6)
FDM alarms	Absence of the received supergroup pilot (see Note 7)	Yes				Absence of pilot		
FDM alarms	Pilot level deviation alarm (Note 8)	Yes						
System alarms	Failure of power supply	Yes					Yes, if possible	Yes, if possible
System alarms	System failure (see Note 9)	Yes					Yes	Yes (see Note 6)
System alarms	Synchronization failure (see Note 10)	Yes						

Note 1 – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault conditions. An open space in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 2 – The fault conditions "Loss of signal at 2 Mbit/s", "Error ratio > 10^{-3}", "Loss of frame alignment", "Loss of multiframe alignment", "Reception of bit 3, time slot 0", "Reception of bit 6, time slot 16, frame 0" and the consequent action "Bit 3, time slot 0 to 1", "Bit 6, time slot 16, frame 0 to 1", "Bit 6, time slot 16, frame 0 to 1" and "AIS sent" are defined in Recommendation G.732.

Note 3 – The 60-channel transmultiplexer should be able to detect the alarm indication signal (AIS) on incoming streams at 2048 kbit/s. When AIS is detected, the prompt maintenance indication associated with the loss of frame alignment, with an excessive error rate or with the loss of multiframe alignment should be blocked.

Note 4 – This action is not necessary when the digital version of Signalling System R2 is used, but may be useful with other applications.

Note 5 – The definition of absence of group pilot used for the operation of the interruption control system is given in the Recommendation cited in [9]. The supergroup pilot can also be used.

Note 6 – The AIS is sent only if the 30 channels of a single PCM stream are in the alarm condition.

Note 7 – Detection of "absence of supergroup pilot" is not obligatory. If the supergroup pilot is not sent, this alarm function can be performed by supervision of the 5 group pilots.

Note 8 – The concept of pilot level deviation alarm corresponds to a variation on the level of the pilot from its nominal value by more than ± 4 dB, as stated in [10]. This applies only to transmultiplexers with automatic internal level regulation.

Note 9 – The "system" fault condition corresponds to a fault on the transmultiplexer detected by the transmultiplexer's supervision system, when it has one.

Note 10 – The "synchronization" fault is that mentionned in § 6 of Recommendation G.793. When the transmultiplexer is synchronized with an external signal or with one of two incoming PCM streams at 2048 kbit/s, the transmultiplexer should transmit an alarm signal in the event of synchronization loss.

TABLE 3/G.793

Fault conditions and consequent actions, applicable for in-band signalling and common channel signalling (Note 1)

Fault conditions		Consequent actions				
		Prompt maintenance alarm indication generated	Alarm indication transmitted to the remote end	Blocking of faulty speech channels	Transmission of alarms	
			Bit 3, time slot 0 to 1 (see Note 2)		Pilot cut-out	AIS sent (see Note 2)
PCM alarms	Loss of signal Error ratio > 10^{-3} Loss of frame alignment (see Note 2)	Yes (see Note 3)	Yes	Yes PCM → FDM	Yes (see Note 4)	
IDM alarms	Absence of the received group pilot (see Note 5)	Yes		Yes FDM → PCM		Yes (see Note 6)
IDM alarms	Absence of the received supergroup pilot (see Note 7)	Yes				
IDM alarms	Pilot level deviation alarm (see Note 8)	Yes				
System alarms	Failure of power supply	Yes			Yes, if possible	Yes, if possible
System alarms	System failure (see Note 9)	Yes			Yes, 5 groups	Yes (see Note 7)
System alarms	Synchronization failure (see Note 10)	Yes				

Note 1 – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault conditions. An open space in the table signifies that the relevant action should not be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 2 – The fault conditions "Loss of signal at 2 Mbit/s", "Error ratio > 10^{-3}", "Loss of frame alignment", and the consequent action "Bit 3, time slot 0 to 1", and "AIS sent" are defined in Recommendation G.732.

Note 3 – The 60-channel transmultiplexer should be able to detect the alarm indication signal (AIS) on incoming streams at 2048 kbit/s. When AIS is detected, the prompt maintenance indication associated with the loss of frame alignment, with an excessive error rate should be blocked.

Note 4 – In the PCM → FDM direction, the pilots must be cut for the 3 groups associated with a PCM multiplex signal in the event of the detection of a fault on the PCM multiplex signal stream. When a single PCM multiplex signal is faulty, this involves the blocking of 6 channels which are not faulty.

Note 5 – The definition of absence of group pilot used for the operation of the interruption control system is given in the Recommendation cited in [9]. The supergroup pilot can also be used.

Note 6 – The AIS is sent only if the 30 channels of a single PCM stream are in the alarm condition.

Note 7 – Detection of "absence of supergroup pilot" is not obligatory. If the supergroup pilot is not sent, this alarm function can be performed by supervision of the 5 group pilots.

Note 8 – The concept of pilot level deviation alarm corresponds to a variation on the level of the pilot from its nominal value by more than ± 4 dB as stated in the Recommendation cited in [10]. This applies only to transmultiplexers with automatic internal level regulation.

Note 9 – The "system" fault condition corresponds to a fault on the transmultiplexer detected by the transmultiplexer's supervision system, when it has one.

Note 10 – The "synchronization" fault is that mentionned in § 6 of the Recommendation G.793. When the transmultiplexer is synchronized with an external signal or with one of the two incoming PCM streams at 2048 kbit/s, the transmultiplexer should transmit an alarm signal in the event of synchronization loss.

References

[1] CCITT Recommendation *Recommendations concerning translating equipments*, Vol. III, Rec. G.233.

[2] CCITT Recommendation *Pilots on groups, supergroups, etc.*, Vol. III, Rec. G.241.

[3] CCITT Recommendation *Interruption control*, Vol. VI, Rec. Q.416.

[4] CCITT Recommendation *Recommendations relating to the accuracy of carrier frequencies*, Vol. III, Rec. G.225.

[5] CCITT Recommendation *Signal receiver*, Vol. VI, Rec. Q.415.

[6] CCITT Recommendation *Signal sender*, Vol. VI, Rec. Q.414.

[7] CCITT Recommendation *Digital line signalling code*, Vol. VI, Rec. Q.421, § 3.1.2.

[8] CCITT Recommendation *Conversion between analogue and digital versions of system R2 line signalling*, Vol. VI, Rec. Q.430.

[9] CCITT Recommendation *Interruption control*, Vol. VI, Rec. Q.416, §§ 2.4.3.2 and 2.4.3.3.

[10] CCITT Recommendation *Pilots on groups, supergroups, etc.*, Vol. III, Rec. G.241, § 1.

[11] CCITT Recommendation *Protection against the effect of faulty transmission on groups of circuits*, Vol. VI, Rec. Q.33.

Recommendation G.794

CHARACTERISTICS OF 24-CHANNEL TRANSMULTIPLEXING EQUIPMENTS

(Malaga-Torremolinos, 1984, amended at Melbourne, 1988)

1 Introduction

The 24-channel transmultiplexer is a transmultiplexing equipment which satisfies Recommendations G.791 and G.792 and provides interconnection between a digital signal at 1544 kbit/s and two analogue basic groups (24-channel TMUX-P).

2 Digital interfaces

2.1 *Coding law*

The coding law used is μ-law specified in Recommendation G.711.

2.2 *Interfaces*

The 1544 kbit/s interfaces satisfy Recommendation G.703, § 2.

2.3 *Frame structure*

The 1544 kbit/s frame structure satisfies Recommendation G.704, § 3.1.1.

2.4 *Multiframe structure*

The multiframe structure carried on the F-bit satisfies Recommendation G.704, § 3.1.1.

3 Analogue interfaces

3.1 *Ports*

The analogue interface consists of two 12-channel groups (band 60-108 kHz) which satisfies Recommendation G.232.

The preferred signal levels at the group distribution frame satisfy Recommendation G.233.

3.2 *Pilots*

The 24-channel transmultiplexer should transmit and receive the group pilot in Recommendation G.241.

3.3 *Pilot detection and regulation*

The transmultiplexer may or may not regulate levels on the basis of the levels of the group pilots. If so, the transmultiplexer must meet the conditions of Recommendation G.241.

4 Correspondence between analogue and digital channels

A fixed correspondence is established between the analogue and digital channels. The following correspondence:

PCM 1:	Basic group 1
Channels 1 to 12:	60-108 kHz
PCM 1:	Basic group 2
Channels 13 to 24:	60-108 kHz

5 Synchronization of transmultiplexer

The transmultiplexer must produce virtual analogue carrier frequencies with the accuracy specified in Recommendation G.225 ($\pm 10^{-7}$).

For this purpose, it is recommended:

a) either that the transmultiplexer should have an internal clock of sufficient accuracy;

b) or that the transmultiplexer should be synchronizable with an external signal which may be:
   1) a frequency produced by a central generator: 4, 12, 124 kHz;
   2) or one of the incoming PCM streams which has sufficient accuracy (this may be the case, for example when this PCM stream 1544 kbit/s is produced by a TDM switching equipment).

Note 1 – In the case of a digital filtering transmultiplexer, when synchronization on the incoming PCM stream is not possible, the remote digital terminal should have the sending side synchronized with the receiving side so as to avoid slipping at the transmultiplexer input.

Note 2 – In the case of external synchronization, transmultiplexers often have an internal oscillator locked to the external signal. If, upon loss of the external sync signal, this internal oscillator is allowed to continue to supply the clock for the outgoing digital signal (now in the free-running mode), then this oscillator should have a minimum free-running accuracy of 50×10^{-6}. This is intended to allow the distant end digital terminal to receive an adequate frequency for alarm purposes only, so as not to confuse maintenance and trouble-shooting activities. Also, a local alarm should be given in the event of a fault in the synchronization system or in the absence of the external synchronization signal.

Note 3 – In the case where the transmultiplexer is to be used in a TDMA satellite application, the effect of the satellite Doppler frequency variation must be taken into account. This can be done in two ways:

- either, the TDMA terminal incorporates the Doppler buffer memories of appropriate capacity in the earth station to satellite direction. In this case, the two directions of the TMUX must be synchronized from one of the two 1544 kbit/s PCM streams transmitted by the TDMA receive terminal;
- or, the TDMA terminal does not incorporate Doppler buffers. In this case, the PCM to FDM direction of the TMUX may be synchronized from one of the two 1544 kbit/s streams transmitted by the TDMA receive terminal. In the FDM to PCM direction, the 1544 kbit/s streams transmitted by the TMUX must be made synchronous with the TDMA system transmit clock: this supposes that a synchronization signal (contradirectional with the data) is provided by the TDMA transmit terminal to the TMUX. In the case where the processing in a digital filtering transmultiplexer is made synchronously for the two directions, Doppler buffer memories of appropriate capacity must be incorporated in the PCM interfaces.

6 Signalling

Two different approaches can be envisaged:

6.1 *No signalling translation in TMUX*

This is applicable to applications such as in-band end-to-end signalling, and common channel signalling such as CCITT No. 6 or CCITT No. 7.

6.2 *Translation of analogue signalling (Recommendation Q.21) into 1544 kbit/s PCM line signalling (Recommendation G.733)*

This translation is applicable to the predominant forms of analogue and digital signalling recommended by CCITT for international circuits (excluding signalling system R2) consisting of 12-channel analogue groups *and* 1544 kbit/s PCM digital signals.

7 Fault conditions and consequent actions

The principle governing the handling of alarms is as follows:

The behaviour of the 24-channel transmultiplexer vis-à-vis a 24-channel PCM multiplex equipment should be the same as that of another 24-channel PCM multiplex equipment. Vis-à-vis a channel translator, it should behave like another channel translator.

Table 1/G.794 summarizes the fault conditions and consequent actions in accordance with the frame structure, defined in Recommendation G.704.

TABLE 1/G.794

Fault conditions and consequent action for the 24-channel transmultiplexer

	Consequent Action / Fault Conditions	Prompt maintenance alarm indication (7)	Alarm indication to the remote equipment (3)	AIS sending (4)	Blocking of faulty speech channels	Pilot cut-off to the remote FDM terminal
PCM alarm	Loss of frame alignment and multiframe alignment or Loss of incoming signal (2)	Yes (8)	Yes		Yes (PCM → FDM)	
	Digital error ratio 10^{-4} or 10^{-3} (10)	Yes (8)	Yes			
	Reception of alarm indication from the remote equipment (2, 3)	Yes				
	AIS receiving (4)	Yes			Yes (PCM → FDM)	
FDM alarm	Absence of group pilot (5)	Yes		Yes (9)	Yes	
	Pilot level deviation alarm (11)	Yes, if regulation is present				
System alarm	Failure of power supply (2)	Yes				Yes, depending on network applications
	System failure (6)	Yes	Yes, depending on network applications	Yes, depending on network applications	Yes, depending on network applications	Yes, depending on network applications
	Synchronization failure	Yes				

Note 1 – A *Yes* in the table signifies that an action should be taken as a consequence of the relevant fault conditions. An open space in the table signifies that the relevant action should not be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 2 – The fault conditions "Loss of incoming signal", "Loss of frame alignment and multiframe alignment", "Reception of alarm indication to the remote equipment" and "Failure of power supply" are defined in Recommendation G.733.

Note 3 – For "Alarm indication to the remote equipment", data link bits are used.

Note 4 – The AIS can be used only in the new frame structure to be specified by Study Group XVIII.

Note 5 – The level, at which "Absence of group pilot" is detected, is under study.

Note 6 – The "System failure", which is only for the digital filtering transmultiplexer, corresponds to a fault detected by the transmultiplexer's supervision system, when it has one.

Note 7 – The consequent action "Prompt maintenance Alarm indication" and "Alarm indication to the remote equipment" are defined in Recommendation G.733.

Note 8 – When AIS is detected, the "Prompt maintenance alarm indication" associated with the "Loss of frame alignment and multiframe alignment" with the "Loss of incoming signal" or with the "Digital error ratio 10^{-4}" should be blocked.

Note 9 – The AIS is sent only if the 24 channels of a single PCM stream are in the alarm condition.

Note 10 – Depends on network applications.

Note 11 – "Pilot level deviation alarm" corresponds to a variation on the level of the incoming pilot from its nominal value by more than ± 4 dB, as stated in CCITT Recommendation G.241, § 1. This applies only to transmultiplexers with automatic internal level regulation.

Recommendation G.795

CHARACTERISTICS OF CODECS FOR FDM ASSEMBLIES

(Malaga-Torremolinos, 1984, amended at Melbourne, 1988)

The CCITT,

considering

that codecs capable of encoding/decoding FDM assemblies will:

a) be a useful element in the transmission networks of some Administrations during the period of transition from analogue to digital working;

b) have a limited life and application;

c) already be available in a number of realizations,

recommends

that FDM codecs should conform with the following requirements:

1 General

This Recommendation gives details of the analogue interfaces, the overall analogue-to-analogue performance of a coder/decoder pair and certain details of the digital interfaces to which FDM codecs should conform. The CCITT does not recommend any particular relationship between FDM assemblies and the digital hierarchies to be used in any codec realization nor does it recommend any particular frame structure or encoding law. Administrations intending to use codecs in their networks should ensure that compatible designs of codec are used at each end of a link. For international links, the codecs to be used should be by the agreement of the Administrations concerned. An Annex to this Recommendation gives details supplied by some Administrations of a number of FDM codec realizations.

The application of FDM codecs in a network is explained in Supplement No. 28.

2 Analogue interfaces

2.1 *FDM assemblies*

The constitution of the FDM assemblies at the analogue input and output should conform to Recommendation G.211, Figure 1 *a)*/G.211, for the basic group and Recommendation G.233, Figures 1/G.233 through 5/G.233, as appropriate for the basic supergroup, mastergroup, supermastergroup and 15 supergroup assemblies.

2.2 *Impedances and relative levels*

The impedances and relative levels at the analogue transmission ports should be as indicated in Recommendation G.233, §§ 3 through 6.

2.3 *Return loss*

The return loss against the nominal impedance of all analogue transmission ports should be at least 20 dB in the wanted frequency band. This limit relates to the intrinsic return loss, i.e. that is obtained when the cords connecting the measuring apparatus to the equipment are as short as possible. In view of the station cabling encountered in practice, the return loss recorded at the distribution frame of groups, supergroups, etc., may differ from the intrinsic return loss. This factor should be taken into account in designing and making links.

2.4 *Accuracy of carrier frequencies*

Designers of FDM codecs may find it expedient to translate the analogue signal frequency before coding and after decoding. The accuracy of any carrier frequencies used should conform to Recommendation G.225. It is possible to lock the carriers to the digital signal so that no overall frequency error is caused by the FDM codecs.

3 Digital interfaces

Digital interfaces should conform to the appropriate sections of Recommendation G.703.

4 Encoding law and frame structure

At present the CCITT does not recommend any particular encoding law or frame structure. In some instances it may not be technically or economically feasible to encode one standardized FDM assembly into one standardized hierarchical bit rate. In these cases it is possible that more than one encoded FDM assembly or an encoded FDM assembly and lower order hierarchical bit streams may be combined to form one standardized hierarchical bit rate conforming to Recommendation G.703. Where one or several encoded FDM assemblies are combined with some lower order hierarchical bit streams, then the multiplexing techniques used must be plesiochronous.

5 Analogue performance

The analogue performance is recommended in terms of the overall performance of a coder/decoder pair.

5.1 *Noise*

A maximum value of 800 pW0p is recommended. In practice, this magnitude of noise is expected to occur only on codecs for the higher order FDM assemblies and that significantly lower values will be achieved with codecs for the smaller FDM assemblies (see the Annex to this Recommendation). The use of FDM codecs on comparatively short transmission paths becomes possible when lower levels of codec noise are achieved. The recommended allowance of noise is intended to take account of all sources of noise, i.e. noise due to:

a) analogue processing before the coder and following the decoder,

b) quantization,

c) errors and jitter on the received digital signal as indicated in the G.900 series of Recommendations.

Noise should be measured in accordance with Recommendation G.230 under the loading conditions given in Recommendation G.222, § 4, for the particular FDM assembly used (see Note).

Note – The contribution to this noise made by errors on the digital transmission path is likely to be small. The effect of errors is to give rise to impulsive type interference and its expression in pW0p depends upon the statistics of the error distribution. However, for design purposes, it should be assumed that errors occurring on the digital line system have a Poisson distribution with a long-term mean error ratio of 10^{-7}.

5.2 *Performance under conditions of light loading*

Under conditions of light loading, the quantizing distortion caused by a discrete tone (e.g. a test tone or signalling frequency) may give rise to a structured noise spectrum containing components considerably in excess of the average quantizing distortion level per channel. However, in practice, the presence of a small number of system reference pilots and carrier leaks is sufficient to maintain an adequately uniform noise spectral distribution.

5.3 *Overload point*

Should be as given in Recommendation G.233, § 6 (see Note).

Note – A higher loading is appropriate if digital speech interpolation techniques or 3 kHz spaced channels (Recommendation G.235) are used.

5.4 *Frequency response*

The amplitude/frequency response, the ratio between wanted and unwanted components and the group delay distortion recommended is that given in Recommendation G.242 for through connections of the relevant FDM assemblies. This performance will be adequate to allow direct connection of the FDM codec analogue ports to the low frequency side of following translating equipment. However, if the analogue ports of the FDM codec are to be directly connected to the high frequency side of translating equipment, then the performance required of the FDM codec may appropriately be that performance normally required by the Administration of its translating equipment.

5.5 *Go-return crosstalk*

The go-return crosstalk ratio should not be worse than 80 dB.

This level of crosstalk may be difficult to measure because of the digital processing in the transmission path. It may be necessary to add to the disturbed path a low level activating signal (a sine wave or band limited white noise) to avoid gain enhancement effects.

5.6 *Unwanted modulation by harmonics of the power supply and other low frequencies*

The combined effect of a coder/decoder pair should correspond to a minimum side component attenuation of 57 dB (Recommendation G.229).

5.7 *Phase jitter*

The phase jitter on a signal caused by a coder/decoder pair should not exceed 1° peak-to-peak when measured in the frequency band given in Recommendation G.229, § 2.

Note – The value quoted above is indicated as guidance for design purposes. In practical applications, the codec should tolerate the jitter of the digital interfaces as specified in Recommendations G.823 and G.824.

6 **Fault conditions and consequent actions**

The decoder should detect:

a) loss of frame alignment;

b) loss of digital input signal;

c) the presence of Alarm Indication Signal (AIS) on the digital input port.

For all these conditions, the analogue output signal should be suppressed.

Note – Other conditions and consequent actions are under study.

ANNEX A

(to Recommendation G.795)

FDM codecs

Administration	Analogue interface	Digital interface	Noise performance
British Telecom	Supergroup (312-552 kHz)	8 448 kbit/s	140 pW0p
British Telecom	15 SG assembly (312-4025 kHz)	68 736 kbit/s	< 700 pW0p
China	Mastergroup (812-2044 kHz or 60-1300 kHz)	34 368 kbit/s	< 783 pW0p
NTT	Group (60-108 kHz)	1 544 kbit/s	< 340 pW0p

Supplement No. 28

APPLICATION OF TRANSMULTIPLEXERS, FDM CODECS, DATA-IN-VOICE (DIV) SYSTEMS AND DATA-OVER-VOICE (DOV) SYSTEMS DURING THE TRANSITION FROM AN ANALOGUE TO A DIGITAL NETWORK

(Referred to in Recommendations G.791 to G.795; this supplement is to be found on page 397 of Fascicle III.3 of the *Red Book*, Geneva, 1985.)

Supplement No. 31

STATUS OF WORK OF PRESENTLY CONSIDERED DIGITAL CIRCUIT MULTIPLICATION EQUIPMENT (DCME) DOCUMENTS

(Melbourne, 1988)

(referred to in Recommendation G.763)

The intent is to achieve a single comprehensive DCME Recommendation based on the current work of various Administrations, recognized private operating agencies and recognized standards bodies.

Consideration is being given to make the CCITT Recommendation on DCME applicable to all circumstances where DCME is required (i.e. cable and satellite, various signalling protocols, etc.). It will be of such detail that equipment conforming to it, but obtained from different design sources, would work together satisfactorily within a single system.

Documents important to the study of a detailed DCME Recommendation (planned and available) include:

INTELSAT – A detailed specification – *INTELSAT earth station standards (IESS)* (Document IEES-501 Rev.1) *digital circuit multiplication equipment specification, 32 kbit/s ADPCM with DSI*, (15 March 1988) has been approved and issued by the INTELSAT Board of Governors.

France – Contribution to Study Group XV, April 1988, *Description of a bearer frame format and associated assignment channel used in the CELTIC-3G DCMS, and performance evaluation* (which incorporates a 2 bit overload strategy on speech signals).

EUTELSAT – Detailed EUTELSAT specification (Document BS14-49), *DCME specification, 32 kbit/s ADPCM and DSI*, May 1988, approved by the EUTELSAT Board of Signatories (Note 1).

Committee T1 – *Digital circuit multiplication equipment interworking standard*, under study with draft standard scheduled for submission for voting at the end of 1988 (Note 2).

Note 1 – This specification is based in a large part on the INTELSAT specification IESS-501 Rev.1 with modifications and additions appropriate to the European: countries (particularly R2D signalling system accomodation).

Note 2 – The current draft is based in large part on the INTELSAT specification IESS-501, 16 September 1987, with modifications appropriate to the US national situation.

Supplement No. 32

TRANSFER OF ALARM INFORMATION ON 60-CHANNEL TRANSMULTIPLEXING EQUIPMENT

(Melbourne, 1988)

(referred to in Recommendation G.793)

1 Introduction

In the transition period from analogue to digital networks, interconnection between analogue and digital systems will be necessary. In some cases, transmultiplexing equipment can provide the necessary interconnection as described in Supplement No. 28 of Volume III of the Red Book [1].

Due to the different number of channels contained in the various FDM assemblies and TDM arrangements in both analogue and digital hierarchies, the transmission of alarm information may lead to some difficulties (e.g. blocking of non-faulty channels, etc.) if no special means are foreseen.

Methods for alarm transfer based on international standardized signalling systems are already described in Recommendations G.793. The basic principles are summarized in § 3 below. Other solutions can be implemented in national networks or in international networks by bilateral agreement. Paragraph 4 describes a number of possible methods used by various Administrations.

2 Principles of transmultiplexing

2.1 *Correspondence between FDM and TDM hierarchies* (see Figure 1)

According to Recommendation G.793, the relationship is as shown in Table 1.

TABLE 1

Group	Analogue channels	PCM	PCM channels
1	1 to 12	1	1 to 12
2	1 to 12	1	13 to 24
3	1 to 6	1	25 to 30
3	7 to 12	2	1 to 6
4	1 to 12	2	7 to 18
5	1 to 12	2	19 to 30

Note – In national networks or by agreement between Administrations, other schemes of correspondence between analogue and digital channels may be used.

2.2 *Detection of fault conditions in transmultiplexers*

According to the specification in Rec. G.793, the following fault conditions are detected in transmultiplexers:

a) *digital side*
   - loss of incoming signal, error ratio greater than 10^{-3}, loss of frame alignment;
   - loss of multiframe alignment (when used);
   - detection of a remote alarm.

b) *analogue side*
   - loss of group pilot;
   - loss of supergroup pilot;
   - pilot level deviation alarm.

c) system alarm
   - failure of power supply;
   - system failure (if in-service monitoring is implemented);
   - synchronization failure.

2.3 *Transmission of alarm information* (see Figure 1)

a) *FDM towards TDM*

If one of the group pilots fails, then for the relevant group an individual alarm should be transmitted from the analogue side to the relevant digital output port of the transmultiplexer. In the 60 channel-TMUX, this creates a specific problem in the case of *group 3,* which is split between the two digital streams.

b) *TDM towards FDM*

In the 60 channel-TMUX, if only one of the two digital incoming composite streams fails, no group pilot should be sent to the analogue output port of the transmultiplexer for groups 1 and 2 (or 4 and 5 respectively) and for group 3 where 6 non-faulty channels might then be out of service (see § 3).

In both cases, some kind of per channel alarm information is required to solve the difficulties.

3 Alarm transfer based on international standardized signalling systems

When the 2-bit version of Signalling System R2 is used on the digital side of a TMUX, then a conversion between the digital and the analogue versions of R2 is performed in the TMUX, according to Recommendation Q.430. This conversion allows some alarm transfer on a per-channel basis of the signalling information itself (on the digital side, bits *a* and *b* of time slot 16 are used completely for signalling). Table 2/G.793 refers to this method.

For in-band signalling and common channel signalling, Table 3/G.793 gives the fault conditions and consequent actions. However, the problem of alarm transfer on a per channel basis has not yet been solved, and is currently being studied by Study Group XI for supervision of TDMA/DSI satellite systems.

One possibility is to use bits *a* or *b* of time slot 16 to transmit some alarm indication on a per-channel basis from FDM to PCM, as in the case of the analogue version of S.S.R2 (see § 4.1 below). However, in the opposite direction, when only one PCM stream fails, it is in principle either possible to block 6 non-faulty channels, or not to block 6 faulty channels. Since in the latter case subscribers may be charged even though they are not connected by a speech path, it is preferable to adopt the first alternative.

Alternative methods of alarm transfer are in use in national applications and these are described in § 4 below.

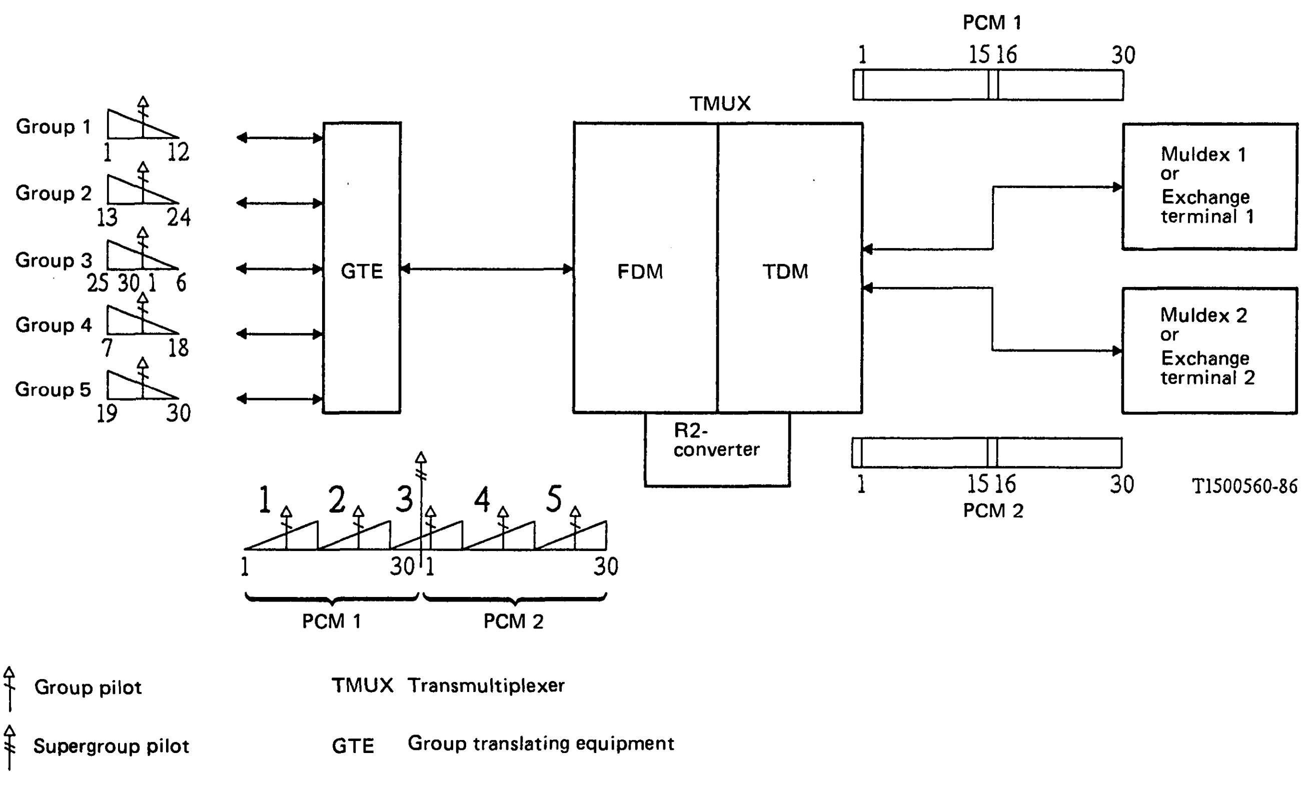


FIGURE 1

Correspondence between FDM-assembly and TDM-arrangement in 60-channel transmultiplexer (Rec. G.793)

4 Methods of alarm transfer used in national applications

4.1 *Analogue version of Signalling System R2*

4.1.1 In national networks, the following arrangements conforming to [2] may be used when the circuits connected to the transmultiplexer are operated with the Signalling System R2.

The 60-channel transmultiplexer establishes a correspondence between the signalling data carried by time slots 16 of the PCM frames and the out-of-band signalling frequencies at 3825 Hz. The specifications concerning these signalling frequencies are contained in Recommendations Q.414 and Q.415.

The signalling bit *a* associated with a channel is used to transmit the presence or absence of the signalling frequency in that channel. The signalling bit *b* associated with a channel is used to transmit alarm information to the channel in the FDM to PCM direction, when the loss of the group pilot carrying the channel is detected.

In this organization, the principles governing the handling of alarms is as follows:

- priority is given to the correct functioning of the interruption control system (Recommendation Q.416);
- the behaviour of a transmultiplexer vis-à-vis a 30 channel PCM multiplex should be the same as that of another 30-channel PCM multiplex. However, the transmultiplexer performs certain functions peculiar to digital multiplexing equipments, such as the emission of the AIS. Vis-à-vis a group modulator, it should behave like another group modulator.

Table 2 summarizes fault conditions and consequent actions.

4.1.2 The same solution may also be used for another national out-of-band signalling systems.

4.1.3 In some cases, it may be desirable for the transmultiplexer to provide locally the information control information relating to the various groups.

4.2 *Other out-of-band signalling systems*

The same methods as for the analogue version of Signalling System R2 can be used. Table 2 also applies.

4.3 *Multiframe in combination with inband and common channel signalling system* [3]

4.3.1 *Inband signalling (Signalling Systems No. 4 and 5)*

In the case of inband signalling, normally no multiframe alignment exists. Therefore time slot 16 may be used for transmission of additional signals, e.g. data signals. In this case, there is no possibility for transmission of pilot-alarms.

If time slot 16 is not used for transmission of additional signals, bit *a* or bit *b* of this time slot can be used for transmission of pilot-alarms in the FDM → PCM direction. In this case, multiframe alignment is necessary.

In the PCM → FDM direction Note 5 of Table 3.

4.3.2 *Common channel signalling*

The following refers only to Signalling System No. 7. This system is optimized for operation in digital telecommunication networks over 64 kbit/s digital channels (see Rec. Q.701). Therefore, digital data links should be preferred. But analogue transmission rates over 4 kHz or 3 kHz channels and modems, e.g. with 2400 bit/s is also possible (Recs. Q.701, Q.702) if no digital channel is available.

Low speed signalling data links can be transmitted over a transmultiplexer. Fault conditions and consequent actions are the same as for inband signalling. (See Table 3)

TABLE 2

Fault conditions and consequent actions, applicable for national networks where Signalling System R2, 1-bit analogue version, is used (see Note 1)

Fault conditions		Consequent actions							
		Prompt maintenance alarm indication generated	Alarm indication transmitted to the remote end		Blocking of faulty speech channels	Blocking of faulty signalling channels	Transmission of alarms		
			Bit 3, time slot 0 to 1 (see Note 2)	Bit 3, time slot 16, frame 0 to 1 (see Note 2) (optional)			Pilot cut-out	AIS sent (see Note 2)	Bit *b*, time slot 16 to 1 (see Note 3)
PCM alarms	Loss of signal Error ratio > 10^{-3} Loss of frame alignment (see Note 2)	Yes (see Note 4)	Yes		Yes PCM ⟶ FDM	Yes PCM ⟶ FDM	Yes (see Note 5)		
	Loss of multitrame alignment (see Note 2)	Yes (see Note 4)		Yes		Yes PCM ⟶ FDM	Yes (see Note 5)		
FDM alarms	Absence of received group pilot (see Note 6)	Yes			Yes FDM ⟶ PCM	Yes FDM ⟶ PCM		Yes (see Note 7)	Yes (see Notes 3 and 7)
	Absence of the received supergroup pilot (see Note 8)	Yes							
	Pilot level deviation alarm (Note 9)	Yes							
System alarms	Failure of poser supply	Yes					Yes, if possible	Yes, if possible	
	System failure (see Note 10)	Yes					Yes, 5 groups	Yes (see Note 7)	Yes (see Notes 3 and 7)
	Synchronization failure (see Note 11)	Yes							

Note 1 – A *Yes* in the table signifies, that an action should be taken as a consequence of the relevant fault conditions. An open space in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the condition, a *Yes* is defined in relation to this action.

Note 2 – The fault conditions "Loss of signal at 2 Mbit/s", "Error ratio > 10^{-3}", "Loss of frame alignment", "Loss of multiframe alignment" and the consequent action "Bit 3, time slot 0 to 1", "Bit 6, time slot 16, frame 0 to 1" and "AIS sent" are defined in Recommendation G.732.

Note 3 – Bits *b* of time slot 16 are used for channel associated transmission of the alarm of an individual group pilot of the affected 12 channels if the FDM → PCM direction, so as to ensure the correct functioning of the interruption control, without having to suppress channels that are not necessarily faulty, for example, in the case of a fault on a single group. In the case of group 3, bits *b* of the concerned 2×6 channels of the two 2048 kbit/s bit streams are affected.

Note 4 – The 60-channel transmultiplexer should be able to detect the Alarm Indication Signal (AIS) on incoming streams at 2048 kbit/s. When AIS is detected, the prompt maintenance indication associated with the loss of frame alignment, with an excessive error rate or with the loss of multiframe alignment should be blocked.

Note 5 – In the PCM → FDM direction, the pilots must be cut for the 3 groups associated with a PCM multiplex signal in the event of the detection of a fault on the PCM multiplex signal stream. When a single PCM multiplex signal is faulty, this involves the blocking of 6 channels which are not faulty.

Note 6 – The definition of absence of group pilot used for the operation of the interruption control system is given in the Recommendation Q.416, §§ 2.4.3.2 and 2.4.3.3. The supergroup pilot can also be used.

Note 7 – The AIS is sent only if the 30 channels of a single PCM stream are in the alarm condition. The sending of AIS then has priority over the setting of bit *b* of time slot 16 to 1.

Note 8 – Detection of "absence of supergroup pilot" is not obligatory. If the supergroup pilot is not sent, this alarm function can be performed by supervision of the 5 group pilots.

Note 9 – The concept of pilot level deviation alarm corresponds to a variation on the level of the pilot from its nominal value by more than ± 4 dB, as stated in Recommendation G.241, § 1. This applies only to transmultiplexers with automatic internal level regulation.

Note 10 – The "system" fault condition corresponds to a fault on the transmultiplexer detected by the transmultiplexer's supervision system, when it has one.

Note 11 – The "synchronization" fault is that mentionned in § 6 of Recommendation G.793. When the transmultiplexer is synchronized with an external signal or with one of the two incoming PCM streams at 2048 kbit/s, the transmultiplexer should transmit an alarm signal in the event of synchronization loss.

TABLE 3

Fault conditions and consequent sections for inband signalling systems and common channel signalling systems with low bit rates (Note 1)

Fault conditions		Consequent actions						
		Prompt maintenance alarm indication generated	Alarm indication transmitted to the remote end		Blocking of faulty speech channels	Transmission of alarms		
			Bit 3, time slot 0 to 1 (see Note 2)	Bit 6, time slot 16, frame 0 to 1 (see Note 2) (optional)		Pilot cut-out	AIS sent (see Note 2)	Bit *a* or bit *b*, time slot 16 to 1 (optional)
PCM alarms	Loss of signal Error ratio > 10^{-3} Loss of frame alignment (see Note 2)	Yes (see Note 4)	Yes		Yes PCM ⟶ FDM	Yes (see Note 5)		
PCM alarms	Loss of multiframe alignment (see Note 2) (optional)	Yes (see Note 4)		Yes		Yes (see Note 5)		
FDM alarms	Absence of the received group pilot (see Note 6)	Yes			Yes FDM ⟶ PCM		Yes (see Note 7)	Yes (see Notes 3 and 7)
FDM alarms	Absence of the received supergroup pilot (see Note 8)	Yes						
FDM alarms	Pilot level deviation alarm (see Note 9)	Yes						
System alarms	Failure of power supply	Yes				Yes, if possible	Yes, if possible	
System alarms	System failure (see Note 10)	Yes				Yes, 5 groups	Yes (see Note 7)	Yes (see Notes 3 and 7)
System alarms	Synchronization failure (see Note 11)	Yes						

Note 1 – A *Yes* in the table signifies, that an action should be taken as a consequence of the relevant fault conditions. An open space in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 2 – The fault conditions "Loss of signal at 2 Mbit/s", "Error ratio > 10^{-3}", "Loss of frame alignment", "Loss of multiframe alignment" and the consequent action "Bit 3, time slot 0 to 1", "Bit 6, time slot 16, frame 0 to 1" and "AIS sent" are defined in Recommendation G.732.

Note 3 – Bits *b* of time slot 16 are used for channel associated transmission of the alarm of an individual group pilot of the affected 12 channels if the FDM → PCM direction, so as to ensure the correct functioning of the interruption control, without having to suppress channels that are not necessarily faulty, for example, in the case of a fault on a single group. In the case of group 3, bits *b* of the concerned 2×6 channels of the two 2048 kbit/s bit streams are affected.

Note 4 – The 60-channel transmultiplexer should be able to detect the Alarm Indication Signal (AIS) on incoming streams at 2048 kbit/s. When AIS is detected, the prompt maintenance indication associated with the loss of frame alignment, with an excessive error rate or with the loss of multiframe alignment should be blocked.

Note 5 – In the PCM → FDM direction, the pilots must be cut for the 3 groups associated with a PCM multiplex signal in the event of the detection of a fault on the PCM multiplex signal stream. When a single PCM multiplex signal is faulty, this involves the blocking of 6 channels which are not faulty.

Note 6 – The definition of absence of group pilot used for the operation of the interruption control system is given in the Recommendation Q.416, §§ 2.4.3.2 and 2.4.3.3. The supergroup pilot can also be used.

Note 7 – The AIS is sent only if the 30 channels of a single PCM stream are in the alarm condition. The sending of AIS then has priority over the setting of bit *b* of time slot 16 to 1.

Note 8 – Detection of "absence of supergroup pilot" is not obligatory. If the supergroup pilot is not sent, this alarm function can be performed by supervision of the 5 group pilots.

Note 9 – The concept of pilot level deviation alarm corresponds to a variation on the level of the pilot from its nominal value by more than ± 4 dB, as stated in Recommendation G.241, § 1. This applies only to transmultiplexers with automatic internal level regulation.

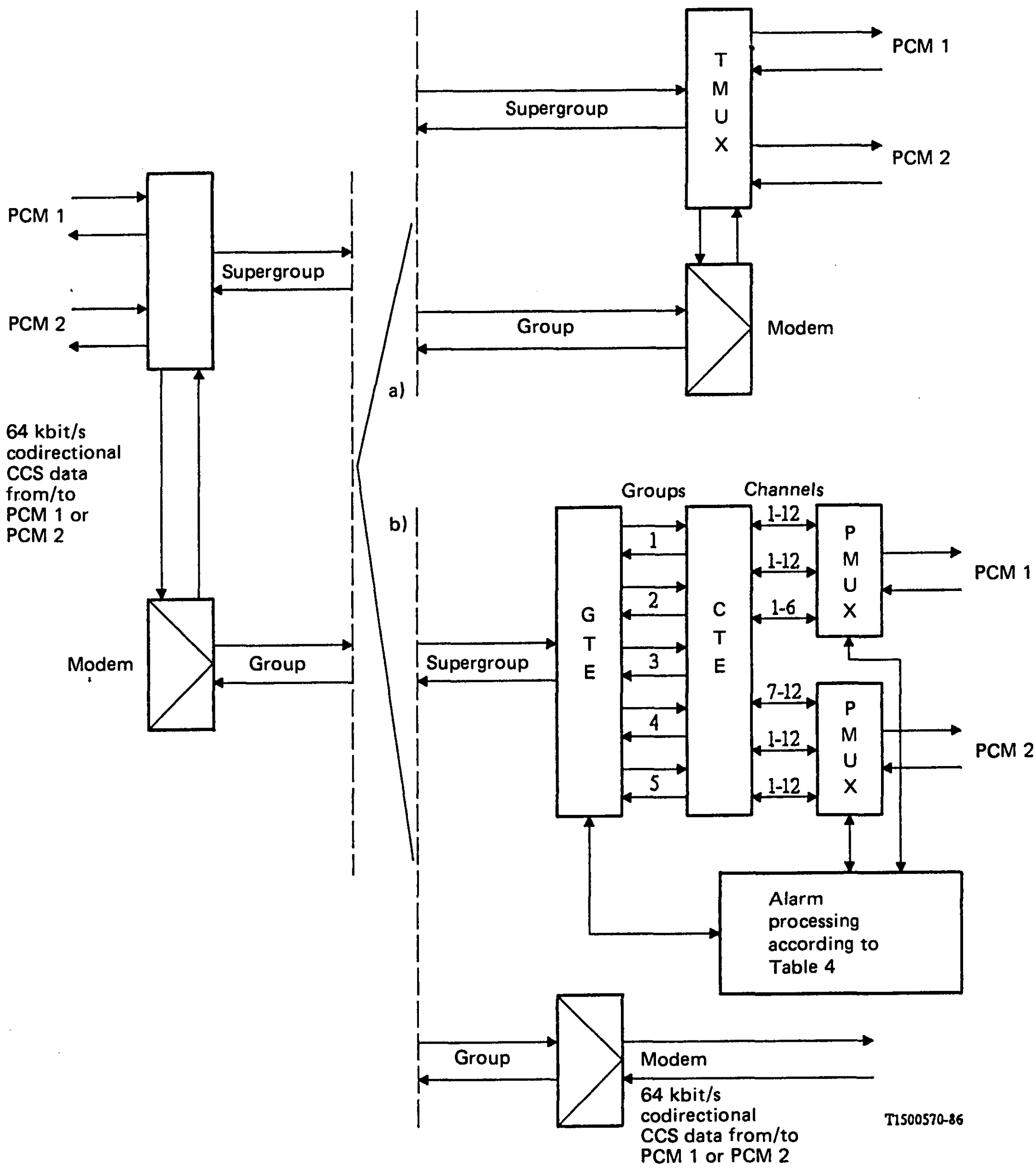
Note 10 – The "system" fault condition corresponds to a fault on the transmultiplexer detected by the transmultiplexer's supervision system, when it has one.

Note 11 – The "synchronization" fault is that mentionned in § 6 of the Recommendation G.793. When the transmultiplexer is synchronized with an external signal or with one of the two incoming PCM streams at 2048 kbit/s, the transmultiplexer should transmit an alarm signal in the event of synchronization loss.

4.4 *Fault conditions and consequent actions for common channel signalling using combinations of cut group pilots*

The alarm transfer procedure detailed in Table 4 is used in a TMUX-TMUX and a TMUX-GTE/CTE/PCM MUX link used by BT (United Kingdom). Figure 2 shows how these two types of link are implemented. The method uses combinations of cut group pilots to transfer standard digital alarms across the analogue portion of the link. One pilot is cut to signal a forward alarm and two pilots are cut to signal a backward alarm. The FDM path is thus effectively transparent to digital alarms, giving consistency with systems which are entirely digital. Key features of this method are that it does not require that alarms be transferred on a per-channel basis and it ensures that all faulty channels are blocked. It therefore avoids the problems mentioned in § 3 above.

No modifications are required to the implementation of the common channel signalling system. The 64 kbit/s common channel signalling channel is extracted from PCM 1 or PCM 2 and sent over one group via a modem.



CCS Common channel signalling

FIGURE 2

Simplified block diagram showing arrangements for:

a) TMUX – TMUX link

b) TMUX – GTE/CTE/PMUX link

TABLE 4

Fault conditions and consequent actions for common channel signalling using combinations of cut group pilots (Note 1)

Fault Conditions \ Consequent Actions			Digital								Analogue						Other	
			AIS in PCM 1 (Note 2)	AIS in PCM 2 (Note 2)	AIS in co-directional 64 kbit/s O/P		AIS in time slot carrying CCS data		Bit 3, time slot 0 to 1		Pilot cut out					Suppress supergroup pilot	Blocking of faulty speech channels	Prompt maintenance alarm indication generated
					PCM 1	PCM 2	PCM 1	PCM 2	PCM 1	PCM 2	1	2	3	4	5			
PCM alarms	Loss of signal Error ratio > 10^{-3} Loss of frame alignment	PCM 1 (Note 2)			Yes				Yes		Yes						Yes PCM → FDM	Yes (Note 3)
PCM alarms	Loss of signal Error ratio > 10^{-3} Loss of frame alignment	PCM 2 (Note 2)				Yes				Yes					Yes		Yes PCM → FDM	Yes (Note 3)
PCM alarms	Loss of 64 kbit/s PCM 1 input (Note 4)						Yes											Yes
PCM alarms	Loss of 64 kbit/s PCM 2 input (Note 4)							Yes										Yes
PCM alarms	Bit 3, time slot 0: PCM 1										Yes	Yes						Optional
PCM alarms	Bit 3, time slot 0: PCM 2													Yes	Yes			Optional
FDM alarms	Loss of Group 1 and Group 2 but not Group 3								Yes									Optional
FDM alarms	Any other combination of Group 1, 2 and 3 losses		Yes								Yes	Yes						Yes
FDM alarms	Loss of Group 4 and Group 5 but not Group 3									Yes								Optional
FDM alarms	Any other combination of Group 3, 4 and 5 losses			Yes										Yes	Yes			Yes
FDM alarms	Loss of supergroup pilot (Note 5)																	Yes
FDM alarms	Pilot level deviation alarm (Note 6)																	Yes

TABLE 4 *(cont.)*

Fault Conditions	Consequent Actions	Digital								Analogue						Other	
		AIS in PCM 1 (Note 2)	AIS in PCM 2 (Note 2)	AIS in co-directional 64 kbit/s O/P		AIS in time slot carrying CCS data		Bit 3, time slot 0 to 1		Pilot cut out					Suppress supergroup pilot	Blocking of faulty speech channels	Prompt maintenance alarm indication generated
				PCM 1	PCM 2	PCM 1	PCM 2	PCM 1	PCM 2	1	2	3	4	5			
System alarms	Failure of power supply	If possible	If possible	If possible	If possible					If possible					If possible		Yes
	System failure (Note 7)	Yes	Yes	Yes	Yes					Yes	Yes	Yes	Yes	Yes	If possible		Yes
	Synchronization failure (Note 8)	Yes	Yes	Yes	Yes					Yes	Yes	Yes	Yes	Yes	If possible		Yes

Note 1 – A *Yes* in the table signifies, that an action should be taken as a consequence of the relevant fault conditions. An open space in the table signifies that the relevant action should *not* be taken as a consequence of the relevant fault condition, if this condition is the only one present. If more than one fault condition is simultaneously present, the relevant action should be taken if, for at least one of the conditions, a *Yes* is defined in relation to this action.

Note 2 – The fault conditions "Loss of signal", "Error ratio $> 10^{-3}$", "Loss of frame alignment", "Loss of multiframe alignment" and the consequent action "Bit 3, time slot 0 to 1", and "AIS sent" are defined in Recommendation G.732.

Note 3 – The TMUX should be able to detect the alarm indication signal (AIS) on incoming streams at 2048 kbit/s. When AIS is detected, the prompt maintenance indication associated with the loss of frame alignment and/or an excessive error ratio should be blocked.

Note 4 – For transmultiplexers not required to handle common channel signalling, in either or both PCM streams, it shall be possible to program the TMUX to suppress the alarms associated with these fault conditions.

Note 5 – Detection of absence of supergroup pilot is not obligatory. If the supergroup pilot is not sent, this alarm function can be performed by supervision of the 5 group pilots.

Note 6 – The concept of pilot level deviation alarm corresponds to a variation on the level of the pilot from its nominal value by more than ± 4 dB as stated in Recommandation G.241, § 1. This applies only to transmultiplexers with automatic internal level regulation.

Note 7 – The "system" fault condition corresponds to a fault on the transmultiplexer detected by the transmultiplexer's supervision system, when it has one.

Note 8 – The "synchronisation" fault is that mentioned in § 6 of Recommendation G.793. When the transmultiplexer is synchronized with an external signal or with one of the two incoming PCM streams at 2048 kbit/s, the transmultiplexer should transmit an alarm signal in the event of synchronisation loss.

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