INTERNATIONAL TELECOMMUNICATION UNION

CCITT

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

RED BOOK

VOLUME VIII – FASCICLE VIII.1

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

RECOMMENDATIONS OF THE V SERIES

VIIITH PLENARY ASSEMBLY
MALAGA-TORREMOLINOS, 8-19 OCTOBER 1984

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CONTENTS OF THE CCITT BOOK
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Volume IV – *(4 fascicles, sold separately)*

FASCICLE IV.1 – Maintenance; general principles, international transmission systems, international telephone circuits. Recommendations M.10-M.762 (Study Group IV).

FASCICLE IV.2 – Maintenance; international voice frequency telegraphy and fascimile, international leased circuits. Recommendations M.800-M.1375 (Study Group IV).

FASCICLE IV.3 – Maintenance; international sound programme and television transmission circuits. Series N Recommendations (Study Group IV).

FASCICLE IV.4 – Specifications of measuring equipment. Series 0 Recommendations (Study Group IV).

Volume V – Telephone transmission quality. Series P Recommendations (Study Group XII).

Volume VI – *(13 fascicles, sold separately)*

FASCICLE VI.1 – General Recommendations on telephone switching and signalling. Interface with the maritime mobile service and the land mobile services. Recommendations Q.1-Q.118 *bis* (Study Group XI).

FASCICLE VI.2 – Specifications of Signalling Systems Nos. 4 and 5. Recommendations Q.120-Q.180 (Study Group XI).

FASCICLE VI.3 – Specifications of Signalling System No. 6. Recommendations Q.251-Q.300 (Study Group XI).

FASCICLE VI.4 – Specifications of Signalling Systems R1 and R2. Recommendations Q.310-Q.490 (Study Group XI).

FASCICLE VI.5 – Digital transit exchanges in integrated digital networks and mixed analogue-digital networks. Digital local and combined exchanges. Recommendations Q.501-Q.517 (Study Group XI).

FASCICLE VI.6 – Interworking of signalling systems. Recommendations Q.601-Q.685 (Study Group XI).

FASCICLE VI.7 – Specifications of Signalling System No. 7. Recommendations Q.701-Q.714 (Study Group XI).

FASCICLE VI.8 – Specifications of Signalling System No. 7. Recommendations Q.721-Q.795 (Study Group XI).

FASCICLE VI.9 – Digital access signalling system. Recommendations Q.920-Q.931 (Study Group XI).

FASCICLE VI.10 – Functional Specification and Description Language (SDL). Recommendations Z.101-Z.104 (Study Group XI).

FASCICLE VI.11 – Functional Specification and Description Language (SDL), annexes to Recommendations Z.101-Z.104 (Study Group XI).

FASCICLE VI.12 – CCITT High Level Language (CHILL). Recommendation Z.200 (Study Group XI).

FASCICLE VI.13 – Man-Machine Language (MML). Recommendations Z.301-Z.341 (Study Group XI).

Volume VII – *(3 fascicles, sold separately)*

FASCICLE VII.1 – Telegraph transmission. Series R Recommendations (Study Group IX). Telegraph services terminal equipment. Series S Recommendations (Study Group IX).

FASCICLE VII.2 – Telegraph switching. Series U Recommendations (Study Group IX).

FASCICLE VII.3 – Terminal equipment and protocols for telematic services. Series T Recommendations (Study Group VIII).

Volume VIII – *(7 fascicles, sold separately)*

FASCICLE VIII.1 – Data communication over the telephone network. Series V Recommendations (Study Group XVII).

FASCICLE VIII.2 – Data communication networks: services and facilities. Recommendations X.1-X.15 (Study Group VII).

FASCICLE VIII.3 – Data communication networks: interfaces. Recommendations X.20-X.32 (Study Group VII).

FASCICLE VIII.4 – Data communication networks: transmission, signalling and switching, network aspects, maintenance and administrative arrangements. Recommendations X.40-X.181 (Study Group VII).

FASCICLE VIII.5 – Data communication networks: Open Systems Interconnection (OSI), system description techniques. Recommendations X.200-X.250 (Study Group VII).

FASCICLE VIII.6 – Data communication networks: interworking between networks, mobile data transmission systems. Recommendations X.300-X.353 (Study Group VII).

FASCICLE VIII.7 – Data communication networks: message handling systems. Recommendations X.400-X.430 (Study Group VII).

Volume IX – Protection against interference. Series K Recommendations (Study Group V). Construction, installation and protection of cable, and other elements of outside plant. Series L Recommendations (Study Group VI).

Volume X – *(2 fascicles, sold separately)*

FASCICLE X.1 – Terms and definitions.

FASCICLE X.2 – Index of the Red Book.

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CONTENTS OF FASCICLE VIII.1 OF THE RED BOOK

Series V Recommendations

Data communication over the telephone network

PRELIMINARY NOTES

1 The Questions entrusted to each Study Group for the Study Period 1985-1988 can be found in Contribution No. 1 to that Study Group.

2 In this Volume, the expression "Administration" is used for shortness to indicate both a telecommunication Administration and a recognized private operating agency.

3 The status of annexes and appendices attached to the Series V Recommendations should be interpreted as follows:

- an *annex* to a Recommendation forms an integral part of the Recommendation;
- an *appendix* to a Recommendation does not form part of the Recommendation and only provides some complementary explanation or information specific to that Recommendation.

FASCICLE VIII.1

Series V Recommendations

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

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PRINCIPLES GOVERNING THE COLLABORATION BETWEEN THE CCITT AND OTHER INTERNATIONAL ORGANIZATIONS IN THE STUDY OF DATA COMMUNICATIONS

Recommendation A.20 published in Volume I is reproduced below for the convenience of the reader of the Series V Recommendations.

Recommendation A.20

COLLABORATION WITH OTHER INTERNATIONAL ORGANIZATIONS OVER DATA TRANSMISSION

(Geneva, 1964; amended at Mar del Plata, 1968, and at Geneva, 1972, 1976 and 1980; Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that, according to Article 1 of the agreement between the United Nations and the International Telecommunication Union, the United Nations recognizes the International Telecommunication Union as the specialized agency responsible for taking such action as may be appropriate under its basic instrument for the accomplishment of the purposes set forth therein;

(b) that Article 4 of the International Telecommunication Convention (Nairobi, 1982) states that the purposes of the Union are:

"a) to maintain and extend international cooperation between all Members of the Union for the improvement and rational use of telecommunications of all kinds, as well as to promote and to offer technical assistance to developing countries in the field of telecommunications;

b) to promote the development of technical facilities and their most efficient operation with a view to improving the efficiency of telecommunication services, increasing their usefulness and making them, so far as possible, generally available to the public;

c) to harmonize the actions of nations in the attainment of those ends;"

(c) that Article 40 of the Convention states that, in furtherance of complete international coordination on matters affecting telecommunication, the Union shall cooperate with international organizations having related interests and activities;

(d) that in the study of data transmission the CCITT has to collaborate with the organizations dealing with data processing and office equipment and particularly the International Organization for Standardization (ISO) and the International Electrotechnical Commission (IEC);

(e) that this collaboration has to be organized in a manner that will avoid duplication of work and decisions that would be contrary to the principles set out above;

unanimously declares the view

that international standards for data transmission should be established with the following considerations in mind:

(1) Clearly it will be the responsibility of the CCITT to lay down standards for *transmission channels*, i.e. aspects of data transmission which require a knowledge of telecommunication networks or affect performance of these networks.

(2) The standardization of signal conversion terminal equipment (modems) is the province of the CCITT; the standardization of the junction (interface) between modem and the data terminal equipment is a matter of agreement between the CCITT and the ISO or the IEC.

(3) Devices designed to detect and (or) correct errors must take account of:

- the error rate tolerable to the user;
- the line transmission conditions;
- the code, which has to meet the exigencies of the data alphabet and the requirements of error control (this must be such as to give an output satisfactory to the user) together with the requisite signalling (synchronism, repetition signals, etc.).

Standardization here may not come wholly within the CCITT's province, but the CCITT has very considerable interests at stake.

(4) The alphabet (as defined in Fascicle X.1 – Terms and Definitions) is a "table of correspondence between an agreed set of characters and the signals which represent them".

The CCITT and the ISO reached agreement on an alphabet for general (but not exclusive) use for data and message transmission and have standardized a common alphabet which is known as International Alphabet No. 5 (CCITT Recommendation T.50 and ISO Standard No. 646-1983; ISO 7-bit coded character set for information interchange).

Complementary study of some control characters of the alphabet should be effected cooperatively.

(5) Coding (as defined in Fascicle X.1 – Terms and Definitions) is "a system of rules and conventions according to which the telegraph signals forming a message or the data signals forming a block should be formed, transmitted, received and processed". Hence, it consists of a transformation of the format of the signals in the alphabet for taking account of synchronous methods, and introduction of redundancy in accordance with the error control system. This is not a field in which the CCITT alone may be able to decide; however, no decision should be taken without reference to the Committee, because of the possible restrictions which transmission and switching peculiarities may impose on coding.

When the general switched network is used (telephone or telex) and when the error control devices are subject to restrictions (switching signals – reserved sequences), it is the CCITT which is in fact responsible for any necessary standardization in conjunction with other bodies.

(6) The limits to be observed for transmission performance on the transmission path (modem included) fall within the competence of the CCITT; the limits for the transmission performance of the sending equipment and the margin of terminal data equipment (depending on the terminal apparatus and the transmission path limits) should be fixed by agreement between the ISO and the CCITT.

(7) In all instances, the CCITT alone can lay down manual and automatic operating procedures for the setting-up, holding and clearing of calls for data communications when the general switched networks are used, including type and form of signals to be interchanged at the interface between data terminal equipment and data circuit terminating equipment.

(8) When a public data network is involved, the CCITT has the responsibility to provide the Recommendations which apply. Where these Recommendations have an impact on the basic design and features of data processing systems and office equipment [normally the Data Terminal Equipment (DTE)], they shall be the subject of consultation between CCITT and ISO and in some cases a mutual agreement may be desirable. Likewise when the ISO is developing or changing standards that may affect compatibility with the public data network there shall be consultation with the CCITT.

SECTION 1

GENERAL

Recommendation V.1

EQUIVALENCE BETWEEN BINARY NOTATION SYMBOLS AND THE SIGNIFICANT CONDITIONS OF A TWO-CONDITION CODE

(New Delhi, 1960; amended at Geneva, 1964 and 1972)

Binary numbering expresses numbers by means of two digits normally represented by the symbols 0 and 1. Transmission channels are especially well suited to the transmission of signals by a modulation having two significant conditions (two-condition modulation). These two significant conditions are sometimes called "space" and "mark" or "start" and "stop", or they may be called condition A or condition Z [1].

It is very useful to make the two conditions of a two-condition modulation correspond to the binary digits 0 and 1. Such equivalence will facilitate the transmission of numbers resulting from binary calculation, the conversion of codes for binary numbers and of codes for decimal numbers, maintenance operations and relations between transmission personnel and the personnel in charge of data-processing machines.

At first sight, it does not seem to matter whether the symbol 0 corresponds in transmission to condition A or condition Z, the symbol 1 then corresponding to condition Z or condition A or vice versa.

In telegraphy, however, when a telegraphic communication is set up and the sending of signals is stopped (called the idle condition of the line), the signal sent over the line consists of condition Z throughout the suspension of transmission.

It is logical (and for certain VF telegraph systems also essential) to use the same rule in data transmission. During the "idle periods" of transmission, condition Z should be applied to the circuit input.

Data transmission on a circuit is often controlled by perforated tape. On perforated tapes used for telegraphy, condition Z is represented by perforation. When binary numbers are represented by means of perforations, it is customary to represent the symbol 1 by a perforation. It is therefore logical to make this symbol 1 correspond to condition Z.

For these reasons, the CCITT

unanimously declares the following view:

1 In transmitting data by two-condition code, in which the digits are formed using binary notation, the symbol 1 of the binary notation will be equivalent to condition Z of the modulation, and the symbol 0 of the binary notation will be equivalent to condition A of the modulation.

2 During periods when there is no signal sent to the input of the circuit, the circuit input condition is condition Z.

3 If perforation is used, one perforation corresponds to one unit interval under condition Z.

4 In accordance with Recommendation R.31, the sending of symbol 1 (condition Z) corresponds to the tone being sent on a channel using amplitude modulation.

5 In accordance with Recommendation R.35, when frequency modulation is used, the sending of symbol 0 corresponds to the higher frequency, while the sending of symbol 1 corresponds to the lower frequency.

6 a) For phase modulation with reference phase:

the symbol 1 corresponds to a phase equal to the reference phase;

the symbol 0 corresponds to a phase opposed to the reference phase.

b) For differential two-phase modulation where the alternative phase changes are 0 degree or 180 degrees:

the symbol 1 corresponds to a phase inversion from the previous element;

the symbol 0 corresponds to a no-phase inversion from the previous element.

7 A summary of equivalence is shown in Table 1/V.1.

TABLE 1/V.1

Summary of equivalence (see Note 1)

	Digit 0 "Start" signal in start-stop code Line available condition in telex switching "Space" element of start-stop code Condition A	Digit 1 "Stop" signal in start-stop code Line idle condition in telex switching (Note 2) "Mark" element of start-stop code Condition Z
Amplitude modulation	Tone-off	Tone-on
Frequency modulation	High frequency	Low frequency
Phase modulation with reference phase	Opposite phase to the reference phase	Reference phase
Differential two-phase modulation where the alternative phase changes are 0 degree or 180 degrees	No phase inversion	Inversion of the phase
Perforations	No perforation	Perforation

Note 1 – The standardization described in this Recommendation is general, whether over telegraph-type circuits or over circuits of the telephone type, making use of electromechanical or electronic devices.

Note 2 – It primarily applies to anisochronous use.

Reference

[1] CCITT Definition: *Position A; position Z*, Vol. X, (Terms and Definitions).

POWER LEVELS FOR DATA TRANSMISSION OVER TELEPHONE LINES

(New Delhi, 1960; amended at Geneva, 1964 and 1980)

The objectives in specifying data signal levels are as follows:

a) To ensure satisfactory transmission and to permit coordination with devices such as signalling receivers or echo suppressors, the data signal levels on international circuits should be controlled as closely as possible,

b) To ensure correct performance of multichannel carrier systems from the point of view of loading and noise, the mean power of data circuits should not differ much from the conventional value of channel loading (−15 dBm0 for each direction of transmission: see Note below). This conventional value makes allowance for a reasonable proportion P (dependent on the transmission systems and probably less than 50%; the value will have to be specified in subsequent studies) of the channels in a multichannel system being used for nonspeech applications at fixed power levels at about −13 dBm0 for each direction of transmission.

If the proportion of nonspeech applications (including data) does not exceed the above value P, the mean power of −13 dBm0 for each direction of transmission would be allowable for data transmission also.

However, assuming that the proportion of nonspeech circuits is appreciably higher than P (due to the development of data transmission) on international carrier systems, a reduction of this power by 2 dB might be reasonable (these values require further study).

Note – The distribution of long-term mean power among the channels in a multichannel carrier telephone system (conventional mean value of −15 dBm0), probably has a standard deviation in the neighbourhood of 4 dB (see [2]).

c) It is probable that Administrations will wish to fix specific values for the signal power level of data modulators either at the subscriber's line terminals or at the local exchanges. The relation between these values and the power levels on international circuits depends on the particular national transmission plan; in any case, a wide range of losses among the possible connections between the subscriber and the input to international circuits must be expected.

d) Considerations a) to c) suggest that specification of the maximum data signal level only is not the most useful form. One alternative proposal would be to specify the nominal power at the input to the international circuit. The nominal power would be the statistically estimated mean power obtained from measurement on many data transmission circuits.

For these reasons, the CCITT

unanimously declares the following view:

1 Data transmission over leased telephone circuits (private wires) set up on carrier systems

1.1 The maximum power output of the subscriber's equipment into the line shall not exceed 1 mW at any frequency.

1.2 For systems transmitting tones continuously, e.g., frequency-modulation systems, the maximum power level at the zero relative level point shall be −13 dBm0. When transmission of data is discontinued for any appreciable time, the power level should preferably be reduced to −20 dBm0 or lower.

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[1] Recommendation V.2 corresponds to Recommendation H.15 [1].

1.3 For systems not transmitting tones continuously, e.g., amplitude-modulation systems, the signal characteristics should meet all of the following requirements:

i) The maximum value of the 1-minute mean power shall not exceed −13 dBm0.

ii) Provisionally, the maximum value of the instantaneous power shall not exceed a level corresponding to that of a 0 dBm0 sine wave signal. This limit should be confirmed or amended after further study.

iii) Provisionally, the maximum signal power determined for a 10-Hz bandwidth centred at any frequency shall not exceed −10 dBm0. This limit should be confirmed or amended after further study.

Note 1 – It is estimated that the proportion of international circuits which are carrying data transmissions is approximately 20%. If the proportion should reach a high level (approximately 50% or even less in the case of high-usage systems), the limits now proposed would need to be reconsidered.

Note 2 – Supplement No. 16 [3] of the Yellow Book, Volume III, gives information on the out-of-band power of signals applied to leased telephone-type circuits.

2 Data transmission over the switched telephone system

2.1 The maximum power output of the subscriber's equipment into the line shall not exceed 1 mW at any frequency.

2.2 For systems transmitting tones continuously, such as frequency- or phase-modulation systems, the power level of the subscriber's equipment should be fixed at the time of installation to allow for loss between his equipment and the point of entry to an international circuit, so that the corresponding nominal level of the signal at the international circuit input shall not exceed −13 dBm0.

2.3 For systems not transmitting tones continously, e.g. amplitude-modulation systems, the signal characteristics should meet all of the following requirements (see also Note 1 to § 1.3):

i) The maximum value of the 1-minute mean power shall not exceed −13 dBm0.

ii) Provisionally, the maximum value of the instantaneous power shall not exceed a level corresponding to that of a 0 dBm0 sine wave signal. This limit should be confirmed or amended after further study.

iii) Provisionally, the maximum signal power determined for a 10 Hz bandwidth centred at any frequency shall not exceed −10 dBm0. This limit should be confirmed or amended after further study.

Note 1 – In practice, it is no easy matter to assess the loss between a subscriber's equipment and the international circuit, so that § 2 of the present Recommendation should be taken as providing general planning guidance.

Note 2 – In switched connections, the loss between subscribers' telephones may be high: 30 to 40 dB. The level of the signals received will then be very low, and these signals may suffer disturbance from the dialling pulses sent over other circuits.

If there is likely to be a heavy demand for international connections for data transmission over the switched network, some Administrations might want to provide special 4-wire subscriber lines. If so, the levels to be used might be those proposed for leased circuits.

References

[1] CCITT Recommendation *Power levels for data transmission over telephone lines*, Vol. III, Rec. H.51.

[2] *Measurement of the load of telephone circuits*, Green Book, Vol. III-2, Supplement No. 5, ITU, Geneva, 1973.

[3] *Out-of-band characteristics of signals applied to leased telephone-type circuits*, Vol. III, Supplement No. 16.

GENERAL STRUCTURE OF SIGNALS OF INTERNATIONAL ALPHABET No. 5 CODE FOR DATA TRANSMISSION OVER PUBLIC TELEPHONE NETWORKS[1)]

(Mar del Plata, 1968; amended at Geneva, 1976 and 1980)

The CCITT,

I. *considering, firstly,*

the agreement between the International Organization for Standardization (ISO) and the CCITT on the main characteristics of a seven-unit alphabet [International Alphabet No. 5 (IA5)] to be used for data transmission and for telecommunications requirements that cannot be met by the existing five-unit International Telegraph Alphabet No. 2 (ITA2);

the interest, both to the users and to the telecommunication services, of an agreement concerning the chronological order of transmission of bits in serial working;

declares the view

that the agreed rank number of the unit in the alphabetical table of combinations should correspond to the chronological order of transmission in serial working on telecommunication circuits;

that, when this rank in the combination represents the order of the bit in binary numbering, the bits should be transmitted in serial working with the low order bit first;

that the numerical meaning corresponding to each information unit considered in isolation is that of the digit:

0 for a unit corresponding to condition A (travail = space), and

1 for a unit corresponding to condition Z (repos = mark),

in accordance with the definitions of these conditions for a two-condition transmission system;

II. *considering, moreover,*

that it is often desirable, in data transmission, to add an extra "parity" unit to allow for the detection of errors in received signals;

the possibility offered by this addition for the detection of faults in data terminal equipment;

the need to reserve the possibility of making this addition during the transmission itself, after the seven information units proper have been sent;

declares the view

that signals of the International Alphabet No. 5 code for data transmission should, in general, include an additional "parity" unit;

that the rank of this unit and, hence, the chronological order of the transmission in serial working should be the eighth of the combination thus completed;

III. *considering*

that, in start-stop systems working with electromechanical equipment, the margin of such equipment and the reliability of the connection are considerably increased by the use of a stop element corresponding to the duration of two unit intervals of the modulation;

that for transmissions over telephone circuits via modems installed on the user's premises, the latter must be able to use the connections at the highest possible practical rate in characters per second, and that in such a case a single-unit stop element leads to a gain of about 10% as regards this practical rate;

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1) See Recommendation X.4 [1] for data transmission over public data networks.

that, however, it does not appear that the production of electronic devices capable of working at will with start-stop signals having a stop element equal to one or two unit intervals should lead to costly complications and that such an arrangement can have the advantage of appreciably limiting the error rate without greatly reducing the practical efficiency of the connection;

declares the view

that in start-stop systems using combinations of the seven-unit alphabet normally followed by a parity unit, the first information unit of the transmitted combination should be preceded by a start element corresponding to condition A (space);

that the duration of this start element should be a one-unit interval for the modulation rate under consideration, at transmitter output;

that the combination of seven information units, normally completed by its parity unit, should be followed by a stop element corresponding to condition Z (mark);

that for start-stop systems using the seven-unit code on switched telephone networks, a two-unit stop element should be used with electromechanical data terminal equipments operating at modulation rates up to and including 200 bauds. In other cases, the use of a one-unit stop element is preferable. However, this is subject to a mutual agreement between Administrations concerned;

that similar situations when a one-unit stop element can be used may apply to leased circuits;

that the start-stop receivers should be capable of correctly receiving start-stop signals comprising a single-unit stop element, whose duration will be reduced by a time interval equal to the deviation corresponding to the degree of gross start-stop distortion permitted at receiver input. However, for electromechanical equipment which must use a two-unit stop element (eleven-unit code signal) with a modulation rate of 200 bauds or less, receivers should be capable of correctly receiving signals with a stop element reduced to one unit;

IV. *considering, finally,*

that the direction of the parity unit can only be that of the even parity on the perforated tapes, particularly owing to the possibility of deletion (combination 7/15 of the alphabet) which causes a hole to appear in all tracks;

that, on the other hand, the odd parity is considered essential in the equipment which depends on transitions in the signals to maintain synchronism [in cases where combination 1/6 (SYNC) of the alphabet does not permit of an economical solution];

declares the view

that the parity unit of the signal should correspond to the even parity in links or connections operated on the principle of the start-stop system;

that this parity should be odd on links or connections using end-to-end synchronous operation;

that arrangements should be made when necessary to reverse the direction of the parity unit at the input and output of the synchronous equipment connected either to apparatus working on the start-stop principle or receiving characters on perforated tape;

that the detection of a character out-of-parity may be represented by:

a) reverse question mark (⸮) graphic character or a representation of the capital letters SB (see ISO 2047) provided that these letters occupy a single character position on the screen or printer, and could have been entered by a single key stroke, recognizing it may be difficult to achieve a legible "SB" character from some matrix printers or displays where the characters are printed; or

b) a recording of the 1/10 (SUB) character on the tape or other storage medium, where provided

and that, where a SUB character occurs in a received transmission, or is presented to a DTE via a storage medium, e.g. paper tape, then the reaction should be as in a) and b) above.

Reference

[1] CCITT Recommendation *General structure of signals of International Alphabet No. 5 code for data transmission over public data networks*, Vol. VIII, Rec. X.4.

Recommendation V.5

STANDARDIZATION OF DATA SIGNALLING RATES FOR SYNCHRONOUS DATA TRANSMISSION IN THE GENERAL SWITCHED TELEPHONE NETWORK

(former Recommendation V.22, Geneva, 1964; amended at Mar del Plata, 1968, at Geneva, 1972 and 1976, and at Malaga-Torremolinos, 1984)

1 Data transmission by international communications carried on the general switched telephone network using a synchronous transmission procedure will be done with a specific mode of modulation, two- or multi-condition, and serial transmission (see Note 1). For synchronous data transmission on leased telephone-type circuits see Recommendation V.6.

2 The data signalling rates for synchronous transmission in the general switched telephone network will be:

600, 1200, 2400, 4800 and 9600 bits (see Note 2).

The users will choose among these rates, in accordance with their needs and the facilities afforded by the connection.

3 Data signalling rates should in no case deviate from the nominal value by more than ± 0.01%.

Note 1 – The application of parallel data transmission is a subject of other Recommendations.

Note 2 – Modems for use in the general switched telephone network at these data signalling rates; see Recommendations V.23, V.26 *bis* and V.27 *ter* respectively for a half-duplex mode of operation, and V.22, V.22 *bis*, V.26 *ter* and V.32, respectively, for a duplex-mode of operation.

Note 3 – For data transmission at 300 bit/s, see Recommendation V.21.

Recommendation V.6

STANDARDIZATION OF DATA SIGNALLING RATES FOR SYNCHRONOUS DATA TRANSMISSION ON LEASED TELEPHONE-TYPE CIRCUITS

(former Recommendation V.22 bis, Geneva, 1972; amended at Geneva, 1976, and at Malaga-Torremolinos, 1984)

1 Data transmission by international communications carried on leased telephone-type circuits (either normal quality or special quality circuits) using a synchronous transmission procedure will be done with a specific mode of modulation, two- or multi-condition, and serial transmission (see Note 1). For synchronous data transmission in the general switched telephone network see Recommendation V.5.

2 It is recommended that for synchronous transmission the data signalling rates should be divided into two distinct classes to be known as "preferred" and "supplementary", both of which are included in the "permitted" data signalling rates.

a) *Preferred range of data signalling rates (bits per second)*

600 (see Note 2)	4800 (see Note 2)
1200 (see Note 2)	9600 (see Note 2)
2400 (see Note 2)	14 400 (see Note 4)

b) *Supplementary range of data signalling rates (bits per second)*

3000 (see Note 3)	7200 (see Note 2)
6000 (see Note 3)	12 000 (see Note 3, Note 4)

c) *Permitted range of data signalling rates (bits per second)*

The range is defined as 600 times "N" bits per second where $1 \leqslant N \leqslant 24$; N: a positive integer.

In determining the permitted range, the CCITT has in mind the need to restrict the number of data signalling rates (and hence modem design required), yet at the same time to allow the best use to be made of technical progress in both modem development and improvement in the telephone plant. It is considered that a geometric progression in standard rates provides the most satisfactory basis of development.

3 Data signalling rates should in no case deviate from the nominal value by more than ± 0.01%.

Note 1 – The application of parallel data transmission is a subject of other Recommendations.

Note 2 – Modems for use on leased telephone-type circuits at these data signalling rates; see Recommendations V.22, V.22 *bis*, V.23, V.26, V.26 *ter*, V.27, V.27 *bis*, V.29 and V.32.

Note 3 – It is recognized that there is a usage of these data signalling rates for the connection of DTEs to circuit switched public data networks. Addition of other data signalling rates for this purpose is under consideration.

Note 4 – Modems for use on leased telephone-type circuits at these signalling rates are under study.

Recommendation V.7

DEFINITIONS OF TERMS CONCERNING DATA COMMUNICATION OVER THE TELEPHONE NETWORK

(Geneva, 1980; amended at Malaga-Torremolinos, 1984)

Note – This Recommendation contains only new and amended definitions of terms concerning data communication over the telephone network which were elaborated by Study Group XVII since 1977 and approved by the VIIth and VIIIth Plenary Assemblies of the CCITT.

It should be noted that there exist a large number of relevant definitions in force which have been published in the *List of definitions of essential telecommunication terms*, Part I (including its two Supplements), *Green Book*, Volume VIII and *Orange Book*, Volume VIII.2.

1 effective data transfer rate

F: débit effectif du transfert des données

S: velocidad real de transferencia de datos

The average number of bits, characters, or blocks per unit time transferred from a data source to a data sink and accepted as valid. It is expressed in bits, characters, or blocks per second, minute, or hour.

2 error control

F: contrôle des erreurs

S: control de errores (protección contra errores)

That part of a protocol controlling the detection and possibly the correction of transmission errors.

3 data concentrator

F: concentrateur de données

S: concentrador de datos

Equipment that permits a common transmission medium to serve more *data sources* than there are data channels currently available within the transmission medium.

4 simple multipoint circuit

F: circuit multipoint simple

S: circuito multipunto simple

A multipoint circuit that does not contain more than two DCEs in series and that provides for centralized multipoint operation.

5 inband signalling

F: signalisation dans la bande

S: señalización dentro de banda

The exchange of control signals between interconnected DCEs using the DCE line signal band with which data in the forward channel are transmitted. The transmission of DTE data, if any, is disrupted.

6 out-of-band signalling

F: signalisation hors bande

S: señalización fuera de banda

The exchange of control signals between interconnected DCEs using signals other than those for the transmission of data in the forward channel. The transmission of DTE data is not disrupted.

7 coded inband signalling

F: signalisation dans la bande avec codage

S: señalización codificada dentro de banda

Inband signalling by which control signals are exchanged via data in the forward channel.

8 half-duplex operation

F: exploitation en semi-duplex

S: explotación (o funcionamiento) semidúplex

The exchange of data in either direction, one direction at a time.

9 interface rate

F: débit à l'interface

S: velocidad de interfaz

The transfer rate of the bit stream found on the physical interchange circuits.

10 information rate

F: débit d'information

S: velocidad de información

The transfer of information bits (the equivalent of the bit rate of circuit 103 or 104 on a V.24 interface).

11 control signalling rate

F: débit de la signalisation de commande

S: velocidad de señalización de control

The transfer rate of the encoded and multiplexed control signalling (the equivalent of V.24 and V.25 interchange circuits, except the data and timing circuits, insofar as required for an application, with the possibility of adding other signalling).

12 parallel automatic calling

F: appel automatique en parallèle

S: llamada automática paralelo; llamada automática en modo paralelo

A procedure by which a DTE, by use of the 200 series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in parallel form on interchange circuits 206 to 209.

13 serial automatic calling

F: appel automatique en série

S: llamada automática serie; llamada automática en modo serie

A procedure by which a DTE, by use of the 100 series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission from DTE to DCE, of each digit to be dialled, is achieved in serial form on interchange circuit 103.

SECTION 2

INTERFACES AND VOICE-BAND MODEMS

Recommendation V.10

ELECTRICAL CHARACTERISTICS FOR UNBALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR GENERAL USE WITH INTEGRATED CIRCUIT EQUIPMENT IN THE FIELD OF DATA COMMUNICATIONS[1)]

(Geneva, 1976; amended Geneva, 1980)

1 Introduction

This Recommendation deals with the electrical characteristics of the generator, receiver and interconnecting leads of an unbalanced interchange circuit employing a differential receiver.

In the context of this Recommendation an unbalanced interchange circuit is defined as consisting of an unbalanced generator connected to a receiver by an interconnecting lead and a common return lead.

Annexes and Appendices are provided to give guidance on a number of application aspects as follows:

Annex A Compatibility with other interfaces

Annex B Considerations for coaxial cable applications – V.10 COAXIAL

Appendix I Waveshaping

Appendix II Cable guidelines

Note – Generator and load devices meeting the electrical characteristics of this Recommendation need not operate over the entire data signalling rate range specified. They may be designed to operate over narrower ranges to satisfy specific requirements more economically, particularly at lower data signalling rates.

The interconnecting cable is normally not terminated, but the matter of terminating coaxial interconnecting cable is dealt with in Annex B. Where the interchange circuit incorporates the special provisions for coaxial applications with cable termination this shall be referred to as "complying with Recommendation V.10 (COAXIAL)".

Reference measurements are described which may be used to verify certain of the recommended parameters but it is a matter for individual manufacturers to decide what tests are necessary to ensure compliance with the Recommendation.

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1) This Recommendation is also designated as X.26 in the Series X Recommendations.

2 Field of application

The electrical characteristics specified in this Recommendation apply to interchange circuits operating with data signalling rates up to 100 kbit/s[2)], and are intended to be used primarily in Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE) implemented in integrated circuit technology.

This Recommendation is not intended to apply to equipment implemented in discrete component technology, for which the electrical characteristics covered by Recommendation V.28 are more appropriate.

Typical points of application are illustrated in Figure 1/V.10.

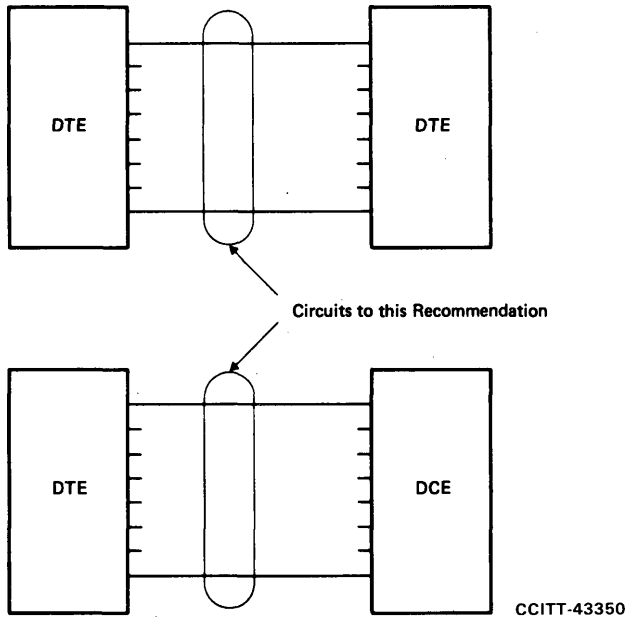

FIGURE 1/V.10

Typical applications of unbalanced interchange circuits

Whilst the unbalanced interchange circuit is primarily intended for use at the lower data signalling rates, its use should be avoided in the following cases:

1) where the interconnecting cable is too long for proper unbalanced circuit operation;

2) where extraneous noise sources make unbalanced circuit operation impossible;

3) where it is necessary to minimize interference with other signals.

Whilst a restriction on maximum cable length is not specified, guidelines are given with respect to conservative operating distance as a function of data signalling rates (see Appendix II).

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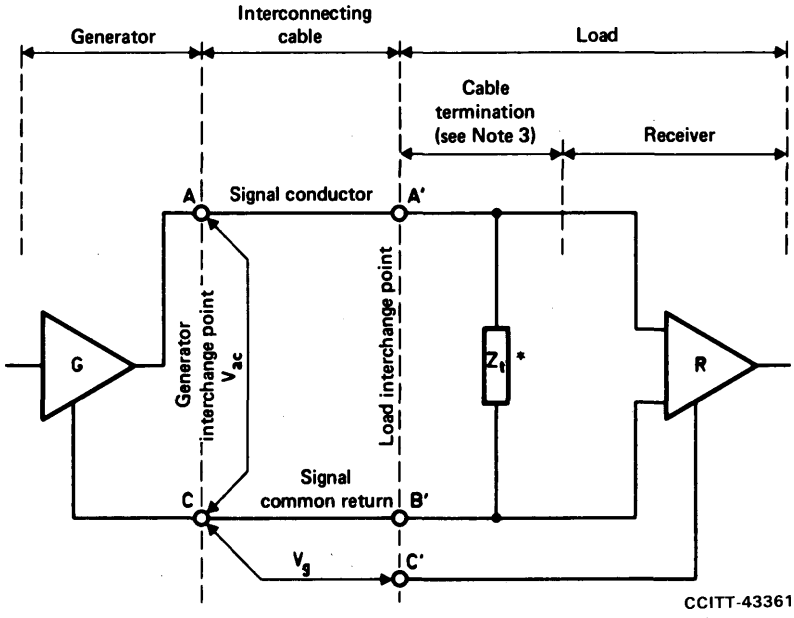
2) Signalling rates above the suggested 100 kbit/s may also be employed, but the maximum suggested operating distances should be shortened accordingly (see Figure II-1/V.10).

3 Symbolic representation of an interchange circuit (Figure 2/V.10)



V_{ac} = generator output voltage
V_g = ground potential difference
A = generator active interchange point
C = generator common return point
A' = load active interchange point
B' = load common return point
C' = receiver zero reference point

* This terminating resistor is only used with "V.10-COAXIAL", see Annex B

Note 1 – Two interchange points are shown. The output characteristics of the generator, excluding any interconnecting cable, are defined at the "generator interchange point". The elecrical characteristics to which the receiver must respond are defined at the "load interchange point".

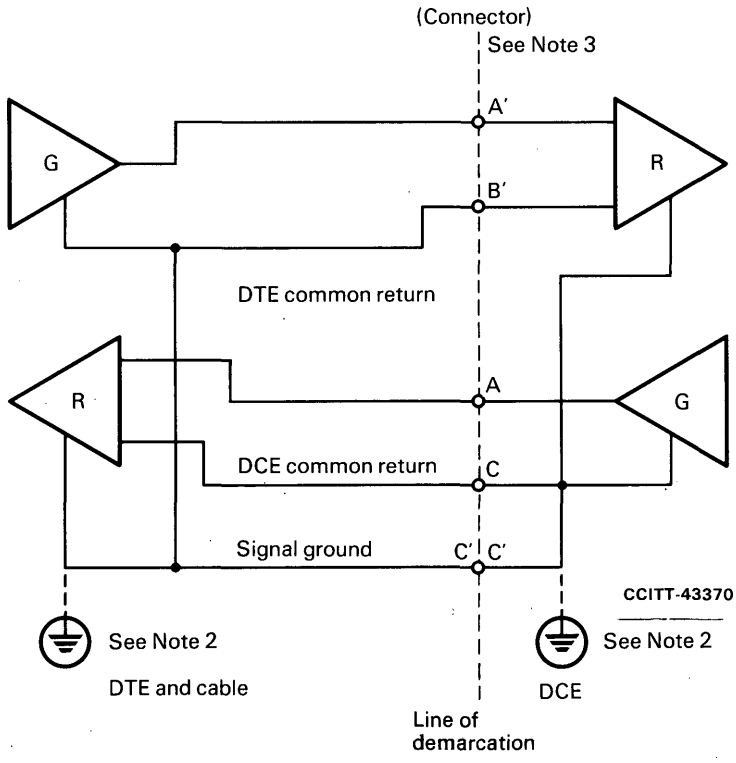
Note 2 – The connection of the signal common return is dealt with in § 10 below. Points C and C' may be connected to protective ground if required by national regulations.

Note 3 – The interconnecting cable is normally not terminated. The termination of coaxial interconnecting cable is dealt with in Annex B.

FIGURE 2/V.10

Symbolic representation of an unbalanced interchange circuit

For data transmission applications, it is commonly accepted that the interface cabling is provided by the DTE. This introduces the line of demarcation between the DTE plus cable and the DCE. This line is also called the interchange point and physically implemented in the form of a connector. The applications also require interchange circuits in both directions. This leads to an illustration as shown in Figure 3/V.10.



Note 1 – The zero volt reference interchange points C′ may be interconnected via the signal ground conductor.
Note 2 – Signal ground may be further connected to external protective ground if national regulations require.
Note 3 – The type of connector with this electrical characteristic specification depends on the application. ISO specifies, for data transmission over telephone type facilities, a 37-pin connector in ISO 4902.

FIGURE 3/V.10

Practical representation of the interface

4 Generator polarities and receiver significant levels

4.1 *Generator*

The signal conditions for the generator are specified in terms of the voltage between output points A and C shown in Figure 2/V.10.

When the signal condition 0 (space) for data circuits, or ON for control and timing circuits, is transmitted the output point A is positive with respect to point C. When the signal condition 1 (mark) for data circuits, or OFF for control and timing circuits, is transmitted the output point A is negative with respect to point C.

4.2 *Receiver*

The receiver significant levels are shown in Table 1/V.10, where $V_{A'}$ and $V_{B'}$ are respectively the voltage at points A′ and B′ relative to point C′.

TABLE 1/V.10

Receiver significant levels

	$V_{A'}-V_{B'} \leqslant -0.3$ V	$V_{A'}-V_{B'} \geqslant +0.3$ V
Data circuits	1	0
Control and timing circuits	OFF	ON

5 Generator

5.1 *Output impedance*

The total dynamic output impedance of the generator shall be equal to or less than 50 ohms.

5.2 *Static reference measurements*

The generator characteristics are specified in accordance with measurements illustrated in Figure 4/V.10 and described in §§ 5.2.1 to 5.2.4 below.

5.2.1 *Open circuit measurement* [Figure 4a)/V.10]

The open circuit voltage measurement is made with a 3900-ohm resistor connected between points A and C. In both binary states, the magnitude of the signal voltage (V_0) shall be equal to or greater than 4.0 volts but not greater than 6.0 volts.

5.2.2 *Test termination measurement* [Figure 4b)/V.10]

With a test load of 450 ohms connected between output points A and C, the magnitude of the output voltage (V_t) in both binary states shall be equal to or greater than 0.9 of the magnitude of V_0.

5.2.3 *Short-circuit measurement* [Figure 4c)/V.10]

With the output points A and C short-circuited the current (I_s) flowing through point A in both binary states shall not exceed 150 milliamperes.

5.2.4 *Power-off measurements* [Figure 4d)/V.10]

Under power-off condition, with a voltage ranging between +0.25 volt and −0.25 volt applied between the output point A and point C, the magnitude of the output leakage current (I_x) shall not exceed 100 micro-amperes.

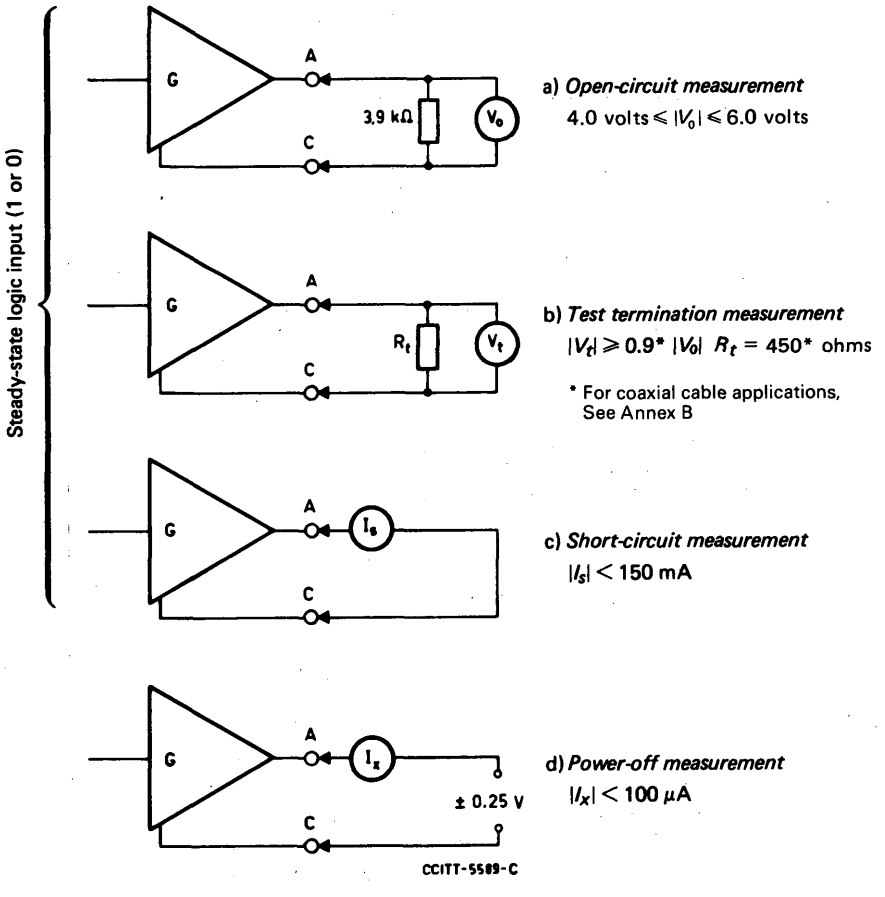


FIGURE 4/V.10

Generator parameter reference measurements

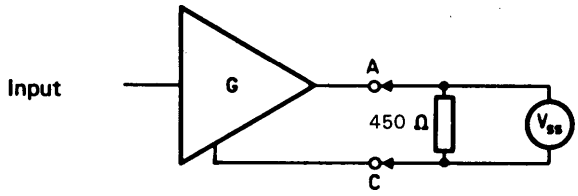
5.3 *Generator output rise-time measurement* (Figure 5/V.10)

5.3.1 *Waveform*

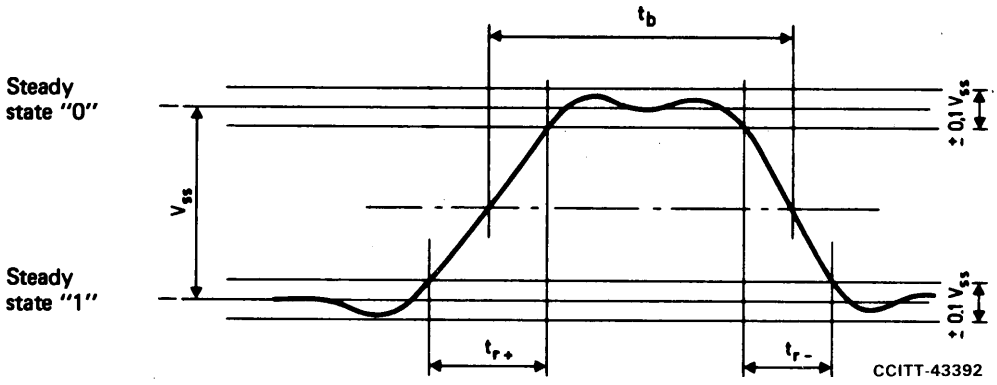
The measurement will be made with a resistor of 450 ohms connected between points A and C. A test signal, with a nominal signal element duration t_b and composed of alternate ones and zeros, shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 of V_{ss}.

5.3.2 *Waveshaping*

Waveshaping of the generator output signal shall be employed to control the level of interference (near-end crosstalk) which may be coupled to adjacent circuits in an interconnection. The rise time (t_r) of the output signal shall be controlled to ensure the signal reaches 0.9 V_{ss} between 0.1 and 0.3 of the duration of the unit interval (t_b) at signalling rates greater than 1 kbit/s, and between 100 and 300 microseconds at signalling rates of 1 kbit/s or less. The method of waveshaping is not specified but examples are given in Appendix I.



V_{ss} = Voltage difference between steady state signal conditions



t_b = nominal duration of the test signal element
$100\ \mu s \leq t_r \leq 300\ \mu s$ when $t_b \geq 1$ ms
$0.1\ t_b \leq t_r \leq 0.3\ t_b$ when $t_b < 1$ ms

FIGURE 5/V.10

Generator output rise-time measurement

6 Load

6.1 *Characteristics*

The load consists of a receiver (R) as shown in Figure 2/V.10. The electrical characteristics of the receiver are specified in terms of the measurements illustrated in Figures 6/V.10, 7/V.10 and 8/V.10 and described in §§ 6.2, 6.3 and 6.4 below. A circuit meeting these requirements results in a differential receiver having a high input impedance, a small input threshold transition region between −0.3 and +0.3 volts differential, and allowance for an internal bias voltage not to exceed 3 volts in magnitude.

The receiver is electrically identical to that specified for the balanced receiver in Recommendation V.11.

6.2 *Receiver input voltage – current measurements* (Figure 6/V.10)

With the voltage V_{ia} (or V_{ib}) ranging between -10 volts and $+10$ volts, while V_{ib} (or V_{ia}) is held at 0 volt, the resultant input current I_{ia} (or I_{ib}) shall remain within the shaded range shown in Figure 6/V.10. These measurements apply with the power supply of the receiver in both the power-on and power-off conditions.

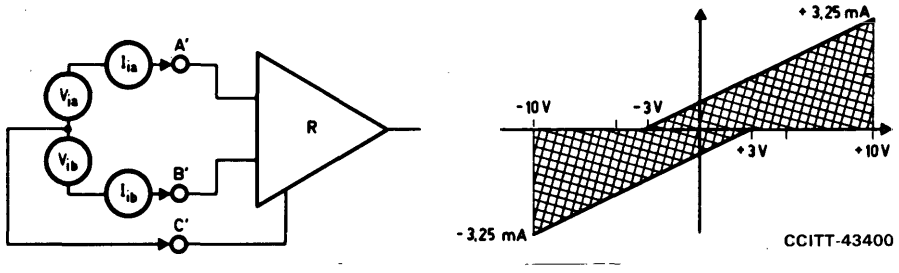
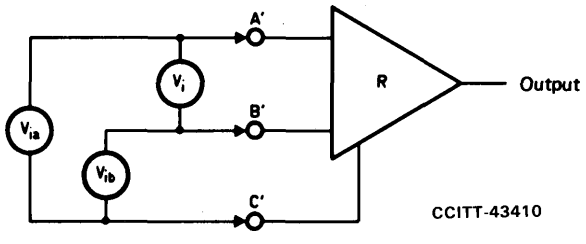


FIGURE 6/V.10

Receiver input voltage-current measurements

6.3 *DC input sensitivity measurements* (Figure 7/V.10)

Over the entire common-mode voltage (V_{cm}) range of $+7$ volts to -7 volts, the receiver shall not require a differential input voltage (V_i) of more than 300 millivolts to assume correctly the intended binary state. Reversing the polarity of V_i shall cause the receiver to assume the opposite binary state.



Applied voltages		Resulting input voltage	Output binary state	Purpose of measurement
V_{ia}	V_{ib}	V_i		
−12 V	0 V	−12 V	(not specified)	To ensure no damage to receiver inputs
0 V	−12 V	+12 V		
+12 V	0 V	+12 V		
0 V	+12 V	−12 V		
+10 V	+ 4 V	+ 6 V	0	To guarantee correct operation at V_i = 6 V (maintain correct logic state)
+ 4 V	+10 V	− 6 V	1	
−10 V	− 4 V	− 6 V	1	
− 4 V	−10 V	+ 6 V	0	
				300 mV threshold measurement
+0.30 V	0 V	+0.3 V	0	V_{cm} = 0 V
0 V	+0.30 V	−0.3 V	1	
+7.15 V	+6.85 V	+0.3 V	0	V_{cm} = +7 V
+6.85 V	+7.15 V	−0.3 V	1	
−7.15 V	−6.85 V	−0.3 V	1	V_{cm} = −7 V
−6.85 V	−7.15 V	+0.3 V	0	

FIGURE 7/V.10

Receiver input sensitivity measurement

The maximum voltage (signal plus common-mode) present between either receiver input and receiver ground shall not exceed 10 volts nor cause the receiver to malfunction. The receiver shall tolerate a maximum differential voltage of 12 volts applied across its input terminals without being damaged.

In the presence of the combinations of input voltages V_{ia} and V_{ib} specified in Figure 7/V.10, the receiver shall maintain the specified output binary state and shall not be damaged.

Note – Designers of equipment should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiving equipment; therefore, appropriate techniques should be implemented to prevent such behaviour. For example, adequate hysteresis may be incorporated in the receiver to prevent such conditions.

6.4 *Input balance test* (Figure 8/V.10)

The balance of the receiver input resistances and internal bias voltages shall be such that the receiver shall remain in the intended binary state under the conditions shown in Figure 8/V.10 and described as follows:

a) with $V_i = +720$ millivolts and V_{cm} varied between -7 and $+7$ volts;

b) with $V_i = -720$ millivolts and V_{cm} varied between -7 and $+7$ volts;

c) with $V_i = +300$ millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study);

d) with $V_i = -300$ millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study).

Note – The values of V_i are provisional and are the subject of further study.

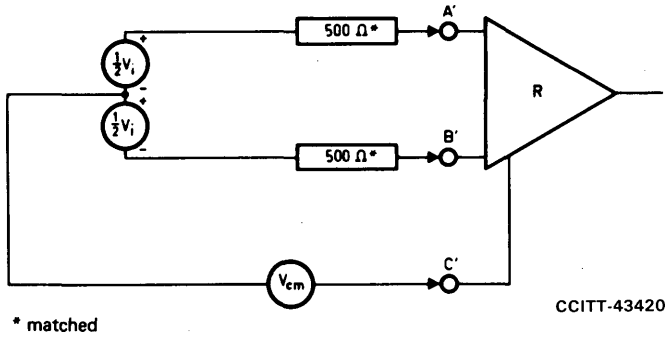


FIGURE 8/V.10

Receiver input balance test

7 Environmental constraints

In order to operate an unbalanced interchange circuit at data signalling rates ranging between 0 and 100 kbit/s, the following conditions apply:

1) The total peak differential noise measured between the points A′ and B′ at the load interchange point (with the generator interchange point connected to a 50-ohm resistor substituted for the generator) shall not exceed the expected amplitude of the received signal minus 0.3 volts (provisional value).

2) The worst-case combination of generator-receiver ground potential difference (V_g, Figure 2/V.10) and longitudinally induced peak random noise voltage measured between the receiver points A′ or B′ and C′ with the generator ends of the cable A and C joined together shall not exceed 4 volts.

8 Circuit protection

Unbalanced generator and load devices complying with this Recommendation shall not be damaged under the following conditions:

1) generator open circuit;

2) short-circuit between the conductors of the interconnecting cable;

3) short-circuit between the conductors and Point C or C′.

The above faults 2) and 3) might cause power dissipation in the interchange circuit devices to approach the maximum power dissipation that may be tolerated by a typical integrated circuit (IC) package. The user is therefore cautioned that where multiple generators and receivers are implemented in a single IC package, only one such fault per package might be tolerable at any one time without damage occurring.

The user is also cautioned that the generator and receiver devices complying with this Recommendation might be damaged by spurious voltages applied between their input or output points and points C and C′ (Figure 2/V.10). In those applications where the interconnecting cable may be inadvertently connected to other circuits or where it may be exposed to a severe electromagnetic environment, protection should be employed.

9 Category 1 and category 2 receivers

In order to provide flexibility in the choice of generator (V.10 or V.11), two categories of receiver are defined as follows:

Category 1 – Receivers shall have both input terminals A′ and B′ connected to individual terminals at the load interchange point, independent of all other receivers, as shown in Figure 9/V.10, and as applied in Annex A, Figure A-1/V.10.

Category 2 – Receivers shall have one terminal connection for each A′ input terminal at the load interchange point, and all B′ input terminals shall be connected together within the DCE or DTE and shall be brought to one common B′ input terminal as shown in Figure 10/V.10.

The specification of the category to be used in any application is part of the appropriate DCE Recommendation, using this type of interface electrical characteristics.

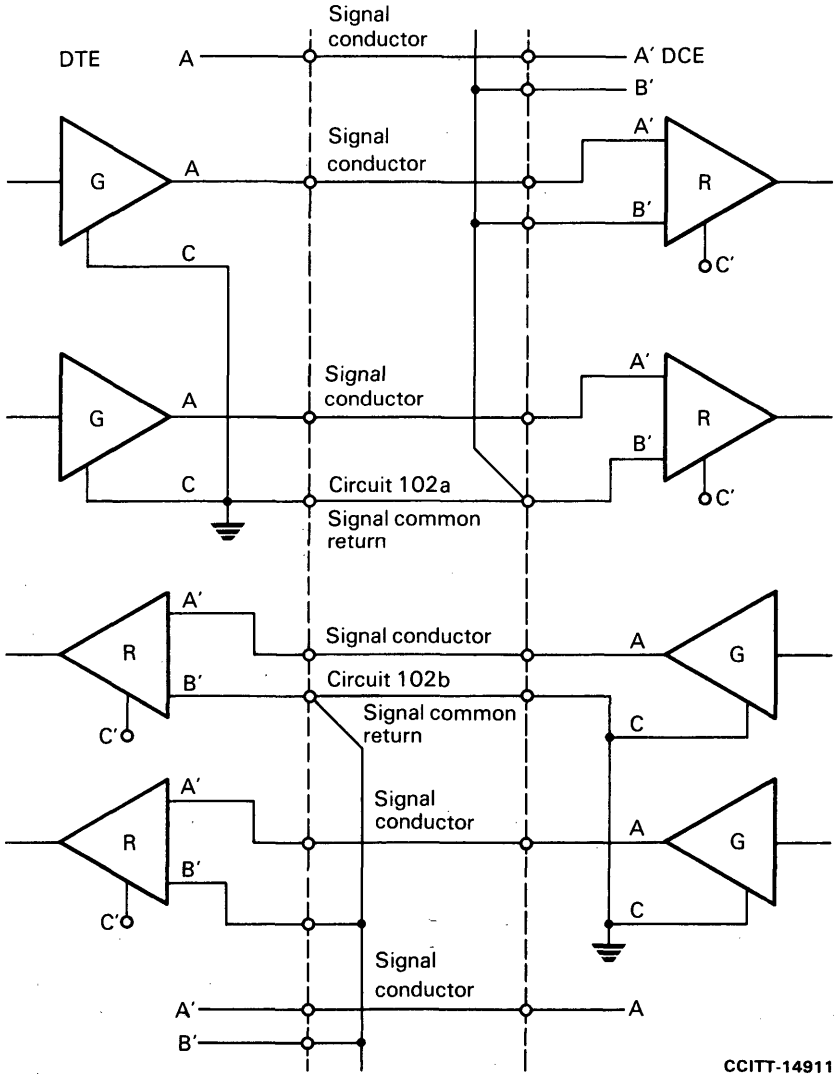


FIGURE 9/V.10

Interconnection of signal common return for category 1 receivers

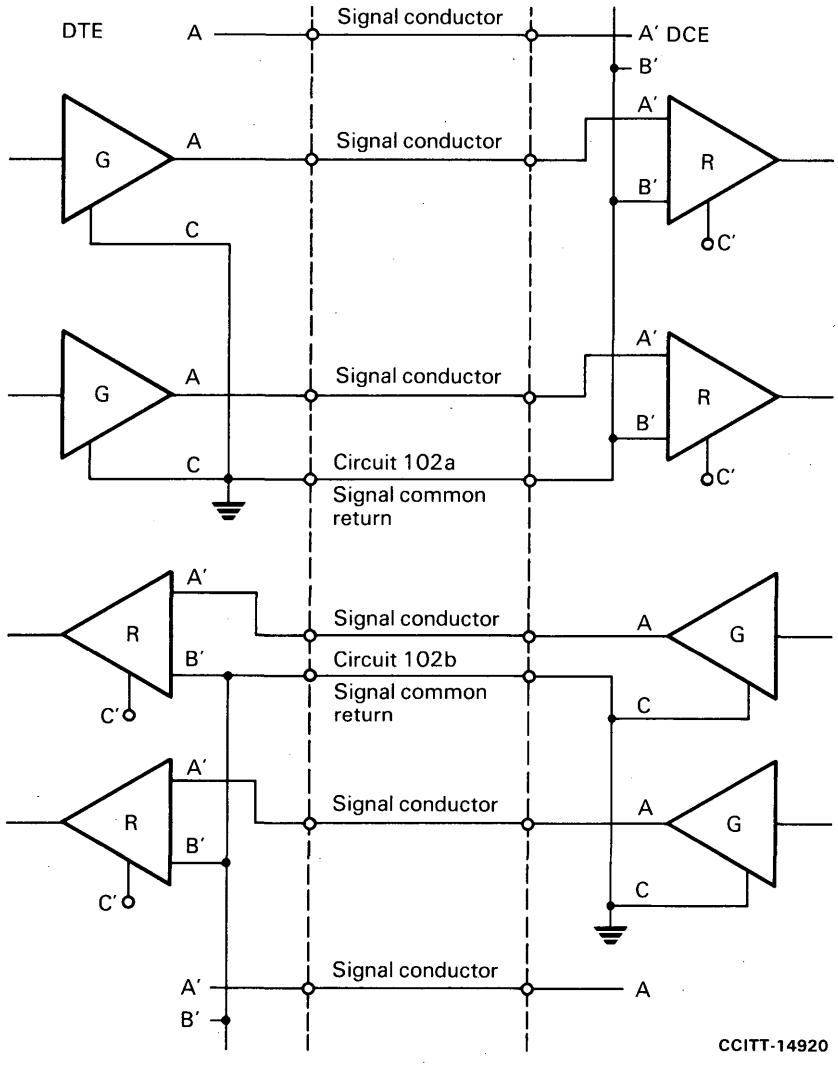


FIGURE 10/V.10

Interconnection of signal common return for category 2 receivers

10 Signal common return

The interconnection between the generator and the load interchange points in Figure 2/V.10 shall consist of a signal conductor for each circuit and one signal common return for each direction as shown in Figures 9/V.10 and 10/V.10. Signal common return may be implemented by more than one lead, where required to accomplish interworking, as described in § A.2 and as shown in Figure A-1/V.10.

To minimize the effects of ground potential difference V_g and longitudinally-coupled noise on the signal at the load interchange point, the signal common return shall be connected to ground only at the C terminal of the generator interchange point. For example, the B′ terminal of all the receivers in DTE which interconnect with unbalanced generators in DCE shall connect to signal common return circuit 102b, which is connected to ground only in DCE. Signal common return circuit 102a is used to interconnect terminal B′ of the receivers in DCE with the grounded terminal C of the unbalanced generators in DTE, as in Figures 9/V.10 and 10/V.10.

11 Detection of generator power-off or circuit failure

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator power-off condition;
2) receiver not interconnected with a generator;
3) open-circuited interconnecting cable;
4) short-circuited interconnecting cable;
5) input signal to the load remaining within the transition region (± 300 millivolts) for an abnormal period of time.

When detection of one or more fault conditions is required by specific applications, additional provisions are required in the load and the following items must be determined:

a) which interchange circuits require fault detection;
b) what faults must be detected;
c) what action must be taken when a fault is detected, e.g. which binary state must the receiver assume?

The interpretation of a fault condition by a receiver (or load) is application dependent. Each application may use a combination of the following classification:

Type 0 – No interpretation. A receiver or load does not have fault detection capability.

Type 1 – Data circuits assume a binary 1 state. Control and timing circuits assume an OFF condition.

Type 2 – Data circuits assume binary 0 state. Control and timing circuits assume an ON condition.

Type 3 – Special interpretation. The receiver or load provides a special indication for interpreting a fault condition. This special indication requires further study.

The association of the circuit failure detection to particular interchange circuits in accordance with the above types is a matter of the functional and procedural characteristics specification of the interface.

The interchange circuits monitoring circuit fault conditions in the general telephone network interfaces are indicated in Recommendation V.24.

The interchange circuits monitoring circuit fault conditions in data network interfaces are indicated in Recommendation X.24 [1].

The receiver fault detection type required is specified in the relevant DCE Recommendations.

12 Measurements at the physical interchange point

The following information provides guidance for measurements when maintenance persons examine the interface for proper operation at the interchange point.

12.1 *Listing of essential measurements*

- open-circuit measurements;
- test-termination measurement;
- short-circuit measurement;
- generator output rise time;
- d.c. input sensitivity measurements.

12.2 *Listing of optional measurements*

- the total generator resistance between points A and C shall be equal to or less than 50 ohms;
- power-off measurements;
- receiver input voltage espace-espace current measurements;

– input balance test;

– check of the required circuit fault detection (§ 11).

The parameters defined in this Recommendation are not necessarily measurable at the physical interchange point. This is for further study.

ANNEX A

(to Recommendation V.10)

Compatibility with other interfaces

A.1 *Compatibility of Recommendation V.10 and Recommendation V.11 interchange circuits in the same interface*

The electrical characteristics of Recommendation V.10 are designed to allow the use of balanced (see Recommendation V.11) and unbalanced circuits within the same interface. For example, the balanced circuits may be used for data and timing whilst the unbalanced circuits may be used for associated control circuit functions.

A.2 *Recommendation V.10 interworking with Recommendation V.11*

The differential receiver specifications of Recommendations V.10 and V.11 are electrically identical. It is therefore possible to interconnect an equipment using Recommendation V.10 receivers and generators on one side of the interface with an equipment using Recommendation V.11 generators and receivers on the other side of the interface. Such interconnection would result in interchange circuits according to Recommendation V.11 in one direction and interchange circuits according to Recommendation V.10 in the other direction. Where such interworking is contemplated, the following technical considerations must be taken into account.

A.2.1 Interconnecting cable lengths are limited by performance of the circuits working to the Recommendation V.10 side of the interface.

A.2.2 The optional cable termination resistance (Z_t), if implemented, in the equipment using Recommendation V.11 must be removed.

A.2.3 V.10-type receivers shall be of category 1 (see Figure A-1/V.10).

A.3 *Recommendation V.10 interworking with Recommendation V.28*

The unbalanced electrical characteristics of Recommendation V.10 have also been designed to permit limited interworking, under certain conditions, with generators and receivers to Recommendation V.28. Where such interworking is contemplated, the following technical limitations must be considered:

A.3.1 Separate DTE and DCE signal return paths will not be available at the Recommendation V.28 side of the interface.

A.3.2 Data signalling-rate limitations according to Recommendation V.28 shall apply.

A.3.3 Interconnecting cable lengths are limited by the Recommendation V.28 performance restrictions.

A.3.4 Probability of satisfactory operation will be enhanced by providing the maximum generator voltage possible on the Recommendation V.10 side of the interface within the limitations stipulated in Recommendation V.10.

A.3.5 Whilst Recommendation V.28 type generators may use potentials in excess of 12 volts, many existing equipments are designed to operate with power supplies of 12 volts or less. Where this is the case, no further protection of Recommendation V.10 receivers is required; however, in the general case, protection against excessively high voltages from Recommendation V.28 generators must be provided for the Recommendation V.10 receivers.

A.3.6 Power-off detectors in Recommendation V.28 receivers may not necessarily work with Recommendation V.10 generators.

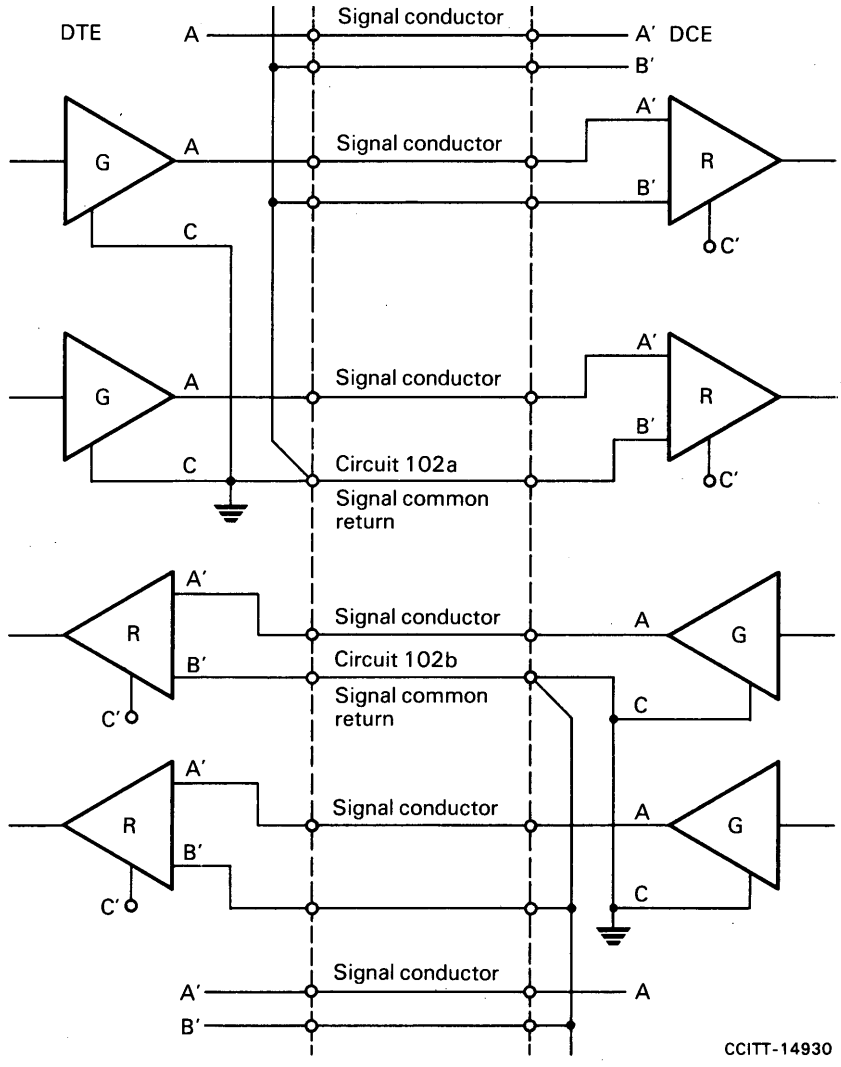


FIGURE A-1/V.10

Interconnection of signal common return by more than one conductor in order to accomplish interoperation of V.10 generators with category 1 receivers

ANNEX B

(to Recommendation V.10)

Considerations for coaxial cable applications – V.10 COAXIAL[3)]

It is recognized that where coaxial cables are used for interconnecting purposes it may be desirable to include a terminating resistance at the receiver end of the cable. This is considered to be a special case for which special generator characteristics are required. The terminating resistance shall in no case be less than 50 ohms and the reference measurements under §§ 5.2.2 and 5.3 shall be made with a 50-ohm test termination. Use of this special application will require appropriate agreement with the proper authority.

3) All the electrical characteristics specified in Recommendation V.10 other than those set down in this Annex are applicable to the coaxial cable case with a cable case with a cable termination.

The alternative set of electrical characteristics applied in the coaxial cable case is the following:

5.2.2 *bis* *Test termination measurement* [Figure 4b)/V.10]

With a test load (R_t) of 50 ohms connected between output points A and C, the magnitude of the output voltage (V_t) shall be equal to or greater than 0.5 of the magnitude of V_0.

5.3.1 *bis* *Waveform* (Figure 5/V.10)

The measurement will be made with a resistor of 50 ohms connected between points A and C. A test signal, with a nominal signal element duration t_b and composed of alternate ones and zeros, shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 of V_{ss}.

5.3.2 *bis* *Waveshaping*

Waveshaping is not normally required for coaxial cable applications.

10 *bis* *Signal common return*

In applications where coaxial cables are used, the screen of the coaxial cable shall be connected to ground only at point C at the generator end as shown in Figure B-1/V.10.

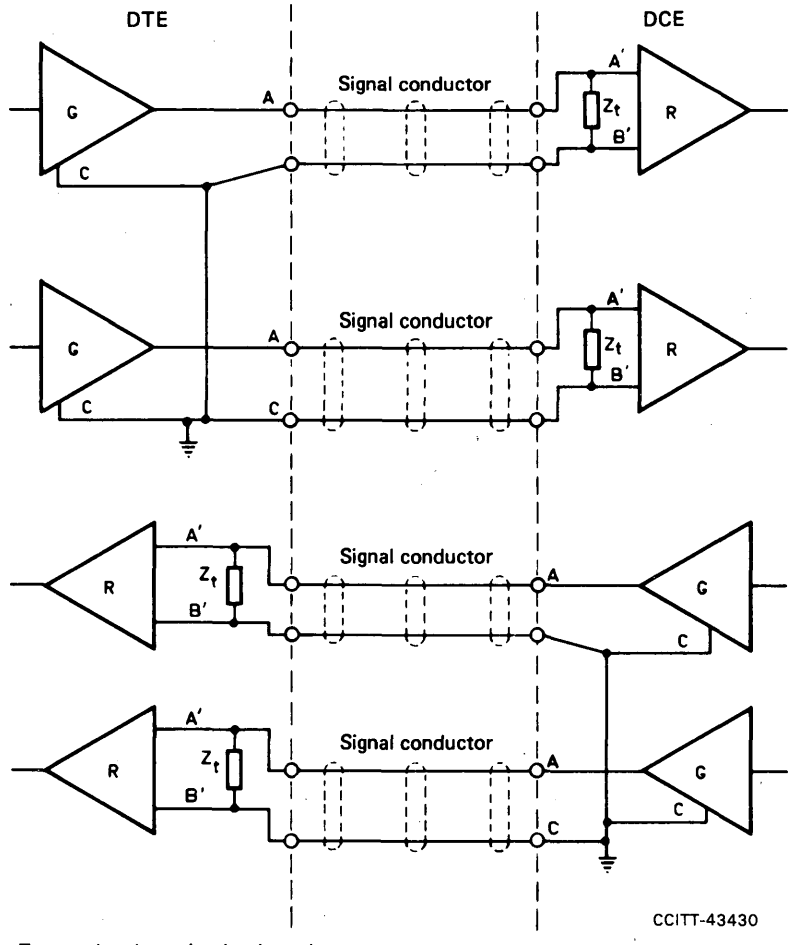


FIGURE B-1/V.10

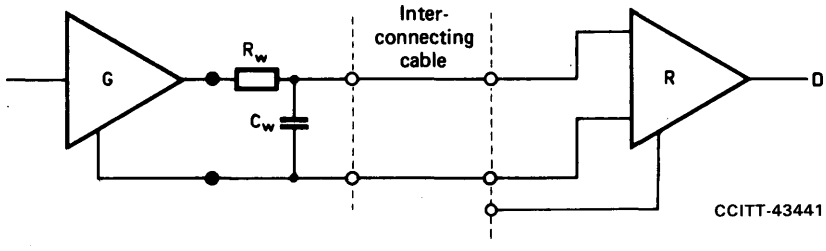
Interconnection with coaxial cable

APPENDIX I

(to Recommendation V.10)

Waveshaping

The required waveshaping may be accomplished either by providing a slew-rate control in the generator or by inserting an RC filter at the generator interchange point. A combination of these methods may also be employed. An example of the RC filter method is shown in Figure I-1/V.10. Typical values of capacitance C_w, with the value of R_w selected so that $R_w + R_d$ is approximately 50 ohms, are given for typical cable with an interconductor shunt capacitance of approximately 0.05 microfarads per kilometre.



R_d = generator internal resistance
R_w = 50 ohms – R_d

C_w (microfarads)	Data signalling rate range (kbit/s)
1.0	0 - 2.5
0.47	2.5 - 5.0
0.22	5.0 - 10
0.1	10 - 25
0.047	25 - 50
0.022	50 - 100

FIGURE I-1/V.10

Example method of waveshaping

APPENDIX II

(to Recommendation V.10)

Cable Guidelines

No electrical characteristics of the interconnection cable are specified in this Recommendation. However, guidance is given herein concerning operational constraints imposed by cable length and near-end crosstalk.

The maximum operating distance for the unbalanced interchange circuit is primarily a function of the amount of interference (near-end crosstalk) coupled to adjacent circuits in the equipment interconnection. Additionally the unbalanced circuit is susceptible to exposure to differential noise resulting from any imbalance between the signal conductor and signal common return at the load interchange point. Increasing the physical separation and interconnection cable length between the generator and load interchange points might increase the exposure to common-mode noise and the degree of near-end crosstalk. Accordingly, users are advised to restrict the cable length to a minimum consistent with the generator-load physical separation requirements.

The curve of cable length versus data signalling rate given in Figure II-1/V.10 may be used as a conservative guide. This curve is based upon calculations and empirical data using twisted-pair telephone cable with a shunt capacitance of 0.052 microfarads per kilometre, a 50-ohm source impedance, a 6-volt source signal and maximum near-end crosstalk of 1-volt peak. The rise time (t_r) of the source signal at signalling rates below 1000 bit/s is 100 microseconds and above 1000 bit/s is 0.1 t_b (see Figure 5/V.10).

The user is cautioned that the curve given in Figure II-1/V.10 does not account for common-mode noise or near-end crosstalk levels beyond the limits specified, that may be introduced between the generator and load by exceptionally long cables. On the other hand operation within the signalling-rate and distance bounds of Figure II-1/V.10 will usually ensure that the distortion of the signal appearing at the receiver input will be acceptable. Many applications, however, can tolerate greater levels of signal distortion, and correspondingly greater cable lengths can be employed. The generation of near-end crosstalk can be reduced by increasing the amount of waveshaping employed.

Experience has shown that in most practical cases the operating distance at the lower data signalling rates may be extended to several kilometres.

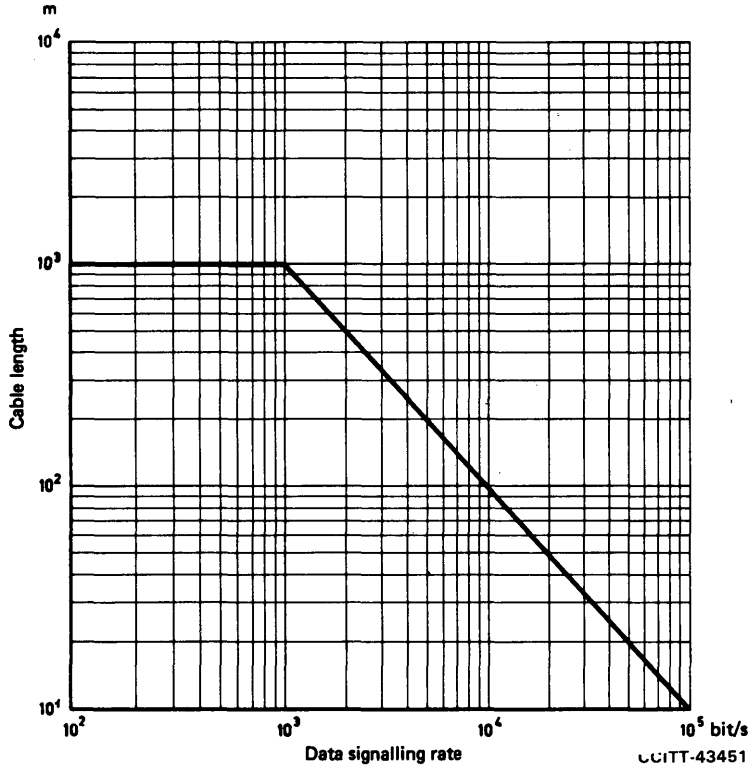


FIGURE II-1/V.10

Data signalling rate vs cable length for unbalanced interchange circuit

Reference

[1] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks*, Vol. VIII, Rec. X.24.

ELECTRICAL CHARACTERISTICS FOR BALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR GENERAL USE WITH INTEGRATED CIRCUIT EQUIPMENT IN THE FIELD OF DATA COMMUNICATIONS[1)]

(Geneva, 1976; amended Geneva, 1980)

1 Introduction

This Recommendation deals with the electrical characteristics of the generator, receiver and interconnecting leads of a differential signalling (balanced) interchange circuit with an optional d.c. offset voltage.

The balanced generator and load components are designed to cause minimum mutual interference with adjacent balanced or unbalanced interchange circuits (see Recommendation V.10) provided that waveshaping is employed on the unbalanced circuits.

In the context of this Recommendation, a balanced interchange circuit is defined as consisting of a balanced generator connected by a balanced interconnecting pair to a balanced receiver. For a balanced generator the algebraic sum of both the outlet potentials, with respect to earth, shall be constant for all signals transmitted; the impedances of the outlets with respect to earth shall be equal. The degree of balance and other essential parameters of the interconnecting pair is a matter for further study.

An Annex and two Appendices are provided to give guidance on a number of application aspects as follows:

Annex A Compatibility with other interfaces.

Appendix I Cable and termination.

Appendix II Multipoint operation.

Note – Generator and load devices meeting the electrical characteristics of this Recommendation need not operate over the entire data signalling rate range specified. They may be designed to operate over narrower ranges to satisfy requirements more economically, particularly at lower data signalling rates.

Reference measurements are described which may be used to verify certain of the recommended parameters but it is a matter for individual manufacturers to decide what tests are necessary to ensure compliance with the Recommendation.

2 Field of application

The electrical characteristics specified in this Recommendation apply to interchange circuits operating with data signalling rates up to 10 Mbit/s, and are intended to be used primarily in Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE) implemented in integrated-circuit technology.

This Recommendation is not intended to apply to equipment implemented in discrete component technology, for which the electrical characteristics covered by Recommendation V.28 are more appropriate.

Typical points of application are illustrated in Figure 1/V.11.

Whilst the balanced interchange circuit is primarily intended for use at the higher data signalling rates, its use at the lower rates may be necessary in the following cases:

1) where the interconnecting cable is too long for proper unbalanced circuit operation;
2) where extraneous noise sources make unbalanced circuit operation impossible;
3) where it is necessary to minimize interference with other signals.

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1) This Recommendation is also designated as X.27 in the Series X Recommendations.

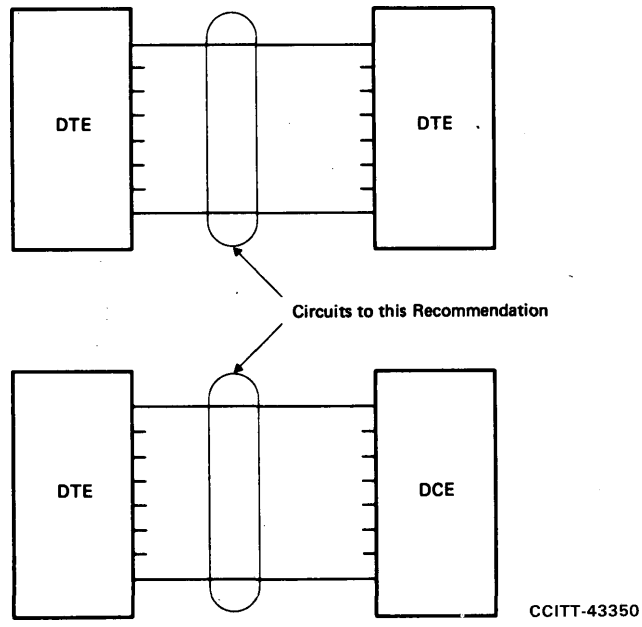
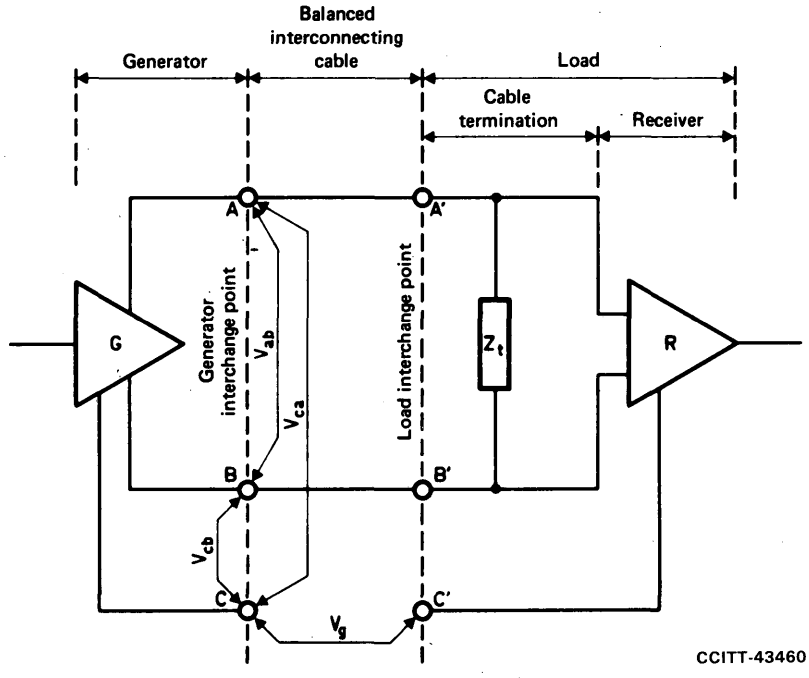


FIGURE 1/V.11

Typical applications of balanced interchange circuits

3 Symbolic representation of interchange circuit (Figure 2/V.11)



V_{ab} = generator output voltage between points A and B
V_{ca} = generator voltage between points C and A
V_{cb} = generator voltage between points C and B
Z_t = cable termination impedance
V_g = ground potential difference
A, B and A', B' = interchange points
C, C' = zero volt reference interchange points

Note 1 – Two interchange points are shown. The output characteristics of the generator, excluding any interconnecting cable, are defined at the "generator interchange point". The electrical characteristics to which the receiver must respond are defined at the "load interchange point".

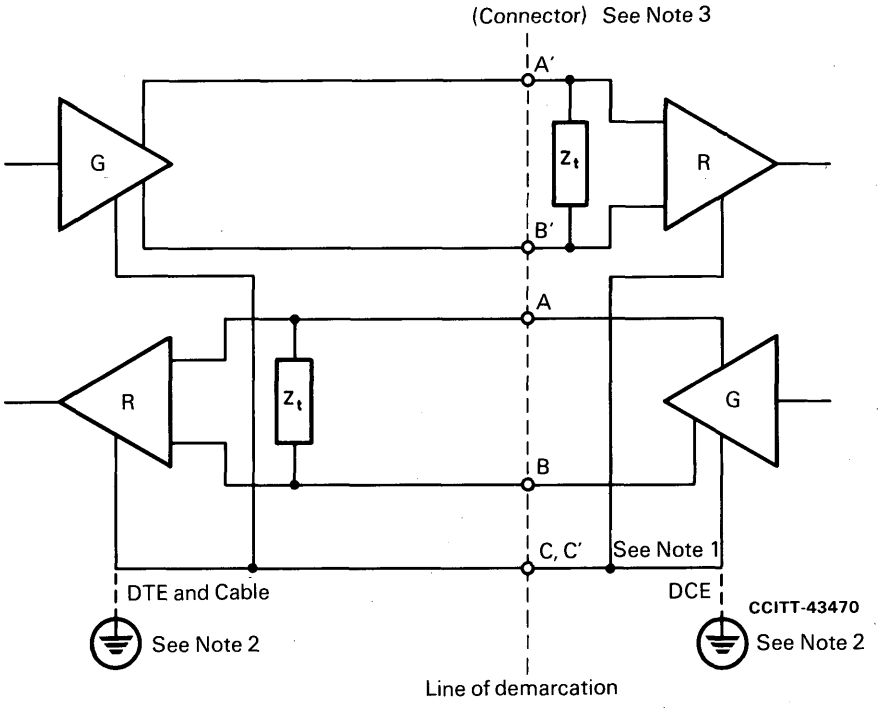
Note 2 – Points C and C' may be interconnected and further connected to protective ground if required by national regulations.

FIGURE 2/V.11

Symbolic representation of a balanced interchange circuit

The equipment at both sides of the interface may implement generators as well as receivers in any combination. Consequently, the symbolic representation of the interchange circuit, Figure 2/V.11 above, defines a generator interchange point as well as a load interchange point.

For data transmission applications, it is commonly accepted that the interface cabling will be provided by the DTE. This introduces the line of demarcation between the DTE plus cable and the DCE. This line is also called the interchange point and physically implemented in the form of a connector. The applications also require interchange circuits in both directions. This leads to an illustration as shown in Figure 3/V.11.



Note 1 – The zero volt reference interchange point C, C′ may be interconnected via the signal ground conductor.

Note 2 – Signal ground may be further connected to external protective ground if national regulations require.

Note 3 – The type of connector with this electrical characteristic specification depends on the application. ISO specifies, for data transmission over telephone type facilities, a 37-pin connector in ISO 4902 and, for data transmission over data network facilities, a 15-pin connector in ISO 4903.

FIGURE 3/V.11

Practical representation of the interface

4 Generator polarities and receiver significant levels

4.1 *Generator*

The signal conditions for the generator are specified in terms of the voltage between output points A and B shown in Figure 2/V.11.

When the signal condition 0 (space) for data circuits or ON for control and timing circuits is transmitted, the output point A is positive with respect to point B. When the signal condition 1 (mark) for data circuits or OFF for control and timing circuits is transmitted, the output point A is negative with respect to point B.

4.2 *Receiver*

The receiver differential significant levels are shown in Table 1/V.11, where $V_{A'}$ and $V_{B'}$ are respectively the voltages at points A′ and B′ relative to point C′.

TABLE 1/V.11

Receiver differential significant levels

	$V_{A'}-V_{B'} \leqslant -0.3$ V	$V_{A'}-V_{B'} \geqslant +0.3$ V
Data circuits	1	0
Control and timing circuits	OFF	ON

5 Generator

5.1 *Resistance and d.c. offset voltage*

5.1.1 The total generator resistance between points A and B shall be equal to or less than 100 ohms and adequately balanced with respect to point C. (It is left for further study as to the degree of balance required both statically and dynamically.)

5.1.2 The magnitude of the generator d.c. offset voltage (see § 5.2.2 below) shall not exceed 3 V under all operating conditions.

5.2 *Static reference measurements*

The generator characteristics are specified in accordance with measurements illustrated in Figure 4/V.11 and described in §§ 5.2.1 to 5.2.4 below.

5.2.1 *Open-circuit measurement* [Figure 4a)/V.11]

The open-circuit voltage measurement is made with a 3900-ohm resistor connected between points A and B. In both binary states, the magnitude of the differential voltage (V_0) shall not be more than 6.0 volts, nor shall the magnitude of V_{0a} and V_{0b} be more than 6.0 volts.

5.2.2 *Test-termination measurement* [Figure 4b)/V.11]

With a test load of two resistors, each 50 ohms, connected in series between the output points A and B, the differential voltage (V_t) shall not be less than 2.0 volts or 50% of the magnitude of V_0, whichever is greater. For the opposite binary state the polarity of V_t shall be reversed ($-V_t$). The difference in the magnitudes of V_t and $-V_t$ shall be less than 0.4 volt. The magnitude of the generator offset voltage V_{0s} measured between the centre of the test load and point C shall not be greater than 3.0 volts. The magnitude of the difference in the values of V_{0s} for one binary state and the opposite binary state shall be less than 0.4 volt.

Note – Under some conditions this measurement does not determine the degree of balance of the internal generator impedances to point C. It is left for further study whether additional measurements are necessary to ensure adequate balance in generator output impedances.

5.2.3 *Short-circuit measurement* [Figure 4c)/V.11]

With the output points A and B short-circuited to point C, the current flowing through each of the output points A or B in both binary states shall not exceed 150 milliamperes.

5.2.4 *Power-off measurements* [Figure 4d)/V.11]

Under power-off condition with voltages ranging between +0.25 volt and −0.25 volt applied between each output point and point C, as indicated in Figure 4d)/V.11, the magnitude of the output leakage currents (I_{xa} and I_{xb}) shall not exceed 100 microamperes.

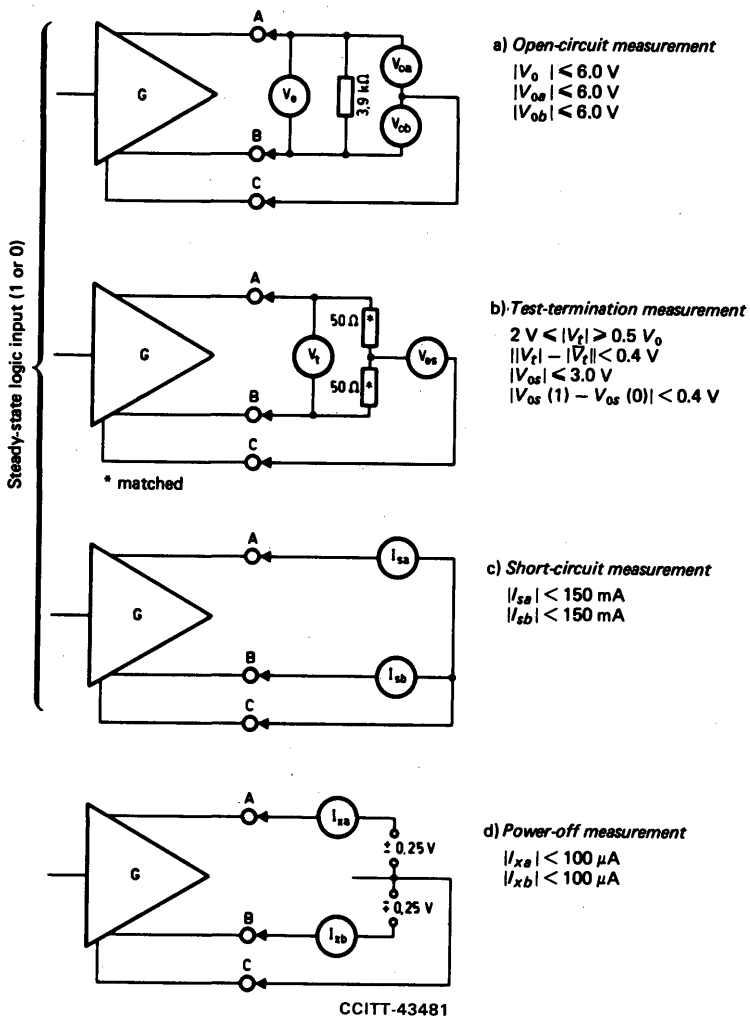


FIGURE 4/V.11

Generator-parameter reference measurements

5.3 *Dynamic voltage balance and rise time measurements* (Figure 5/V.11)

With the measurement configuration shown in Figure 5/V.11, a test signal with a nominal signal element duration t_b and composed of alternate ones and zeros, shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 V_{ss} within 0.1 of t_b or 20 nanoseconds, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{ss} from the steady state value.

The resultant voltage due to imbalance (V_E) shall not exceed 0.4 V peak-to-peak (the value of V_E is provisional and is subject to further study to determine whether voltage peaks of very short duration should be included).

6 Load

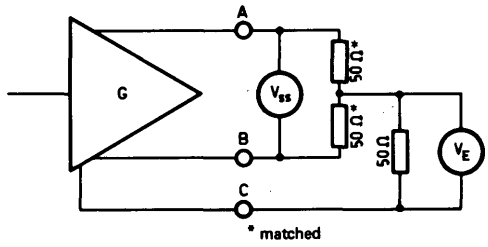
6.1 *Characteristics*

The load consists of a receiver (R) and an optional cable termination resistance (Z_t) as shown in Figure 2/V.11. The electrical characteristics of the receiver are specified in terms of the measurements illustrated in Figures 6/V.11, 7/V.11 and 8/V.11 and described in §§ 6.2, 6.3 and 6.4 below. A circuit meeting these requirements results in a differential receiver having a high input impedance, a small input threshold transition region between −0.3 and +0.3 volts differential, and allowance for an internal bias voltage not to exceed 3 volts in magnitude.

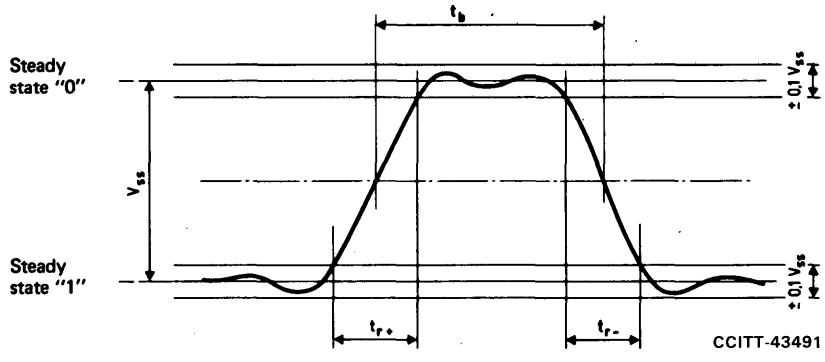
The receiver is electrically identical to that specified for the unbalanced receiver in Recommendation V.10.

6.2 *Receiver input voltage – current measurements* (Figure 6/V.11)

With the voltage V_{ia} (or V_{ib}) ranging between -10 volts and $+10$ volts, while V_{ib} (or V_{ia}) is held at 0 volt, the resultant input current I_{ia} (or I_{ib}) shall remain within the shaded range shown in Figure 6/V.11. These measurements apply with the power supply of the receiver in both the power-on and power-off conditions.



V_E < 0.4 V peak-to-peak (provisional)
V_{ss} = Voltage difference between steady-state signal conditions



t_b = nominal duration of the test signal element
for $t_b \geq 200$ ns, $t_r \leq 0.1\ t_b$
for $t_b < 200$ ns, $t_r \leq 20$ ns

FIGURE 5/V.11

Generator dynamic balance and rise-time measurements

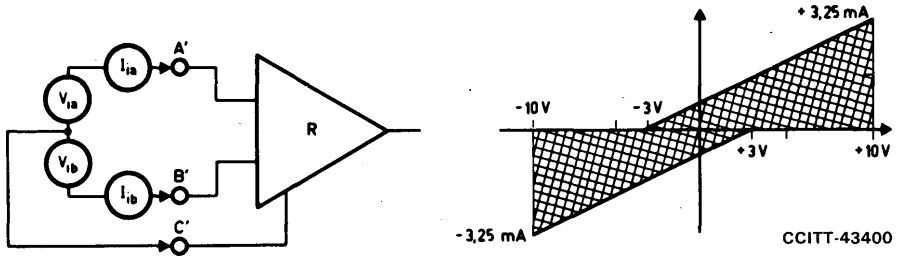


FIGURE 6/V.11

Receiver input voltage-current measurements

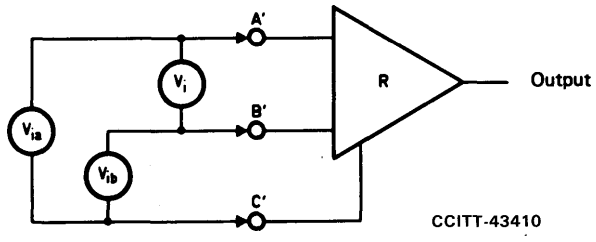
6.3 *D.c. input sensitivity measurements* (Figure 7/V.11)

Over the entire common mode voltage (V_{cm}) range of +7 volts to −7 volts, the receiver shall not require a differential input voltage (V_i) of more than 300 millivolts to assume correctly the intended binary state. Reversing the polarity of V_i shall cause the receiver to assume the opposite binary state.

The maximum voltage (signal plus common mode) present between either receiver input and receiver ground shall not exceed 10 volts nor cause the receiver to malfunction. The receiver shall tolerate a maximum differential voltage of 12 volts applied across its input terminals without being damaged.

In the presence of the combination of input voltages V_{ia} and V_{ib} specified in Figure 7/V.11, the receiver shall maintain the specified output binary state and shall not be damaged.

Note – Designers of equipment should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiving equipment; therefore, appropriate techniques should be implemented to prevent such behaviour. For example, adequate hysteresis may be incorporated in the receiver to prevent such conditions.



Applied voltages		Resulting input voltage	Output binary state	Purpose of measurement
V_{ia}	V_{ib}	V_i		
−12 V	0 V	−12 V	(not specified)	To ensure no damage to receiver inputs
0 V	−12 V	+12 V		
+12 V	0 V	+12 V		
0 V	+12 V	−12 V		
+10 V	+ 4 V	+ 6 V	0	To guarantee correct operation at V_i = 6 V (maintain correct logic state)
+ 4 V	+10 V	− 6 V	1	
−10 V	− 4 V	− 6 V	1	
− 4 V	−10 V	+ 6 V	0	
				300 mV threshold measurement
+0.30 V	0 V	+0.3 V	0	V_{cm} = 0 V
0 V	+0.30 V	−0.3 V	1	
+7.15 V	+6.85 V	+0.3 V	0	V_{cm} = +7 V
+6.85 V	+7.15 V	−0.3 V	1	
−7.15 V	−6.85 V	−0.3 V	1	V_{cm} = −7 V
−6.85 V	−7.15 V	+0.3 V	0	

FIGURE 7/V.11

Receiver input sensitivity measurement

6.4 *Input balance test* (Figure 8/V.11)

The balance of the receiver input resistance and internal bias voltages shall be such that the receiver shall remain in the intended binary state under the conditions shown in Figure 8/V.11 and described as follows:

a) with $V_i = +720$ millivolts and V_{cm} varied between -7 and $+7$ volts;

b) with $V_i = -720$ millivolts and V_{cm} varied between -7 and $+7$ volts;

c) with $V_i = +300$ millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study);

d) with $V_i = -300$ millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study).

Note – The values of V_i are provisional and are the subject of further study.

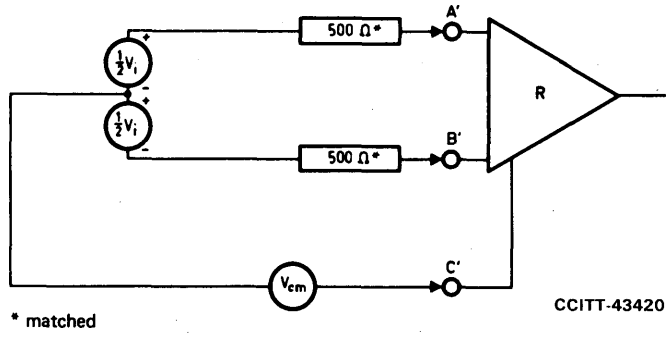


FIGURE 8/V.11

Receiver input balance test

6.5 *Terminator*

The use of a cable terminating impedance (Z_t) is optional depending upon the specific environment in which the interchange circuit is employed (see Appendix I). In no case shall the total load resistance be less than 100 ohms.

7 Environmental constraints

In order to operate a balanced interchange circuit at data signalling rates ranging between 0 and 10 Mbit/s, the following conditions apply:

1) For each interchange circuit a balanced interconnecting pair is required.

2) Each interchange circuit must be appropriately terminated (see Appendix I).

3) The total common-mode voltage at the receiver must be less than 7 volts peak. This value is provisional and is subject to further study.

The common mode voltage at the receiver is the worst case combination of:

a) generator-receiver ground-potential difference (V_g, Figure 2/V.11);

b) longitudinally induced random noise voltage measured between the receiver points A′ or B′ and C′ with the generator ends of the cable A, B and C joined together; and

c) generator d.c. offset voltage, if any.

Unless the generator is of a type which generates no d.c. offset voltage, the sum of a) and b) above, which is the element of the common mode voltage due to the environment of the interchange circuit, must be less than 4 volts peak.

8 Circuit protection

Balanced generator and load devices complying with this Recommendation shall not be damaged under the following conditions:

1) generator open circuit;

2) short-circuit between the conductors of the interconnecting cable;

3) short-circuit between either or both conductors and point C or C′.

The above faults 2) and 3) might cause power dissipation in the interchange circuit devices to approach the maximum power dissipation that may be tolerable by a typical integrated circuit (IC) package. The user is therefore cautioned that where multiple generators and receivers are implemented in a single IC package, only one such fault per package might be tolerable at any one time without damage occurring.

The user is also cautioned that the generator and receiver devices complying with this Recommendation might be damaged by spurious voltages applied between their input or output points and points C or C′ (Figure 2/V.11). In those applications where the interconnecting cable may be inadvertently connected to other circuits, or where it may be exposed to a severe electromagnetic environment, protection should be employed.

9 Detection of generator power-off or circuit failure

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator power-off condition;

2) receiver not interconnected with a generator;

3) open-circuited interconnecting cable;

4) short-circuited interconnecting cable;

5) input signal to the load remaining within the transition region (± 300 millivolts) for an abnormal period of time.

When detection of one or more fault conditions is required by specific applications, additional provisions are required in the load and the following items must be determined:

a) which interchange circuits require fault detection;

b) what faults must be detected;

c) what action must be taken when a fault is detected, e.g. which binary state must the receiver assume?

The interpretation of a fault condition by a receiver (or load) is application dependent. Each application may use a combination of the following classification:

Type 0 – No interpretation. A receiver or load does not have fault detection capability.

Type 1 – Data circuits assume a binary 1 state. Control and timing circuits assume an OFF condition.

Type 2 – Data circuits assume binary 0 state. Control and timing circuits assume an ON condition.

Type 3 – Special interpretation. The receiver or load provides a special indication for interpreting a fault condition. This special indication requires further study.

The association of the circuit failure detection to particular interchange circuits in accordance with the above types is a matter of the functional and procedural characteristics specification of the interface.

The interchange circuits monitoring circuit fault conditions in the general telephone network interfaces are indicated in Recommendation V.24.

The interchange circuits monitoring circuit fault conditions in public data network interfaces are indicated in Recommendation X.24 [1].

The receiver fault detection type required is specified in the relevant DCE Recommendations.

10 Measurements at the physical interchange point

The following information provides guidance for measurements when maintenance persons examine the interface for proper operation at the interchange point.

10.1 *Listing of essential measurements*

- the magnitude of the generator d.c. offset voltage under all operating conditions;
- open-circuit measurements;
- test-termination measurement;
- short-circuit measurement;
- dynamic voltage balance and rise time;
- d.c. input sensitivity measurements.

10.2 *Listing of optional measurements*

- The total generator resistance between points A and B shall be equal to or less than 100 ohms and adequately balanced with respect to point C. (It is left for further study as to the degree of balance required both statically and dynamically);
- power-off measurements;
- receiver input voltage-current measurements;
- input balance test;
- check of the required circuit fault detection (§ 9).

The parameters defined in this Recommendation are not necessarily measurable at the physical interchange point. This is for further study.

ANNEX A

(to Recommendation V.11)

Compatibility with other interfaces

A.1 *Compatibility of Recommendation V.10 and Recommendation V.11 interchange circuits in the same interface*

The electrical characteristics of Recommendation V.11 are designed to allow the use of unbalanced (see Recommendation V.10) and balanced circuits within the same interface. For example, the balanced circuits may be used for data and timing whilst the unbalanced circuits may be used for associated control circuit functions.

A.2 *Recommendation V.11 interworking with Recommendation V.10*

The differential receiver specifications of Recommendations V.10 and V.11 are electrically identical. It is therefore possible to interconnect an equipment using Recommendation V.10 receivers and generators on one side of the interface with an equipment using Recommendation V.11 generators and receivers on the other side of the interface. Such interconnection would result in the interchange circuits according to Recommendation V.11 in one direction and interchange circuits according to Recommendation V.10 in the other direction. Where such interworking is contemplated, the following technical considerations must be taken into account.

A.2.1 Interconnecting cable lengths are limited by performance of the circuits working to the Recommendation V.10 side of the interface.

A.2.2 The optional cable termination resistance (Z_t), if implemented, in the equipment using Recommendation V.11 must be removed.

A.2.3 V.10-type receivers shall be of category 1.

A.3 *Recommendation V.11 interworking with Recommendation V.35*

Equipment having interchange circuits according to Recommendation V.11 is not capable of interworking with equipment having balanced interchange circuits according to the electrical characteristics of Recommendation V.35.

APPENDIX I

(to Recommendation V.11)

Cable and termination

No electrical characteristics of the interconnecting cable are specified in this Recommendation. Guidance is given herein concerning operational constraints imposed by the length, balance and terminating resistance of the cable.

I.1 *Cable*

Over the length of the cable, the two conductors should have essentially the same values of:

1) capacitance to ground;
2) longitudinal resistance and inductance;
3) coupling to adjacent cables and circuits.

I.2 *Cable length*

The maximum permissible length of cable separating the generator and the load in a point-to-point application is a function of the data signalling rate. It is further influenced by the tolerable signal distortion and the environmental constraints such as ground potential difference and longitudinal noise. Increasing the distance between generator and load might increase the exposure to ground potential difference.

As an illustration of the above conditions, the curves of cable length versus data signalling rate in Figure I-1/V.11 may be used for guidance.

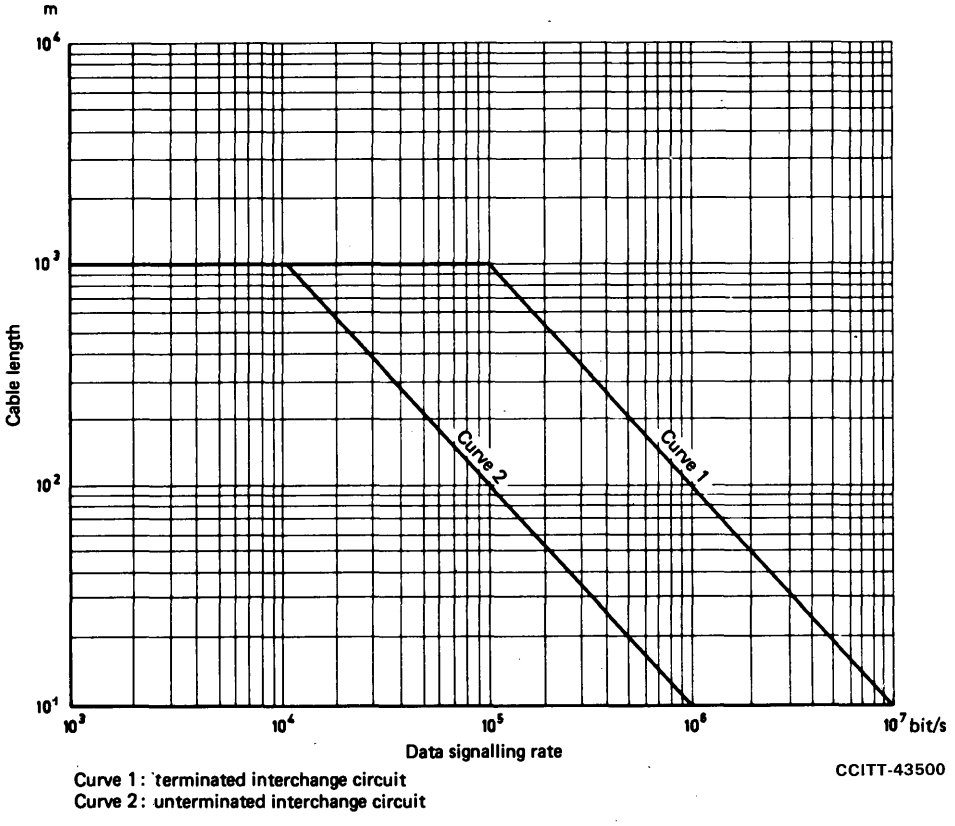


FIGURE I-1/V.11

Data signalling rate vs cable length for balanced interchange circuit

These curves are based upon empirical data using twisted pair telephone cable (0.51-mm wire diameter) both unterminated and terminated in a 100-ohm resistive load. The cable length restrictions shown by the curves are based upon the following assumed signal quality requirements at the load:

1) signal rise and fall time equal to, or less than, one-half the duration of the signal element;

2) a maximum voltage loss between generator and load of 6 dB.

At the higher data signalling rates (see Figure I-1/V.11) the sloping portion of the curves shows the cable length limitation established by the assumed signal rise and fall time requirements. The cable length has been arbitrarily limited to 1000 metres by the assumed maximum allowable loss of 6 dB.

These curves assume that the environmental limits specified in this Recommendation have been achieved. At the higher data signalling rates these conditions are more difficult to attain due to cable imperfections and common-mode noise. Operation within the data signalling rate and distance bounds of Figure I-1/V.11 will usually ensure that distortion of the signal appearing at the receiver input will be acceptable. Many applications, however, can tolerate much greater levels of signal distortion and in these cases correspondingly greater cable lengths may be employed.

Experience has shown that in many practical cases the operating distance at lower signalling rates may extend to several kilometres.

For synchronous transmission where the data and signal element timing are transmitted in opposite directions, the phase relationship between the two may need to be adjusted to ensure conformity with the relevant requirements of signal quality at the interchange point.

I.3 *Cable termination*

The use of a cable termination resistance (Z_t) is optional and dependent on the specific application. At the higher data signalling rates (above 200 kbit/s) or at any data signalling rate where the cable propagation delay is of the order of half the signal element duration a termination should be used to preserve the signal rise time and minimize reflections. The terminating impedance should match as closely as possible the cable characteristic impedance in the signal spectrum.

Generally, a resistance in the range of 100 to 150 ohms will be satisfactory, the higher values leading to lower power dissipation.

At the lower data signalling rates, where distortion and rise-time are not critical, it may be desirable to omit the termination in order to minimize power dissipation in the generator.

APPENDIX II

(to Recommendation V.11)

Multipoint operation

It is considered that further study is required before parameters for this application can be defined and this Appendix, giving provisional figures, is intended as a guideline for this study, which is intended to lead to the development of a new Recommendation.

II.1 *General*

The point-to-point interchange circuit arrangement of one generator and one load might be expanded to a multipoint arrangement by adding generators, receivers or both, at interchange points along the interconnecting cable.

Only one generator at a given time would present its differential voltage at its interchange point. All other generators would be isolated by an appropriate control, and assume the high impedance state defined below. All receivers would be continuously in an operating condition.

Terminating impedances may be necessary at more than one point of the multipoint interconnection, but their specification is not included in this Recommendation. The combined load impedance presented to any active generator by other generators, receivers, cable and terminators must not be less than 100 ohms.

The operation of a multipoint arrangement must not be perturbed by any of its components when they are either in a high impedance state or a power-off state[2]. The generators and receivers must tolerate without damage the transmitted signals with their maximum amplitude within the specified limits.

Generators on the same multipoint line must have the same nominal d.c. offset voltage in order to operate correctly. However, generators with different d.c. offsets could be used on the same line provided that these differences were compensated at the common reference point.

The controlling data transfer protocol must insure that only one generator is active at one instant in time in order to avoid contention. In the contention case the generator devices can be damaged if three or more are active simultaneously.

II.2 *High impedance state*

II.2.1 *Static measurements*

When in the high impedance state and with test loads of 50 ohms connected between each generator output point and point C, the magnitude of the voltage V_h measured between points A and B shall not exceed 4 mV whatever the logical condition of the generator input data lead (Figure II-1/V.11).

When the generator is in the high impedance state, with voltages ranging between -6 V and $+6$ V applied between each output point and point C, as indicated in Figure II-2/V.11, the magnitude of the output leakage currents I_{xa} and I_{xb} shall not exceed 150 μA.

The same situation applies in the power-off condition.

II.2.2 *Dynamic measurements*

During transitions of the generator output between the low impedance state and the high impedance state, the differential signal measured across a 100-ohm test load connected between the generator points A and B shall be such that the amplitude changes from 10% to 90% of the steady state voltage in less than 10 μs.

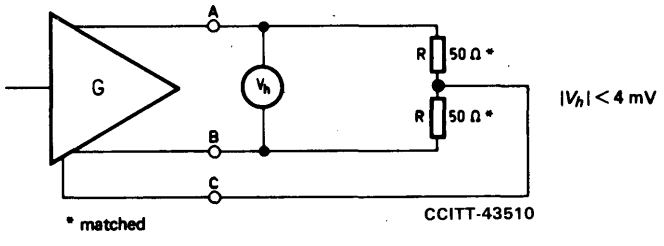


FIGURE II-1/V.11

High impedance state static measurement

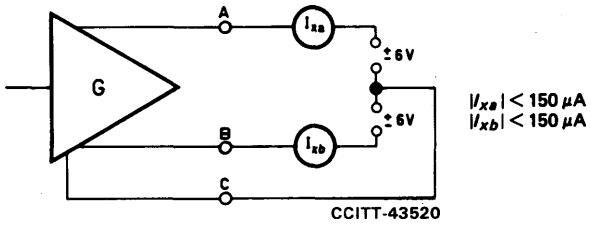


FIGURE II-2/V.11

Generator output leakage current measurement

Reference

[1] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks*, Vol. VIII, Rec. X.24.

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[2] In the power-off state of any device it is assumed that the supply collapses to zero and is replaced by a very low impedance or short circuit.

USE OF ACOUSTIC COUPLING FOR DATA TRANSMISSION

(Geneva, 1972; amended at Malaga-Torremolinos, 1984)

Note – Acoustic coupling is a technique used to couple the output of a modem to an analogue telecommunication facility using acoustic energy/power between the device and a telephone instrument. As such, it provides for minimum complexity of attachment as well as excellent galvanic isolation. However, the technique does limit the data signalling rates used and does limit the functionality which can be provided by the associated modem. Since this arrangement will generally be used to communicate with a permanently installed V Series modem at a remote station, the characteristics of the modem will, accordingly, comply with requirements defined elsewhere in these Series V Recommendations, e.g., V.21 or V.23. As far as functionality permits, interfaces with the associated DTE will be as defined in those Recommendations. Because of operator intervention required in manipulating the telephone handset, automatic calling and automatic answering are not normally considered part of the functionality of an acoustically coupled modem. However, an acoustically coupled modem can call a remote station which has automatic answering capability and can observe the protocol defined in Recommendation V.25, § 6, "Manual data station calling automatic answering data station" as modified herein.

The CCITT,

considering

that there is a wide variety of telephone instruments in existence and that the acoustic path involved in the use of any coupling device cannot be accurately prescribed for all cases, and hence it will be difficult to ensure satisfactory transmission in all situations,

recommends

1 that acoustic coupling of data transmission equipment via telephone instruments to the telephone transmission network should not be used for permanent installations.

It is, however, recognized that there may be a need for a means to provide temporary connection of portable data transmission equipment to the network in circumstances where it may not be possible to obtain convenient access to the subscriber's line terminals.

The use of acoustic coupling for temporary communications is subject to the agreement of the Administration in charge of the telephone network to which the equipment will be connected.

If an Administration decides to permit acoustic coupling for temporary data transmission stations, the acoustic coupling equipment conforms to the following:

1) The maximum power output of the subscriber's equipment to the line shall not exceed 1 mW at any frequency.

   The mean permitted telephone line signal power shall not exceed -13 dBm0.

2) If p is the signal power in the frequency band 0-4 kHz, the signal power outside this band shall not exceed the following values when integrated over any period of approximately 3 seconds:

   p – 20 dB in the band 4 to 8 kHz,

   p – 40 dB in the band 8 to 12 kHz,

   p – 60 dB in each 4-kHz band above 12 kHz.

3) The frequencies emitted by the transducer shall be such as not to interfere with national and international telephone signalling systems and pilot signals involved in the telephone connection envisaged.

4) Adequate protection shall be provided in the transducer to avoid causing any dangerous electric potential and currents to the telephone system.

5) It shall not be possible to cause acoustic shock to telephone users under any normal condition or when the acoustic coupler develops any single fault.

6) The mechanical arrangements of the transducer shall not cause mechanical damage to the telephone instrument.

7) In addition to the contents of this Recommendation, the regulations of the national Administration must also be complied with.

2 that acoustically coupled equipment be compatible with "hard-wired counterparts" at the remote location to the extent that:

1) The characteristics of the equivalent V Series (V.21, V.23, etc.) modem line signals are complied with (otherwise communication will be impossible).

2) An equivalent V.24 interface is provided to the DTE, with the following exceptions:
   - circuit 108 is power ON indicator only, and cannot be used to control the connection of the modem to the line;
   - circuit 125 is inoperative; only manual answering can be accomplished.

3) Acoustically coupled modem equipment designed to operate with remote modems:
   - which have automatic answering capability, and
   - which are specifically dedicated and are adapted (by means of optionally extended answer tone duration) to working with acoustically coupled calling stations

   shall operate in the mode prescribed in Recommendation V.25, § 6 where placement of the telephone instrument handset on the acoustic coupler by the operator is tantamount to depressing a data button, as specified in § 6.

   These modems shall also comply with the response time requirements of circuits 106 and 109 as specified in the appropriate modem Recommendation.

Recommendation V.16

MEDICAL ANALOGUE DATA TRANSMISSION MODEMS

(Geneva, 1976)

The CCITT,

considering that:

(a) computer-aided automatic ECG (electro-cardiogram) interpretation is being made available by special diagnostic centres to general practitioners and hospitals at remote places and suitable transmission equipment is necessary for this reason;

(b) such a service can be implemented to advantage in a special data collection system using simple remote stations and a high-quality central unit;

(c) for such applications particularly suitable and compatible transmission facilities are necessary which must not interfere with other telephone services;

(d) analogue as well as digitalized transmission of the analogue data (e.g. ECG records) are in principle possible;

(e) in most cases, however, on-line transmission with analogue transmission methods can be implemented more easily and economically;

(f) in practice, analogue transmission generally promises a sufficient degree of quality;

(g) in cases of emergency and monitoring of implanted pacemakers, very simple, acoustically coupled equipment may be of great assistance to the persons concerned;

unanimously declares the following view:

1 Analogue transmission of medical analogue data, e.g. ECGs, should be permitted in the public telephone network. Reliable, sufficiently interference-free transmission cannot be taken for granted on every connection or route. Therefore, it is necessary to test the connections under consideration before such a service is definitely introduced.

2 This service requires two basically different transmission devices (modems):

1) transmission equipment for simultaneous transmission of three ECG signals on a telephone channel from a remote station to the central station, preferably for direct galvanic coupling to the telephone channel;

2) transmission equipment, preferably for emergency use and for monitoring of implanted pacemakers, to simultaneously transmit only one ECG signal from a remote station to a central station with acoustic or galvanic coupling to a telephone channel.

The ECG station usually consists of an ECG recorder, including separating amplifier, data input/output device and the modem specified in this Recommendation (see Figure 1/V.16).

The central station usually comprises the central modem specified herein and the interpretation system for ECGs (e.g. a computer programmed for ECG interpretation).

This Recommendation covers the modems, the desired transmission characteristics of the ECG transmission channel as well as the necessary interchange circuits and the method of transmitting the digital data associated with the ECG (e.g. patients' identification codes, control signals in both transmission directions and the interpretation record).

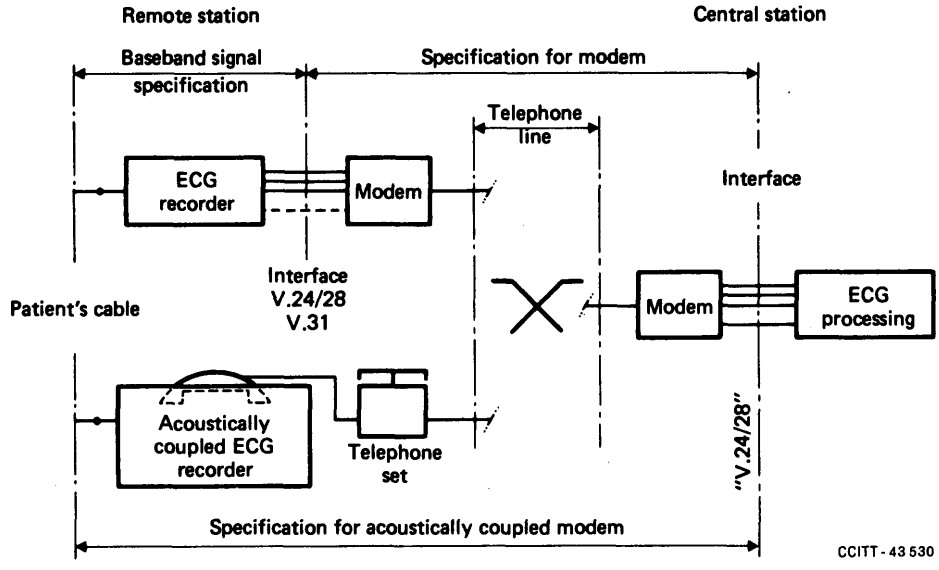

FIGURE 1/V.16

Example of analogue transmission of medical analogue data

3 Modems for simultaneous analogue transmission of three ECG records

3.1 *Basic characteristics of the analogue channels*

The equipment specified below is mainly intended for operation with direct galvanic coupling to telephone lines.

3.1.1 *Baseband signal*

Baseband signal requirements at the modem input:

– number of simultaneously transmitted ECG records	3
– frequency response of the separating amplifier	flat
– signal-to-noise ratio with 10 Hz square wave signals ± 1 V	⩾ 50 dB (unweighted)
– full scale limit (see Note 1)	± 2.5 V
– linearity deviation of an ECG channel related to full scale and the optimum straight line	1%
– permissible group delay distortion of the input signal at the modulator input (including channel filter in the baseband)	from 3 to 60 Hz $\Delta\tau \leqslant 2$ ms (outside this range, see Figure 2/V.16)
– spectrum: if a.c. coupling is applied, a time constant of $\tau = 3.2$ s, corresponding to a lower cut-off frequency of 0.5 Hz, should be used.	
– baseband pre-emphasis (see Note 2) (between separating amplifier and modem)	rise of 6 dB/octave; cut-off frequency: 15 Hz

Note 1 – Existing instruments (ECG recorders, etc.) are designed for ± 2.5 V full scale. If, however, the International Electrotechnical Commission specifies ± 1 V or ± 1.25 V as the full scale limit, this value should be adopted. The slope of the modulator characteristic (see § 3.1.2 below) must then be adjusted accordingly.

Note 2 – This value will require further study if, at a later date, amplitude compandors are used to improve the signal-to-noise ratio.

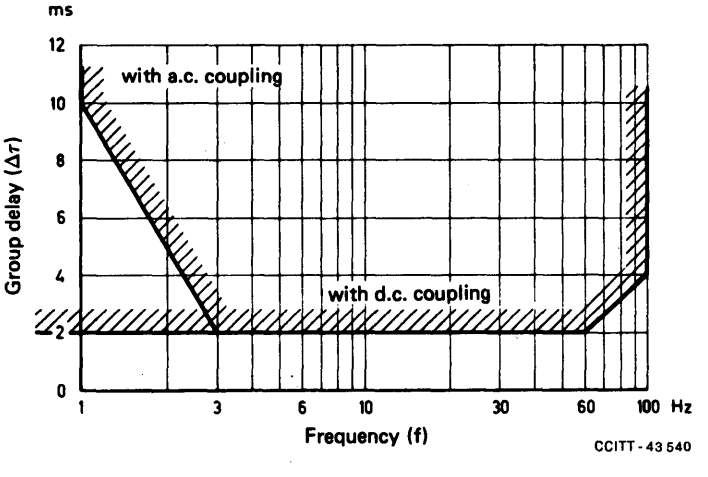

FIGURE 2/V.16

Permissible group-delay distortion in the baseband

3.1.2 *Requirements for the transmission equipment (modems)*

The modem should be capable of transmitting baseband signals with a bandwidth of up to approximately 100 Hz. The transmission equipment (modems) should not deteriorate the performance of the baseband signal as specified under § 3.1.1 above by more than 10%. The exact value of the admissible deterioration needs further study.

Since the centre channel of the transmission equipment will in future be used for digital transmission of ECG-associated digital data and other biological data, it must be capable of transmitting d.c. components. The same should apply to the other channels.

– *line signals* for transmitting the ECG:	signals as specified under § 3.1.1 above.
– modulation method:	frequency modulation
– subcarrier frequencies f_n and associated maximum transmission levels p_n:	
f_1 = 950 Hz ± 6 Hz f_2 = 1400 Hz ± 15 Hz (see Note 1) f_3 = 2100 Hz ± 15 Hz	p_1 = 7 dB p_2 = 5 dB p_3 = 3 dB lower than the resulting level p_0 as specified in Recommendation V.2
– resulting maximum level:	p_0 as specified in Recommendation V.2
– simultaneous transmission of all three subcarriers is mandatory, if subcarriers f_1 and/or f_3 are used.	
– maximum frequency deviation per channel in the case of linear operation:	Δf = ± 100 Hz
– slope of the modulator characteristic (subcarrier deviation sensitivity):	40 Hz/V (see Note 2)
– a positive signal should cause a rise in the subcarrier frequency	
– FM channel bandwidth (3 dB points):	⩽ 350 Hz
– resulting level accepted by receiver (upper threshold-level):	– 6 dBm to –43 dBm
– lower threshold level:	–46 dBm

Note 1 – This frequency selection makes allowance for the following boundary conditions:

a) best possible decoupling between the three ECG channels. Nonlinear distortion may cause a small degree of cross-talk;

b) CCITT standardized subcarrier frequencies (2100 Hz and 1400 Hz) should be used as far as possible;

c) no interference to existing CCITT signalling systems by simulation of switching signals.

Some of the existing ECG transmission systems use subcarrier frequencies f_1 = 1075 Hz, f_2 = 1935 Hz, f_3 = 2365 Hz. Due to the relatively slow modulation by ECGs, the modulated subcarrier frequencies f_2 and f_3 may simulate signals of CCITT Signalling Systems No. 2 and No. 4. This would cause interference to the ordinary telephone service. Where this kind of interference is not to be expected, use of the subcarrier frequencies concerned should be allowed over a transition period covering two CCITT study periods. Thereafter, the aforementioned frequencies (950 Hz, 1400 Hz and 2100 Hz) only should be used in the interest of mutual compatibility of the ECG transmission systems from different suppliers.

Note 2 – This value should be changed to 100 Hz/V, or 80 Hz/V if the full-scale voltage of ± 1 V or ± 1.25 V (see § 3.1.1 above) is applied.

3.2 *Forward digital data transmission from the remote station to the central station*

The analogue centre channel with a subcarrier frequency f_2 = 1400 Hz should be used for transmission of ECG-associated digital data. Channel characteristics are:

– centre frequency:	f_2 = 1400 Hz (see Note)
symbol 1, (mark):	$f_z = f_2 - 80$ Hz
symbol 0, (space):	$f_a = f_2 + 80$ Hz
– coding:	International Alphabet No. 5 as indicated in Recommendations V.3 and V.4, with start/stop transmission
– nominal modulation rate:	100 bauds
– power level:	$p_2 \leqslant -11$ dBm

Note – In addition to the aforementioned signalling system, the following systems for forward digital data transmission are also in use:

a) tri-level code, derived from frequencies $f_{1,2,3}$ and $f_{1,2,3}$ ± approximately 100 Hz;

b) serial code with f_1 = 1075 Hz ± 40 Hz and frequency shift keying (FSK);

c) signalling with push-button telephone frequencies as specified in Recommendation Q.23 [1].

These variants should be allowed to remain in use for a transition period of two study periods. Afterwards, only the above recommended version should be used in order to obtain mutual technical compatibility of the instruments. This should also apply to future developments.

3.3 *Digital transmission in the backward direction from the central station to the remote station*

In order to send back interpretation results, control signals, etc., a digital backward channel with the following parameters should be provided:

– modulation by frequency shift keying with the following frequencies:	
symbol 1 (mark):	f_z = 390 Hz (see Note)
symbol 0 (space):	f_a = 570 Hz
– nominal modulation rate:	200 bauds
– coding:	International Alphabet No. 5 as indicated in Recommendations V.3 and V.4, with start/stop transmission
– transmission level:	as specified in Recommendation V.2
– idle condition:	symbol 1 (mark), 390 Hz
– level accepted by receiver:	– 6 dBm to –40 dBm
– lower threshold level:	–46 dBm.

Note – f_z = 390 Hz is in accordance with Recommendation V.23. For single tone signalling, f = 389 Hz (EIA standard for tone signalling) should be allowed for a transition period of two study periods. Afterwards, the above CCITT standard should be applied.

3.4 *Calibration signal*

At the beginning of the ECG recording a standardized calibration signal can be transmitted from the ECG recorder. By transmitting the combination ENQ (0/5) of International Alphabet No. 5 to the remote station (ECG recorder) the central station should call up and repeat this calibration signal whenever desired.

3.5 *Quality control*

In order to monitor the transmission quality and eliminate those parts of the transmitted ECG which contain interference pulses, suitable monitoring measures should be provided in the central modem. If a part of the transmitted ECG is disturbed, the central unit should send the signal DEL to the remote station.

A 40-dB signal-to-noise ratio in the baseband ECG channel is provisionally recommended as threshold level. The exact value needs further study.

3.6 *Interchange circuits*

The following interchange circuits should be optional. If interchange circuits are required, the following circuits should be provided:

3.6.1 *Interchange circuits between recording system and remote station modem*

If interchange circuits are necessary between the recorder and the modem, their functions should be in accordance with Recommendation V.24, and their electrical values in accordance with Recommendation V.28 or V.31, except circuits carrying analogue signals.

3.6.2 *Interchange circuits between the central modem and the interpretation system*

If these interchange circuits are necessary, they should also be in accordance with Recommendations V.24 and V.28.

The choice of the required interchange circuits needs further study.

3.7 *Procedures*

The required procedures also need further study with respect to mutual compatibility, echo suppressor disabling, answering tones, etc.

Note – A frequency scheme of subcarrier frequencies and associated digital channels is given in Figure 3/V.16.

4 Modem for simultaneous analogue transmission of one ECG record

4.1 *General*

This specification enables single channel equipment for direct galvanic coupling or acoustic coupling to be designed which is compatible with the centre channel of the three-channel transmission equipment described in § 3 above.

4.2 Baseband signal when transmitting from the remote station to the central unit as specified in § 3.1.1 above but with the following amendments to be made to the parameters of the line signals:

- frequency: $f_2 = 1400$ Hz;
- power level: $p_2 \leqslant -6$ dBm.

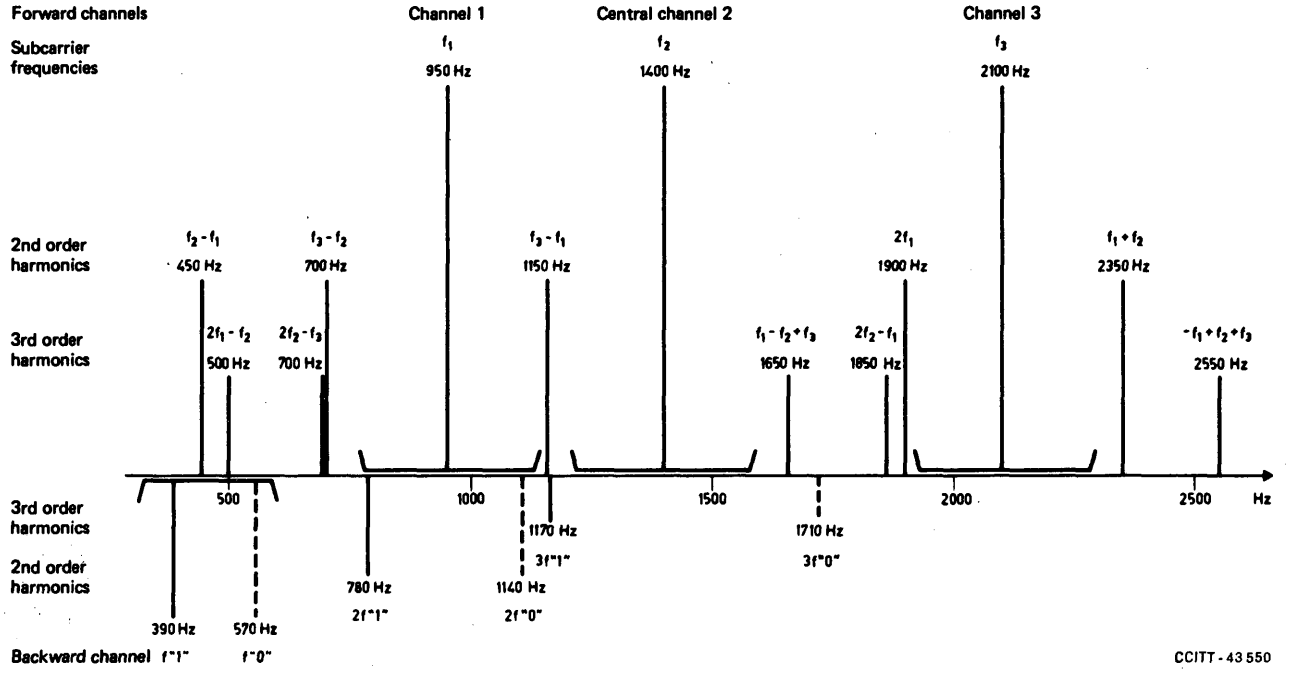

FIGURE 3/V.16

Frequency scheme of subcarrier frequencies and associated digital channels

In the case of acoustic coupling the above power level should not be exceeded at the output of the telephone set. The full scale limit may be extended to ± 5 mV. Linear operation is required up to ± 2.5 mV in this case. The slope of the modulator characteristic should be 40 Hz/mV for linear operation. These parameters are related to the patient's cable.

4.3 *Digital transmission in the forward direction*

Due to the limited number of possible applications, the use of the digital forward transmission channel should be optional. If provided, it should be in accordance with the digital transmission method described under § 3.2 above.

4.4 *Digital transmission in the backward direction*

The use of the digital backward channel should be optional. If provided, it should be in accordance with § 3.3 above. If no digital backward channel is provided, the answering tone (389 Hz) should be sent.

4.5 *Single channel central modem*

If required, a single channel central modem for direct galvanic coupling to the telephone line can also be designed with the parameters of the centre channel. The maximum deviation may be extended to 200 Hz. Here, all means for transmission of ECG-associated digital data are optional. If provided, they should be in accordance with the digital transmission method described under §§ 3.2 and 3.3 above.

Reference

[1] CCITT Recommendation *Technical features of push-button telephone sets*, Vol. VI, Rec. Q.23.

Recommendation V.19

MODEMS FOR PARALLEL DATA TRANSMISSION USING TELEPHONE SIGNALLING FREQUENCIES

(Geneva, 1976; amended at Malaga-Torremolinos, 1984)

Systems for parallel data transmission can be used economically when the transmitting sets (outstations) use the signalling frequencies of push-button telephone sets to transmit data to a central receiving set (instation) via the switched telephone network.

1 Scope

In many networks, the introduction of keyboard telephone sets allows simple, one-way data transmission at speeds up to about 10 characters per second to be made from a large number of push-button telephone sets serving as outstations to a common instation, via the general switched telephone network. Transmissions in the instation-to-outstation direction are generally confined to simple acoustic signals and voice replies.

The CCITT therefore

unanimously recommends

that the modems to be used for stations operating in the general switched telephone network should meet the specifications shown below.

2 General characteristics

2.1 *Data channel*

The transmission system uses two sets of frequencies in accordance with Recommendation Q.23 [1]. Each character is transmitted in the form of two simultaneously transmitted frequencies. These two frequencies belong to two separate sub-assemblies. Each of these two assemblies consists of four frequencies ["2 (1/4)" code]. This coding can thus be used to transmit 16 different character combinations and perhaps more (see Note).

The actual transmission consists in sending a frequency pair for a time greater than 30 ms, followed by a silence period of not less than 25 ms.

Note – In order to stretch the set of characters, several frequency pairs may be transmitted before the silence period. It should be noted that in this case character coding and decoding will not be effected by the DCE but by the DTE.

2.2 *Backward channel*

The following possibilities might be considered:

a) a telephone channel not simultaneous with data transmission in the forward direction;

b) a backward channel for audible signalling;

c) a backward channel for electrical signalling.

Possibilities b) and c) are provided on a basis of non-simultaneity or, optionally, simultaneity with the data transmission channels in the forward direction.

A loudspeaker will be built into the outstation modem. Optionally, a continuous signalling output may be provided. If the national regulations permit, an output for response to the channel may also be provided as an option.

3 Frequency assignments

3.1 *Data transmission channel*

The 2 groups of 4 frequencies specified in Recommendation Q.23 [1] are defined as follows:

– low group frequencies: 697, 770, 852, 941 Hz;

– high group frequencies: 1209, 1336, 1477, 1633 Hz.

The frequency pairs are assigned to the different digits as shown in Table 1/V.19.

TABLE 1/V.19

	B_1 = 1209 Hz	B_2 = 1336 Hz	B_3 = 1477 Hz	B_4 = 1633 Hz
A_1 = 697 Hz	1	2	3	A
A_2 = 770 Hz	4	5	6	B
A_3 = 852 Hz	7	8	9	C
A_4 = 941 Hz	*	0	#	D

3.2 *Backward channel*

For audible signals and electrical signalling, the backward channel frequency will be 420 Hz. This frequency may be amplitude-modulated at a rate of up to 5 bauds.

Use may also be made of an FM backward channel similar to that of the Recommendation V.23 type modem, or of the No. 2 transmission channel of a Recommendation V.21 type modem (if the frequency 1633 Hz is not used). These two types of backward channel may be used at the same time as the data frequencies in the forward direction; the use of these backward channels is optional.

4 Tolerances

4.1 *Data frequency tolerances*

The data frequency tolerances are defined in Recommendation Q.23 [1]; the difference between each frequency and its nominal frequency must not exceed ± 1.8% of the nominal frequency. Apart from this tolerance of ± 1.8% on transmission, the instation receiver should be able to accept a difference of ± 6 Hz due to the carrier systems.

4.2 *Frequency tolerance on backward channel*

The tolerance of 420 Hz on the backward channel should be ± 4 Hz; the receiver of the outstation should also be able to accept a difference of ± 6 Hz due to the carrier systems.

5 Line power levels

On the basis of Recommendation V.2, the following maximum power levels are recommended for each frequency transmitted, measured at the relative zero point:

– 13 dBm0 for the data transmission channel without the simultaneous backward channel;

– 16 dBm0 for the data transmission channel with the simultaneous backward channel;

– 10 dBm0 for the non-simultaneous backward channel;

– 16 dBm0 for the simultaneous backward channel.

6 Power levels on reception

In view of the provision of Recommendation V.2 and the statistical values of the maximum transmission loss between subscribers, it is recommended that the instation receiver should be able to detect frequency pairs received at – 45 dBm.

Note – Studies should be continued with a view to permitting levels on reception below – 45 dBm.

7 Character reception

A character will be detected and delivered to the DTE interface if, and only if, the two frequencies corresponding to the character are detected and are stable for at least 10 ms.

The silent period will be detected and delivered to the DTE interface if no frequency belonging to the code appears for at least 10 ms.

Note – During silent periods, the microphone of the telephone set is connected to the telephone line, so that interfering signals (ambient noise, speech) may be received. The receiver must be fitted with devices capable of distinguishing between these interfering signals and data signals (speech protection). It would be advisable to study further the method of assessing receiver response to the simulation of data signals by interfering signals. A reproducible test signal should be defined, so that comparable measurements can be made.

8 Detection of line signal received on the data channel

Circuit 109 must be in the ON position when a character is received; the circuit may be switched from ON to OFF:

1) on detection of the silent period;
2) after a time-out of 60 ± 10 ms following detection of the silent period.

9 Timing for characters received

By its very principle, the system is asynchronous; however, it may be useful to provide the DTE, on an optional basis, with a signal which indicates the sampling times of the data wires. In this case, it is advisable to use circuit 131, which will switch from OFF to ON when the character reaches the interface, and then back to OFF after a time T. This time will be chosen in such a way that the data are stable at the DTE interface.

The value $T = 15$ ms may be recommended by way of example.

This clock may optionally be disabled on reception of a silent period.

10 Interface of instation modem

The functional characteristics of the interchange circuits concerned are as defined in Recommendation V.24 (see Note 1).

10.1 *List of interchange circuits concerned*

102 Signal ground or common return

104 Received data [8 circuits. These circuits are designated A_1, A_2 ... B_4 according to their correspondence with the relevant frequency in Table 1/V.19 (see Note 2 below)]

105 Request to send (see Note 3 below)

107 Data set ready

108/1 Connect data set to line (see Note 4 below)

108/2 Data terminal ready (see Note 4 below)

109 Data channel received line signal detector

125 Calling indicator

130 Transmit backward tone

191 Transmitted voice answer (see Note 3 below)

The following interchange circuits are optional:

110 Data signal quality detector

131 Received character timing

Note 1 – Manufacturers who marketed a modem of this type prior to the publication of this Recommendation may regard the interface defined in this paragraph as optional.

Note 2 – To make the interface compatible with the relevant specifications of Recommendation V.20, the combination A_4, B_4 may be transmitted on circuit 104 instead of a pause ("1" on all circuits), provided circuit 107 is in the ON position and circuit 105 is in the OFF position. This simulated idle combination is optional.

Note 3 – These circuits are required if the "telephone channel" facility is provided in the modem. The electrical characteristics of interchange circuit 191 are still under study.

Note 4 – Circuit 108 must be available either as circuit 108/1 – *Connect data set to line*, or as circuit 108/2 – *Data terminal ready.*

10.2 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

11 Interface of outstation modems

In view of the purpose of these modems, which are or will be more or less integrated in economic terminals, the specification of the interface is liable to result in a much higher equipment cost. Hence no interface is recommended.

Reference

[1] CCITT Recommendation *Technical features of push-button telephone sets*, Vol. VI, Rec. Q.23.

PARALLEL DATA TRANSMISSION MODEMS STANDARDIZED FOR UNIVERSAL USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

(former Recommendation V.30, Mar del Plata, 1968;
amended at Geneva, 1972 and 1980, and at Malaga-Torremolinos, 1984)

There is a need for one-way data transmission systems where a large number of low-cost sending stations (outstations) transmit to a central receiving station (instation) over the switched telephone network.

The following systems are desired:

a) transmitting 16-character combinations;

b) transmitting 64-character combinations;

c) transmitting 256-character combinations.

In most cases a character signalling rate of 20 characters per second will be sufficient; 40 characters per second may be required for some applications of the 16-character combination system.

The transmission from the instation to the outstations is limited either to simple acknowledgement signals (data collection systems) or to analogue signals (voice-answering systems).

The use of normal push-button telephone sets in the outstation for some of these applications may be of advantage for the user. However, it is recognized that for the time being on some telephone systems there exist certain limitations in the frequency band 600 to 900 Hz. This is due to the characteristics of the telecommunication path, such as signalling frequencies and metering pulses. Therefore, for a universal system the frequency band of the data channel is 900 to 2000 Hz, which excludes the use of the normal push-button telephone set.

A so-called parallel data-transmission system using two or three times one out of four frequencies can fulfil the above requirements.

For these reasons, the CCITT

unanimously declares the following:

1 Parallel data-transmission systems can be used economically when a large number of low-cost sending stations (outstations) wish to transmit to a central receiving station (instation) over the switched telephone network (or on leased telephone circuits).

Apart from the possibility of the use, on a restricted scale, of a system that is compatible with multifrequency push-button telephone signalling devices, the following system is recommended as a universally applicable system for the switched telephone circuits.

2 Facilities

2.1 *Data channel*

The basic system has a maximum of 16-character combinations and a modulation rate of up to 40 bauds. This permits a character signalling rate of up to 20 characters per second when an inter-character rest condition is used, or up to 40 characters per second with the use of a binary timing channel. This basic system consists of two groups of four frequencies, one frequency from each group being transmitted simultaneously (two times one out of four).

The basic system includes provision for expansion up to 64-character combinations by the addition of a third four-frequency group (three times one out of four). No use is foreseen for the system with 64-character combinations at character signalling rates above 20 characters per second, within this class of inexpensive parallel transmission equipment.

An expansion of the basic system to cater for 256 characters (up to 20 characters per second) is achieved by using only two groups for the conveyance of data, each character being transmitted in two sequential parts. The two half characters are positively identified by the two different conditions of a binary channel. The timing channel mentioned above is recommended to be used for this purpose.

Where an inter-character rest condition is required the full number of frequency combinations in the modem will not be available to the user as character combinations:

a) with the 16-frequency combination system, only 15 characters will be available unless a timing channel is used from frequency group B;

b) with the 64-frequency combination system only 63 characters are available.

These recommended systems have an inherent transmission error-detecting capability.

2.2 *Backward channel*

Provision is made for the following facilities:

a) a speech channel non-simultaneous with forward data;

b) a backward channel for audible signalling;

c) a backward channel for electrical signalling purposes.

Facilities b) and c) are provided, either non-simultaneous or optionally simultaneous with the forward data channels.

A loudspeaker will be provided in the outstation modem. On an optional basis a d.c. signalling output will be provided. If national regulations permit, a voice-answering output will also be provided on an optional basis.

3 Frequency allocations

3.1 *Data channels*

Frequency allocations and designations as shown in Table 1/V.20 are recommended.

TABLE 1/V.20

Group \ Channel No.	1	2	3	4
A	920 Hz	1000 Hz	1080 Hz	1160 Hz
B	1320 Hz	1400 Hz	1480 Hz	1560 Hz
C	1720 Hz	1800 Hz	1880 Hz	1960 Hz

For the basic 16-character system only groups A and C are used.

If an inter-character rest condition is used, during the time no input data circuits are operated, rest frequencies are sent to line. The highest frequency in each group is recommended to be the rest frequency.

3.2 *Timing channel*

If a timing channel is provided in the 16-character system this should consist of a selected pair of group B frequencies. The recommended frequencies are F_{B2} = 1400 Hz and F_{B3} = 1480 Hz.

In the case where this timing channel will be used to identify the two halves of the character in the 256-character system, the higher frequency is transmitted simultaneously with the first half of the character.

No timing channel is provided in the 64-character combination system.

3.3 *Backward channel*

For the backward channel, two non-exclusive options exist.

3.3.1 *Amplitude modulated 5 bit/s backward channel*

The frequency of the amplitude modulated backward channel for audible and electrical signalling shall be 420 Hz. This tone may be amplitude modulated at rates of up to 5 bit/s.

3.3.2 *Frequency modulated 75 bit/s backward channel*

The modulation rate and characteristic frequencies for this backward channel are as follows:

	[F_Z] [(symbol 1,] [mark)]	[F_A] [(symbol 0,] [space)]
Modulation rate up to 75 bauds	420 Hz	480 Hz

In the absence of any signal on the backward channel interface, the condition Z signal is to be transmitted.

The frequency modulated backward channel can be used simultaneously with the forward data frequencies.

3.4 *Tolerances*

The tolerances on both data and backward frequencies should be ± 4 Hz.

The receiver should cater for ± 6 Hz difference due to carrier systems in addition to the transmitter tolerance of ± 4 Hz.

4 Power levels

Based on Recommendation V.2 the following maximum power levels measured at the zero relative level point are recommended for each transmitted frequency:

4.1 *Data and timing channels*

4.1.1 16-character system without timing channel and with a non-simultaneous backward channel: −13 dBm0.

4.1.2 All other cases: −16 dBm0.

4.2 *Backward channel*

4.2.1 Non-simultaneous: −10 dBm0.

4.2.2 Simultaneous: −16 dBm0.

In systems where either the simultaneous or the non-simultaneous backward channel is used, all power levels should be −16 dBm0.

The maximum difference between any data tone at the transmitter terminal should be 1 dB.

5 Threshold levels of the data channel received signal detector

When the level of the received signal in group C exceeds −49 dBm, circuit 109 shall be ON. When the level of this received signal is less than −54 dBm, circuit 109 shall be OFF. The detector circuit which causes circuit 109 to turn ON or OFF shall exhibit hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for the ON to OFF transition.

Group C was chosen for this purpose because it is the most critical from a received level point of view.

6 Threshold levels on the backward channels

The expected minimum level is for the amplitude modulated backward channel is −45 dBm for the 420 Hz tone. This information is provided to assist equipment manufacturers.

Level of the received line signal of the frequency modulated backward channel:

greater than −43 dBm circuit 122 ON

less than −48 dBm circuit 122 OFF.

The condition of circuit 122 for levels between −43 dBm and −48 dBm is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

7 Instation modem interface

The functional characteristics of interchange circuits comply with Recommendation V.24.

7.1 *List of interchange circuits:*

102 Signal ground or common return

104 Received data [12 or 8 circuits depending on whether Group B is provided or not. These received data circuits are designated A1, A2 ... C4, each corresponding to its relevant frequency (see Table 1/V.20)]

105 Request to send (see Note 2)

107 Data set ready

108/1 Connect data set to line (see Note 1)

108/2 Data terminal ready (see Note 1)

109 Data channel received line signal detector

118 Transmitted backward channel data (see Note 2)

120 Transmit backward channel line signal (see Note 2)

121 Backward channel ready (see Note 2)

125 Calling indicator

130 Transmit backward tone (see Note 3)

191 Transmitted voice answer (see Note 4)

The following optional interchange circuits may be provided:

110 Data signal quality detector

124 Select frequency groups

131 Received character timing

Note 1 – This circuit shall be capable of use as circuit 108/1 – *Connect data set to line* or circuit 108/2 – *Data terminal ready*, depending upon its use.

Note 2 – These circuits are required if the 75 bit/s frequency modulated backward channel is provided in the modem. See also Note 4.

Note 3 – This circuit is required if the 5 bit/s amplitude modulated backward channel is provided in the modem.

Note 4 – These circuits are required if the speech channel facility is provided in the modem. The electrical characteristics of interchange circuits 191 and 192 are left for further study. The pin allocation on the interface connector is the same for circuits 191A and 121 and 191B and 118, respectively. If both the speech channel and the 75 bit/s backward channel are provided in the modem, means have to be provided to switch between those circuits.

7.2 The electrical characteristics of the interchange circuits comply with Recommendation V.28.

Data circuits: when the frequency corresponding to the circuit is ON, the appropriate interchange circuit will be negative. When the frequency in this channel is OFF, the interchange circuit will be positive.

For timing purposes in the 256-character system, a single interchange circuit is selected from Group B so that positive polarity indicates the first half of the character period and a negative polarity indicates the second half of the character.

8 Outstation modem interface

The functional characteristics of interchange circuits comply with Recommendation V.24.

8.1 *List of essential interchange circuits:*

102 Signal ground or common return (see Note 4)

103 Transmitted data (nine or six circuits depending on whether Group B is provided or not). These circuits are designated A1, A2 ... C3, each corresponding to its relevant frequency (see Table 1/V.20)

105 Request to send

129 Request to receive

8.2 The following optional interchange circuits may be provided:

107 Data set ready

108/1 Connect data set to line

108/2 Data terminal ready

119 Received backward channel data (see Note 1)

122 Backward channel received line signal detector (see Note 2)

125 Calling indicator

192 Received voice answer (see Note 3)

When the optional timing channel is used then the appropriate data circuits are operated.

Note 1 – The electrical characteristics for this circuit are for further study. See also Note 4.

Note 2 – This circuit carries the data of the 5 bit/s amplitude modulated backward channel, if provided.

Note 3 – See § 7.1, Note 4 above.

Note 4 – The transmitted data circuits (103) will all use the same common return (102). The control circuits may operate each on their own return circuit. The pin allocation on the interface connector is the same for circuits 192 and 119. If both the speech channel and the 75 bit/s backward channel are provided in the modem, means have to be provided to switch between those circuits.

8.3 *Electrical characteristics*

The data and control interchange circuits at the outstation will be operated by the opening or closing of contacts carrying only direct current. The electrical characteristics of interchange circuits comply with Recommendation V.31, except circuit 119. The electrical characteristics for this interchange circuit are for further study.

9 Correspondence for each group (Table 2/V.20)

TABLE 2/V.20

At outstation closing of circuit	Number of the channel on line	At instation negative polarity on circuit
1	1	1
2	2	2
3	3	3
None	4	4

Not more than one circuit per group may be closed at a time.

10 Character set

This Recommendation includes the allocation of transmission frequencies to the interchange circuits.

The allocation of interchange circuits to the code combinations to be transmitted, i.e. definition of a character set, must conform to the conditions defined in this Recommendation and must take into account the application requirements and the type of input media (paper tape, punched cards, keyboards, etc.).

For this reason the recommendation for a character set is primarily for ISO in collaboration with CCITT.

Note – Examples of alphabets and coding methods are given in references [1], [2], [3] and [4].

References

[1] *Coding methods for parallel transmission*, White Book, Vol. VIII, Supplement 20, ITU, Geneva, 1969.

[2] *Proposals of coding for parallel transmission*, White Book, Vol. VIII, Supplement 21, ITU, Geneva, 1969.

[3] *Parallel transmission on switched telephone circuits*, Blue Book, Vol. VIII, Supplement 56, ITU, Geneva, 1964.

[4] *Low-speed parallel data sets*, Blue Book, Vol. VIII, Supplement 57, ITU, Geneva, 1964.

Recommendation V.21

300 BITS PER SECOND DUPLEX MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK[1)]

(Geneva, 1964; amended at Mar del Plata, 1968, and at Geneva, 1972, 1976 and 1980, and at Malaga-Torremolinos, 1984)

Note – The modem, designed for use on connections set up by switching in the general telephone network, can obviously be used on leased lines.

A system of data transmission at a low data signalling rate, such that data could be transmitted over a telephone circuit operated alternatively for telephone calls and data transmissions, using simple input/output equipment and easy operating procedures, would be economical.

The data signalling rate must be such as to allow the use of current types of data sources and sinks, especially electromechanical devices.

The system for data transmission will be duplex, either for simultaneous two-way data transmission or for the transmission of signals sent in the backward direction for error-control purposes. The transmission must be such that use can be made of normal telephone circuits, and this applies both to the bandwidth available and to the restrictions imposed by signalling in the telephone networks.

The two correspondents are brought into contact by a telephone call, and the circuit is put into the data-transmission position:

a) manually by agreement between the operators, or

b) automatically.

1) See Note under § 2 of this Recommendation.

For these reasons, the CCITT

unanimously declares the following view:

1 Data transmission may take place at low data signalling rates on telephone calls set up on switched telephone circuits (or on leased telephone circuits).

2 The communication circuit for data transmission is a duplex circuit whereby data transmission in both directions simultaneously is possible at 300 bit/s or less.

The modulation is a binary modulation obtained by frequency shift, resulting in a modulation rate being equal to the data signalling rate.

Note – Attention is drawn to the fact that there may be in operation some old-type V.21 modems for which the maximum data signalling rate is 200 bit/s.

3 For channel No. 1, the nominal mean frequency is 1080 Hz.

For channel No. 2, it is 1750 Hz.

The frequency deviation is ± 100 Hz. In each channel, the higher characteristic frequency (F_A) corresponds to a binary 0.

The characteristic frequencies[2)] as measured at the modulator output must not differ by more than ± 6 Hz from the nominal figures.

A maximum drift frequency of ± 6 Hz is assumed for the line. Hence the demodulation equipment must tolerate drifts of ± 12 Hz between the frequencies received and their nominal values.

4 Data may be transmitted by synchronous or asynchronous procedures. With synchronous operation, the modem will not have to provide the signals which would be necessary to maintain synchronism when transmission is not proceeding.

5 When echo control device disabling is required, it is recommended that the procedures specified in Recommendation V.25 be followed.

6 The maximum power output of the modem into the line shall not exceed 1 mW.

The power level of the modem should be adjusted to make allowance for loss between this equipment and the point of entry to an international circuit, so that the corresponding nominal level of the signal at the international circuit input shall not exceed −13 dBm0 (see Recommendation V.2, § 2).

7 a) When both channels are used for simultaneous both-way data transmission, channel No. 1 is used for transmission of the caller's data (i.e. the person making the telephone call) towards the called station, while channel No. 2 is used for transmission in the other direction.

b) When one channel is used for data transmission and the other is used for transmission of check signals, service signals, etc., only, it is channel No. 1 which is used for transmission from the calling to the called station regardless of the direction in which the data are transmitted.

c) The procedure for the assignment of the channels described under a) and b) above applies in the case of the general service of data transmission, making it possible to transmit data or check signal, service signal, etc., bilaterally between any two subscribers. In special cases which do not come under this rule, the procedure of assignment of the channels is determined by the prior agreement between the correspondents, bearing in mind the requirement proper to each service.

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2) The nominal characteristic frequencies;
channel No. 1 (F_A = 1180 Hz and F_z = 980 Hz);
channel No. 2 (F_A = 1850 Hz and F_z = 1650 Hz).

8 Interchange circuits

8.1 *List of interchange circuits essential for the modems when used on the general switched telephone network or non-switched leased telephone circuits* (see Table 1/V.21)

The configurations of interchange circuits are those essential for the particular switched network or leased circuit requirement indicated. Where one or more of such requirements are provided in a modem, then all of the appropriate interchange circuit facilities should be provided.

TABLE 1/V.21

Interchange circuit		General switched telephone network including terminals equipped for manual calling, manual answering, automatic calling, automatic answering (Note 1)	Non-switched leased telephone circuits (Note 1)	
Number	Designation		Point-to-point	Multipoint
102	Signal ground or common return	X	X	X
103	Transmitted data	X	X	X
104	Received data	X	X	X
105	Request to send	–	X (Note 2)	X
106	Ready for sending	X	X	X
107	Data set ready	X	X	X
108/1	Connect data set to line	X (Note 3)	X	X
108/2	Data terminal ready	X (Note 3)	X (Note 4)	–
109	Data channel received line signal detector	X	X	X
125	Calling indicator	X	–	–
126	Select transmit frequency	–	–	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 9).

Note 2 – Circuit 105 is not required when alternate voice/data service is used on non-switched leased point-to-point circuits.

Note 3 – This circuit shall be capable of operation as circuit 108/1 – *connect data set to line* or circuit 108/2 – *data terminal ready* depending on its use.

Note 4 – In the leased point-to-point case, where alternate voice/data service is to be provided, circuit 108/2 may be used optionally.

8.2 *Response times of circuits 106 and 109*

8.2.1 *Definitions*

8.2.1.1 Circuit 109 response times are the times that elapse between the connection or removal of a tone to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuit 109.

The test tone should have a frequency corresponding to the characteristic frequency of binary 1 and be derived from a source with an impedance equal to the nominal input impedance of the modem under test.

The level of the test tone should fall into the level range between 1 dB above the actual threshold of the received line signal detector and the maximum admissible level of the received signal. At all levels within this range the measured response times shall be within the specified limits.

8.2.1.2 Circuit 106 response times are the times from the connection of an ON or OFF condition on:

- circuit 105 (where it is provided) to the appearance of the corresponding OFF or ON condition on circuit 106;
- circuit 109 (where circuit 105 is not provided) to the appearance of the corresponding ON or OFF condition on circuit 106.

8.2.2 *Response times*

TABLE 2/V.21

Circuit 106		
OFF to ON	20-50 ms (see Note 1)	400-1000 ms (see Note 2)
ON to OFF	⩽ 2 ms	
Circuit 109		
OFF to ON	⩽ 20 ms (see Note 1)	300-700 ms (see Note 2)
ON to OFF	20-80 ms	

Note 1 – These times are used on leased point-to-point networks without alternate voice-data facilities and on leased multipoint facilities.

Note 2 – These times are used in the general switched network service and on leased point-to-point circuits with alternate voice data.

8.3 *Threshold of data channel received line signal detector*

Level of received line signal at received line signal terminals of modem for all types of connection, i.e. general switched telephone network or non-switched leased telephone circuit:

greater than −43 dBm circuit 109 ON

less than −48 dBm circuit 109 OFF

The condition of circuit 109 for levels between −43 dBm and −48 dBm is not specified except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than for the ON to OFF transition.

Where transmission conditions are known on switched or leased circuits, Administrations should be permitted at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

8.4 *Fault condition of interchange circuits*

See Recommendation V.28, § 7 for association of the receiver failure detection types).

8.4.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

8.4.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

8.4.3 All other circuits not referred to above may use failure detection type 0 or 1.

9 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

10 The following information is provided to assist equipment manufacturers:

a) The nominal range of attenuations in subscriber-to-subscriber connections is from 5 to 30 dB at the reference frequency (800 or 1000 Hz), assuming up to 35 dB attenuation at the frequency 1750 Hz.

b) The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

Reference

[1] CCITT Recommendation *Echo suppressors*, Vol. III, Rec. G.164.

Recommendation V.22

1200 BITS PER SECOND DUPLEX MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK AND ON POINT-TO-POINT 2-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1980; amended at Malaga-Torremolinos, 1984)

1 Introduction

1.1 This modem is intended for use on connections on General Switched Telephone Networks (GSTNs), and on point-to-point circuits when suitably conditioned.

The principal characteristics of this modem are as follows:

a) duplex operation on 2-wire GSTN and point-to-point leased circuits,

b) channel separation by frequency division,

c) differential phase shift modulation for each channel with synchronous line transmission at 600 bauds (nominal),

d) inclusion of a scrambler,

e) inclusion of test facilities.

1.2 Recognizing the wide range of application, this Recommendation provides for three alternative configurations. The choice of alternative is a matter for the Administration concerned. The facilities given by the alternatives are:

Alternative A

1200 bit/s synchronous
600 bit/s synchronous (optional)

Alternative B

1200 bit/s synchronous
600 bit/s synchronous (optional) } as in Alternative A

1200 bit/s start-stop
600 bit/s start-stop (optional)

Alternative C

1200 bit/s synchronous
600 bit/s synchronous (optional)
1200 bit/s start-stop
600 bit/s start-stop (optional) } as in Alternative B

An asynchronous mode having capability of handling 1200 bit/s start-stop and anisochronous data at up to 300 bit/s.

The selection of the asynchronous mode is made during the handshaking sequence (see § 6). This gives compatibility between Alternative B and Alternative C.

Note – The possibility of transmitting low speed anisochronous data in Alternatives A and B is left for further study.

2 Line signals

2.1 *Carrier and guard tone frequencies*

The carrier frequencies shall be 1200 ± 0.5 Hz for the low channel and 2400 ± 1 Hz for the high channel. A guard tone of 1800 Hz ± 20 Hz, to be transmitted only when the modem is transmitting in the high channel, may be disabled as a national option. An alternative guard tone of 550 ± 20 Hz may be incorporated as a national option. The question of international calls between countries requiring different guard tones is left for further study.

2.2 *Data and guard tone line signal levels*

The 1800-Hz guard tone shall be at a level of 6 ± 1 dB below the level of the data power in the high channel. The level of the optional 550 Hz tone is for further study. The total power transmitted to line shall be in accordance with Recommendation V.2 and shall be the same for transmission in either channel. Because of the 1800-Hz guard tone, the power level of data signals in the high channel will be approximately 1 dB lower than data signals in the low channel.

2.3 *Fixed compromise equalizer*

Fixed compromise equalization shall be incorporated in the modem. Such equalization shall be equally shared between transmitter and receiver. The characteristics of the equalizer shall be the responsibility of each Administration to recommend nationally. The possibility of producing compromise characteristics for international implementation is for further study.

2.4 *Spectrum and group-delay characteristic*

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal shall have a frequency spectrum equivalent to the square root of a raised cosine shaping with a 75% roll-off and within the limits of Figure 1/V.22. Similarly, the group delay of the transmitter output shall be within ± 150 microseconds over the frequency range 900 Hz-1500 Hz (low channel) and 2100 Hz-2700 Hz (high channel). These figures are provisional.

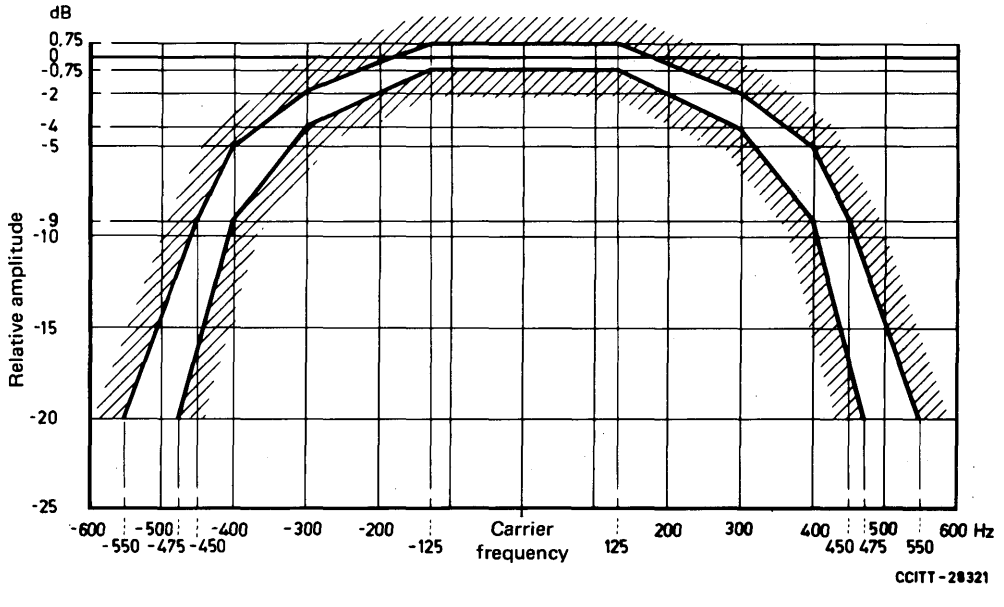


FIGURE 1/V.22

Amplitude limits for transmitted line signal (unequalized)

2.5 *Modulation*

2.5.1 *Data signalling rates*

Alternatives A and B: The data signalling rate transmitted to line shall be 1200 bit/s or 600 bit/s ± 0.01% with a modulation rate of 600 baud ± 0.01%.

Alternative C: In Modes i), ii), iii) and iv) (§ 4) the data signalling rates are as in Alternatives A and B. In Mode v), the data signalling rate transmitted to line shall be 1205 ± 1 bit/s with a modulation rate of 602.5 ± 0.5 baud. Optionally in Mode v), the line rate shall be 1223 ± 2 bit/s with a modulation rate of 611.5 ± 1 baud.

2.5.2 *Encoding of data bits*

2.5.2.1 *1200 bits per second*

The data stream to be transmitted shall be divided into groups of 2 consecutive bits (dibits). Each dibit shall be encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.22). At the receiver, the dibits shall be decoded and the bits reassembled in correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.22

Dibit values (1200 bit/s)	Bit values (600 bit/s)	Phase change (Modes i, ii, iii, iv)	Phase change (Mode v)
00	0	+ 90°	+ 270°
01	–	0°	+ 180°
11	1	+ 270°	+ 90°
10	–	+ 180°	0°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5.2.2 *600 bits per second*

Each bit shall be encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.22).

2.6 *Received signal frequency tolerance*

Noting that the frequency tolerance of the transmitter carriers is ± 1 Hz or less, and assuming a maximum shift of ± 6 Hz in the connection, the receiver shall be able to accept errors of at least ± 7 Hz in the received frequencies.

3 Interchange circuits

3.1 *Table of interchange circuits* (Note 1 of Table 2/V.22)

Essential and optional interchange circuits are listed in Table 2/V.22.

TABLE 2/V.22

Interchange circuits (Note 1)

Interchange circuit		Notes
No.	Description	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	Note 2
106	Ready for sending	
107	Data set ready	
108/1	Connect data set to line	Note 3
108/2	Data terminal ready	Note 3
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	Note 4
113	Transmitter signal element timing (DTE source)	Note 5
114	Transmitter signal element timing (DCE source)	Note 6
115	Receiver signal element timing (DCE source)	Note 6
125	Calling indicator	Note 7
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 3.5).

Note 2 – Some automatic calling equipments are designed to emit a calling tone to line by turning ON circuit 105 to the calling modem. The general switched telephone network (GSTN) constant carrier handshake is such that no calling tone will be emitted by the V.22 modem when used with these equipments.

Note 3 – This circuit shall be capable of operation as circuit 108/1 or 108/2 depending on its use.

Note 4 – This circuit is optional if only the 1200 bit/s speed [modes i) and ii) as defined in §§ 4.1, 4.2 and 4.3] is provided in the modem. If the 600 bit/s speed [modes iii) and iv)] is also provided, this circuit is essential.

Note 5 – When the modem is not operating in a synchronous mode any signals on this circuit shall be disregarded and the data terminal equipment may not have a generator connected.

Note 6 – When the modem is not operating in a synchronous mode, this circuit shall be clamped to the OFF condition and the data terminal equipment may not terminate the circuit.

Note 7 – This circuit is for use with the general switched telephone network only.

3.2 *Circuits 106 and 109 response times* (see Table 3/V.22)

Circuit 106 response times are from the application of an ON or OFF condition on circuit 105. See also § 6 for operating sequences.

TABLE 3/V.22

	Constant carrier	Controlled carrier
Circuit 106		
OFF to ON	⩽ 2 ms	210 to 275 ms
ON to OFF	⩽ 2 ms	⩽ 2 ms
Circuit 109		
OFF to ON	105 to 205 ms	105 to 205 ms
ON to OFF	10 to 24 ms	10 to 24 ms

3.3 *Circuit 109 thresholds*

High channel threshold:

greater than −43 dBm circuit 109 ON
less than −48 dBm circuit 109 OFF

Low channel threshold:

greater than −43 dBm circuit 109 ON
less than −48 dBm circuit 109 OFF

The condition of circuit 109 between the ON and OFF levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than for the ON to OFF transition.

Circuit 109 thresholds are specified at the input to the modem excluding the effects of the compromise equalizer.

Circuit 109 shall not respond to the 1800-Hz or 550-Hz guard tones, or the 2100-Hz (nominal) answer tone during the handshake sequence.

Administrations are permitted to change these thresholds where transmission conditions are known.

3.4 *Circuit 111 and data rate control*

Data rate selection may be by switch (or similar means) or by circuit 111 or a combination of both.

The ON condition on circuit 111, where provided, shall select 1200 bit/s operation and the OFF condition shall select 600 bit/s operation.

3.5 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.6 *Fault condition of interchange circuits*

(See Recommendations V.28, § 7 for association of the receiver failure detection types.)

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection type 0 or 1.

4 Modes of operation over the DTE/DCE interface

4.1 *Alternative A*

The modem can be configured for the following modes of operation:

Mode i) 1200 bit/s ± 0.01% synchronous

Mode iii) 600 bit/s ± 0.01% synchronous (optional).

In these modes of operation, the modem shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or circuit 114. The data shall then be scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.2.

In addition to standard V.24 transmitter timing arrangements, the modem shall provide capabilities to derive transmit signal element timing from receiver signal element timing.

4.2 *Alternative B*

The modem can be configured for the following modes of operation:

Mode i) 1200 bit/s ± 0.01% synchronous

Mode ii) 1200 bit/s start-stop 8, 9, 10 or 11 bits per character

Mode iii) 600 bit/s ± 0.01% synchronous } optional

Mode iv) 600 bit/s start-stop 8, 9, 10 or 11 bits per character }

The synchronous modes are as given in Alternative A.

4.2.1 *Transmitter*

In the start-stop modes, the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of 1200 or 600 bits per second. The start-stop data shall be converted to a form suitable for transmission synchronously at 1200 or 600 bits per second ± 0.01%, then scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.2. The modem shall derive its line signal clock from internal clock circuits or, alternatively, from receiver signal element timing, as an installation option.

It shall be possible to condition the converter to accept the following character formats; viz:

a) a one-unit start element, followed by seven data units, and a stop element of one unit in length (9-bit characters),

b) a one-unit start element, followed by eight data units, and a stop element of one unit in length (10-bit characters),

c) a one-unit start element, followed by nine data units, and a stop element of one unit in length (11-bit characters).

The converter may also accept characters consisting of:

d) a one-unit start element, followed by six data units, and a stop element of one unit in length (8-bit characters).

Note that character formats c) and d) do not conform to International Alphabet No. 5.

The character format selected shall be the same for both transmitter and receiver. The characters shall be in accordance with Recommendation V.4. It shall be possible to transmit characters contiguously or with any additional continuous stop element of arbitrary length between characters.

Note – In each of the four formats, data units can be replaced by additional stop units. For example, format c) will allow 11 bit characters consisting of a one-unit start element, followed by eight data units and a stop element of two units to be handled.

4.2.1.1 *Basic signalling rate range*

The intracharacter signalling rate (signalling rate of the start bit and information bits within each character) provided by the DTE on circuit 103 must be 1200 or 600 bit/s +1%, −2.5%. In Mode ii), the character rate (the reciprocal of the time interval between successive start bits) provided by the DTE over circuit 103 must not exceed:

151.5 characters per second for 8-bit characters

134.7 characters per second for 9-bit characters

121.2 characters per second for 10-bit characters

110.2 characters per second for 11-bit characters

When the character rate is:

from 150 to 151.5 characters per second for 8-bit characters

from 133.3 to 134.7 characters per second for 9-bit characters

from 120.0 to 121.2 characters per second for 10-bit characters

from 109.1 to 110.2 characters per second for 11-bit characters

the start-stop to synchronous converter in the modem transmitter shall as often as is necessary delete the stop bits of the incoming characters. No more than one stop bit shall be deleted for any eight consecutive characters.

When the character rate provided by the DTE on circuit 103 is less than:

150 characters per second for 8-bit characters

133.3 characters per second for 9-bit characters

120.0 characters per second for 10-bit characters

109.1 characters per second for 11-bit characters

the start-stop to synchronous converter in the modem is transmitting more bits per second than are provided by the DTE. The converter shall therefore insert extra stop bits in between the transmitted characters.

In Mode iv) the character rates are half those for Mode ii).

4.2.1.2 *Extended signalling rate range (optional)*

Certain DTEs and multiplexers are not within the +1% overspeed limit. Facilities may therefore be provided to enable the modem to accept data from a DTE having an intracharacter signalling rate of 1200 or 600 bit/s +2.3%, −2.5% with 8, 9, 10 or 11 bits per character by deletion of up to one stop bit in any four consecutive characters. A modem transmitter set to work with 2.3% maximum overspeed can handle data received from a DTE in accordance with § 4.2.1.1.

4.2.1.3 *Break signal*

If the converter detects M to $2M + 3$ bits, all of "start" polarity, where M is the number of bits per character in the selected format, the converter shall transmit $2M + 3$ bits of "start" polarity. If the converter detects more than $2M + 3$ bits all of "start" polarity the converter shall transmit all these bits as "start" polarity.

Note – The DTE must transmit on circuit 103 at least $2M$ bits of "stop" polarity after the "start" polarity break signal before sending further data characters. This ensures the receiving modem can regain character synchronism.

4.2.2 *Receiver*

The intracharacter signalling rate provided to the DTE over circuit 104 shall be in the range 1200 to 1221 bit/s. The nominal length of the start and data elements for all characters shall be the same. The length of the stop element shall not be reduced by more than 12½% for the basic signalling rate range (or 25% for the optional extended signalling rate range) to allow for overspeed in the transmitting terminal.

The use of the basic signalling rate range is preferred since it results in lower distortion. The choice of range shall be made at the time of installation, and shall be the same for both transmitter and receiver. It is not intended to be under customer control.

4.2.2.1 *Break signal*

The $2M + 3$ or more bits of "start" polarity received from the transmitting modem shall be output on circuit 104. The modem shall then regain character synchronism from the following "stop" to "start" transition.

4.3 *Alternative C*

The modem can be configured for the following modes of operation.

Mode i) 1200 bit/s ± 0.01% synchronous

Mode ii) 1200 bit/s start-stop 8, 9, 10 or 11 bits per character

Mode iii) 600 bit/s ± 0.01% synchronous } optional

Mode iv) 600 bit/s start-stop 8, 9, 10 or 11 bits per character } optional

Mode v) An asynchronous mode having capability of handling 1200 bit/s start-stop and anisochronous data at up to 300 bit/s.

Modes i) to iv) are as given in Alternative B.

4.3.1 *Basic modes*

In Alternative C, the modem shall incorporate Modes i), ii), iii) and iv) given in Alternative B, plus Mode v), in which the modem transmitter sends data at a rate always greater than the input data rate, and thus disables the receiver buffer. The GSTN handshaking sequence allows automatic selection of Modes ii) or v). Modes i), iii) and iv) must be selected at installation. On leased circuits there is no automatic mode selection. The line encoding for specific dibit values is described in Table 1/V.22.

4.3.2 *Transmitter*

In Mode v), the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of a 0 to 300 bit/s or 1200 bit/s automatically. The transmitter buffer that converts incoming data to a synchronous data stream at 1205 bit/s or 1223 bit/s shall:

a) start its asynchronous bit counter on either data transition,

b) always transmit the last bit received over circuit 103 after the bit counter has elapsed,

c) sample incoming data during the bit count at 1205 Hz or 1223 Hz depending upon line rate.

This will assure that incoming data at 0 to 300 bit/s shall pass through the buffer with a maximum introduced distortion of 25% at 300 bit/s (and 12.5% at 150 bit/s), and that break signals pass through the buffer unchanged.

The length and structure of incoming characters shall be the same as given in Alternative B. Within Mode v) at 1200 bit/s asynchronous, two adjacent character formats, e.g. 9- and 10-bit character, can be handled automatically. As in Alternative B, the modem shall derive its line signal clock from internal clock circuits, or alternatively, from receiver signal element timing, as an installation option.

4.3.3 *Basic signalling rate range*

In Mode v), the intracharacter signalling rate provided by the DTE on circuit 103 must be:

1205 bit/s line rate	0 to 301 bit/s and 1170 to 1204 bit/s
1223 bit/s line rate	0 to 305 bit/s and 1190 to 1221 bit/s

Selection of line rate is made in the transmitter by installer option and automatically detected in the receiver.

5 Scrambler and descrambler

5.1 *Scrambler*

A self synchronizing scrambler having the generating polynomial $1 \oplus x^{-14} \oplus x^{-17}$ shall be included in the modem transmitter. The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. The scrambler output data sequence

$$D_s = D_i \oplus D_s \cdot x^{-14} \oplus D_s \cdot x^{-17}$$

where

D_S is the data sequence at the output of the scrambler

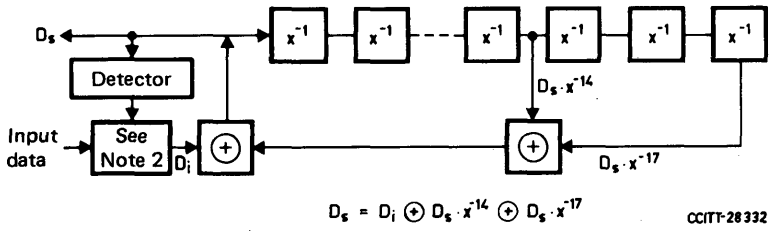
D_i is the data sequence applied to the scrambler

$\oplus$ denotes modulo 2 addition

denotes binary multiplication

Figure 2/V.22 shows a suitable implementation.

To prevent occasional inadvertent instigation of remote loop 2 caused by scrambler lockup, circuitry shall be included to detect a sequence of 64 consecutive ones at the scrambler output (D_s) and, if detected, invert the next input to the scrambler, D_i. This circuitry will not operate during handshaking or during the instigation of remote loop 2.



Note 1 – Marks (binary 1) and spaces (binary 0) at the V.24 interface correspond to ones and zeros, respectively, in this logic diagram.

Note 2 – Circuitry shall be included to detect a sequence of 64 consecutive binary ones at the scrambler output (D_S) and, if detected, invert the next input to the scrambler (D_i).

FIGURE 2/V.22

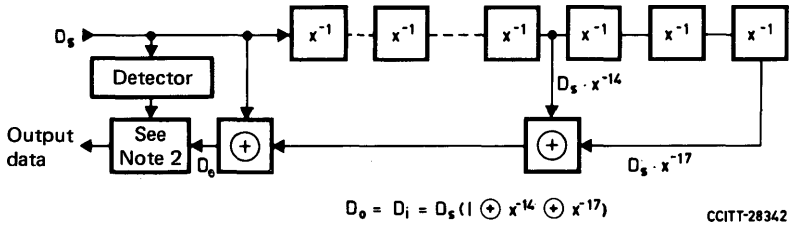
Scrambler

5.2 *Descrambler*

A self synchronizing descrambler having the polynomial $1 \oplus x^{-14} \oplus x^{-17}$ shall be provided in the modem receiver. The message data sequence produced after demodulation shall be effectively multiplied by the generating polynomial $1 \oplus x^{-14} \oplus x^{-17}$ to form the descrambled message. The coefficients of the recovered message sequence taken in descending order form the output data sequence D_o, which is given by

$$D_o = D_s(1 \oplus x^{-14} \oplus x^{-17})$$

Figure 3/V.22 shows a suitable implementation.



Note 1 – Marks (binary 1) and spaces (binary 0) at the V.24 interface correspond to ones and zeros, respectively, in this logic diagram.

Note 2 – Circuitry may be included to detect a sequence of 64 consecutive ones at the input to the descrambler (D_S) and, if detected, invert the next output from the descrambler, (D_O) This detector should not begin operating until the handshaking sequence is complete. If this circuitry is included, detection of the initiation signal described in § 7.1.1 (unscrambled binary ones) should be performed at the point D_O.

FIGURE 3/V.22

Descrambler

6 Operating sequences

6.1 *Channel and operating mode selection*

On the general switched telephone network, the modem at the calling data station shall transmit in the low channel and receive in the high channel (call mode). The modem at the answering data station shall receive in the low channel and transmit in the high channel (answer mode).

Where calls are established on the GSTN by operators, bilateral agreement between users on channel allocation will be necessary. On point-to- point leased circuits, channel allocation will be by bilateral agreement between Administrations or users. In these cases the method of selection of call or answer mode is a national matter.

On point-to-point leased circuits, selection of Modes i) to v) will be by bilateral agreement between Administrations or users. The method of selection is a national matter.

6.2 *V.25 automatic answering sequence*

The V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted on point-to-point leased circuits or on national connections on the GSTN, where permitted by the Administration.

6.3 *Operating sequences for Alternatives A and B*

6.3.1 *GSTN - constant carrier*

The means of achieving initial synchronism between the call mode modem and the answer mode modem on international GSTN connections is shown in Figure 4/V.22. The alternative handshake without V.25 automatic answering is shown in Figure 5/V.22.

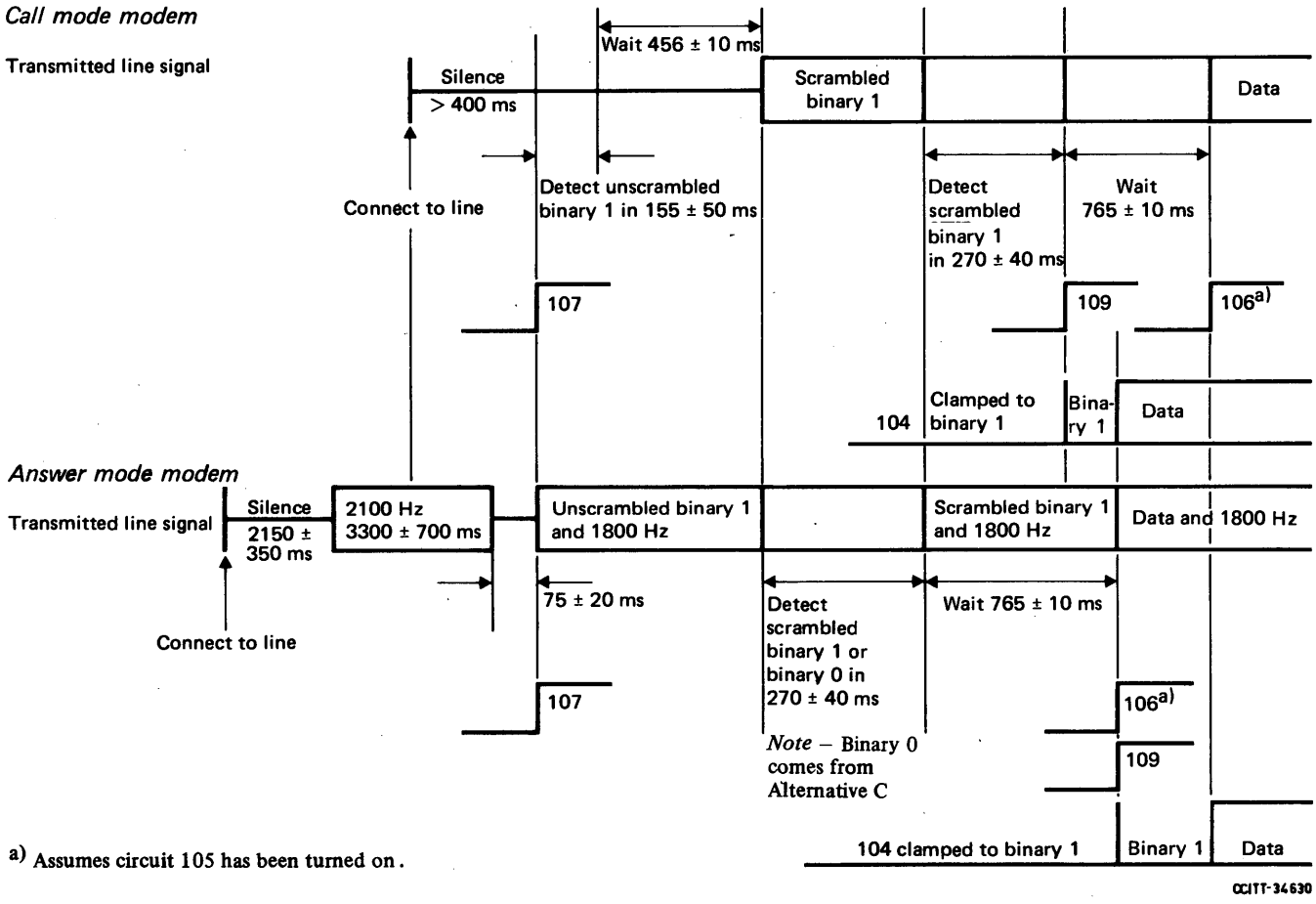
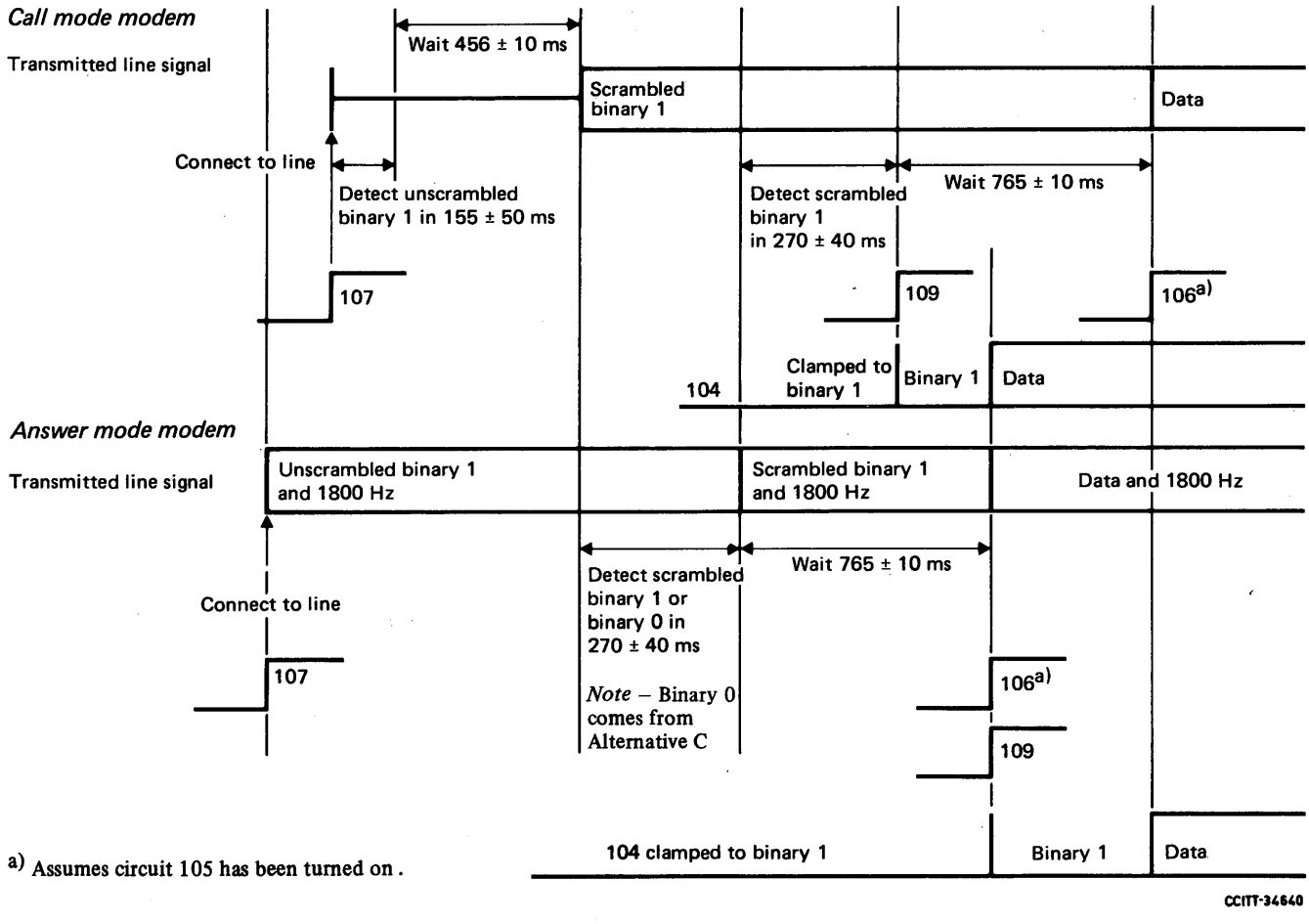


FIGURE 4/V.22

Handshake sequence for Alternatives A and B (with V.25 auto-answering)



a) Assumes circuit 105 has been turned on.

FIGURE 5/V.22

Handshake sequence for Alternatives A and B (without V.25 auto-answer sequence)

6.3.1.1 *Call mode modem*

Once the call mode modem has connected to line, it shall be conditioned to receive signals in the high channel and shall apply an ON condition to circuit 107 in accordance with Recommendation V.25. The modem shall remain silent until unscrambled binary 1 is detected for 155 ± 50 ms, and after waiting for 456 ± 10 ms shall transmit scrambled binary 1 in the low channel. Upon detecting scrambled binary 1 in the high channel in 270 ± 40 ms, the modem shall turn circuit 109 ON, then wait a further 765 ± 10 ms. Circuit 106 shall then respond to the condition of circuit 105 according to Table 3/V.22 constant carrier mode. When circuit 106 is OFF, circuit 103 shall be clamped to the binary 1 condition.

Note – Manufacturers may wish to note that in certain countries, for national purposes, modems are in service which emit an answering tone of 2225 Hz instead of unscrambled binary 1.

6.3.1.2 *Answer mode modem*

Once the answer mode modem has connected to line and immediately following the V.25 answer sequence, the modem shall be conditioned to receive signals in the low channel. It shall then apply an ON condition to circuit 107 and transmit unscrambled binary 1. Upon detecting scrambled binary 1 or 0 in the low channel in 270 ± 40 ms, the modem shall transmit scrambled binary 1 in the high channel, and after waiting for 765 ± 10 ms, apply an ON condition to circuit 109. Circuit 106 shall then respond to the condition of circuit 105 according to Table 3/V.22, constant carrier mode. When circuit 106 is OFF, circuit 103 shall be clamped to the binary 1 condition.

Where both modems are manually connected to line this sequence will apply irrespective of whether the call or answer mode modem is connected to line first.

After completion of the handshake sequence, any inadvertent loss and reappearance of the received line signal should not cause another handshake sequence to be generated. Circuit 109 should respond with the response times given in Table 3/V.22.

6.3.2 *GSTN and point-to-point leased circuits - controlled carrier*

Once an ON condition has been applied to circuit 105 by the DTE, the modem shall transmit a synchronizing signal corresponding to binary 1 applied to circuit 103. The ON condition shall be applied to circuit 106, 210 to 275 ms after starting to transmit the synchronizing signal. The receiving modem shall establish timing and descrambler synchronization and then turn circuit 109 ON in 105 to 205 ms.

Each direction of transmission shall be independently controlled.

Note – Controlled carrier operation on GSTN is optional. For circuits with echo suppressors, controlled carrier working is not recommended.

6.4 *Operating sequence for Alternative C*

Refer to Figure 6/V.22.

6.4.1 *GSTN - constant carrier*

6.4.1.1 *Call mode modem*

If configured for Modes i), iii), or iv), the handshake sequence proceeds as for Alternative B. If configured for Mode v), the handshaking sequence shall automatically select Mode ii) or v). This sequence shall be as follows:

Once the call mode modem has connected to line, it shall be conditioned to receive signals in the high channel and shall apply an ON condition to circuit 107 in accordance with Recommendation V.25. The modem shall remain silent until unscrambled binary 1 [Mode ii)] is detected for 155 ± 50 ms and after waiting for 456 ± 10 ms shall transmit scrambled binary 0 [Mode ii)] in the low channel. Upon detecting scrambled binary 1 [Mode ii)] in the high channel within 270 ± 40 ms, the modem shall turn circuit 109 ON, enter Mode ii), then wait a further 765 ± 10 ms. Upon detecting scrambled binary 1 [Mode v)] in the high channel in 270 ± 40 ms, the modem shall turn ON circuit 109, enter Mode v), then wait a further 765 ± 10 ms. Circuit 106 shall then respond to the condition of circuit 105 according to Table 3/V.22 constant carrier mode. When circuit 106 is OFF, circuit 103 shall be clamped to the binary 1 condition.

See also the note in § 6.3.1.1.

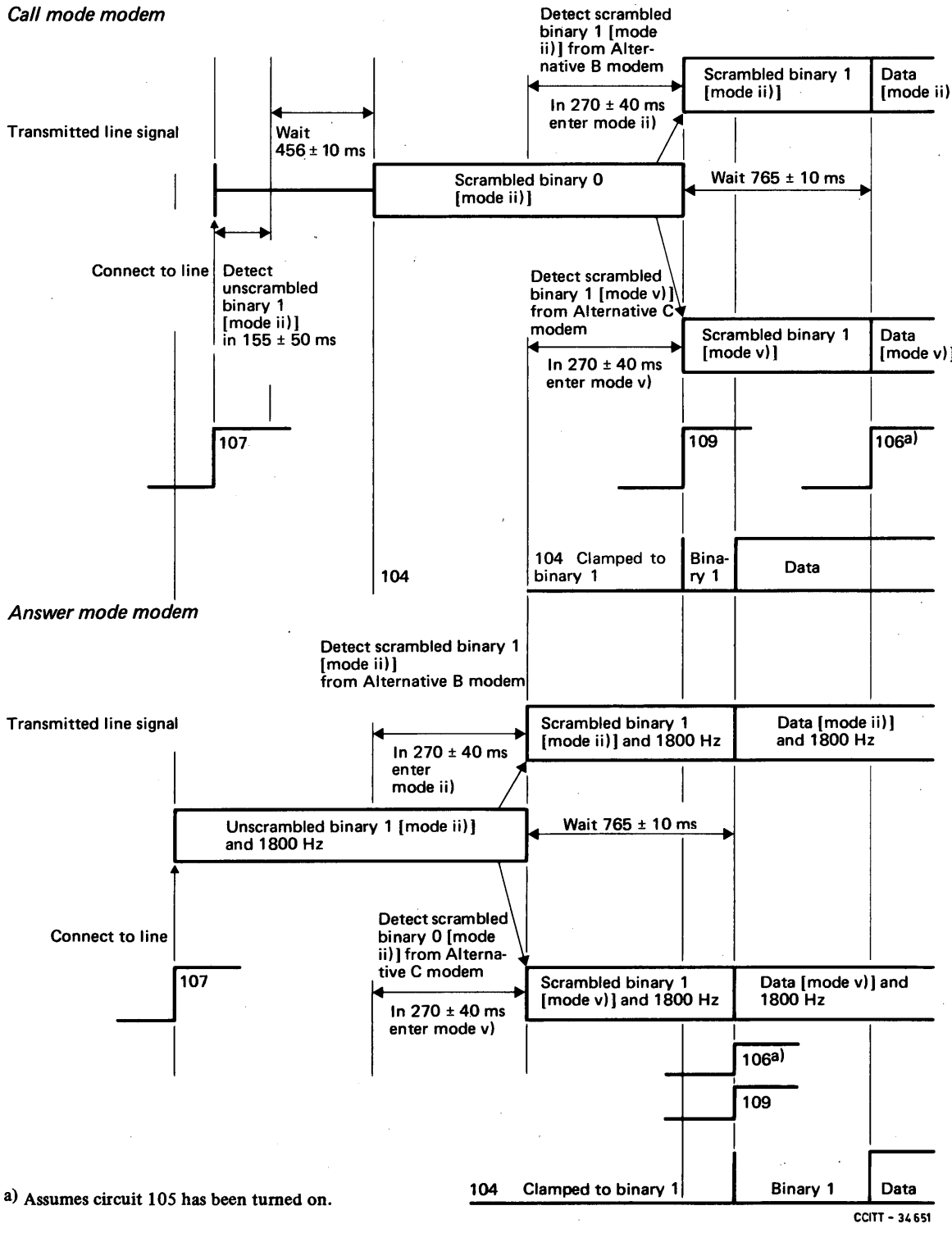


FIGURE 6/V.22

Handshake sequence for Alternative C (without V.25 auto-answer sequence)

6.4.1.2 *Answer mode modem, Mode v)*

Once the answer mode modem has connected to line and immediately following the V.25 answer sequence, the modem shall be conditioned to receive signals in the low channel. It shall then apply an ON condition to circuit 107 and transmit unscrambled binary 1 [Mode ii)].

If scrambled binary 0 [Mode ii)] is detected in the low channel for 270 ± 40 ms, the modem shall enter Mode v), transmit scrambled binary 1 [Mode v)] in the high channel and after waiting for 765 ± 10 ms apply an ON condition to circuit 109.

If scrambled binary 1 [Mode ii)] is detected in the low channel for 270 ± 40 ms, the modem shall enter Mode ii), transmit scrambled binary 1 [Mode ii)] in the high channel and after waiting for 765 ± 10 ms apply an ON condition to circuit 109.

Circuit 106 shall respond to the condition of circuit 105 according to Table 3/V.22 constant carrier mode. When circuit 106 is OFF circuit 103 shall be clamped to the binary 1 condition.

6.4.2 *GSTN and point-to-point leased circuits*

Controlled carrier operation as in § 6.3.2.

7 Testing facilities

7.1 *Test loops*

Test loops 2 (local and remote) and 3 as defined in Recommendation V.54 shall be provided. Interface operation shall be as defined in Recommendation V.54. Instigation and termination sequences are not compatible with Recommendation V.54.

7.1.1 *Instigation of remote loop 2*

Signals controlling the application of remote loop 2 may only be transmitted after the synchronizing handshake has been completed.

As in Recommendation V.54, the modems are referred to as modem A and modem B.

When modem A is instructed to instigate a remote loop 2, the modem shall transmit an initiation signal of unscrambled binary 1.

Modem B shall detect 154-231 ms of the initiation signal, and then transmit to modem A scrambled alternate binary ones and zeros (reversals) at 1200 bit/s (or 600 bit/s).

Modem A shall detect 231-308 ms of scrambled reversals, cease transmission of the initiation signal, and then transmit scrambled binary 1 at 1200 bit/s (or 600 bit/s).

Modem B shall detect the loss of initiation signal and activate loop 2 within modem B.

Modem A, upon receiving 231-308 ms of scrambled binary 1 shall indicate to the DTE that it may begin sending test messages.

7.1.2 *Termination of remote loop 2*

When modem A is instructed to terminate a remote loop 2, the line signal shall be suppressed for a period of 77 ± 10 ms, after which transmission shall be restored.

Modem B detects the loss of line signal in 17 ± 7 ms and detects the reappearance of the signal within 155 ± 50 ms, after which it returns to normal operation.

7.2 *Self tests*

7.2.1 *Self test end-to-end*

Upon activation of the self-test switch an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate shall be applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals shall be connected to the output of the descrambler. The presence of errors shall be indicated by a visual indicator. All generating interchange circuits except 114 (if used), 115 and 142 shall be clamped to the binary 1 or OFF condition. If circuit 113 is used, the DCE shall disregard this interchange circuit and use its internal clock.

7.2.2 *Self test with loop 3*

Loop 3 shall be applied to the modem as defined in Recommendation V.54. The self-test switch shall be activated and DCE operation shall be as in § 7.2.1.

7.2.3 *Self test with remote loop 2*

The modem shall be conditioned to instigate a loop 2 at the remote modem as specified in § 7.1. The self-test switch shall be activated and DCE operation shall be as in § 7.2.1.

It shall be possible to perform the above tests (§§ 7.2.1, 7.2.2 and 7.2.3) with or without the DTE connected to the modem. These tests employ an internally generated data pattern that is controlled by a switch on the DCE.

7.2.4 During any self-test mode, interchange circuits 103, 105 and 108 will be ignored. Note that self tests do not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver.

Note – Inclusion of remote loop signalling according to Recommendation V.54 is for further study.

Recommendation V.22 *bis*

2400 BITS PER SECOND DUPLEX MODEM USING THE FREQUENCY DIVISION TECHNIQUE STANDARDIZED FOR USE ON THE GENERAL SWITCHED TELEPHONE NETWORK AND ON POINT-TO-POINT 2-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that there is a demand for data transmission at 2400 bit/s in the duplex mode over the General Switched Telephone Network (GSTN) and on point-to-point 2-wire leased telephone-type circuits;

(b) that there is a demand to have the fall-back mode compatibility with modems in accordance with Recommendation V.22;

(c) that in this case the frequency division technique shall be used,

(unanimously) declares

that the characteristics of the modems for this service shall provisionally be as follows:

1 Introduction

These modems are intended for use on connections on the GSTN and on point-to-point 2-wire leased telephone-type circuits (see Note). The principal characteristics of these modems are as follows:

a) duplex mode of operation on the GSTN and point-to-point leased circuits,

b) channel separation by frequency division,

c) quadrature amplitude modulation for each channel with synchronous line transmission at 600 baud (nominal),

d) inclusion of a scrambler,

e) inclusion of an adaptive equalizer and a compromise equalizer,

f) inclusion of test facilities,

g) data signalling rates of:
2400 bit/s synchronous,
2400 bit/s start-stop,
1200 bit/s synchronous,
1200 bit/s start-stop,

h) it is compatible with a V.22 modem operating in Modes i) or ii) at the 1200 bit/s signalling rate and includes automatic bit rate recognition.

Note – In certain countries the use of such modems over the GSTN may not be allowed.

2 Line signals

2.1 *Carrier and guard tone frequencies*

The carrier frequencies shall be 1200 ± 0.5 Hz for the low channel and 2400 ± 1 Hz for the high channel. A guard tone of 1800 ± 20 Hz, to be transmitted only when the modem is transmitting in the high channel, may be disabled as a national option. An alternative guard tone of 550 ± 20 Hz, to be transmitted only when the modem is transmitting in the high channel, may be incorporated as a national option.

2.2 *Data and guard tone line signal levels*

The 1800 Hz or 550 Hz guard tones shall be levels 6 ± 1 dB or 3 ± 1 dB, respectively, below the level of the data signal power in the high channel. Because of the 1800 Hz guard tone, the power level of data signals in the high channel will be approximately 1 dB lower than that of data signals in the low channel.

2.3 *Fixed compromise equalizer*

Fixed compromise equalization shall be incorporated in the modem transmitter.

2.4 *Spectrum and group delay characteristics*

The transmitted line signals, excluding the characteristics of the fixed compromise equalizer, shall have a frequency amplitude spectrum equivalent to the square root of a raised cosine shaping with 75% roll-off and within the limits shown in Figure 1/V.22 *bis*. Similarly, the group delay of the transmitter output shall be within the range of ± 150 microseconds over the frequency ranges 900-1500 Hz (low channel) and 2100-2700 Hz (high channel). These figures are provisional.

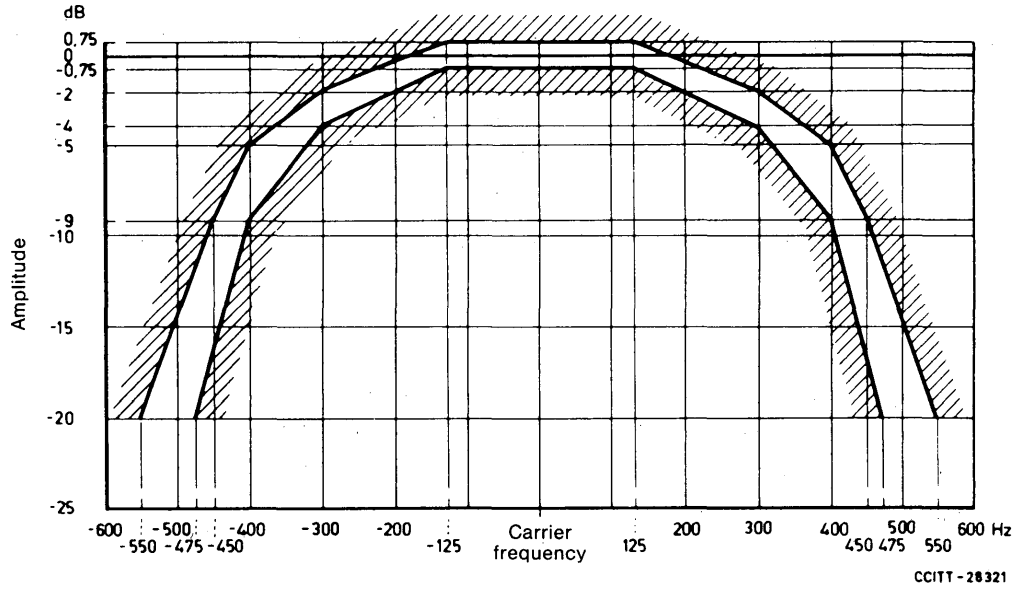


FIGURE 1/V.22 *bis*

Amplitude limits for transmitted line signal (unequalized)

2.5 *Modulation*

2.5.1 *Data signalling rates*

The data rate transmitted to line shall be 2400 bit/s or 1200 bit/s ± 0.01% with a modulation rate of 600 baud ± 0.01%.

2.5.2 *Encoding of data bits*

2.5.2.1 *2400 bits per second*

The data stream to be transmitted shall be divided into groups of 4 consecutive bits (quadbits). The first two bits of a quadbit shall be encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. (See Figure 2/V.22 *bis* and Table 1/V.22 *bis*.)

The last two bits of each quadbit define one of 4 signalling elements associated with the new quadrant (see Figure 2/V.22 *bis*). The left hand bits in Table 1/V.22 *bis* and Figure 2/V.22 *bis* are the first of each pair in the data stream as it enters the modulator portion of the modem after the scrambler.

2.5.2.2 *1200 bits per second*

The data stream to be transmitted shall be divided into groups of 2 consecutive bits (dibits). The dibits shall be encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element (see Table 1/V.22 *bis*). The signalling elements corresponding to 01 in the signal constellation (Figure 2/V.22 *bis*) shall be transmitted irrespective of the quadrant concerned. This ensure compatibility with Recommendation V.22.

2.6 *Received signal frequency tolerance*

The receiver shall be able to operate with received frequency offsets of up to ± 7 Hz.

3 Interchange circuits

3.1 *Essential and optional interchange circuits*

These are listed in Table 2/V.22 *bis*.

3.2 *Circuits 106 and 109 response times*

After the handshaking sequences, circuit 106 will follow OFF to ON or ON to OFF transitions of circuit 105 within 3.5 ms. The OFF to ON transition of circuit 109 is part of the handshake sequence specified in § 6. Circuit 109 shall turn OFF 40 to 65 ms after the level of the received signal appearing at the line terminal of the modem falls below the relevant threshold defined in § 3.3. In the fall-back mode, the response time may be reduced to a value in the 10 to 24 ms range specified in Recommendation V.22. Following a dropout, after the initial handshake, circuit 109 shall turn ON 40 to 205 ms after the level of the received signal appearing at the line terminal of the modem exceeds the relevant threshold defined in § 3.3.

3.3 *Circuit 109 threshold*

High channel threshold:

- greater than −43 dBm — circuit 109 ON
- less than −48 dBm — circuit 109 OFF

Low channel threshold:

- greater than −43 dBm — circuit 109 ON
- less than −48 dBm — circuit 109 OFF

TABLE 1/V.22 *bis*

Line encoding

First two bits in quadbit (2400 bit/s) or dibit values (1200 bit/s)	Phase quadrant change	
00	1 → 2 2 → 3 3 → 4 4 → 1	90°
01	1 → 1 2 → 2 3 → 3 4 → 4	0°
11	1 → 4 2 → 1 3 → 2 4 → 3	270°
10	1 → 3 2 → 4 3 → 1 4 → 2	180°

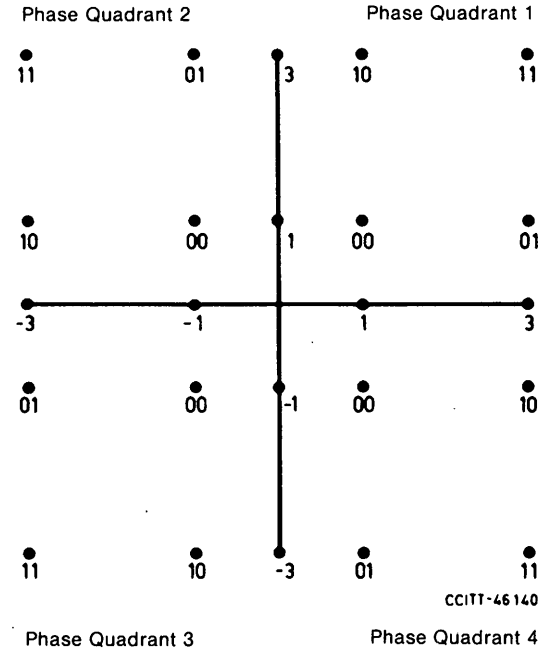


FIGURE 2/V.22 *bis*

Signal constellation

TABLE 2/V.22 *bis*

Interchange circuits (Note 1)

Interchange circuit		Notes
No.	Description	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	Note 2
106	Ready for sending	
107	Data set ready	
108/1	Connect data set to line	Note 3
108/2	Data terminal ready	Note 3
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE Source)	Note 4
112	Data signalling rate selector (DCE Source)	
113	Transmitter signal element timing (DTE Source)	Note 5
114	Transmitter signal element timing (DCE Source)	Note 6
115	Receiver signal element timing (DCE Source)	Note 6
125	Calling indicator	Note 7
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 – All essential interchange circuits and any others which are provided must comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided must be properly terminated in the data terminal equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.5).

Note 2 – Some automatic calling equipments are designed to emit a calling tone to line by turning ON circuit 105 to the calling modem. The general switched telephone network (GSTN) constant carrier handshake is such that no calling tone will be emitted by the V.22 *bis* modem when used with these equipments.

Note 3 – This circuit shall be capable of operation as circuit 108/1 or 108/2 depending on its use.

Note 4 – This circuit is optional.

Note 5 – When the modem is not operating in a synchronous mode at the interface, any signals on this circuit shall be disregarded and the data terminal equipment may not have a generator connected.

Note 6 – When the modem is not operating in a synchronous mode at the interface, this circuit shall be clamped to the OFF condition and the data terminal equipment may not terminate the circuit.

Note 7 – This circuit is for use with the general switched telephone network only.

The condition of circuit 109 between the ON and OFF levels is not specified except that the signal detector shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for the ON to OFF transition.

Circuit 109 thresholds are specified at the input to the modem when receiving scrambled binary 1.

Administrations are permitted to change these thresholds where transmission conditions are known.

Circuit 109 shall not respond to the 1800 Hz or the 550 Hz guard tones, or the 2100 Hz (nominal) answer tone during the handshake sequence.

3.4 *Circuit 111 and data rate control*

Data rate selection may be by switch (or similar means) or by circuit 111 or a combination of both.

The ON condition on circuit 111, where provided, shall select 2400 bit/s operation and the OFF condition shall select 1200 bit/s operation.

3.5 *Electrical characteristics of interchange circuits*

3.5.1 Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.6 *Fault condition of interchange circuits*

See Recommendation V.28, § 7 for association of the receiver failure detection types.)

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Modes of operation

The modem can be configured for the following modes of operation:

Mode 1 2400 bit/s ± 0.01% synchronous

Mode 2 2400 bit/s start-stop 8, 9, 10 or 11 bits per character (see § 4.1.1)

Mode 3 1200 bit/s ± 0.01% synchronous

Mode 4 1200 bit/s start-stop 8, 9, 10 or 11 bits per character (see § 4.1.1).

4.1 *Transmitter*

In the synchronous modes of operation, the modem shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or circuit 114. The data shall then be scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.

In the start-stop modes, the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of 2400 or 1200 bits per second. The start-stop data shall be converted to a form suitable for transmission synchronously at 2400 or 1200 bits per second ± 0.01%, then scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.2. The modem shall derive its line signal clock from internal clock circuits, or alternatively, from receiver signal element timing, as an installation option.

It shall be possible to condition the converter to accept the following character formats; viz:

a) a one-unit start element, followed by seven data units, and a stop element of one unit in length (9-bit characters);

b) a one-unit start element, followed by eight data units, and a stop element of one unit in length (10-bit characters);

c) a one-unit start element, followed by nine data units, and a stop element of one unit in length (11-bit characters).

The converter may also accept characters consisting of:

d) a one-unit start element, followed by six data units, and a stop element of one unit in length (8-bit characters).

Note that character formats c) and d) do not conform to International Alphabet No. 5.

The character format selected shall be the same for both transmitter and receiver. The characters shall be in accordance with Recommendation V.4 regardless of whether they conform to International Alphabet No. 5. It shall be possible to transmit characters continuously or with any additional continuous stop element of arbitrary length between characters.

Note – In each of the four formats, data units can be replaced by additional stop units. For example, format c) will allow 11-bit characters consisting of a one-unit start element, followed by eight data units and a stop element of two units to be handled.

4.1.1 *Basic signalling rate ranges*

The intracharacter signalling rate (signalling rate of the start bit and information bits within each character) provided by the DTE on circuit 103 must be 2400 or 1200 bit/s +1%, −2.5%. In Mode 2, the character rate (the reciprocal of the time interval between successive start bits) provided by the DTE over circuit 103 must not exceed:

303 characters per second for 8-bit characters

269.3 characters per second for 9-bit characters

242.4 characters per second for 10-bit characters

220.4 characters per second for 11-bit characters

When the character rate is:

from 300 to 303 characters per second for 8-bit characters

from 266.7 to 269.3 characters per second for 9-bit characters

from 240 to 242.2 characters per second for 10-bit characters

from 218.2 to 220.4 characters per second for 11-bit characters

the start-stop to synchronous converter in the modem transmitter shall as often as is necessary delete the stop bits of the incoming characters. No more than one stop bit shall be deleted for any 8 consecutive characters.

When the character rate provided by the DTE on circuit 103 is less than:

300 characters per second for 8-bit characters

266.7 characters per second for 9-bit characters

240 characters per second for 10-bit characters

218.2 characters per second for 11-bit characters

the start-stop to synchronous converter in the modem is transmitting more bits per second than are provided by the DTE. The converter shall therefore insert extra stop bits in between the transmitted characters.

In Mode 4 the character rates are half those for Mode 2.

4.1.2 *Extended signalling rate range (optional)*

Certain DTEs and multiplexers are not within the +1% overspeed limit. Facilities may therefore be provided to enable the modem to accept data from a DTE having an intracharacter signalling rate of 2400 or 1200 bit/s +2.3%, −2.5%, with 8, 9, 10 or 11 bits per character by deletion of up to one stop bit in any four consecutive characters. A modem transmitter set to work with 2.3% maximum overspeed can handle data received from a DTE in accordance with § 4.1.1.

4.1.3 *Break signal*

If the converter detects M to $2M+3$ bits all of "start" polarity, where M is the number of bits per character in the selected format, the converter shall transmit $2M+3$ bits of "start" polarity. If the converter detects more than $2M+3$ bits all of "start" polarity the converter shall transmit all these bits as "start" polarity.

Note – The DTE must transmit on circuit 103 at least $2M$ bits of "stop" polarity after the "start" polarity break signal before sending further data characters. This ensures the receiving modem can regain character synchronism.

4.2 *Receiver*

The intracharacter signalling rate provided to the DTE over circuit 104 shall be in the range 1200 to 1221 bit/s when operating in Mode 4 and in the range 2400 to 2442 bit/s when operating in Mode 2. The nominal length of the start and data elements for all characters shall be the same. The length of the stop element shall not be reduced by more than 12.5% for the basic signalling rate range (or 25% for the optional extended signalling rate range) to allow for overspeed in the transmitting terminal.

The use of the basic signalling rate range is preferred since it results in lower distortion. The choice of range shall be made at the time of installation, and shall be the same for both transmitter and receiver. It is not intended to be under customer control.

4.2.1 *Break signal*

The $2M + 3$ or more bits of "start" polarity received from the transmitting modem shall be output on circuit 104. The modem shall then regain character synchronism from the following "stop" to "start" transition.

5 Scrambler and descrambler

5.1 *Scrambler*

A self synchronizing scrambler having the generating polynomial $1 \oplus x^{-14} \oplus x^{-17}$ shall be included in the modem transmitter. The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. The scrambler output data sequence shall thus be:

$$D_s = D_i \oplus D_s \cdot x^{-14} \oplus D_s \cdot x^{-17}$$

where

D_s is the data sequence at the output of the scrambler

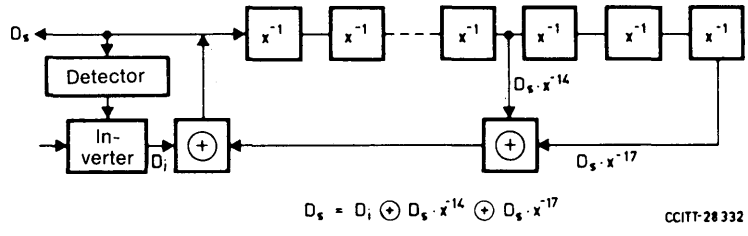
D_i is the data sequence applied to the scrambler

$\oplus$ denotes module 2 addition

$\cdot$ denotes binary multiplication.

Figure 3/V.22 *bis* shows a suitable implementation.

To prevent occasional inadvertent instigation of remote loop 2 caused by scrambler lockup, circuitry shall be included to detect a sequence of 64 consecutive ones at the scrambler output (D_s) and, if detected, invert the next input to the scrambler (D_i) and reset the counter of 64 consecutive ones. This circuitry shall operate whenever the scrambler is operational. No scrambler initialization is required during the handshake or retrain sequence.



Note – Marks (binary 1) and spaces (binary 0) at the V. 24 interface correspond to ones and zeros, respectively, in this logic diagram.

FIGURE 3/V.22 *bis*
Scrambler

5.2 *Descrambler*

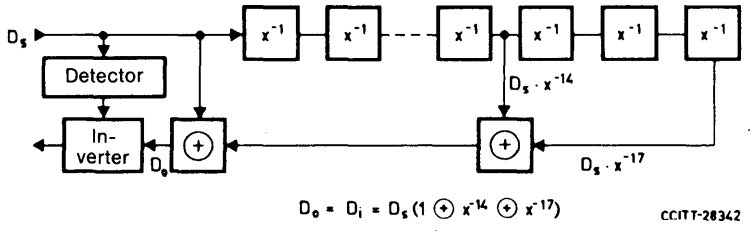
A self synchronizing descrambler having the polynomial $1 \oplus x^{-14} \oplus x^{-17}$ shall be provided in the modem receiver. The message data sequence produced after demodulation shall be effectively multiplied by the generating polynomial $1 \oplus x^{-14} \oplus x^{-17}$ to form the descrambled message. The coefficients of the recovered message sequence taken in descending order form the output data sequence D_o, which is given by

$$D_o = D_s (1 \oplus x^{-14} \oplus x^{-17})$$

where the notation is as defined in § 5.1.

Circuitry may be included to detect a sequence of 64 consecutive ones at the input to the descrambler (D_s) and, if detected, invert the next output from the descrambler (D_o). This detector shall operate whenever the descrambler is operational.

Figure 4/V.22 *bis* shows a suitable implementation.



Note – Marks (binary 1) and spaces (binary 0) at the V. 24 interface correspond to ones and zeros, respectively, in this logic diagram.

FIGURE 4/V.22 *bis*

Descrambler

6 Operating sequences

6.1 *Channel allocation and signalling rate selection*

6.1.1 *GSTN*

On the general switched telephone network, the modem at the calling data station shall transmit in the low channel and receive in the high channel (call mode). The modem at the answering data station shall receive in the low channel and transmit in the high channel (answer mode).

In some situations however, such as when calls are established on the GSTN by operators, bilateral agreement on channel allocations will be necessary.

Signalling rate selection at the call mode modem shall be either manual or by means of a logical condition applied on circuit 111 (if this circuit is provided). The handshake sequence, as defined in § 6.3.1, allows each modem to automatically condition itself to operate at the correct signalling rate.

6.1.2 *Point-to-point leased circuits*

Channel allocation and signalling rate selection on point-to-point leased circuits will, in general, be by bilateral agreement between users.

6.2 *V.25 automatic answering sequence*

The V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted in national connections on point-to-point leased circuits or on the GSTN, where permitted by the Administrations.

6.3 *Handshake sequence*

6.3.1 *GSTN*

The means of achieving synchronism between the calling modem and the answering modem on international GSTN connections is shown in Figures 5/V.22 *bis*, 6/V.22 *bis* and 7/V.22 *bis*. Both calling and answering modems shall be manually conditioned to operate either in the synchronous modes (Modes 1 and 3), or in the start-stop modes (Modes 2 and 4). If both calling and answering modems are V.22 *bis* modems, the handshake will normally condition both modems to operate at 2400 bit/s. If however one or both of the modems has been set to operate at 1200 bit/s, either manually or via circuit 111, then the handshake will condition both modems to operate at 1200 bit/s. If either the calling or answering modem is a V.22 modem operating in V.22 Modes i) or ii) the handshake will condition both the V.22 *bis* and V.22 modem to operate at 1200 bit/s. The signalling rate is communicated to the DTE by a logical condition on circuit 112. The handshake sequence is independent of which modem, calling or answering, is connected to line first.

6.3.1.1 *Interworking at 2400 bit/s*

6.3.1.1.1 *Calling modem*

a) On connection to line the calling modem shall be conditioned to receive signals in the high channel at 1200 bit/s and transmit signals in the low channel at 1200 bit/s in accordance with § 2.5.2.2. It shall apply an ON condition to circuit 107 in accordance with Recommendation V.25. The modem shall initially remain silent.

b) After 155 ± 10 ms of unscrambled binary 1 has been detected, the modem shall remain silent for a further 456 ± 10 ms then transmit an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s for 100 ± 3 ms. Following this signal the modem shall transmit scrambled binary 1 at 1200 bit/s.

c) If the modem detects scrambled binary 1 in the high channel at 1200 bit/s for 270 ± 40 ms, the handshake shall continue in accordance with §§ 6.3.1.2.1 c) and d). However, if unscrambled repetitive double dibit 00 and 11 at 1200 bit/s is detected in the high channel, then at the end of receipt of this signal the modem shall apply an ON condition to circuit 112.

d) 600 ± 10 ms after circuit 112 has been turned ON the modem shall begin transmitting scrambled binary 1 at 2400 bit/s, and 450 ± 10 ms after circuit 112 has been turned ON the receiver may begin making 16-way decisions.

e) Following transmission of scrambled binary 1 at 2400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the modem shall be ready to transmit data at 2400 bit/s.

f) When 32 consecutive bits of scrambled binary 1 at 2400 bit/s have been detected in the high channel the modem shall be ready to receive data at 2400 bit/s and shall apply an ON condition to circuit 109.

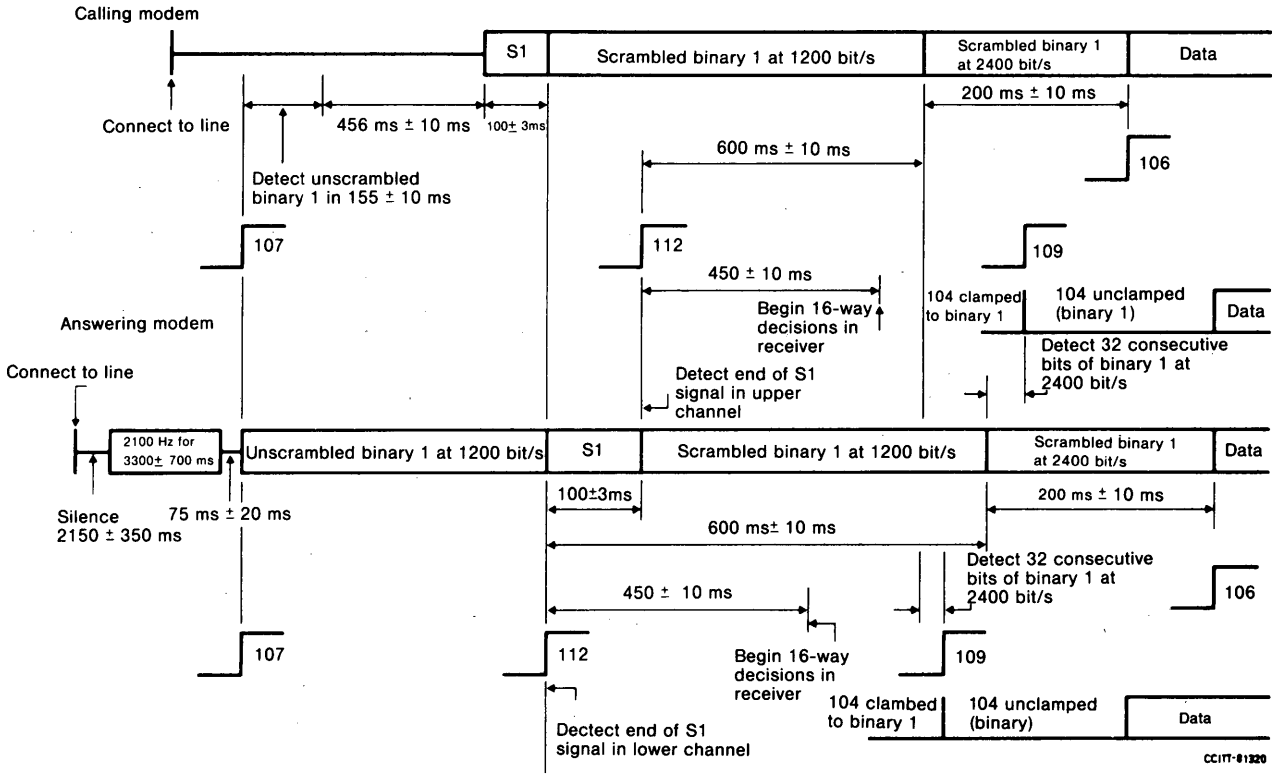
6.3.1.1.2 *Answering modem*

a) On connection to line the answering modem shall be conditioned to transmit signals in the high channel at 1200 bit/s in accordance with § 2.5.2.2 and receive signals in the low channel at 1200 bit/s. Following transmission of the answer sequence in accordance with Recommendation V.25, the modem shall apply an ON condition to circuit 107 and then transmit unscrambled binary 1 at 1200 bit/s.

b) If the modem detects scrambled binary 1 or 0 in the low channel at 1200 bit/s for 270 ± 40 ms, the handshake shall continue in accordance with §§ 6.3.1.2.2 b) and c). However, if unscrambled repetitive double dibit 00 and 11 at 1200 bit/s is detected in the low channel, at the end of receipt of this signal the modem shall apply an ON condition to circuit 112 and then transmit an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s for 100 ± 3 ms. Following these signals the modem shall transmit scrambled binary 1 at 1200 bit/s.

c) 600 ± 10 ms after circuit 112 has been turned ON the modem shall begin transmitting scrambled binary 1 at 2400 bit/s, and 450 ± 10 ms after circuit 112 has been turned ON the receiver may begin making 16-way decisions.

d) Following transmission of scrambled binary 1 at 2400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the modem shall be ready to transmit data at 2400 bit/s.



V.22 bis signal:
S1 = Unscrambled double dibit 00 and 11 at 1200 bit/s for 100 ± 3 ms.

FIGURE 5/V.22 *bis*

Handshake sequence at 2400 bit/s (with V.25 automatic ansvering)

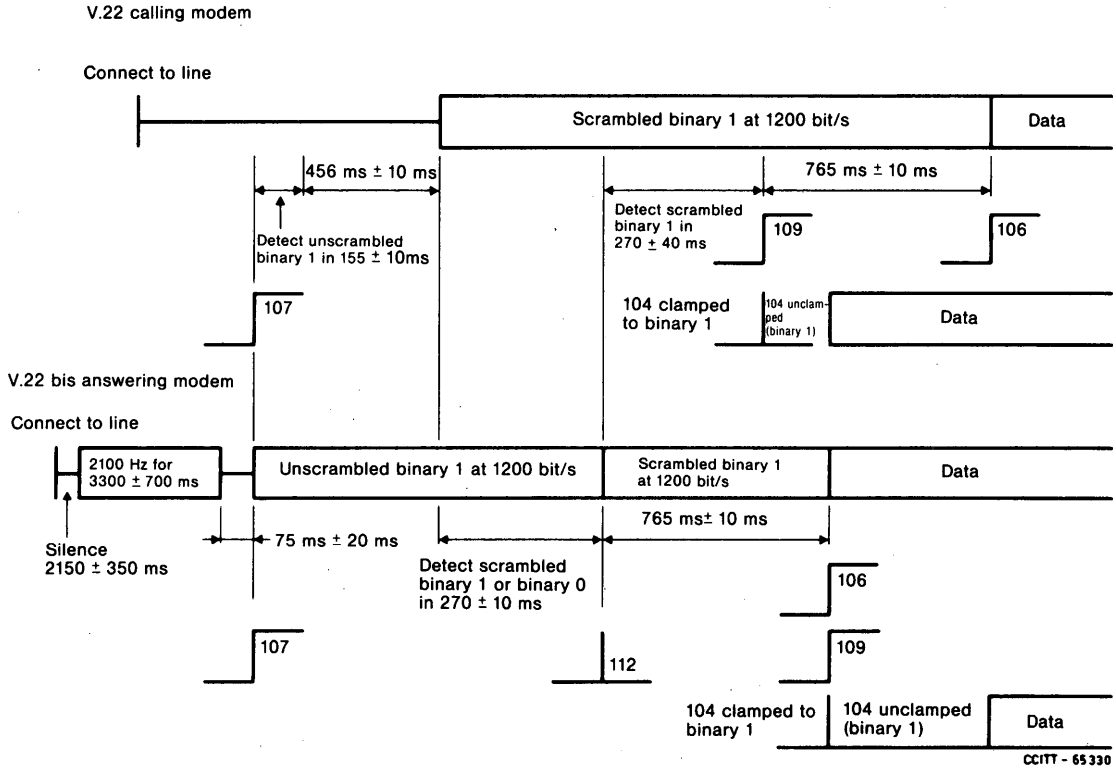


FIGURE 6/V.22 *bis*

Handshake sequence at 1200 bit/s with V.22 calling modem (with V.25 automatic answering)

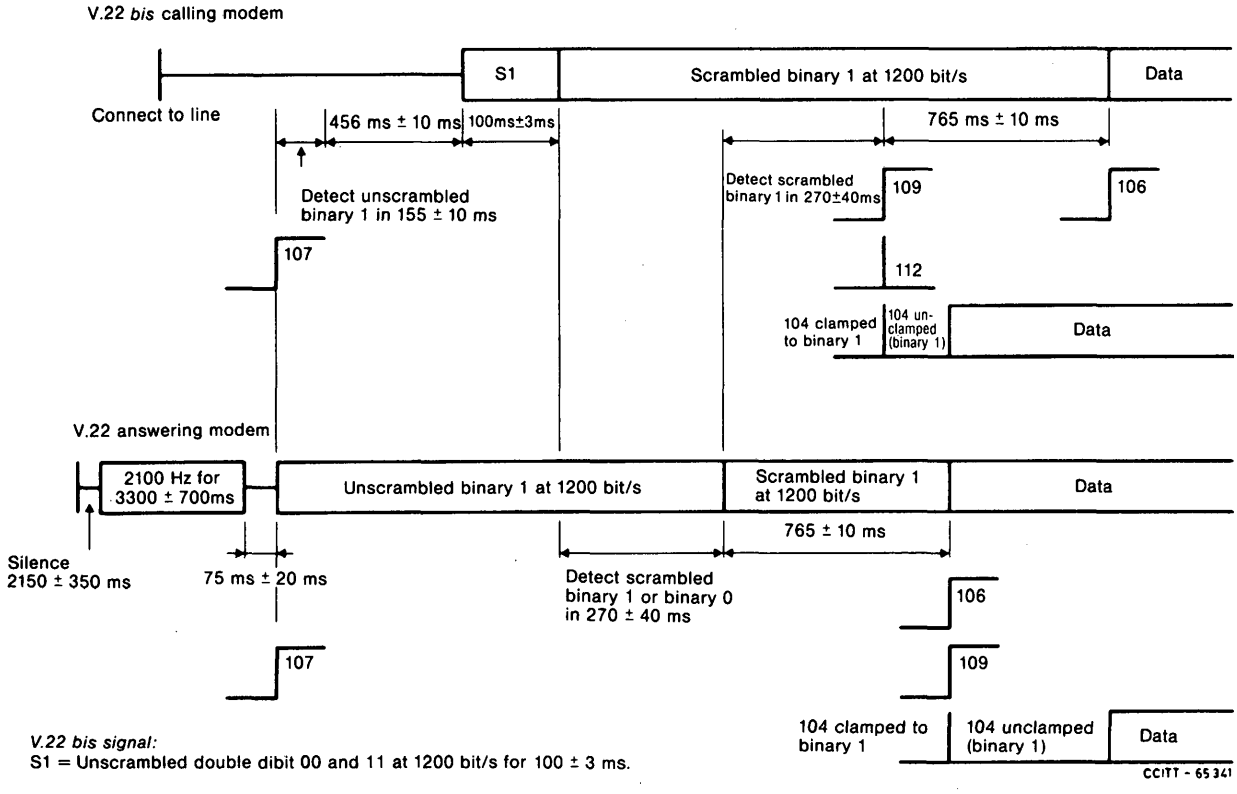


FIGURE 7/V.22 *bis*

Handshake sequence at 1200 bit/s with V.22 answering modem (with V.25 automatic answering)

e) When 32 consecutive bits of scrambled binary 1 at 2400 bit/s have been detected in the low channel the modem shall be ready to receive data at 2400 bit/s and shall apply an ON condition to circuit 109.

6.3.1.2 *Interwoking at 1200 bit/s*

The following handshake is identical to the Recommendation V.22 alternative A and B handshake.

6.3.1.2.1 *Calling modem*

a) On connection to line the calling modem shall be conditioned to receive signals in the high channel at 1200 bit/s and transmit signals in the low channel at 1200 bit/s in accordance with § 2.5.2.2. It shall apply an ON condition to circuit 107 in accordance with Recommendation V.25. The modem shall initially remain silent.

b) After 155 ± 10 ms of unscrambled binary 1 has been detected, the modem shall remain silent for a further 456 ± 10 ms then transmit scrambled binary 1 at 1200 bit/s (a preceding V.22 *bis* signal, as shown in Figure 7/V.22 *bis*, would not affect the operation of a V.22 answer modem).

c) On detection of scrambled binary 1 in the high channel at 1200 bit/s for 270 ± 40 ms the modem shall be ready to receive data at 1200 bit/s and shall apply an ON condition to circuit 109 and an OFF condition to circuit 112.

d) 765 ± 10 ms after circuit 109 has been turned ON, circuit 106 shall be conditioned to respond to circuit 105 and the modem shall be ready to transmit data at 1200 bit/s.

6.3.1.2.2 *Answering modem*

a) On connection to line the answering modem shall be conditioned to transmit signals in the high channel at 1200 bit/s in accordance with § 2.5.2.2 and receive signals in the low channel at 1200 bit/s.

Following transmission of the answer sequence in accordance with V.25 the modem shall apply an ON condition to circuit 107 and then transmit unscrambled binary 1 at 1200 bit/s.

b) On detection of scrambled binary 1 or 0 in the low channel at 1200 bit/s for 270 ± 40 ms the modem shall apply an OFF condition to circuit 112 and shall then transmit scrambled binary 1 at 1200 bit/s.

c) After scrambled binary 1 has been transmitted at 1200 bit/s for 765 ± 10 ms the modem shall be ready to transmit and receive data at 1200 bit/s, shall condition circuit 106 to respond to circuit 105 and shall apply an ON condition to circuit 109.

Note - Manufacturers may wish to note that in certain countries, for national purposes, modems are in service which emit an answering tone of 2225 Hz instead of unscrambled binary 1.

6.3.2 *Point-to-point leased circuits*

6.3.2.1 *Interworking at 2400 bit/s*

Operation on leased circuits shall be continuous carrier in both directions. On initial power on and after line signal interruptions, operation shall be according to § 6.5.

6.4 *Retrain sequence (2400 bit/s operation)*

A retrain may be initiated during data transmission between two V.22 *bis* modems if either modem incorporates a means of detecting loss of equalization.

Transmission of a retrain sequence shall be initiated either by detection of loss of equalization or by detection of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem.

The following sequence of events shall take place during the retrain:

a) Following detection of loss of equalization or the end of detection of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem, the OFF condition shall be applied to circuit 106 and circuit 104 may be clamped to binary 1. The modem shall transmit an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s for 100 ± 3 ms. Following this signal the modem shall transmit scrambled binary 1 at 1200 bit/s.

b) 600 ± 10 ms after the end of detection of unscrambled repetitive double dibit 00 and 11 at 1200 bit/s from the distant modem, the modem shall begin transmitting scrambled binary 1 at 2400 bit/s and 450 ± 10 ms after the end of this detection the receiver may begin making 16-way decisions.

c) Following transmission of scrambled binary 1 at 2400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the modem shall be ready to transmit data at 2400 bit/s.

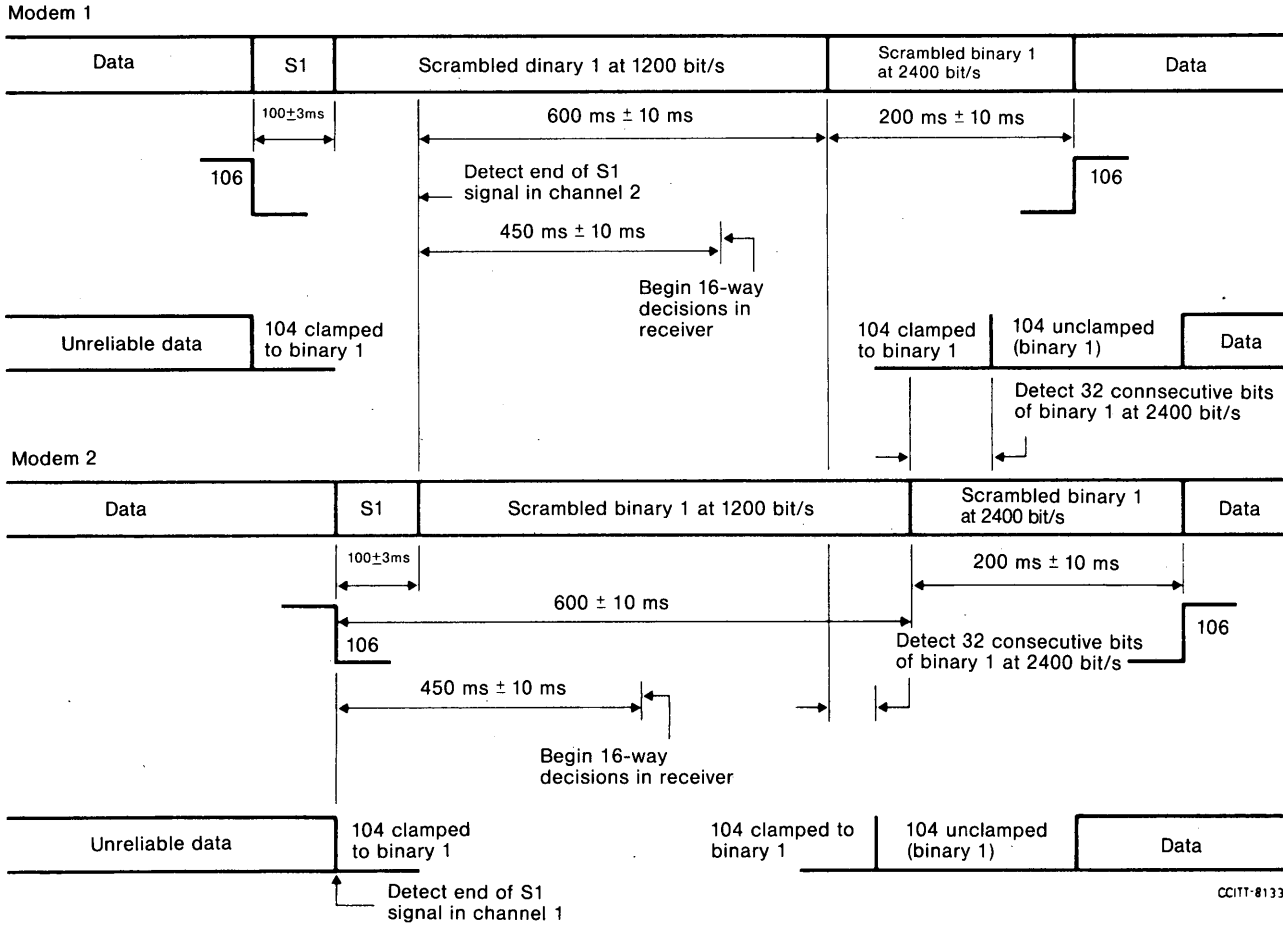
d) When 32 consecutive bits of scrambled binary 1 at 2400 bit/s have been detected from the remote modem, the modem shall be ready to receive data at 2400 bit/s and shall remove the clamp from circuit 104.

A retrain between two modems is shown in Figure 8/V.22 *bis*. Clocks presented on circuits 114 and 115 shall remain at 2400 bit/s during the entire retrain sequence.

If a modem has transmitted a retrain signal and has not received unscrambled repetitive double dibit 00 and 11 at 1200 bit/s immediately prior, or during, or within a time interval equal to the maximum expected two-way propagation delay, the modem shall return to the beginning of the retrain signal as defined above and repeat the procedure until unscrambled repetitive double dibit 00 and 11 is received from the remote modem. A time interval of 1.2 seconds is recommended for the maximum expected two-way propagation delay.

If the modem fails to synchronize on the received retrain sequence, the modem shall transmit another retrain signal.

During this retraining, circuits 109 and 107 shall remain ON.



V.22 bis signal:
S1 = Unscrambled double dibit 00 and 11 at 1200 bit/s for 100 ± 3 ms.

FIGURE 8/V.22 *bis*
A retrain at 2400 bit/s

6.5 *Operation after loss of line signal*

When the modem detects loss of received line signal (as specified in §§ 3.2 and 3.3) it shall turn OFF circuit 109 and shall clamp circuit 104 to binary 1. If received line signal is then detected (as specified in §§ 3.2 and 3.3) the modem shall turn ON circuit 109 but shall leave circuit 104 clamped to binary 1. If during the next 100 ms the modem detects a retrain sequence it shall proceed according to § 6.4 above. If the modem has not detected a retrain sequence by the end of the same 100 ms it shall remove the clamp from circuit 104. If at any time after turning ON circuit 109 following a drop out the modem detects loss of equalization, it shall proceed according to § 6.4 above.

6.6 *Fallback from 2400 bit/s to 1200 bit/s working*

(for further study.)

7 Testing facilities

7.1 *Test loops*

Test loops 2 (local and remote) and 3 as defined in Recommendation V.54 shall be provided. Interface operation shall be as defined in Recommendation V.54. Instigation and termination sequences are not compatible with Recommendation V.54.

7.1.1 *Instigation of remote loop 2*

Signals controlling the application of remote loop 2 may only be transmitted after the synchronizing handshake has been completed.

As in Recommendation V.54, the modems are referred to as Modem A and Modem B.

When Modem A is instructed to instigate a remote loop 2, the modem shall transmit an initiation signal of unscrambled binary 1 at 2400 bit/s (or 1200 bit/s).

Modem B shall detect 154-231 ms of the initiation signal, and then transmit to Modem A scrambled alternating binary ones and zeros (reversals) at 2400 bit/s (or 1200 bit/s).

Modem A shall detect 231-308 ms of scrambled reversals, cease transmission of the initiation signal, and then transmit scrambled binary 1 at 2400 bit/s (or 1200 bit/s).

Modem B shall detect the loss of initiation signal and achieve loop 2 within Modem B.

Modem A, upon receiving 231-308 ms of scrambled binary 1 shall indicate to the DTE that it may begin sending test messages.

7.1.2 *Termination of remote loop 2*

When Modem A is instructed to terminate a remote loop 2 the line signal shall be suppressed for a period of 77 ± 10 ms, after which transmission shall be restored.

Modem B detects the loss of line signal in 40 to 65 ms and detects the re-appearance of the signal within 155 ± 50 ms, after which the modem B returns to normal operation.

7.2 *Self tests*

7.2.1 *Self test end-to-end*

Upon activation of the self test switch, an internally generated data pattern of alternative binary ones and zeros (reversals) at the selected bit rate shall be applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals, shall be connected to the output of the descrambler. The presence of errors shall be indicated by a visual indicator. All generating interchange circuits except 114 (if used), 115, 125 and 142 shall be clamped to the binary 1 or OFF condition. If circuit 113 is used, the DCE shall disregard this interchange circuit and use its internal clock.

7.2.2 *Self test with loop 3*

Loop 3 shall be applied to the modem as defined in Recommendation V.54. The self-test switch shall be activated and DCE operation shall be as in § 7.2.1.

7.2.3 *Self test with remote loop 2*

The modem shall be conditioned to instigate a loop 2 at the remote modem as specified in § 7.1. The self-test switch shall be activated and DCE operation shall be as in § 7.2.1.

It shall be possible to perform the above tests (in §§ 7.2.1, 7.2.2 and 7.2.3) with or without the DTE connected to the modem. These tests employ an internally generated data pattern that is controlled by a switch on the DCE.

7.2.4 During any self-test mode, interchange circuits 103, 105 and 108 will be ignored. Note that self tests do not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver.

Note – Inclusion of remote loop signalling according to Recommendation V.54 is for further study.

600/1200-BAUD MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

(Geneva, 1964; amended at Mar del Plata, 1968, Geneva, 1972, 1976 and 1980, and at Malaga-Torremolinos, 1984)

Note – The modem, designed for use on connections set up by switching in the general telephone network, can obviously be used on leased lines.

1 The principal characteristics recommended for a modem to transmit data at medium speed in the general switched telephone network are as follows:

- use of modulation rates up to 600/1200 bauds on the communication channel (see Recommendation V.5);
- frequency modulation with synchronous or asynchronous mode of operation;
- inclusion of a backward channel at modulation rates up to 75 bauds for error control, use of this channel being optional.

2 Modulation rates and characteristic frequencies for the forward data-transmission channel

	F_0	F_Z (symbol 1, mark)	F_A symbol 0, space)
Mode 1: up to 600 bauds	1500 Hz	1300 Hz	1700 Hz
Mode 2: up to 1200 bauds	1700 Hz	1300 Hz	2100 Hz

It is understood that the modem would be used in mode 1 when the presence of long loaded cables and/or the presence on some connections of signalling receivers operating close to 2000 Hz would prevent satisfactory transmission in mode 2. The modem could be used in mode 2 on suitable connections.

3 Tolerances on the characteristic frequencies for the forward channel

It should be possible with all rates of modulation to permit a tolerance, at the transmitter, of ± 10 Hz on both the F_A and F_Z frequencies. This tolerance should be considered as a limit.

Acceptance of these tolerances would give a tolerance of ± 10 Hz for the mean-frequency $F_0 = (F_A + F_Z)/2$.

The tolerance on the frequency difference $F_A - F_Z$ with regard to the nominal value would be ± 20 Hz.

A maximum frequency drift of ± 6 Hz has been assumed in the connection between the modems which might consist of several carrier circuits connected in tandem. This would make the tolerances on the mark and space frequencies at the receiving modem ± 16 Hz.

4 Modulation rate and characteristic frequencies for the backward channel

The modulation rate and characteristic frequencies for the backward channel are as follows:

	F_Z (symbol 1, mark)	F_A (symbol 0, space)
Modulation rate up to 75 bauds	390 Hz	450 Hz

In the absence of any signal on the backward channel interface, the condition Z signal is to be transmitted.

5 Tolerances on the characteristic frequencies of the backward channel

As the backward channel is a VF telegraph-type channel, the frequency tolerances should be as recommended in Recommendation R.35 [1] for frequency-shift voice-frequency telegraphy.

The ± 6-Hz frequency drift in the connection between the modems postulated in § **3** above would produce additional distortion in the backward channel. This should be taken into account in the design.

6 Division of power between the forward and backward channels

Considering the following table which shows the levels of power for total power remaining equal to 1 mW:

Forward channel level	*Backward channel level*
(dBm)	(dBm)
0	$-\infty$
−1	−7
−2	−4
−3	−3

equal division of power between the forward and backward channels could be recommended provisionally.

7 The following information is provided to assist equipment manufacturers:

a) The nominal range of attenuations in subscriber-to-subscriber connections is from 5 to 30 dB at the reference frequency (800 or 1000 Hz), assuming up to 35-dB attenuation at the recommended mean frequency (F_0) of the forward channel.

b) A convenient range of sensitivity at the mean frequency F_0 for data receivers has been found to be −40 to 0 dBm for the forward channel at the subscribers' terminals.

c) The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

8 Interchange circuits

The configurations of interchange circuits are those essential for the particular switched network or leased circuit requirement as indicated in Tables 1/V.23 and 2/V.23. Where one or more of such requirements are provided in a modem, then all the appropriate interchange circuits should be provided.

8.1 *List of interchange circuits essential for the modems when used on the general switched telephone network, including terminals equipped for manual calling or answering or automatic calling or answering* (see Table 1/V.23).

8.2 *List of interchange circuits essential for the modems when used on non-switched leased telephone circuits* (see Table 2/V.23)

8.3 *Response times of circuits 106 and 109, 121 and 122*

8.3.1 *Definitions*

8.3.1.1 Circuits 109 and 122 response times are the times that elapse between the connection or removal of a tone to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuits 109 and 122.

The test tone should have a frequency corresponding to the characteristic frequency of binary 1 and be derived from a source with an impedance equal to the nominal input impedance of the modem.

The level of the test tone should fall within the level range between 3 dB above the actual threshold of the received line signal detector and the maximum admissible level of the received signal. At all levels within this range the measured response times shall be within the specified limits.

TABLE 1/V.23

Interchange circuit		Forward (data) channel one-way system (Note 1)				Forward (data) channel either way system (Note 1)	
No.	Designation	Without backward channel		With backward channel		Without backward channel	With backward channel
		Transmit end	Receive end	Transmit end	Receive end		
102	Signal ground or common return	X	X	X	X	X	X
103	Transmitted data	X	–	X	–	X	X
104	Received data	–	X	–	X	X	X
105	Request to send	–	–	–	–	X	X
106	Ready for sending	X	–	X	–	X	X
107	Data set ready	X	X	X	X	X	X
108/1 or 108/2 (Note 2)	Connect data set to line Data terminal ready	X	X	X	X	X	X
109	Data channel received line signal detector	–	X	–	X	X	X
111	Data signalling rate selector (DTE)	X	X	X	X	X	X
114 (Note 3)	Transmitter signal element timing (DCE)	X	–	X	–	X	X
115 (Note 3)	Receiver signal element timing (DCE)	–	X	–	X	X	X
118	Transmitted backward channel data	–	–	–	X	–	X
119	Received backward channel data	–	–	X	–	–	X
120	Transmit backward channel line signal	–	–	–	–	–	X
121	Backward channel ready	–	–	–	X	–	X
122	Backward channel received line signal detector	–	–	X	–	–	X
125	Calling indicator	X	X	X	X	X	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 9).

Note 2 – This circuit shall be capable of operation as circuit 108/1 – *Connect data set to line* or circuit 108/2 – *Data terminal ready* depending on its use.

Note 3 – These circuits are required when the optional clock is implemented in the modem.

TABLE 2/V.23

Interchange circuit		Forward (data) channel one-way system (Note 1)				Forward (data) channel either way or both ways simultaneously system (Note 1)	
No.	Designation	Without backward channel		With backward channel		Without backward channel	With backward channel
		Transmit end	Receive end	Transmit end	Receive end		
102	Signal ground or common return	X	X	X	X	X	X
103	Transmitted data	X	–	X	–	X	X
104	Received data	–	X	–	X	X	X
105	Request to send	X	–	X	–	X	X
106	Ready for sending	X	–	X	–	X	X
107	Data set ready	X	X	X	X	X	X
108/1	Connect data set to line	X	X	X	X	X	X
109	Data channel received line signal detector	–	X	–	X	X	X
111	Data signalling rate selector (DTE)	X	X	X	X	X	X
114 (Note 2)	Transmitter signal element timing (DCE)	X	–	X	–	X	X
115 (Note 2)	Receiver signal element timing (DCE)	–	X	–	X	X	X
118	Transmitted backward channel data	–	–	–	X	–	X
119	Received backward channel data	–	–	X	–	–	X
120	Transmit backward channel line signal	–	–	–	X	–	X
121	Backward channel ready	–	–	–	X	–	X
122	Backward channel received line signal detector	–	–	X	–	–	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 9).

Note 2 – These circuits are required when the optional clock is implemented in the modem.

8.3.1.2 Circuit 106 response times are from the connection of an ON or OFF condition on:

- circuit 105 (where it is provided) to the appearance of the corresponding ON or OFF condition on circuit 106;
- circuit 122 (where circuit 105 is not provided) to the appearance of the corresponding ON or OFF condition on circuit 106 in a configuration having a single data channel together with a single backward channel only.
- circuit 107 (where circuits 105 and 122 are not provided) to the appearance of the corresponding ON or OFF condition on circuit 106;

8.3.1.3 Circuit 121 response times are from the connection of an ON or OFF condition on:

- circuit 120 (where it is provided) to the appearance of the corresponding ON or OFF condition on circuit 121;
- circuit 109 (where circuit 120 is not provided) to the appearance of the corresponding ON or OFF condition on circuit 121.

8.3.2 *Response times*

TABLE 3/V.23

Circuit 106		
OFF to ON	750 ms to 1400 ms (see Note 1)	a) 20 ms to 40 ms (see Note 2) b) 200 ms to 275 ms (see Note 2)
ON to OFF	⩽ 2 ms	
Circuit 109		
OFF to ON	300 ms to 700 ms (see Note 1)	10 ms to 20 ms (see Note 1)
ON to OFF	5 ms to 15 ms	
Circuit 121		
OFF to ON	80 ms to 160 ms	
ON to OFF	⩽ 2 ms	
Circuit 122		
OFF to ON	< 80 ms	
ON to OFF	15 ms to 80 ms	

Note 1 – For automatic calling and answering, the longer response times of circuits 106 and 109 are to be used during call establishment only.

Note 2 – The choice of response times depends upon the system application:
a) no protection given against line echoes;
b) protection given against line echoes.

Note 3 – The above parameters are provisional and are the subject of further study.

8.4 *Threshold of data channel and backward channel received line signal detectors*

Level of received line signal at receive line terminals of modem for all types of connections, i.e. general switched telephone network or non-switched leased telephone circuits:

greater than	−43 dBm	circuits 109/122 ON
less than	−48 dBm	circuits 109/122 OFF

The condition of circuits 109 and 122 for levels between −43 dBm and −48 dBm is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

Where transmission conditions are known on switched or leased circuits, Administrations should be permitted at the time of modem installation to change these response levels of the received line signal detectors to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

8.5 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

i) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 milliseconds following the ON to OFF transition on circuit 105. The use of this additional delay is optional, based on system considerations;

ii) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

8.6 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types).

8.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

8.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

8.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

9 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

10 Equipment for the disablement of echo suppressors

When echo control device disabling is required, it is recommended that the procedures specified in Recommendation V.25 be followed.

11 Inclusion of a clock in the modem

A clock is not an essential item in the standardized modem. However, the modem may conveniently include a clock when used primarily for synchronous transmission.

If such a clock is included in the modem, a synchronizing pattern consisting of alternate binary 0 and binary 1 at clock rate should be transmitted for the whole interval between the OFF to ON transitions of interchange circuits 105 and 106. Users should note that part of this synchronizing pattern may appear at the distant receiver on circuit 104 after the OFF to ON transition of circuit 109. The data terminal equipment should make provision to differentiate between these false signals and true data.

Reference

[1] CCITT Recommendation *Standardization of FMVFT systems for a modulation rate of 50 bauds*, Vol. VII, Rec. R.35.

Recommendation V.24

LIST OF DEFINITIONS FOR INTERCHANGE CIRCUITS BETWEEN DATA TERMINAL EQUIPMENT AND DATA CIRCUIT-TERMINATING EQUIPMENT[1)]

(Geneva, 1964, amended at Mar del Plata, 1968, Geneva, 1972, 1976 and 1980, Malaga-Torremolinos, 1984)

1 Scope

1.1 This Recommendation applies to the interconnecting circuits being called interchange circuits at the interface between DTE and DCE for the transfer of binary data, control and timing signals and analogue signals as appropriate. This Recommendation also applies to both sides of separate intermediate equipment, which may be inserted between these two classes of equipment (see Figure 1/V.24).

Electrical characteristics for interchange circuits are detailed in appropriate Recommendations for electrical characteristics, or in certain special cases, in Recommendations for DCE.

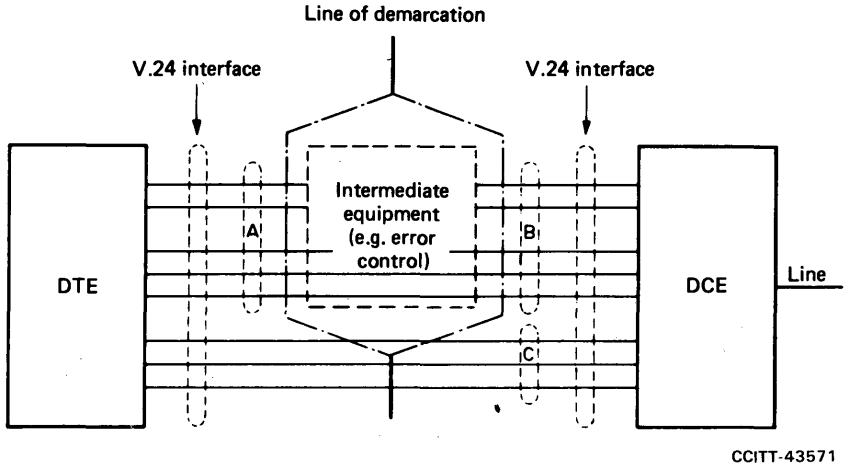
In any type of practical equipment a selection will be made from the range of interchange circuits defined in this Recommendation, as appropriate.

The actual interchange circuits to be used in a particular DCE are those indicated in the appropriate Recommendation.

The usage and operational requirements of the interchange circuits and the interaction between them are recommended in § 4. For proper operation of the DCE it is important that the guidelines in § 4 are observed.

1.2 The DCE may include signal converters, timing generators, pulse regenerators, and control circuitry, together with equipment to provide other functions such as error control, automatic calling and automatic answering. Some of this equipment may be separate intermediate equipment or it may be located in the DTE.

1) In this Recommendation the terms "data terminal equipment" and "data circuit-terminating equipment" are indicated by DTE and DCE respectively.



Without intermediate equipment the selections A and B are identical.
Selection C may be a selection specifically for automatic calling.

FIGURE 1/V.24

Illustration of general layout of equipment

1.3 The range of interchange circuits defined in this Recommendation is applicable, for example:

a) to synchronous and asynchronous data communications;

b) to data transmission on leased line service, either 2-wire or 4-wire, either point-to-point or multipoint operation;

c) to data transmission on switched network service, either 2-wire or 4-wire;

d) where short interconnecting cables are used between DTE and DCE. An explanation of short cables is given in § 2 below.

1.4 A DTE interface conforming to this Recommendation may also be used for attachment to a Public Data Network (PDN). For these cases, additional information on interchange circuit implementation and operational requirements may be recorded in Series X Recommendations.

2 Line of demarcation

The interface between DTE and DCE is located at a connector, which is the interchange point between these two classes of equipment. Separate connectors may be provided for the interchange circuits associated with the signal-conversion or similar equipment and those associated with the parallel automatic calling equipment. For mechanical characteristics of the interface refer to ISO 2110 or ISO 4902 as appropriate.

The connector(s) will not necessarily be physically attached to the DCE and may be mounted in a fixed position near the DTE.

An interconnecting cable or cables will normally be provided with the DTE. The use of short cables is recommended. Their length should be limited solely by the load capacitance and other electrical characteristics specified in the relevant Recommendation on electrical characteristics.

3 Definitions of interchange circuits

3.1 *100 series — General application*

A list of these interchange circuits is presented in tabular form in Table 1/V.24.

TABLE 1/V.24

100-series interchange circuits by category

Interchange circuit number	Interchange circuit name	Ground	Data		Control		Timing	
			From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	2	3	4	5	6	7	8	9
102	Signal ground or common return	X						
102a	DTE common return	X						
102b	DCE common return	X						
102c	Common return	X						
103	Transmitted data			X				
104	Received data		X					
105	Request to send					X		
106	Ready for sending				X			
107	Data set ready				X			
108/1	Connect data set to line					X		
108/2	Data terminal ready					X		
109	Data channel received line signal detector				X			
110	Data signal quality detector				X			
111	Data signal rate selector (DTE)					X		
112	Data signal rate selector (DCE)				X			
113	Transmitter signal element timing (DTE)							X
114	Transmitter signal element timing (DCE)						X	
115	Receiver signal element timing (DCE)						X	
116	Select standby					X		
117	Standby indicator				X			
118	Transmitted backward channel data			X				
119	Received backward channel data		X					
120	Transmit backward channel line signal					X		
121	Backward channel ready				X			
122	Backward channel received line signal detector				X			
123	Backward channel signal quality detector				X			
124	Select frequency groups					X		
125	Calling indicator				X			
126	Select transmit frequency					X		
127	Select receive frequency					X		
128	Receiver signal element timing (DTE)							X
129	Request to receive					X		
130	Transmit backward tone					X		
131	Received character timing						X	
132	Return to non-data mode					X		
133	Ready for receiving					X		
134	Received data present				X			
136	New signal					X		
140	Loopback / Maintenance test					X		
141	Local loopback					X		
142	Test indicator				X			
191	Transmitted voice answer					X		
192	Received voice answer				X			

Circuit 102 – Signal ground or common return

This conductor establishes the signal common return for unbalanced interchange circuits with electrical characteristics according to Recommendation V.28 and the d.c. reference potential for interchange circuits according to Recommendations V.10, V.11 and V.35.

Within the DCE, this circuit shall be brought to one point, and it shall be possible to connect this point to protective ground or earth by means of a metallic strap within the equipment. This metallic strap can be connected or removed at installation, as may be required to meet applicable safety regulations or to minimize the introduction of noise into electronic circuitry. Caution should be exercised to prevent the establishment of ground loops carrying high currents.

Circuit 102a – DTE common return

This conductor is connected to the DTE circuit common return and is used as the reference potential for the unbalanced Recommendation V.10-type interchange circuit receivers within the DCE.

Circuit 102b – DCE common return

This conductor is connected to the DCE circuit common return and is used as the reference potential for the unbalanced Recommendation V.10-type interchange circuit receivers within the DTE.

Note – Where a mixture of Recommendations V.10 and V.11 circuits is used in the same interface, separate provision must be made for the Recommendation V.10 common return circuits 102a and 102b, and for a d.c. reference potential conductor circuit 102, or protective ground connection, as required.

Circuit 102c – Common return

This conductor establishes the signal common return for single-current interchange circuits controlled by contact closure with electrical characteristics according to Recommendation V.31, in cases where a common return is used.

Within the equipment containing the signal source of the interchange circuit, this conductor must be isolated from signal ground and protective ground, irrespective of whether it is located within the DCE or within the DTE.

Circuit 103 – Transmitted data

Direction: To DCE

The data signals originated by the DTE:

1) to be transmitted via a data channel to one or more remote data stations,
2) to be passed to the DCE for maintenance test purposes under control of the DTE, or
3) for the programming or control of serial automatic calling DCEs,

are transferred on this circuit to the DCE.

Circuit 104 – Received data

Direction: From DCE

The data signals generated by the DCE:

1) in response to data channel line signals received from a remote data station,
2) in response to the DTE maintenance test signals, or
3) data signals generated by a serial automatic calling DCE, in response to programming or control signals from the DTE,

are transferred on this circuit to the DTE.

Note – The reception conditions for maintenance test signals are specified with circuit 107.

Circuit 105 – Request to send

Direction: To DCE

Signals on this circuit control the data channel transmit function of the DCE.

The ON condition causes the DCE to assume the data channel transmit mode.

The OFF condition causes the DCE to assume the data channel non-transmit mode, when all data transferred on circuit 103 have been transmitted.

Circuit 106 – Ready for sending

Direction: From DCE

Signals on this circuit indicate whether the DCE is prepared to accept data signals for transmission on the data channel or for maintenance test purposes under control of the DTE.

The ON condition indicates that the DCE is prepared to accept data signals from the DTE.

The OFF condition indicates that the DCE is not prepared to accept data signals from the DTE.

Circuit 107 – Data set ready

Direction: From DCE

Signals on this circuit indicate whether the DCE is ready to operate.

The ON condition, where circuit 142 is OFF or is not implemented, indicates that the signal converter or similar equipment is connected to the line and that the DCE is ready to exchange further control signals with the DTE to initiate transfer of data.

The ON condition, in conjunction with the ON condition of circuit 142, indicates that the DCE is prepared to exchange data signals with the DTE for maintenance test purposes.

The OFF condition, in conjunction with the ON condition on circuit 106, indicates that the DCE is ready to exchange data signals associated with the programming or control of serial automatic calling DCEs.

The OFF condition, in conjunction with the OFF condition on circuit 106, indicates:

1) that the DCE is not ready to operate in the data transfer phase,

2) that it has detected a fault condition which may be network or DCE dependent, or

3) that it has detected a disconnect indication from the remote station or from the network.

Note – Provision of the capability defined in 2) and 3) above is a matter for Administrations unless it is specified in a DCE Recommendation.

Circuit 108/1 – Connect data set to line

Direction: To DCE

Signals on this circuit control switching of the signal-conversion or similar equipment to or from the line.

The ON condition on this circuit may also be used to initiate a direct call facility for automatic calling DCEs.

The OFF condition causes the DCE to remove the signal-conversion or similar equipment from the line, when the transmission to line of all data previously transferred on circuit 103 and/or circuit 118 has been completed.

Circuit 108/2 – Data terminal ready

Direction: To DCE

Signals on this circuit control switching of the signal-conversion or similar equipment to or from the line.

The ON condition, indicating that the DTE is ready to operate, prepares the DCE to connect the signal-conversion or similar equipment to the line and maintains this connection after it has been established by supplementary means.

The DTE is permitted to present the ON condition on circuit 108/2 whenever it is ready to transmit or receive data.

The OFF condition causes the DCE to remove the signal-conversion or similar equipment from the line, when the transmission to line of all data previously transferred on circuit 103 and/or circuit 118 has been completed.

Circuit 109 – Data channel received line signal detector

Direction: From DCE

Signals on this circuit indicate whether the received data channel line signal is within appropriate limits, as specified in the relevant Recommendation for DCE.

Circuit 109 may also be in the ON condition during the exchange of data signals between the DCE and the DTE, associated with the programming or control of serial automatic calling DCEs.

The OFF condition indicates that the received signal is not within appropriate limits.

Circuit 110 – Data signal quality detector

Direction: From DCE

Signals on this circuit indicate whether there is a reasonable probability of an error in the data received on the data channel. The signal quality indicated conforms to the relevant DCE Recommendation.

The ON condition indicates that there is no reason to believe that an error has occurred.

The OFF condition indicates that there is a reasonable probability of an error.

Circuit 111 – Data signalling rate selector (DTE source)

Direction: To DCE

Signals on this circuit are used to select one of the two data signalling rates of a dual rate synchronous DCE, or to select one of the two ranges of data signalling rates of a dual range asynchronous DCE.

The ON condition selects the higher rate or range of rates.

The OFF condition selects the lower rate or range of rates.

Circuit 112 – Data signalling rate selector (DCE source)

Direction: From DCE

Signals on this circuit are used to select one of the two data signalling rates or ranges of rates in the DTE to coincide with the data signalling rate or range of rates in use in a dual rate synchronous or dual range asynchronous DCE.

The ON condition selects the higher rate or range of rates.

The OFF condition selects the lower rate or range of rates.

Circuit 113 – Transmitter signal element timing (DTE source)

Direction: To DCE

Signals on this circuit provide the DCE with signal element timing information.

The condition on this circuit shall be ON and OFF for nominally equal periods of time and the transition from ON to OFF condition shall nominally indicate the centre of each signal element on circuit 103.

Circuit 114 – Transmitter signal element timing (DCE source)

Direction: From DCE

Signals on this circuit provide the DTE with signal element timing information.

The condition on this circuit shall be ON and OFF for nominally equal periods of time. The DTE shall present a data signal on circuit 103 in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of circuit 114.

Circuit 115 – Receiver signal element timing (DCE source)

Direction: From DCE

Signals on this circuit provide the DTE with signal element timing information.

The condition of this circuit shall be ON and OFF for nominally equal periods of time, and a transition from ON to OFF condition shall nominally indicate the centre of each signal element on circuit 104.

Circuit 116 – Select standby

Direction: To DCE

Signals on this circuit are used to select the normal or standby facilities, such as signal converters and data channels.

The ON condition selects the standby mode of operation, causing the DCE to replace predetermined facilities by their reserves.

The OFF condition causes the DCE to replace the standby facilities by the normal. The OFF condition on this circuit shall be maintained whenever the standby facilities are not required for use.

Circuit 117 – Standby indicator

Direction: From DCE

Signals on this circuit indicate whether the DCE is conditioned to operate in its standby mode with the predetermined facilities replaced by their reserves.

The ON condition indicates that the DCE is conditioned to operate in its standby mode.

The OFF condition indicates that the DCE is conditioned to operate in its normal mode.

Circuit 118 – Transmitted backward channel data

Direction: To DCE

This circuit is equivalent to circuit 103, except that it is used to transmit data via the backward channel.

Circuit 119 – Received backward channel data

Direction: From DCE

This circuit is equivalent to circuit 104, except that it is used for data received on the backward channel.

Circuit 120 – Transmit backward channel line signal

Direction: To DCE

This circuit is equivalent to circuit 105, except that it is used to control the backward channel transmit function of the DCE.

The ON condition causes the DCE to assume the backward channel transmit mode.

The OFF condition causes the DCE to assume the backward channel non-transmit mode, when all data transferred on circuit 118 have been transmitted to line.

Circuit 121 – Backward channel ready

Direction: From DCE

This circuit is equivalent to circuit 106, except that it is used to indicate whether the DCE is conditioned to transmit data on the backward channel.

The ON condition indicates that the DCE is conditioned to transmit data on the backward channel.

The OFF condition indicates that the DCE is not conditioned to transmit data on the backward channel.

Circuit 122 – Backward channel received line signal detector

Direction: From DCE

This circuit is equivalent to circuit 109, except that it is used to indicate whether the received backward channel line signal is within appropriate limits, as specified in the relevant Recommendation for DCE.

Circuit 123 – Backward channel signal quality detector

Direction: From DCE

This circuit is equivalent to circuit 110, except that it is used to indicate the signal quality of the received backward channel line signal.

Circuit 124 – Select frequency groups

Direction: To DCE

Signals on this circuit are used to select the desired frequency groups available in the DCE.

The ON condition causes the DCE to use all frequency groups to represent data signals.

The OFF condition causes the DCE to use a specified reduced number of frequency groups to represent data signals.

Circuit 125 – Calling indicator

Direction: From DCE

Signals on this circuit indicate whether a calling signal is being received by the DCE.

The ON condition indicates that a calling signal is being received.

The OFF condition indicates that no calling signal is being received, and this condition may also appear during interruptions of a pulse-modulated calling signal.

Circuit 126 – Select transmit frequency

Direction: To DCE

Signals on this circuit are used to select the required transmit frequency of the DCE.

The ON condition selects the higher transmit frequency.

The OFF condition selects the lower transmit frequency.

Circuit 127 – Select receive frequency

Direction: To DCE

Signals on this circuit are used to select the required receive frequency of the DCE.

The ON condition selects the lower receive frequency.

The OFF condition selects the higher receive frequency.

Circuit 128 – Receiver signal element timing (DTE source)

Direction: To DCE

Signals on this circuit provide the DCE with signal element timing information.

The condition on this circuit shall be ON and OFF for nominally equal periods of time. The DCE shall present a data signal on circuit 104 in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of the signal on circuit 128.

Circuit 129 – Request to receive

Direction: To DCE

Signals on this circuit are used to control the receive function of the DCE.

The ON condition causes the DCE to assume the receive mode.

The OFF condition causes the DCE to assume the non-receive mode.

Circuit 130 – Transmit backward tone

Direction: To DCE

Signals on this circuit control the transmission of a backward channel tone.

The ON condition causes the DCE to transmit a backward channel tone.

The OFF condition causes the DCE to stop the transmission of a backward channel tone.

Circuit 131 – Received character timing

Direction: From DCE

Signals on this circuit provide the DTE with character timing information, as specified in the relevant Recommendation for DCE.

Circuit 132 – Return to non-data mode

Direction: To DCE

Signals on this circuit are used to restore the non-data mode provided with the DCE, without releasing the line connection to the remote station.

The ON condition causes the DCE to restore the non-data mode. When the non-data mode has been established, this circuit must be turned OFF.

Circuit 133 – Ready for receiving

Direction: To DCE

Signals on this circuit control the transfer of data on circuit 104, indicating whether the DTE is capable of accepting a given amount of data (e.g. a block of data), specified in the appropriate Recommendation for intermediate equipment, for example, error control equipment.

The ON condition must be maintained whenever the DTE is capable of accepting data, and causes the intermediate equipment to transfer the received data to the DTE.

The OFF condition indicates that the DTE is not able to accept data, and causes the intermediate equipment to retain the data.

Circuit 134 – Received data present

Direction: From DCE

Signals on this circuit are used to separate information messages from supervisory messages, transferred on circuit 104, as specified in the appropriate Recommendation for intermediate equipment, e.g. error control equipment.

The ON condition indicates the data which represent information messages.

The OFF condition shall be maintained at all other times.

Circuit 136 – New signal

Direction: To DCE

Signals on this circuit are used to control the response times of the DCE receiver.

The ON condition of circuit 136 instructs the DCE receiver to prepare itself to detect rapidly the disappearance of the line signal (e.g., by disabling the response time circuitry associated with circuit 109). After the received line signal falls below the threshold of the received line signal detector, the DCE will:

1) turn OFF circuit 109, and
2) prepare itself to detect rapidly the appearance of a new line signal (e.g., by resetting the receiver timing recovery circuitry).

Once turned ON, circuit 136 may be turned OFF after one unit interval and must be turned OFF after circuit 109 is turned OFF. Circuit 136 shall be OFF at all other times.

Circuit 140 – Loopback/Maintenance test

Direction: To DCE

Signals on this circuit are used to initiate and release loopback or other maintenance test conditions in DCEs.

The ON condition causes initiation of the maintenance test condition.

The OFF condition causes release of the maintenance test condition.

Circuit 141 – Local loopback

Direction: To DCE

Signals on this circuit are used to control the loop 3 test condition in the local DCE.

The ON condition of circuit 141 causes the establishment of the loop 3 test condition in the local DCE.

The OFF condition of circuit 141 causes the release of the loop 3 test condition in the local DCE.

Circuit 142 – Test indicator

Direction: From DCE

Signals on this circuit indicate whether a maintenance condition exists.

The ON condition indicates that a maintenance condition exists in the DCE, precluding reception or transmission of data signals from or to a remote DTE.

The OFF condition indicates that the DCE is not in a maintenance test condition.

Circuit 191 – Transmitted voice answer

Direction: To DCE

Signals generated by a voice answer unit in the DTE are transferred on this circuit to the DCE.

The electrical characteristics of this analogue interchange circuit are part of the appropriate DCE Recommendation.

Circuit 192 – Received voice answer

Direction: From DCE

Received voice signals, generated by a voice answering unit at the remote DTE, are transferred on this circuit to the DTE.

The electrical characteristics of this analogue interchange circuit are part of the appropriate DCE Recommendation.

3.2 *200-series – Specifically for parallel automatic calling*

A list of these interchange circuits is presented in tabular form in Table 2/V.24.

For parallel automatic calling procedures, refer to Recommendation V.25 for the general switched telephone network and Recommendation S.16 [1] for the telex network.

TABLE 2/V.24

200-series interchange circuits specifically for automatic calling

Interchange circuit number	Interchange circuit name	From DCE	To DCE
201	Signal ground or common return	X	X
202	Call request		X
203	Data line occupied	X	
204	Distant station connected	X	
205	Abandon call	X	
206	Digit signal (2^0)		X
207	Digit signal (2^1)		X
208	Digit signal (2^2)		X
209	Digit signal (2^3)		X
210	Present next digit	X	
211	Digit present		X
213	Power indication	X	

Circuit 201 – Signal ground or common return

This conductor establishes the signal common reference potential for all 200-series interchange circuits. Within the parallel automatic calling equipment this circuit shall be brought to one point, and it shall be possible to connect this point to protective ground or earth by means of a metallic strap within the equipment. This metallic strap can be connected or removed at installation as may be required to meet applicable regulations or to minimize the introduction of noise into electronic circuitry. Caution should be exercised to prevent the establishment of ground loops carrying high currents.

Circuit 202 – Call request

Direction: To DCE

Signals on this circuit are used to condition the parallel automatic calling equipment to originate a call and to switch the automatic calling equipment to or from the line.

The ON condition causes the DCE to condition the parallel automatic calling equipment to originate a call and to connect this equipment to the line.

The OFF condition causes the automatic calling equipment to be removed from the line and indicates that the DTE has released the automatic calling equipment.

Circuit 203 – Data line occupied

Direction: From DCE

Signals on this circuit indicate whether or not the associated line is in use (e.g. for automatic calling, data transmission or voice communication, test procedures).

The ON condition indicates that the line is in use.

The OFF condition indicates that the line is not in use, and that the DTE may originate a call.

Circuit 204 – Distant station connected

Direction: From DCE

Signals on this circuit indicate whether a connection has been established to a remote data station (or telex station).

The ON condition indicates the receipt of a signal from a remote DCE signalling that a connection to that equipment has been established.

The OFF condition shall be maintained at all other times.

Circuit 205 – Abandon call

Direction: From DCE

Signals on this circuit indicate whether a preset time has elapsed between successive events in the calling procedure.

The ON condition indicates that the call should be abandoned.

The OFF condition indicates that call origination can proceed.

Digit signal circuits:

Circuit 206 – Digit signal (2^0)

Circuit 207 – Digit signal (2^1)

Circuit 208 – Digit signal (2^2)

Circuit 209 – Digit signal (2^3)

Direction: To DCE

On these circuits the DTE presents the code combinations shown in Table 3/V.24, being the digits of the data station (or telex station) to be called and the delimiting control characters.

TABLE 3/V.24

Information	Binary states			
	209	208	207	206
Digit 1	0	0	0	1
Digit 2	0	0	1	0
Digit 3	0	0	1	1
Digit 4	0	1	0	0
Digit 5	0	1	0	1
Digit 6	0	1	1	0
Digit 7	0	1	1	1
Digit 8	1	0	0	0
Digit 9	1	0	0	1
Digit 0	0	0	0	0
Control character EON	1	1	0	0
Control character SEP	1	1	0	1

The control character EON (end of number) causes the DCE to take appropriate action to await an answer from the called data station.

The control character SEP (separation) indicates the need for a pause between successive digits or in front of the digit series, and causes the parallel automatic calling equipment to insert the appropriate time interval.

The code combinations listed above are intended to apply only to equipment using Recommendations V.25 and S.16 [1].

Circuit 210 – Present next digit

Direction: From DCE

Signals on this circuit indicate whether the parallel automatic calling equipment is ready to accept the next code combination.

The ON condition indicates that the automatic calling equipment is ready to accept the next code combination.

The OFF condition indicates that the automatic calling equipment is not ready to accept signals on the digit signal circuits.

Circuit 211 – Digit present

Direction: To DCE

Signals on this circuit control the reading of the code combination presented on the digit signal circuits.

The ON condition causes the automatic calling equipment to read the code combination presented on the digit signal circuits.

The OFF condition on this circuit prevents the automatic calling equipment from reading a code combination on the digit signal circuits.

Circuit 213 – Power indication

Direction: From DCE

Signals on this circuit indicate whether power is available within the parallel automatic calling equipment.

The ON condition indicates that power is available within the automatic calling equipment.

The OFF condition indicates that power is not available within the automatic calling equipment.

3.3 *Circuit failures (electrical)*

The following interchange circuits, where implemented, shall be used to detect either a power-off condition in the equipment connected through the interface or the disconnection of the interconnecting cable:

Circuit 105 – Request to send
Circuit 107 – Data set ready
Circuit 108/1 – Connect data set to line
Circuit 108/2 – Data terminal ready
Circuit 120 – Transmit backward channel line signal
Circuit 202 – Call request
Circuit 213 – Power indication

The criteria used to determine a failure condition shall be specified in the appropriate Recommendation for electrical characteristics.

The receiver for these circuits shall interpret the power-off condition or the disconnection of the interconnecting cable as an OFF condition on these circuits.

3.4 *Optional circuits*

In some modem Recommendations optional facilities are defined which require control from the DTE via optional (non-essential) circuits. Additional optional facilities may exist in DCEs also requiring control via interchange circuits defined in this Recommendation.

The DCE should provide means to disable an option, when necessary, in case the DTE is not equipped with circuitry to control this option.

In case the DCE does not provide an option, proper operation of the DTE should not rely on any specific response from the DCE when the DTE activates the control circuit related to that option.

Note – DTEs may be in existence which do not comply with the above requirements. Therefore, for an interim period, DCEs not providing a certain option may provide means to respond to the DTE invocation of that option in the proper way. Especially, this may be the case for simplex or duplex DCEs not providing a carrier switch option (continuous carrier operation) but still responding with circuit 106 to circuit 105.

Furthermore, it is recommended that existing modem Recommendations be amended, where necessary, to clearly define optional facilities.

4 Operational requirements

In the following, operational requirements are given for the usage of interchange circuits. It also explains in further detail the required correlation between interchange circuits, where implemented.

4.1 *Data circuits*

It is evident that proper data transmission may be impaired when the required condition is not present on an implemented control interchange circuit. Therefore, the DTE shall not transfer, on circuit 103, data which is for transmission to line or for maintenance purposes unless an ON condition is present on all of the following four circuits, where implemented: circuit 105, circuit 106, circuit 107 and circuit 108/1 or 108/2.

The DTE may transfer, on circuit 103, data which is for the programming or control of serial automatic calling DCEs when an ON condition is present on circuits 106 and 108/2, and an OFF condition is present on circuit 107. In this situation, the condition of circuit 105 need not be considered, and may be ON for DTE convenience.

All data transferred on circuit 103 during the time an ON condition is present on all of the above four circuits, where implemented, shall be transmitted by the DCE.

Refer also to §§ 4.4 and 4.5 below for further explanation.

The DTE shall not transfer data on circuit 118 unless an ON condition is present on all of the following four circuits, where implemented: circuit 120, circuit 121, circuit 107 and circuit 108/1 or 108/2.

All data transferred on circuit 118 during the time an ON condition is present on all of the above four circuits, where implemented, shall be transmitted by the DCE.

4.2 *Idle periods*

During intervals when circuit 105 and circuit 106 are in the ON condition and no data are available for transmission, the DTE may transmit binary 1 condition, reversals or other sequences to maintain timing synchronizing, e.g. SYN coded characters, idle characters according to the data link control procedure used, etc.

Specific requirements, where applicable, are stated in the appropriate DCE Recommendations.

4.3 *Clamping*

4.3.1 In all applications the DCE shall hold, where implemented:

a) circuit 104 in the binary 1 condition when circuit 109 is in the OFF condition, and

b) circuit 119 in the binary 1 condition when circuit 122 is in the OFF condition.

4.3.2 In addition a DCE constrained to half-duplex operation on a 2-wire line shall also hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition, and for a short time interval (to be specified in Recommendations for DCE) following the ON to OFF transition on circuit 105; and

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition, when circuit 120 is in the ON condition, and for a short time interval (to be specified in Recommendations for DCE) following the ON to OFF transition on circuit 120.

4.4 *Operation of circuits 107, 108/1 and 108/2*

Signals on circuit 107 are to be considered as responses to signals which initiate connection to line, e.g. circuit 108/1. However, the conditioning of a data channel, such as equalization and clamp removal, cannot be expected to occur before circuit 107 is turned ON.

When the DCE is conditioned for automatic answering of calls, connection to the line occurs only in response to a combination of the calling signal and an ON condition on circuit 108/2.

A wiring option shall be provided within the DCE to select either circuit 108/1 or circuit 108/2 operation.

In certain leased line applications, circuit 108 might not be implemented, in which case the condition on this circuit is assumed to be permanently ON.

Under certain test conditions, both the DTE and the DCE may exercise some of the interchange circuits. Thus, when circuit 107 is OFF and circuit 108/1 or 108/2 is OFF, the DTE is to ignore the conditions on any interchange circuit from the DCE, except those on circuit 125 and the timing circuits, and the DCE is to ignore the conditions on any interchange circuit from the DTE.

The OFF condition on circuit 108/1 or 108/2 shall not disable the operation of circuit 125.

When circuit 108/2 is in the ON condition and circuit 107 is in the OFF condition, the DTE may communicate with serial automatic calling DCEs on circuits 103 and 104. This state is recognized by an ON condition on circuit 106.

Under the loop test conditions defined in Recommendation V.54, circuit 107 shall be in the OFF condition and not respond to circuit 108/1 or 108/2 when the DTE is not involved with maintenance testing. Circuit 142 shall be in the ON condition and circuit 107 shall respond to circuit 108/1 or 108/2 when the DTE is involved in maintenance testing with the local or remote DCE.

When circuit 108/1 or 108/2 is turned OFF, it shall not be turned ON again until circuit 107 is turned OFF by the DCE and the OFF state of circuit 107 has been recognized by the DTE.

In the case where the DCE turns circuit 107 OFF first (see Note), the DTE shall consider the call aborted and shall proceed as described below:

Note – The provision of this mode of operation is a matter for Administrations unless it is specified in a DCE Recommendation.

4.4.1 In the case of circuit 108/1, the DTE shall turn this circuit OFF with a minimal delay and shall hold the circuit in the OFF condition for a minimum of 500 ms and until it is ready to initiate a new call, or to answer an incoming call.

The DCE shall not answer an incoming call or initiate a new call until circuit 108/1 has first been turned OFF and then back ON again.

4.4.2 In the case of circuit 108/2, selection of a preferred protocol is left for further study.

Administrations, manufacturers and users are cautioned that protocols developed for this case may involve "lock-up" situations or unauthorized access to data bases.

4.5 *Interrelationship of circuits 103, 105 and 106*

The DTE signals its intent to transmit data by turning ON circuit 105. It is then the responsibility of the DCE to enter the transmit mode, i.e. be prepared to transmit data, and also to alert the remote DCE and condition it to receive data. The means by which a DCE enters the transmit mode and alerts and conditions the remote DCE are described in the appropriate DCE Recommendation.

When the transmitting DCE turns circuit 106 ON with circuit 107 in the ON condition, the DTE is permitted to transfer data across the interface on circuit 103. By turning ON circuit 106 with circuit 107 ON, it is implied that all data transferred across the interface prior to the time that any one of the four circuits (105, 106, 107 and 108/1 or 108/2) is again turned OFF, will be transferred to the line; however, the ON condition of circuit 106 is not necessarily a guarantee that the remote DCE is in the receive mode. (Depending on the complexity and sophistication of the transmitting signal converter, there may be a delay ranging from less than a millisecond up to several seconds between the time a bit is transferred across the interface until the time a signal element representing this bit is transmitted on the line.)

When the transmitting DCE turns circuit 106 ON, with circuit 107 in the OFF condition, the DTE is permitted to transfer programming or control signals to a serial automatic calling DCE across the interface on circuit 103.

During data transfer, the DTE shall not turn circuit 105 OFF before the end of the last bit (data bit or stop element) is transferred across the interface on circuit 103. Similarly, in certain duplex switched network applications where circuit 105 is not implemented (see the specific DCE Recommendations), this requirement applies equally when circuit 108/1 or 108/2 is turned OFF to terminate a switched network call.

Where circuit 105 is provided, the ON and OFF conditions on circuit 106 during the data transfer phase (i.e. circuit 107 ON) shall be responses to the ON and OFF conditions on circuit 105. For the appropriate response times of circuit 106, and for the operation of circuit 106 when circuit 105 is not provided, refer to the relevant Recommendation for the DCE.

For serial automatic calling DCEs, the ON and OFF conditions on circuit 106 outside the data transfer phase (i.e. circuit 107 OFF) shall be dependent on the interface state during the automatic call set-up and associated procedures. The transitions on circuit 106 for this application shall be as detailed in Recommendation V.25 *bis*.

When circuit 105 and circuit 106 are both OFF, the DTE shall maintain a binary 1 condition on circuit 103. When circuit 105 is turned OFF it shall not be turned ON again until circuit 106 is turned OFF by the DCE.

Note – These conditions also apply to the relationship between circuits 120, 121 and 118.

4.6 *Timing circuits*

It is desirable that the transfer of timing information across the interface shall not be restricted to periods when actual transmission of data is in progress; however, during intervals when timing information is not transferred across the interface, the circuit involved should be held in the OFF condition. The following conditions apply:

4.6.1 *Circuit 113 – Transmitter signal element timing* (DTE source)

Where circuit 113 is used, the DTE shall transfer timing information across the interface on this circuit at all times that the timing source in the DTE is capable of generating this information, e.g. when the DTE is in a power-on condition.

4.6.2 *Circuit 114 – Transmitter signal element timing* (DCE source)

Where circuit 114 is used, the DCE shall transfer timing information across the interface on this circuit at all times that the timing source in the DCE is capable of generating this information, e.g. when the DCE is in a power-on condition. It is recognized that a DCE which derives power from the central office battery over the local telephone loop is in a power-off condition when disconnected from the loop, i.e. on-hook.

4.6.3 *Circuit 115 – Receiver signal element timing* (DCE source)

Where circuit 115 is used, the DCE shall transfer timing information across the interface on this circuit at all times that the timing source is capable of generating this information.

It is recognized that a DCE which derives power from the serving central office via the local telephone loop, is in a power-off condition with timing sources stopped, when the DCE is disconnected from the line. It is also recognized that some timing sources will not continue to run indefinitely without a driving (external synchronization) signal.

Accuracy and stability of this signal as defined in the DCE Recommendations are required only when circuit 109 is ON. Drift during the OFF condition of circuit 109 is acceptable; however, resynchronization of the signal on circuit 115 must be accomplished as rapidly as possible following the turning ON of circuit 109 for the next transmission as indicated in the relevant DCE Recommendation.

4.7 *Circuit 125 – Calling indicator*

The operation of circuit 125 shall not be impaired or disabled by any condition on any other interchange circuit.

4.8 *Usage of circuits 126 and 127*

Originally, these circuits were defined for operational control of a 2-wire, frequency-divided duplex DCE, such as the Recommendation V.21-type modem. Transmitter and receiver control were separated, so that local testing of both data channels might be performed as national Administrations required.

The modem according to Recommendation V.21 does not require separate operational control by the DTE of circuits 126 and 127 since it selects the transmit and receive frequencies according to the condition of circuit 125 in switched network operation.

However, the use of circuits 126 and 127 may become necessary in certain types of non-centralized multipoint operation.

4.9 *Circuit 140 – Loopback/Maintenance Test*

4.9.1 *Usage of circuit 140*

Circuit 140 can be used in conjunction with coded commands on circuit 103 in accordance with the provisions of Recommendation V.54.

In systems not including the use of circuit 103, i.e., no coded commands, circuit 140 controls only the remote loopback (loop 2).

In systems that involve the use of circuit 103, additional maintenance applications of circuit 140 are possible. These additional applications remain for further study.

4.9.2 *Interrelationship of circuits 105, 106 and 140*

For automatic control of loop 2 test, circuit 106 is under the control of circuit 140 and circuit 105 is disregarded by the DCE.

4.10 *Interrelationship of circuits 202 to 211*

Circuit 202

Circuit 202 must be turned OFF between calls or call attempts and shall not be turned ON before circuit 203 is turned OFF.

Circuit 204

The ON condition of this circuit must be maintained until the DTE has released the automatic calling equipment, i.e. until circuit 202 is turned OFF.

Circuit 205

The OFF condition shall be maintained on this circuit after circuit 204 comes ON.

The initial time interval starts when circuit 202 comes ON. Subsequent time intervals start each time circuit 210 is turned OFF.

Circuits 206, 207, 208 and 209

The conditions on these four circuits shall not change whilst circuit 211 is ON.

Circuit 210

When circuit 210 is turned OFF, it shall not be turned ON again before circuit 211 is turned OFF.

Circuit 211

Circuit 211 shall neither be turned ON when circuit 210 is in the OFF condition, nor until after the DTE has presented the required code combination on the digit signal circuits.

Circuit 211 shall not be turned OFF before circuit 210 is turned OFF.

Reference

[1] CCITT Recommendation *Connection to the telex network of an automatic terminal using a V.24 DCE/DTE interface*, Vol. VII, Rec. S.16.

AUTOMATIC ANSWERING EQUIPMENT AND/OR PARALLEL AUTOMATIC CALLING EQUIPMENT ON THE GENERAL SWITCHED TELEPHONE NETWORK INCLUDING PROCEDURES FOR DISABLING OF ECHO CONTROL DEVICES FOR BOTH MANUALLY AND AUTOMATICALLY ESTABLISHED CALLS

(Mar del Plata, 1968; amended at Geneva, 1972 and 1976; Malaga-Torremolinos, 1984)

1 Scope

1.1 This Recommendation is concerned with the setting-up of a data connection when automatic answering equipment and/or parallel automatic calling equipment is used over international circuits. The automatic calling procedures defined in this Recommendation make use of the 200-series interchange circuits and are known as "parallel" automatic calling. Automatic calling procedures, which make use of only the 100-series interchange circuits, are known as "serial" automatic calling and are defined in Recommendation V.25 *bis*.

Automatic calling and answering equipment used within any single Administration's area or between two Administrations by bilateral agreement is not necessarily constrained by these proposals. In particular, the use of 2100 Hz answering tone, as described in this Recommendation, could be substituted by another tone when the equipment is used over circuits not equipped with echo control devices. Similarly, the calling tone could be omitted by bilateral agreements but attention is drawn to §§ 7 and 8 below.

In addition, the provisions for echo canceller disabling and for a "calling station response" prior to the termination of answer tone are optional and only applicable to data circuit-terminating equipment (DCE) for which the series V Recommendation specifically calls for such provision(s).

1.2 This Recommendation describes the sequence of events involved in establishing a connection between a parallel automatic calling data station [1)] and an automatic answering data station for Series V Recommendations modems specified for general switched network operations. The system configuration proposed is shown in Figure 1/V.25.

Consideration is given only to:

a) the events which affect the interfaces between the data terminal equipment and the data circuit-terminating equipment, and

b) the events on the line during establishment of a data call.

Interactions within the data circuit-terminating equipment are not considered, since such consideration is unnecessary for purposes of international standardization.

1.3 The proposed procedures are intended to be suitable for the four types of calls, namely:

a) parallel automatic calling data station to automatic answering data station;

b) manual data station to automatic answering data station;

c) parallel automatic calling data station to manual data station;

d) disabling of echo suppressors in the case of manual data stations.

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1) In this Recommendation, the term "data station" is synonymous with the term "terminal installation for data transmission" [1].

1.4 The data terminal equipment is responsible for:

a) during call establishment:
   i) ensuring that the data circuit-terminating equipment is available for operation,
   ii) providing the telephone number,
   iii) deciding to abandon the call if it is unsuccessfully completed;

b) after call is established:
   i) establishing identities,
   ii) exchanging such traffic as is appropriate,
   iii) initiating disconnect at calling and answering data station.

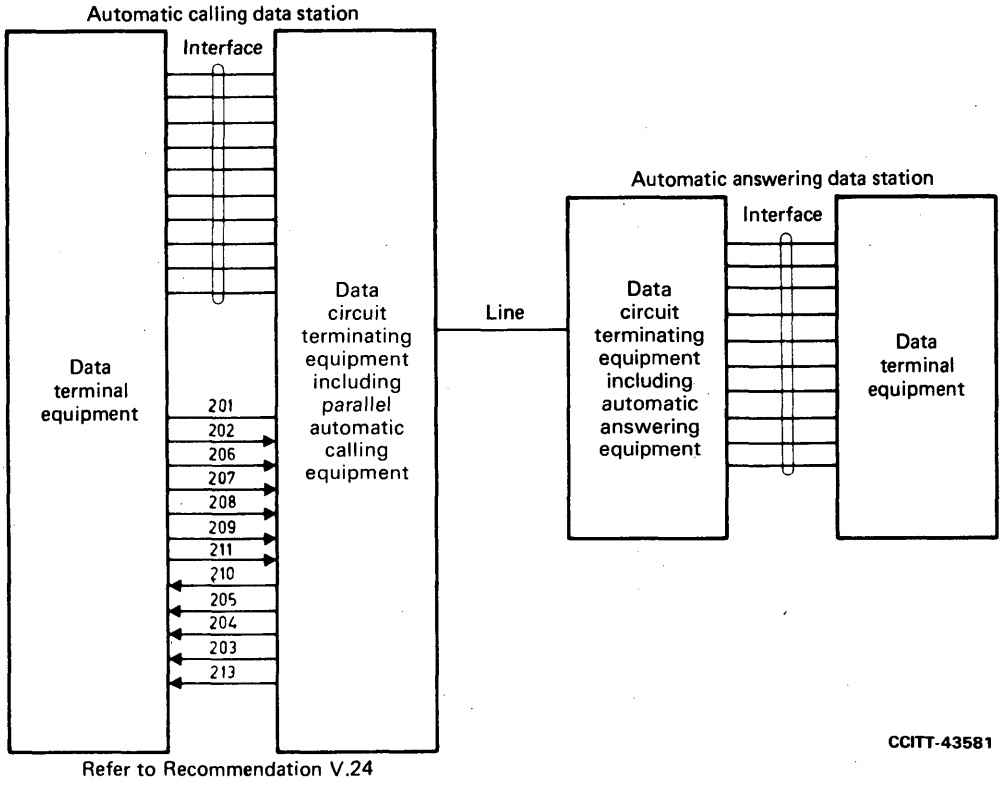

FIGURE 1/V.25

System configuration

2 Abbreviations and definitions

The following abbreviations are used in this Recommendation:

CT 104 = Circuit 104 – Received data
CT 105 = Circuit 105 – Request to send
CT 106 = Circuit 106 – Ready for sending
CT 107 = Circuit 107 – Data set ready
CT 108/1 = Circuit 108/1 – Connect data set to line
CT 108/2 = Circuit 108/2 – Data terminal ready
CT 109 = Circuit 109 – Data channel received line signal detector
CT 119 = Circuit 119 – Received backward channel data
CT 120 = Circuit 120 – Transmit backward channel line signal
CT 121 = Circuit 121 – Backward channel ready
CT 122 = Circuit 122 – Backward channel received line signal detector
CT 125 = Circuit 125 – Calling indicator

CT 201 = Circuit 201 – Signal ground or common return
CT 202 = Circuit 202 – Call request
CT 203 = Circuit 203 – Data line occupied
CT 204 = Circuit 204 – Distant station connected
CT 205 = Circuit 205 – Abandon call
CT 206 = Circuit 206 – Digit signal (2^0)
CT 207 = Circuit 207 – Digit signal (2^1)
CT 208 = Circuit 208 – Digit signal (2^2)
CT 209 = Circuit 209 – Digit signal (2^3)
CT 210 = Circuit 210 – Present next digit
CT 211 = Circuit 211 – Digit present
CT 213 = Circuit 213 – Power indication
DCE = Data circuit-terminating equipment
DTE = Data terminal equipment
EON = End-of-number control character
SEP = Separation control character

The following definitions apply to this Recommendation:

calling tone

The tone transmitted from the calling end. This may be 1300 Hz or any tone corresponding to binary 1 of the DCE in use.[2), 3)]

answering tone

The tone transmitted from the called end.[3)]

starting signal

Binary 1, synchronizing signal or equalizer training signal, as appropriate.[3)]

calling station response

A tone or signal transmitted from the calling DCE in response to its detection, as defined in this Recommendation, of answering tone.[2), 3), 4)]

parallel automatic calling

A procedure by which a DTE, by use of the 200-series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in parallel form on interchange circuits 206 through 209.

serial automatic calling

A procedure by which a DTE, by use of the 100-series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in serial form on interchange circuit 103 (see Recommendation V.25 *bis*).

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2) The calling tone and calling station response should not contain power in the band 2100 ± 250 Hz.

3) The power levels of the signals specified in this Recommendation shall conform to the levels specified in Recommendation V.2.

4) The specification of the calling station response and the timing of its transmission are the subject of the individual Series V Recommendation for the DCE involved. The specifications in this Recommendation cover only limitations on its transmission during call establishment.

3 Interface procedures at call-originating data station

Event

3.1 DTE checks if CT 213 ON, and the following circuits OFF: CT 202, CT 210, CT 205, CT 204, CT 203.

3.2 DTE puts CT 202 ON.

3.3 DTE puts CT 108/2 ON (CT 108/2 can be placed in the ON condition at any time up to and including event 3.16).

3.4 For half-duplex modems, DTE puts CT 105 ON if the calling end wishes to transmit first. CT 105 can be placed ON at any time up to and including event 3.20.

3.5 Line goes "off hook".

3.6 DCE puts CT 203 ON.

3.7 Telephone system puts dial tone on line[5].

3.8 DCE puts CT 210 ON.

3.9 DTE presents the first or appropriate digit on CT 206, CT 207, CT 208 and CT 209.

3.10 DTE puts CT 211 ON after digit signals have been presented.

3.11 DCE dials first digit; then takes CT 210 OFF.

3.12 DTE takes CT 211 OFF.

3.13 Events 3.8 to 3.12 are repeated (but this process may be interrupted by SEP) until the last digit signal is presented and transferred. Event 3.8 is then repeated but event 3.14 follows.

3.14 DTE presents EON on CT 206, CT 207, CT 208 and CT 209; it then puts CT 211 ON.

3.15 DCE takes CT 210 OFF.

3.16 DTE takes CT 211 OFF and puts CT 108/2 ON, if not previously ON.

3.17 The interrupted calling tone, as shown in Figures 2/V.25, 3/V.25 and 4/V.25 is transmitted to line from the calling DCE.

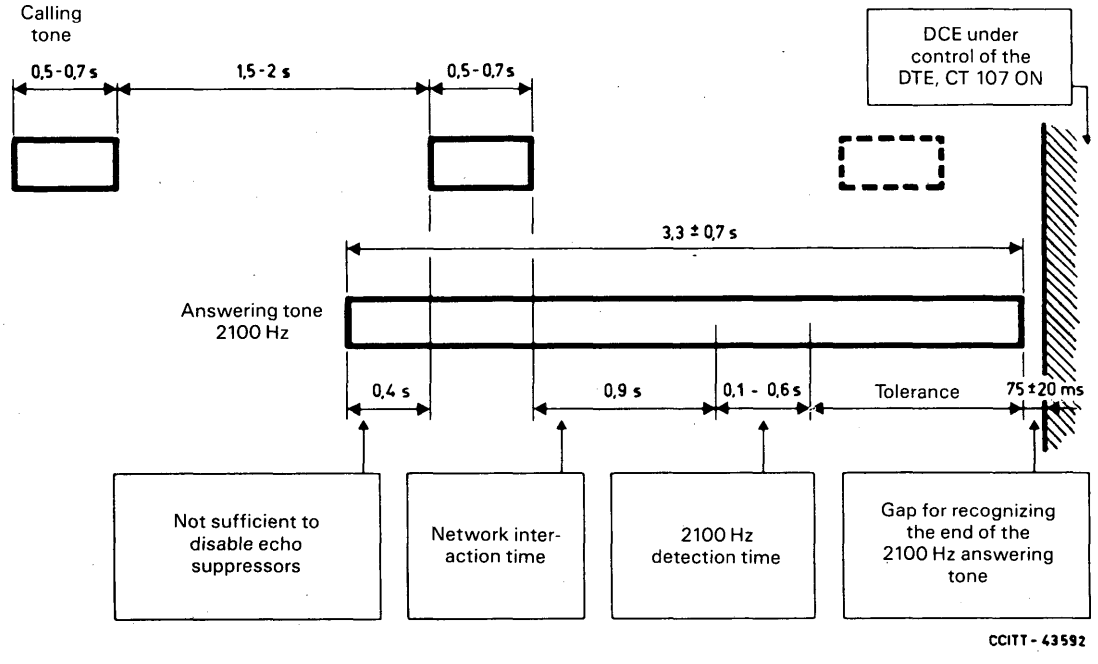
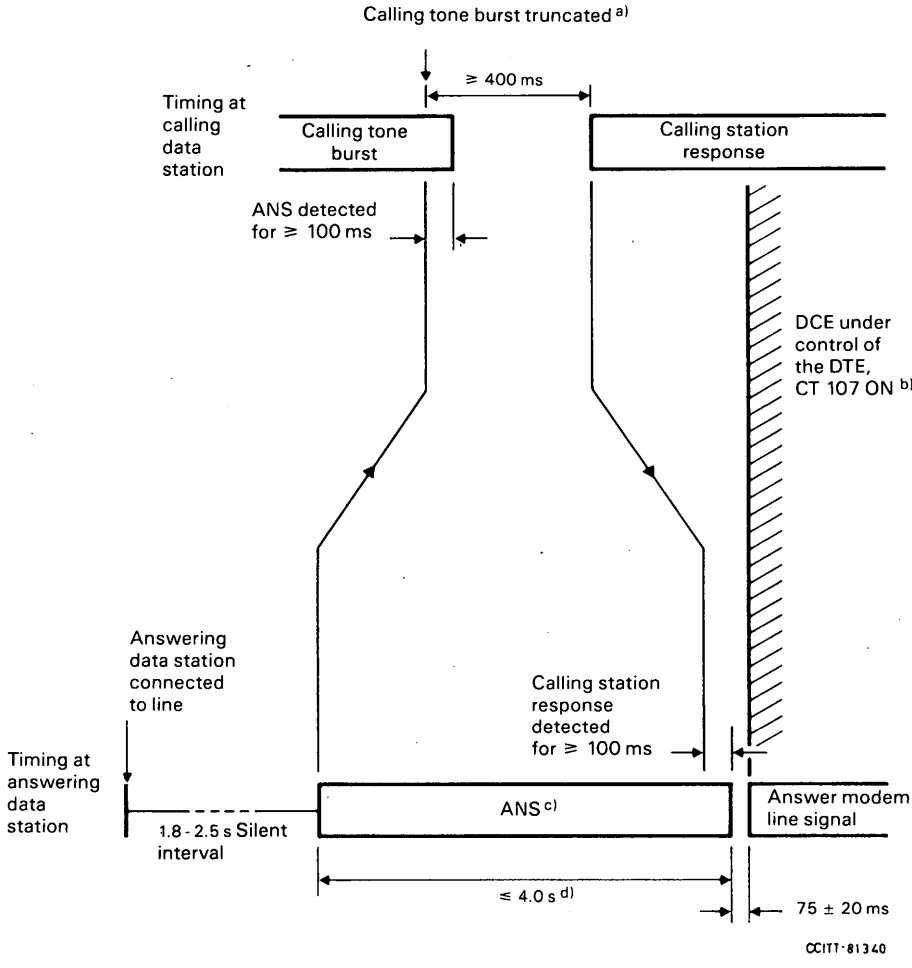


FIGURE 2/V. 25

Timing of line signals

[5] Some countries apply the second dial tone to the line after the initial digit is transferred.



a) If ANS is detected during a calling tone burst, the burst may be truncated. If it is not truncated, the calling station response must be delayed until at least 400 ms after the end of the burst.

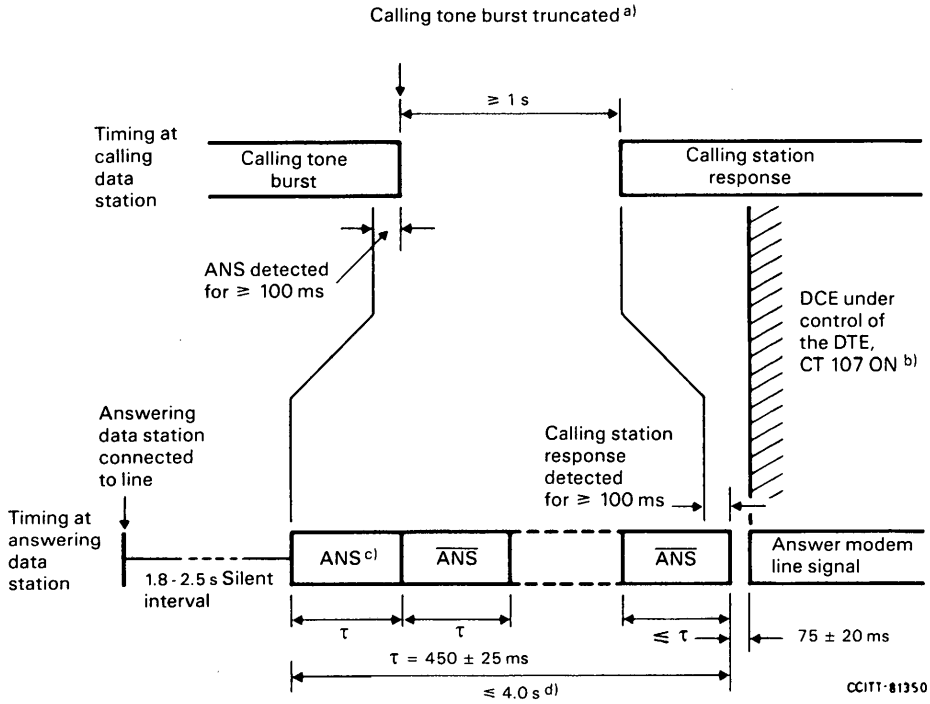
b) See § 3.20 for exception.

c) ANS denotes the answer tone.

d) If a calling station response is not received, the answer tone shall continue for 3.3 ± 0.7 seconds.

FIGURE 3/V.25

Timing of line signals – Optional calling station response



a) If ANS is detected during a calling tone burst, the burst may be truncated. If it is not truncated, the calling station response must be delayed until at least 1 second after the end of the burst.

b) See § 3.20 for exception.

c) ANS denotes the answer tone. $\overline{\text{ANS}}$ denotes the answer tone with its phase reversed.

d) The answer tone duration must be at least 2.6 seconds if a calling station response is not received.

FIGURE 4/V.25

Timing of line signals, optional provision for echo canceller disabling and for calling station response

3.18 a) If the call is answered by a data station, then 2100-Hztone is received by the calling DCE. Echo suppressors are disabled during coincidence of a silent period in the interrupted calling tone (event 3.17) with 2100 Hz answering tone. The 2100-Hz answering tone must not activate CT 104 and CT 109.

b) If the call is not answered, or is answered by a non-data station, then no 2100 Hz is received at the calling data station. If no answering tone is received after an elapsed time, CT 205 comes ON. This time is measured from event 3.15 and selectable in the range of 10-40 seconds. The DTE must respond by turning CT 202 OFF.

3.19 When a 2100-Hz answer tone has been recognized by the DCE for a period of 100 to 600 ms, the interrupted calling tone is discontinued by the DCE as shown in Figures 2/V.25, 3/V.25 and 4/V.25. The DCE transfers control of the connection to the telephone line from CT 202 to CT 108/2.

The DCE may, as shown in Figures 3/V.25 and 4/V.25, transmit the calling station response following the detection of a continuation of the 2100-Hz answer tone for a period of at least 400 ms after the transmission of the calling tone is terminated. As indicated in Figure 4/V.25, the required duration ($\geqslant$ 1 s) of the continuous 2100-Hz period, which must follow the termination of the calling tone, is longer if the answer tone includes phase reversals to disable echo cancellers.

3.20 The DCE examines the line to determine the end of the 2100-Hz answering tone. The DCE detects an absence of the 2100-Hz tone for 75 $\pm$ 20 ms, and then puts CT 107 ON:[6]

i) If CT 105 is ON, the starting signal is put on the line. After its delay as specified in the appropriate Series V Recommendation, CT 106 comes ON and the DTE can then transmit data.

ii) If CT 105 is OFF, the incoming starting signal is recognized and after its delay as specified in the appropriate Series V Recommendation, the DCE puts CT 109 ON to allow the examination of CT 104 by the DTE.

iii) For the duplex modem case, where CT 105 is not used, the starting signal is put on the line after CT 107 is put ON. The DCE then puts ON CT 109 and CT 106 after a delay as specified in the appropriate Series V Recommendation.

Note – There may be an interim period during which certain existing V.21 modems may not be able to provide the silent period between the end of the answering tone and the application of the starting signal. In this case, the use of a selective answering tone detector (see § 11 below) will be essential.

3.21 The DCE turns ON CT 204. The DTE then may turn OFF CT 202 without disconnecting the call.

Note 1 – After event 3.19, both CT 202 and CT 108/2 must be turned OFF to disconnect. The ON of CT 205 is an indication to DTE disconnect.

Note 2 – Where CT 105 or CT 120 is not implemented, the timing of CT 106 or CT 121 shall be related to CT 107 and CT 109 respectively.

4 Interface procedure at answering data station

Event

4.1 Ringing received on line. DCE puts CT 125 ON.

4.2 a) If CT 108/2 is ON, DCE goes "off hook".

b) If CT 108/1 or CT 108/2 is OFF, the DCE waits for CT 108/1 or CT 108/2 to come ON, and then goes "off hook". If CT 108/1 or CT 108/2 does not turn ON, then the call is not answered.

[6] For some DCEs requiring extended training sequences, the associated Series V Recommendation may specify that CT 107 be put ON at some later time, during the handshake sequence, which is more consistent with the specification in Recommendation V.24 of CT 107.

4.3 The DCE goes "off hook", maintains silence on the line for a period between 1.8 and 2.5 s, then transmits 2100-Hz[7] answer tone for a period, as shown in Figures 2/V.25 and 3/V.25. Where it is intended to disable network echo cancellers [3] as well as echo suppressors [2], reversals (180°)[8] in the phase of the 2100-Hz tone shall be introduced, as indicated in Figure 4/V.25, at intervals of 425 to 475 ms. The 2100-Hz answer tone, with continued reversals in its phase, shall continue for 3.3 ± 0.7 s unless a calling station response is received, in which case the 2100-Hz tone may be discontinued after detection of the response for 100 ms.

For the very special application in which an automatically answering modem is permanently dedicated to receive calls only from acoustically coupled originating stations, the modem may, optionally, extend the duration of the answer tone to ten seconds to compensate for operator reaction time in placing the telephone handset on the acoustic coupler. All other timeouts remain the same and the protocol is as defined in § 6. Use of the extended answer tone is restricted expressly to this unique application.

4.4 At the end of the 2100-Hz transmission, the DCE shall not transmit (i.e. provide a silent period) for 75 ± 20 ms. The DCE puts CT 107 ON after this silent period.[9]

5 Proposed line procedures

The line procedures outlined consider the half-duplex case of the Series V Recommendations modems. For reasons of simplicity, the same timing of line signals will be used for duplex modems (including modems with backward channel).

Systems which operate in the half-duplex mode and which employ automatic calling equipment shall determine by prearrangement which of the two data stations – calling or answering – shall first transmit to the other upon the establishment of the data connection. As indicated in § 3 above, the DTE at the data station which is to transmit first must put CT 105 ON, at the appropriate point in the call establishment sequence. For correct operation, it is necessary that the longer response times of CT 106 and CT 109 as specified in the appropriate Series V Recommendation are used during call establishment.

Figures 2/V.25, 3/V.25 and 4/V.25 show the timing of line signals when automatic calling and automatic answering are employed. The sequence of operation is as follows:

After the DCE has dialled the digits of the directory number for the automatic answering data station, followed by the EON character, the DCE sends the calling tone to the answering data station. The calling tone consists of a series of interrupted bursts of binary 1 signal or 1300 Hz, ON for a duration of not less than 0.5 s and not more than 0.7 s and OFF for a duration of not less than 1.5 s and not more than 2.0 s.

1.8 to 2.5 s after the answering data station is connected to the line (i.e., CT 125 and CT 108 are ON), it sends a continuous 2100-Hz answering tone for a duration of not more than 4.0 s. If it is intended to disable network echo cancellers as well as echo suppressors, the answering station reverses the phase of the tone at intervals of 425 to 475 ms (see Figure 4/V.25).

The answering tone propagates towards the calling data station and, during the course of one or two interruptions between bursts of calling tone, causes any echo suppressors on the circuit to disable. If the phase reversals are included in the signal, any echo cancellers in the circuit would also be disabled. The answering tone is recognized by the calling data station for a period of between 100 ms and 600 ms after its arrival. The calling station discontinues the calling tone and may transmit a calling station response. The answering station, after detecting the calling station response, may discontinue transmission of the tone. The answering station shall provide a silent interval of 75 + 20 ms in its transmitted output following the discontinuance of the 2100-Hz tone.

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[7] The 2100-Hz tolerance will be ± 15 Hz in accordance with Recommendation G.164 [2].

[8] The reversal in phase shall be accomplished such that the phase is within 180 ± 10 degrees in 1 ms and that the amplitude of the 2100-Hz tone is not more than 3 dB below its steady state value for more than 400 μs.

[9] For some DCEs requiring extended training sequences, the associated Series V Recommendation may specify that CT 107 be put ON at some later time, during the handshake sequence, which is more consistent with the specification in Recommendation V.24 of CT 107.

The calling data station recognizes the end of the answering 2100-Hz tone for a period of 75 ± 20 ms. At the end of this interval, the DCE may put CT 107 ON. Similarly, the answering data station delays for a period of 75 ± 20 ms after discontinuing the answer tone before it may put CT 107 ON.[10)]

To keep the echo suppressor disabled, it is necessary to ensure that following the 75 ± 20 ms silent period after the transmission of the 2100-Hz answering tone from the answering data station, which serves to disable the echo suppressor or echo canceller during the silent period in the calling tone, energy is maintained as specified in Recommendation G.164 [2].

During the automatic calling and answering procedures, the echo suppressors will be disabled and the echo cancellers will be disabled if the required sequence is transmitted. If signal gaps, at the echo suppressor or canceller, exceed 100 ms at any time, e.g. during modem turn-around, they may become re-enabled. This requires that, to maintain the disabled state of echo control devices on circuits with satellite links, the answering data station resume transmission after the 75 ± 20 ms silent period unless a calling station response is received prior to the silent interval and appropriately continued.

6 Manual data station calling automatic answering data station

The procedure for establishment of a call from a manual data station to an automatic answering data station is similar to that from an automatic calling data station, except that no tone is transmitted from the calling data station until the answering data station has answered. The manual operator dials the required number, hears 2100 Hz returned from the automatic answering data station and then presses his data button to connect the data circuit-terminating equipment to the line during the period that 2100 Hz is being received. CT 107 comes ON at the time specified in event 3.20. Where the calling station is acoustically coupled to the line, placement of the telephone handset on the acoustic coupler is logically equivalent to pressing a "data" button on a permanently installed DCE.

Satisfactory disabling of echo suppressors by the answering tone, however, will require that no speech signals from the microphone at the calling data station enter the telecommunications circuit for a period of at least 1 s during the receipt of answering tone. This may be accomplished by a handset switch or other appropriate means.

7 Automatic calling data station calling manual data station

An operator answering a call from an automatic calling equipment hears an interrupted calling tone of 0.5 to 0.7 s ON and 1.5 to 2.0 s OFF. The data button must be depressed to connect the DCE to line. A period of up to 4.0 s of 2100-Hz tone is transmitted to the calling data station to disable echo suppressors and/or echo cancellers and to notify the calling data station that the connection is being established. This sequence is followed by data transmission, as required.

8 Disabling of echo suppressors in the case of manual data stations

The procedures as described in §§ 6 and 7 above with regard to the manually operated data stations, can obviously be used for disabling echo suppressors when manual switching from voice conversation to data is required, which is the preferred principle of operation. Considering the type of DCE designed to be used in conjunction with manual connection set-up, it will be necessary to equip the DCE with a 2100-Hz answering tone generator. To avoid modifying existing equipment at the data station which receives the answering tone, the following procedure may replace the operation principle of § 6 above. The manual operator operates his data key after the end of the 2100-Hz answering tone. The data station which is to transmit the answering tone is to be agreed between the operators while still in the voice mode.

Care must be exercised in cases of half-duplex modems where transmission of data is started from the data station which transmits the answering tone, to avoid mutilation of the initial data.

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10) For some DCEs requiring extended training sequences, the associated Series V Recommendation may specify that CT 107 be put ON at some later time, during the handshake sequence, which is more consistent with the specification in Recommendation V.24 of CT 107.

Note – Where disabling of echo suppressors is not required in the half-duplex modem case, the 2100-Hz answering tone need not be transmitted. However, the delay between CT 105 to CT 106 ON conditions should be longer than 100 ms in consideration of the echo suppressor suppression hangover time.

9 Protection of ordinary telephone users

As both automatic calling and automatic answering data stations transmit tones to line during call establishment, a normal telephone user who becomes inadvertently connected to one will receive tone signals for a period of sufficient duration to indicate clearly to him that he is incorrectly connected.

10 Manual selection of automatic answering, data mode and voice mode

It is recognized that, at the data station, means should be provided to allow the operator to select between automatic and manual answering of calls. If a call is manually answered, voice mode shall be established. Subsequent switching to the data mode shall be performed by the procedure as specified in § 7 above.

Selection of manual or automatic answering of subsequent calls shall be possible after entering the data mode. As an option, automatic answering may be arranged for all subsequent incoming calls. In this case, manual answering may still be achieved by keeping CT 108/2 OFF to cause an audible signal to occur at the telephone instrument.

The DCE shall be disconnected from the line whenever CT 108/1 or CT 108/2 is turned OFF, irrespective of the means employed in establishing the connection.

Procedures for switching to the voice mode between data transmission within the same call shall ensure that CT 107 is turned OFF while in the voice mode.

11 2100-Hz tone recognition

To protect the 2100-Hz tone detector against faulty operation resulting from interference generated by the interrupted calling tone, the detector may be inhibited during the ON periods of the calling tone.

Additionally, in cases where automatic calling equipment is used to set up the call, the 2100-Hz detector must not respond to spurious tones which may arise from speech or service signals during call establishment. It is suggested that the answering tone detection be prevented when the 2100-Hz signal is accompanied by any other signal of comparable level within the ranges 350 Hz to 1800 Hz and 2500 Hz to 3400 Hz.

Note – The relative inhibiting signal levels recommended for the echo suppressor disabling tone detector of Recommendation G.164 [2] are a useful guide for 2100-Hz tone detector inhibiting levels.

References

[1] CCITT Definition: *Terminal installation for data transmission*, Vol. X (Terms and Definitions).

[2] CCITT Recommendation *Echo suppressors*, Vol. III, Rec. G.164.

[3] CCITT Recommendation *Echo cancellers*, Vol. III, Rec. G.165.

Recommendation V.25 bis

AUTOMATIC CALLING AND/OR ANSWERING EQUIPMENT ON THE GENERAL SWITCHED TELEPHONE NETWORK (GSTN) USING THE 100-SERIES INTERCHANGE CIRCUITS

(Malaga-Torremolinos, 1984)

1 Scope

1.1 This Recommendation is concerned with the setting up of a data connection on the general switched telephone network where the automatic calling equipment used interfaces to the data terminal equipment via the 100-series interchange circuits.

This procedure is known as serial automatic calling. Procedures for parallel automatic calling are defined in Recommendation V.25.

1.2 The Recommendation describes the sequence of events involved in establishing a connection between a serial automatic calling data station [1] and an automatic answering data station for Series V Recommendation modems specified for general switched telephone operation. The system configuration is shown in Figure 1/V.25 *bis*.

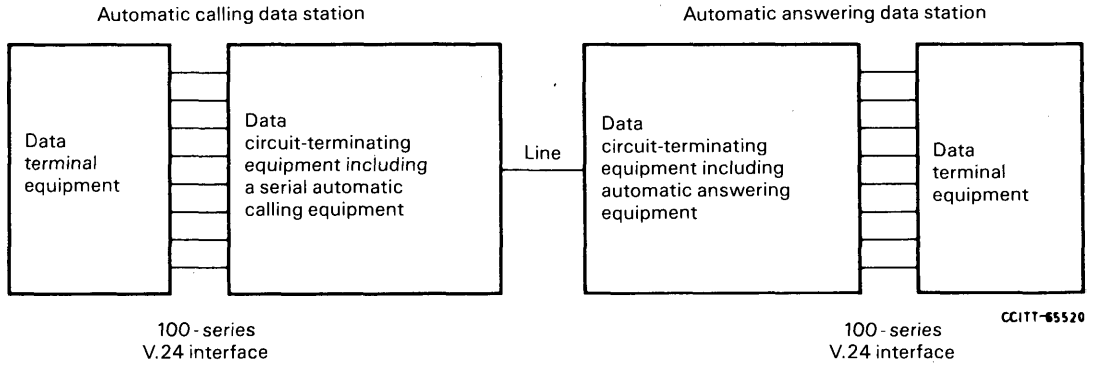

FIGURE 1/V.25 *bis*

1.3 The procedures are intended to be suitable for the following three types of call:

a) serial automatic calling data station to automatic answering data station;

b) manual calling data station to automatic answering data station;

c) serial automatic calling data station to manual answering data station.

It is intended that data terminal equipment designed to control automatic calling equipment in accordance with this Recommendation will also be suitable for use with manually controlled data circuit-terminating equipment, and also that data circuit-terminating equipment incorporating serial automatic calling equipment may be manually controlled where necessary.

1.4 The procedures described should allow automatic calling equipment conforming to this Recommendation to interwork with automatic answering equipment conforming to Recommendation V.25. Similarly, the procedures herein described for automatic answering allow interworking with automatic calling equipment conforming to Recommendation V.25.

1.5 The data terminal equipment is responsible:

a) during call establishment:

i) for ensuring that the data circuit-terminating equipment is available for operation,

ii) for providing the telephone number or selecting a telephone number pre-programmed into the data circuit-terminating equipment,

iii) for deciding to abandon the call if it is unsuccessfully completed;

b) after call establishment:

i) for controlling data transfer,

ii) for initiating disconnect at calling or answering data stations.

1.6 This Recommendation deals with call establishment and clearing. Any specific use of Recommendation V.24 interchange circuits herein described only applies during these phases. The management of interchange circuits and the line during the data transmission phase is not part of this Recommendation.

Details of interface procedures following the OFF to ON transition of circuit 107 on entry of the data transmission phase can be found in the relevant modem Recommendations.

1.7 Annex A gives guidance on the maintenance facilities which may be associated with an automatic calling data circuit-terminating equipment. Methods for testing the automatic calling functions of the data circuit-terminating equipment are included.

1.8 References to automatic calling in the remainder of this Recommendation may be taken as serial automatic calling unless otherwise stated.

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[1] In this Recommendation, the term "data station" is synonymous with the term "terminal installation for data transmission".

2 Abbreviations and definitions

The following abbreviations are used in this Recommendation:

DCE = Data circuit-terminating equipment

DTE = Data terminal equipment.

The following definitions apply to this Recommendation:

command

An instruction issued by the DTE to the DCE as part of the automatic calling procedure.

indication

An instruction or response issued by the DCE to the DTE as part of the automatic calling procedure.

parameter

A variable which may accompany Commands or Indications.

parallel automatic calling

A procedure by which a DTE, by use of the 200-series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in parallel form on interchange circuits 206 to 209.

serial automatic calling

A procedure by which a DTE, by use of the 100-series interchange circuits, may instruct a DCE to perform the call establishment function. The transmission, from DTE to DCE, of each digit to be dialled is achieved in serial form on circuit 103.

3 General

3.1 The automatic calling and/or answering data stations can be operated, according to this Recommendation, in two modes:

- The "addressed call and/or answer authorized by the DTE (circuit 108/2)" mode gives at a calling data station extensive facilities by means of instructions exchanged between the DTE and the DCE on circuits 103 and 104. It gives an answering data station the capacity to accept "a priori" an incoming call.
- The "direct call and/or answer controlled by the DTE (circuit 108/1)" mode gives at a calling data station the capacity of calling a number (or a sequence of numbers) pre-recorded in the DCE, by means of the 108/1 control circuit. It gives to an answering data station the capacity of accepting incoming calls on a "per call" basis.

3.2 Though automatic answering data stations as well as automatic calling and answering data stations may implement both modes of operation, they are configured at installation to operate in either one or the other of the two modes.

4 Addressed call and/or answer authorized by the DTE (circuit 108/2)

4.1 *Interface procedure*

4.1.1 *Interchange circuits involved*

The interchange circuits used in this automatic calling/answering procedure are listed in Table 1/V.25 *bis*. Their use during the automatic calling/answering procedures is described below.

TABLE 1/V.25 *bis*

Interchange circuit		Direction	
Number	Name	from DCE	to DCE
103	Transmitted data		X
104	Received data	X	
106	Ready for sending	X	
107	Data set ready	X	
108/2	Data terminal ready		X
125	Calling indicator	X	

4.1.1.1 *Circuit 103 – Transmitted data*

The instructions issued by the DTE during the automatic calling procedure, known as *commands*, are transmitted to the DCE on this circuit.

4.1.1.2 *Circuit 104 – Received data*

Responses from the DCE to DTE Commands, known as *indications*, are transmitted to the DTE on this circuit.

4.1.1.3 *Circuit 106 – Ready for sending*

The DCE shall turn circuit 106 ON in response to the DTEs circuit 108/2 being ON.

The DCE shall turn circuit 106 OFF:

i) on connection to line when answering tone is detected;

ii) when the DCE aborts the call set-up under the control of DTE by turning 108/2 in the OFF condition.

4.1.1.4 *Circuit 107 – Data set ready*

The DCE shall turn circuit 107 ON:

i) at the end of the automatic call set-up procedure, to indicate to the DTE that the connection is established and the DCE connected to line;

ii) on completion of manual call set-up procedure.

The DCE shall turn circuit 107 OFF:

i) to indicate to the DTE that the connection has been cleared down during the data transfer phase (to be permitted where national regulations require it);

ii) in response to a clear request by the DTE turning OFF circuit 108/2.

4.1.1.5 *Circuit 108/2 – Data terminal ready*

The DTE turns circuit 108/2 ON:

i) to enable the DCE to set up a connection either manually or automatically;

ii) to indicate to the DCE that it is ready to accept an incoming call.

The DTE shall turn circuit 108/2 OFF:

i) to instruct the DCE to clear down the connection during data transfer;

ii) to instruct the DCE to abort the call set-up procedure;

iii) to indicate to the DCE that it is not ready to accept an incoming call.

4.1.1.6 *Circuit 125 – Calling indicator*

The DCE should provide circuit 125 to indicate to the DTE an incoming call. This incoming call will override a call request prior to seizure of the line. The usage of circuit 125 in the DTE is optional.

4.1.1.7 *Other interchange circuits*

The state of other interchange circuits is not part of the procedure. However, to ensure maximum compatibility with existing equipment, the other interchange circuits provided should retain their normal function during the automatic calling procedure.

Particularly to ensure correct operation of the DTE, the condition of circuit 109 should follow the condition of circuit 106.

The DTE may choose to hold circuit 105 ON during the automatic calling procedure, but the DCE is not required to recognize this condition.

4.1.2 *Control information format*

Call set-up is achieved by the use of interchange circuits 106, 107 and 108 together with messages exchanged between the DTE and the DCE on circuits 103 and 104. These messages consist of commands or indications from the DTE or DCE respectively, and may be accompanied by *parameters* where necessary. The commands/indications required for the automatic calling procedure are outlined in Table 2/V.25 *bis* and Table 3/V.25 *bis* together with their parameters.

The use of commands/indications other than the *call request* command (CRC) is optional in the DTE and DCE respectively.

The commands/indications and their parameters are described below.

4.1.2.1 *Call request commands*

These commands from the DTE instruct the DCE to initiate a call set-up procedure. The commands shall include a suffix to indicate the type of call request concerned (see Table 3/V.25 *bis*) and shall be accompanied by one of the following parameters:

i) the number to be dialled. (In applications where additional dial tones are required, separators, "wait tone", etc., may be included in this number);

ii) the identification number of the data station;

iii) the DCE memory address which contains the number to be dialled, this having been previously programmed;

iv) double dial-up parameters. (This procedure is for further study.)

4.1.2.2 *Program commands*

These commands from the DTE instruct the DCE to enter a programming state. The commands shall be accompanied by one or more of the following parameters:

i) the DCE memory address into which the number to be dialled is to be stored, and the number which is to be stored;

ii) double dial-up parameters (this procedure is for further study);

iii) the identification number of the data station.

Note – For the normal programming operation, the command should be followed first by the memory address, and then by the number to be dialled. For double dial-up programming, a separate suffix on the program command is used (see Table 3/V.25 *bis*).

Where a DCE does not contain the programming capability, the lack of response from the DCE to a program command should be interpreted by the DTE by means of a time out as a programming failure. This may also be indicated by an *invalid* indication from the DCE.

Where a DTE is not capable of programming the DCE, it may still initiate call attempts using the *call request* command in the normal way.

TABLE 2/V.25 *bis*

Set of commands and indications (Note 1)

Command/indication	DTE to DCE (command)	DCE to DTE (indication)	Parameters
Call request	X		– Number to be dialled – Memory address of the number to be dialled – Double dial-up request (Note 2) – Identification number
Program	X		– Number to be dialled – Memory address for the number to be dialled – Identification number
List request	X		– (Note 2)
Disregard incoming call	X		– None
Connect incoming call	X		– None
Call failure		X	– Engaged tone – Number not stored – Local DCE busy – Ring tone (time out) – Abort call (time out) – V.25 answer tone not detected – Forbidden call (nationally dependent parameters)
Delayed call		X	– Time to permissible call request (minutes)
Incoming call		X	– None
Valid		X	– None
Invalid		X	– (Note 2)
List		X	– Memory address – Number to be dialled – Status – Identification number

Note 1 – DTE manufacturers should note that a set of indications may not be implemented in a DCE, and allowance for this, by use of suitable time-outs, should be made.

Note 2 – This item is for further study.

TABLE 3/V.25 *bis*

Encoding of commands and indications

Command/indication	IA5 characters	Parameter format		
Call request with:				
number provided	CRN	CRN	Number to be dialled XXXXX XXXX	
number provided with the identification number	CRI	CRI	Number to be dialled XXXXX . . XXXX ;	Identification number YY . . . . YY
memory address provided	CRS	CRS	Memory address XXXXX . . . XX	
double dial-up required	CRD	CRD	For further study ZZZZZ . . . . ZZ	
Program:				
normal	PRN	PRN	Memory address XXX . . X ;	Number to be dialled XX . . . XX
double dial-up	PRD	PRD	For further study ZZZZ . . . . ZZ	
identification	PRI	PRI	Identification number XXXXX XX	
List request of:				
stored numbers	RLN	RLN	For further study ZZZ . . . . . Z	
forbidden numbers	RLF	RLF	For further study ZZZ . . . . . Z	
delayed call numbers	RLD	RLD	For further study ZZZ . . . . . Z	
identification number	RLI	RLI		
Disregard incoming call	DIC	DIC		
Connect incoming call	CIC	CIC		
Call failure indication	CFI	CFI	Parameter XX	
Delayed call	DLC	DLC	Time duration (in minutes) XXX . . . XX	
Incoming call	INC	INC		
Valid	VAL	VAL		
Invalid	INV	INV		
List of:				
stored numbers	LSN	LSN	Memory address XXXX ;	Number to be dialled YYY . . Y ;	Status (for further study) ZZZZ
forbidden numbers	LSF	LSF	XXXX ;	YYY . . Y ;	ZZZZ
delayed call numbers	LSD	LSD	XXXX ;	YYY . . Y ;	ZZZZ
identification number	LSI	LSI	Identification number XXXX XX		

4.1.2.3 *List request commands*

These commands from the DTE instruct the DCE to list the numbers that have been programmed in its memory together with their status. The commands shall include a suffix to indicate the type of list concerned. The command may be accompanied by parameters to select items to be listed. These parameters are for further study.

4.1.2.4 *Disregard incoming call command*

This command from the DTE instructs the DCE not to answer the incoming call which is, or has been, signalled from the DCE to the DTE.

4.1.2.5 *Connect incoming call command*

This command from the DTE instructs the DCE to connect an incoming call that has been disregarded due to a previous disregard incoming call command.

4.1.2.6 *Call failure indication*

This indication may be issued by the DCE in response to a *call request* command from the DTE and may be accompanied by a parameter stating the reason for the failure of the call.

The following parameters indicate the possible conditions that may result in a call failure on the GSTN:

i) engaged tone;

ii) number not stored;

iii) local DCE busy;

iv) ring tone (time out);

v) abort call (time out);

vi) answer tone not detected;

vii) forbidden call;

viii) other parameters dependent on national network variations.

The provision of the *call failure* indication is optional in the DCE. For this reason, the DTE should also be capable of recognizing call failure by means of a time out.

4.1.2.7 *Delayed call indication*

This indication from the DCE may be implemented depending on national regulations, and informs the DTE that, owing to repeated unsuccessful call attempts, no further call attempt will be accepted for a time given by the accompanying parameter.

4.1.2.8 *Incoming call indication*

This indication may be provided by the DCE to inform the DTE that a ring tone has been detected on the telephone line.

Note – In the event of collision between an incoming call and a call request, the incoming call will have priority.

4.1.2.9 *Valid indication*

This indication may be provided by the DCE to acknowledge a program command, and to inform the DTE that the command has been accepted.

4.1.2.10 *Invalid indication*

This indication may be provided by the DCE when it receives an invalid command, or receives a command which it is incapable of executing.

The use of parameters with this indication is for further study.

4.1.2.11 *List indications*

A series of such indications should be provided by the DCE to list specific items stored in its memory according to the *list request* command previously made by the DTE. These indications will be accompanied by one or more of the following parameters:

i) the DCE memory address into which the number is stored;

ii) the number stored;

iii) the status of this number;

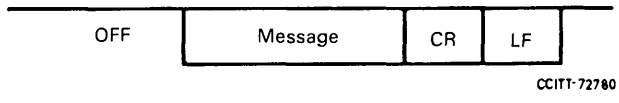
iv) the identification number of the data station.

4.1.3 *Format for commands and indications*

Commands and indications may be encoded in the formats specified below, according to application.

4.1.3.1 *Asynchronous operation*

The format for asynchronous operation shall be as shown in Figure 2/V.25 *bis*.



Note - In commands from the DTE the *new line* function may sometimes be encoded in a way other than CR + LF (see Recommendation T.50, § 4.1.2.2) and allowance for this should be provided.

FIGURE 2/V.25 *bis*

In this mode of operation, the character format shall be one start element followed by 8-bit data units and one-unit stop element. The 8-bit data units are formed by a 7-bit IA5 character in accordance with Recommendation T.50 together with an even parity unit in accordance with Recommendation V.4.

Where the DCE operating rate is variable, the transmision rate for commands and parameters should be the maximum data rate permitted by the modem Recommendation, i.e.: 300, 600, 1200 and 2400 bit/s.

Note – These bit rates are the minimum which should be provided. The addition of other bit rates is for further study.

4.1.3.2 *Synchronous character oriented operation*

The format for synchronous character oriented operation shall be in accordance with ISO 1745, and shall be as shown in Figure 3/V.25 *bis*.

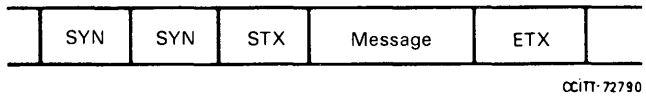


FIGURE 3/V.25 *bis*

In this mode of operation, consecutive 8-bit data units are used. The 8-bit data units are formed by a 7-bit IA5 character in accordance with Recommendation T.50 with an odd parity bit in accordance with Recommendation V.4.

The bit rate used for the data transfer shall apply.

4.1.3.3 *Synchronous bit oriented operation*

HDLC (High Level Data Link Control) format shall be used for synchronous bit oriented operation, and shall be as shown in Figure 4/V.25 *bis*.

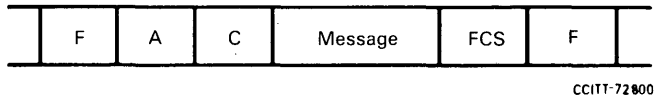


FIGURE 4/V.25 *bis*

The message is the information field of a UI frame transmitted with the P bit set to 1 and the global address. Consequently, the A and C fields are as follows:

A = 11111111, C = 11001000

The introduction of other addresses is for further study.

The usage of the P bit set to 0 for signalling that other command/indications are coming is also for further study.

Within the message, consecutive 8-bit data units are used and submitted to the HDLC framing (zero insertion). The 8-bit data units are formed by a 7-bit IA5 character in accordance with Recommendation T.50 together with an odd parity unit in accordance with Recommendation V.4.

The transmission mode and the bit rate used for the data transfer shall apply.

4.1.4 *Message format and encoding*

The message format shall comprise:

i) a three-character command/indication (see Table 3/V.25 *bis*);

ii) one or more parameters separated by ";" characters (see Table 4/V.25 *bis*).

TABLE 4/V.25 *bis*

Parameters alphabet

Parameter	IA5 coding
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
Wait tone	:
Separator 2 (Note)	<
Separator 3 (Note)	=
Separator 4 (Note)	>
Engaged tone	ET
Number not stored	NS
Local DCE busy	CB
Ring tone	RT
Abort call	AB
Answer tone not detected	NT
Forbidden call	FC
Parameter delimiter	;

Note – For national use.

4.1.5 *Command/indication exchange protocol*

The exchange of commands and indications between the DTE and the DCE can be regarded as asynchronous and balanced.

4.1.5.1 The following basic rules apply:

- Every command is to be followed by, at least, one indication or by circuit 107 going ON in the case of successful call.
- Several indications may be issued by the DCE one after the other, either of the same nature or of a different nature.
- The issue by the DTE of several commands one after the other is for further study.

4.1.5.2 *Erroneous command/indication*

- Whenever a command/indication is detected with a level II framing error [incorrect framing, parity or CRC, see § 4.1.3], this command/indication is disregarded.
- Whenever a DCE detects an error in the message of a command, it acknowledges negatively this command by issuing an *invalid* indication (INV). However, DCEs are allowed to consider that the use of particular presentation characters within the parameter field, as for example "space" or "." to present the digits of the number to be dialled, is not an error.

4.2 *Interface procedures at the calling data station*

The DTE/DCE interface procedure for automatic calling and answering is shown in the state diagram in Figure 5/V.25 *bis*.

The call set-up procedure is as follows:

- When the DTE is not ready to answer an incoming call or to enter the dialogue with the DCE, the interface is in state 1, *DTE not ready*.
- Prior to entering the dialogue with the DCE, the DTE shall signal 108/2 = ON and the interface is then in state 2, *DTE ready*.
- The DCE signals to the DTE that it is ready to enter the dialogue with the DTE by signalling 106 = ON, state 3, *DTE-DCE dialogue*. In this state, the DTE can issue commands and the DCE may issue indications.
- To initiate a call set-up, the DTE shall issue a *call request* command and move to state 4, *call establishment*. If the *call request* command contains a PSTN (public switched telephone network) number, the DCE shall proceed with the call set-up procedure. If it contains a DCE memory address, the DCE shall use its stored number.
- The DCE remains in state 4 during the dialling process.
- If the call is established and the answering tone is detected (see § 6.1), the interface moves to state 5, *answer tone detected*, and circuit 106 is turned OFF.
- If the call fails, the DCE may issue a *call failure* indication while in state 4 and return to state 3. During transmission of a calling station identification and the subsequent disconnection from the line following a call failure, the DCE may turn circuit 106 OFF and return to state 2, when it is not capable of handling new commands from the DTE.
- On completion of the line procedures (see § 6.1), circuit 107 is turned ON and the interface moves to state 6, *call connected*. From this state the DTE may enter the *data transfer* phase, state 12, in the normal manner.
- While the DCE is in state 3 or state 4, prior to going *off hook*, an incoming call shall be signalled to the DTE using circuit 125 and/or using the *incoming call* indication. The interface then moves to state 10, *incoming call accepting*. If in this state the DTE wishes not to answer the incoming call, it may issue a *disregard incoming call* command. In this case the interface will remain in state 10 and allow exchange of indications and commands other than *call request*. The collision of a call request with an incoming call before the latter has been detected is for further study.
- The DTE may clear a call or call attempt at any time by turning circuit 108/2 OFF, state 7, *clearing by DTE*. The interface will then move to state 1 or 8 for circuit 125 OFF or ON respectively.

4.3 *Interface procedures at the answering data station*

The DTE/DCE interface procedure for automatic calling and answering is shown in the state diagram in Figure 5/V.25 *bis*. The procedure is as follows:

- When the DTE is not ready to answer an incoming call or to enter the dialogue with the DCE, the interface is in state 1, *DTE not ready.*
- Prior to entering the dialogue with the DCE, the DTE shall signal 108/2 = ON and the interface is then in state 2, *DTE ready.*
- The DCE signals to the DTE that it is ready to enter the dialogue with the DTE by signalling 106 = ON, state 3, *DTE-DCE dialogue.* In this state the DTE can issue commands and the DCE may issue indications.
- An incoming call is indicated to the DTE using circuit 125 and/or with an *incoming call* indication, and by this means the interface will move from state 3 or 4 to state 10, *incoming call accepting.* (In the case of state 4, the incoming call may only be detected prior to the DTE going *off hook.*)
- If an incoming call occurs when the DTE is in state 1, *DTE not ready*, the DCE moves to state 8, *incoming call.* The DTE may then turn circuit 108/2 ON, in response to this call or in order to enter the dialogue with the DCE. The interface thus moves to state 9, *incoming call recognized.* The DCE will respond by turning circuit 106 ON and thus also in this case the interface moves to state 10.
- While in state 10, the DTE may reject the incoming call by turning circuit 108/2 OFF or issue a *disregard incoming call* command. In the latter case, the interface will remain in state 10 and allow exchange of indications and commands other than *call request.* If no *disregard incoming call* command has been issued within a period determined by national regulations, or when this command is reset by a subsequent *connect incoming call* command, the DCE shall accept the incoming call and move to state 11, *incoming call accepted* turning circuit 106 OFF, and from there to state 13, *line seized*, by turning circuit 125 OFF.
- Simple DCEs, having no programming capabilities, need not respond to the DIC and CIC commands.
- In this case the DCE will connect the incoming call immediately or after a predetermined period dependent on national regulations, thus moving directly from state 9, *incoming call recognized* to state 13, *line seized.*
- On completion of the line procedures (see § 6.1), circuit 107 is turned ON and the interface moves to state 6, *call connected.* From this state the DTE may enter the *data transfer* phase, state 12 in the normal manner.

5 Direct call and/or answer controlled by the DTE (circuit 108/1)

The *direct call* operating mode provides the DTE with the facility of setting up a call on the PSTN to a predefined data station, without a message exchange between the DTE and the DCE. The PSTN number to be called (or sequence of PSTN numbers) is recorded in the DCE. This Recommendation does not cover the method for recording the number in the DCE.

5.1 *Interchange circuits involved*

The interchange circuits used in this automatic calling/answering procedure are listed in Table 5/V.25 *bis.*

5.1.1 *Circuit 107 – Data set ready*

The DCE shall turn circuit 107 ON:

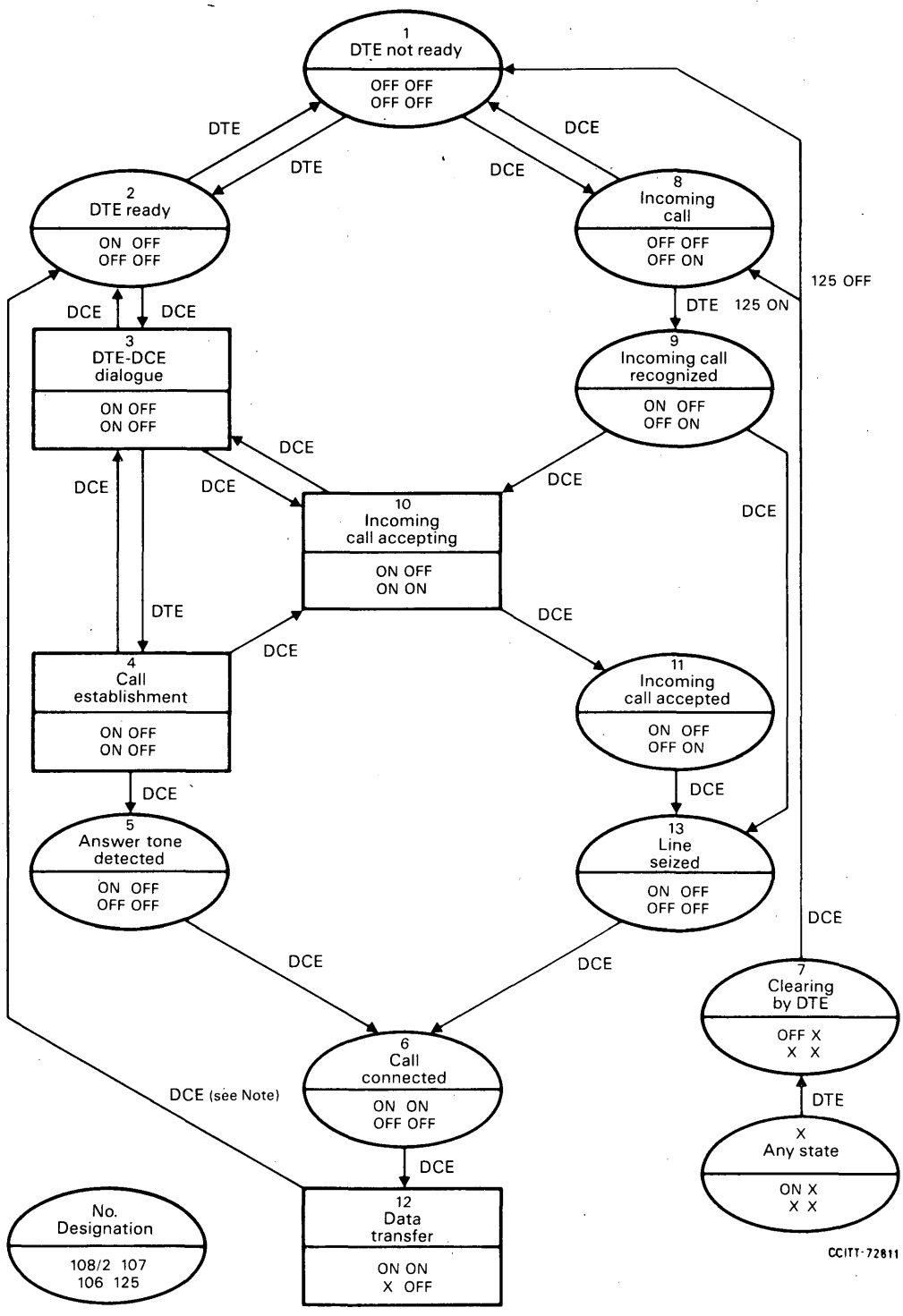
i) at the end of the automatic call set-up procedure, to indicate to the DTE that the connection is established and the DCE connected to line;

ii) on completion of manual call set-up procedure.

The DCE shall turn circuit 107 OFF:

i) to indicate to the DTE that the connection has been cleared down during the data transfer phase (to be permitted where national regulations require it);

ii) in response to a clear request by the DTE turning OFF circuit 108/1 while in the data transfer state.



Note - Procedures after disconnection by the DCE are for further study. (See Recommendation V.24, § 4.4.2.)

FIGURE 5/V.25 *bis*

Addressed call 108/2 response mode

TABLE 5/V.25 *bis*

Interchange circuit		Direction	
Number	Name	from DCE	to DCE
107	Data set ready	X	
108/1	Connect data set to line		X
125	Calling indicator	X	

5.1.2 *Circuit 108/1 – Connect data set to line*

The DTE shall turn circuit 108/1 ON:

i) to instruct the DCE to seize the line, dial the pre-recorded number and execute the connection procedure on the PSTN as the caller party;

ii) to instruct the DCE to seize the line and execute the connection procedure on the PSTN as the called party if circuit 125 is in the ON condition.

The DTE shall turn circuit 108/1 OFF:

i) to instruct the DCE to clear down the connection during data transfer;

ii) to instruct the DCE to abort the call set-up procedure;

iii) to indicate to the DCE that it is not ready to accept an incoming call.

5.1.3 *Circuit 125 – Calling indicator*

The DCE shall provide circuit 125.

5.2 *Interface procedure at the calling data station*

The state diagram shown in Figure 6/V.25 *bis* displays the allowed transitions between the different interface states. The call set-up appears on the left side of Figure 6/V.25 *bis* and proceeds as follows:

- The DTE, whenever it wishes to initiate a call, checks that circuit 125 is in the OFF condition, then turns ON circuit 108/1. A timer (T1) is started on the transition from state 1, *idle* to state 2.
- The DCE turns ON circuit 107 when it has recognized the successful establishment of the call, thus moving to state 3, *data transfer.*
- If the first call attempt is unsuccessful, the DCE may make further attempts according to its programming and national regulations. During this period, the interface remains in state 2.
- When in state 1, the DCE will turn circuit 125 ON whenever an incoming call occurs, and the interface moves to state 5, *incoming call.* State 6, *incoming call accepted,* is reached when the DTE turns ON circuit 108/1 to accept the call, which in turn leads to state 7, *answering station connecting.* The DCE may abort the incoming call by turning OFF circuit 108/1 when in state 7, and return to state 1.
- When in state 2, the DCE will turn circuit 125 ON whenever an incoming call has been detected prior to the DCE seizing the line. The interface then moves to state 6 as incoming calls have priority have over call set-up attempts. The DCE should remain in state 6 for at least 100 ms (this value is for further study) before entering state 7, to allow the DTE to recognize the ON condition on circuit 125.
- While in state 2, the DTE can abort the call attempt by turning OFF circuit 108/1. This may be done if timer T1 expires with circuit 107 remaining in the OFF condition.

Note – Timeout T1 could range from 1 to 5 minutes depending on the programming of the DCE and national regulations.

5.3 *Interface procedure at the answering data station*

This mode provides the DTE with the facility of accepting an incoming call on a "per call" basis.

This operating mode is shown on the right hand side of the state diagram shown in Figure 6/V.25 *bis* and proceeds as follows:

- The DCE turns ON circuit 125 whenever it detects a ringing signal on the line and moves from state 1, *idle*, to state 5, *incoming call.*
- If the DTE does not want to accept the call, it may hold circuit 108/1 in the OFF condition. After the end of the ringing signal, the interface returns to state 1.
- If the DTE wishes to accept the call, it turns circuit 108/1 ON, and moves from state 5, *incoming call*, to state 6, *incoming call accepted*, and then to state 7, *answering station connecting.*
- In state 7, *answering station connecting*, the DCE accepts the call as detailed in § 6. While in this state the DTE may abort the connection by turning OFF circuit 108/1.
- On completion of the connection procedure, the DCE turns ON circuit 107, moving then from state 7, *answering station connecting*, to state 3, *data transfer.*

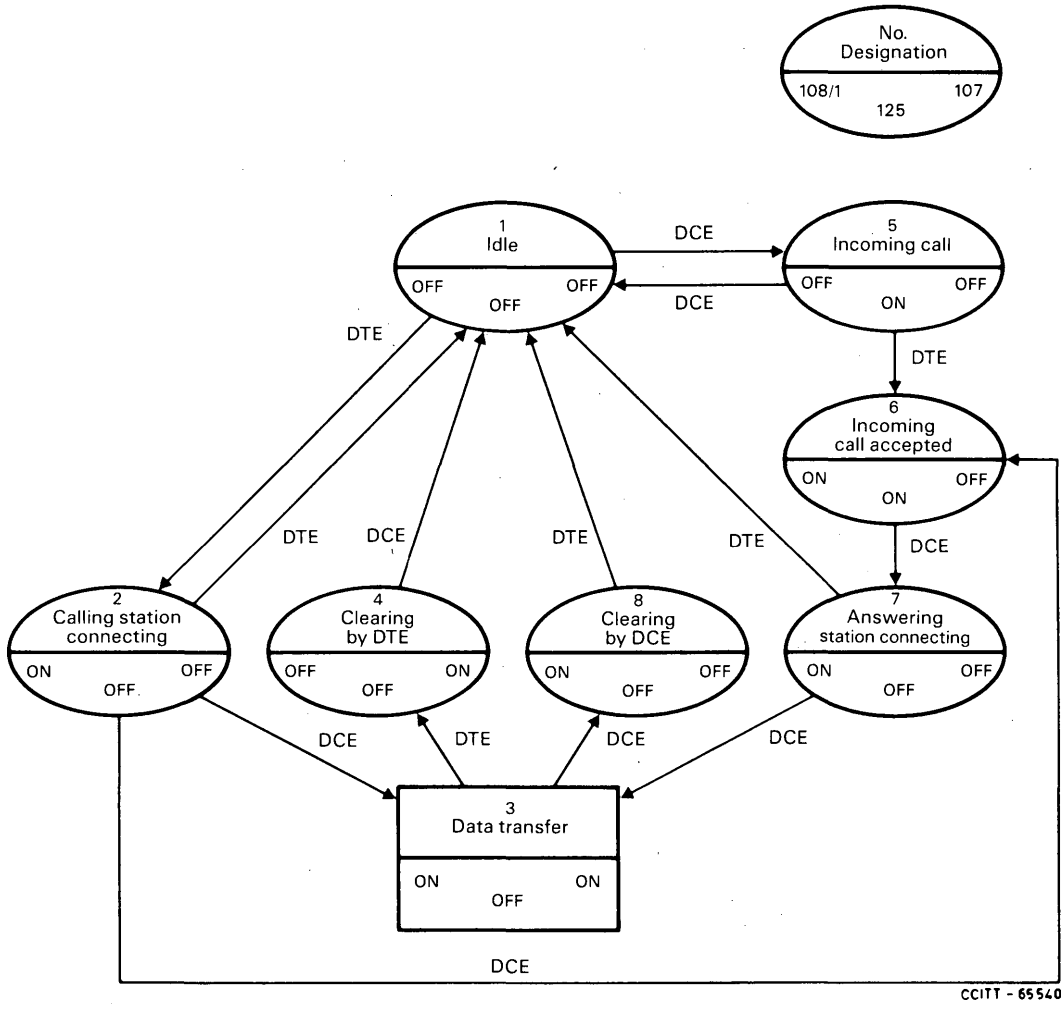


FIGURE 6/V.25 *bis*

Simplified procedure for direct call 108/1 answer mode

6 Line procedures

6.1 *Line procedure at the calling DCE*

- Whenever the DCE has received the *call request* (see Figure 5/V.25 *bis* and Figure 6/V.25 *bis*), the DCE seizes the line by going *off hook.*
- Dialling may proceed when dial tone has been detected, or, where national regulations permit this, after a fixed time delay. The value of this delay will be dependent on the national network.

- On completion of dialling, or, where possible, on recognizing the other end going off hook, a calling tone as specified in Recommendation V.25 is transmitted.
- During interruptions of the calling tone, the DCE monitors the line in order to detect call progress tones from the network and/or the answering tone, as specified in Recommendation V.25 provided by the remote DCE. If no answering tone is detected within a time-out, the DCE may go on hook and may issue an appropriate *call failure* indication. It may slso issue *call failure* indication on recognition of specific signalling tones from the network.
- When the answering tone has been recognized by the DCE as detailed in Recommendation V.25, it turns circuit 106 to the OFF condition.
- All other actions including the turning ON of circuit 107 and the completion of the connection procedure, are as detailed in Recommendation V.25.

The policy for handling unsuccessful calls may be dependent on the national networks. In this respect, a first level action by the call originating data station, which could involve blocking, by either the DCE or the DTE, of further call attempts is not part of this Recommendation.

A second level action, which could permit the Administrations to trace erroneous calls when a subscriber complains, should be, where required by the Administration, implemented in the following way:

6.1.1 *Calling station identification* (where required by the Administration)

To enable the Administrations to have means to trace the originator of erroneous calls, an identification message has to be transmitted on the line by the call originating data station.

6.1.1.1 *Criteria for transmission of identification information*

The calling station identification information should be transmitted after the transmission of the calling tone when:

- the answering tone is not received within a time interval T2 from the end of the last digit dialled, or
- the answering tone is not received within a time interval T3 from detection of the remote end by DCE going *off hook.*

The choice of time outs T2 and T3 and their durations is dependent on national regulations.

Whenever the DCE enters the transmission of the identification information on the line, it will defer the execution of any *clearing request* made by the DTE which puts circuit 108 in the OFF condition until the transmission of this identification information is completed.

The complete identification information should be transmitted successively 3 times or more.

6.1.1.2 *Modulation method*

The identification signal should be asynchronously frequency modulated with the frequencies 1300 Hz (mark) and 2100 Hz (space) in such a way that it is possible to receive this signal with a modem according to Recommendation V.23.

The modulation rate should be 1200 bauds. In cases where this rate cannot be realized, a modulation rate of 300 bauds should be used.

6.1.1.3 *Format of identification information*

The identification information should be encoded according to International Alphabet No. 5 with one start bit, one stop bit and an even parity bit according to Recommendations T.50 and V.4. The first digits of the identification number should contain the country code of the subscriber's telephone number.

6.1.1.4 *Implementation*

In addition to the contents of this Recommendation, the regulations of the national Administrations must also be complied with. The additional requirements may be:

- the use of the CRI command with or without the identification number;
- generation and storage of the identification number;
- complete structure and content of the identification number (except the first two digits);
- recording and detection of the identification information.

6.2 *Line procedure at the answering DCE*

- When ringing is received on the line, the DCE turns ON circuit 125 and where implemented, issues an *incoming call* indication if circuits 108/2 and 106 are in the ON condition.
- If circuit 108/1 or circuit 108/2 is OFF, the DCE waits for circuit 108 to be turned ON.
- If circuit 108/2 is ON, and the *disregard incoming call* command is not received within a period of time determined by national regulations, the DCE goes *off hook*.
- When circuit 108/1 is ON, the DCE goes *off hook* after a period of time determined by national regulations.
- If circuit 108 is not turned ON, then the call is not answered.
- Whenever the DCE goes *off hook*, it turns OFF circuit 106 if not already OFF.
- After going *off hook*, the DCE completes the connection procedure and turns circuit 107 ON, as detailed in Recommendation V.25.

7 Manual calling and answering

The operational procedures for manual calling to an automatic answering data station, and automatic calling to a manual answering data station, are the same as detailed in Recommendation V.25, §§ 6 and 7, with the exception that circuit 106 has to be turned OFF before turning ON circuit 107, in the mode *addressed call and/or answer authorized by the DTE.*

Where the answering data station is expected to have a manual answering mode, this may be indicated to the calling DCE. The method for doing this is for further study.

ANNEX A

(to Recommendation V.25 *bis*)

Test facilities

Guidance on maintenance facilities

This annex contains information on test facilities thought to be desirable in relation to implementations of Recommendation V.25 *bis* automatic calling procedures.

The adoption of such procedures and especially the provision of centralized maintenance facilities by Administrations may not be assumed.

In order to enable a fault to be located in either the DTE or the DCE, the DTE should not be involved in the test. The test may be initiated, e.g. by pressing a button on the DCE, whereas indication of the test result may be presented, e.g. by means of a visual indicator.

The actual test consists of two stages: a DCE self-test and a test in cooperation with a maintenance centre. In which order these two stages are activated is not specified in this Recommendation. The test of the modem part of the DCE will not be part of this Recommendation, but should be performed separately according to Recommendation V.54.

A.1 *DCE self-test stage*

In this stage, the DCE will test as many functions and hardware as reasonably possible.

The test should comprise a loop at the DTE-DCE interface similar to Recommendation V.54 loop 2 including all circuits normally exercised during the call set-up and clear phase. Further parts of the test depend on the DCE implementation, e.g. in case of a microprocessor-based design a functional test of the CPU, RAM and ROM would be appropriate.

A.2 *DCE test with maintenance centre*

In this stage, the procedure is as follows:

A.2.1 The user sets up manually a call with the maintenance centre (MC).

A.2.2 On answering the call, the MC will send an answering tone of appropriate length to ensure detection by the DCE.

A.2.3 As soon as the answering tone is detected, the DCE should be connected with the line.

A.2.4 After detecting the end of the answering tone, the DCE starts sending the dialling digits 1, 2, 3, 4, 5, 6, 7, 8, 9, 0 in accordance with the regulations of the Administration involved.

Note – They shall have the same spacing as during the automatic call set-up.

A.2.5 In case not all numbers are detected faultlessly, the MC will send a 2100 Hz tone for 0.4 ± 0.1 s indicating a negative test result and disconnect from the line.

A.2.6 On detecting the 2100 Hz tone, the DCE will end the test procedure and indicate a negative test result.

A.2.7 If all numbers are received correctly, the MC will send a 1300 Hz tone for 0.4 ± 0.1 s and start sending signalling tone towards the DCE to be defined by the Administration involved.

A.2.8 At the end of this sequence, a 2100 Hz tone will be sent for 0.4 ± 0.1 s and the MC will disconnect.

A.2.9 The DCE receiving the 2100 Hz tone will give a positive or negative indication depending on the test result and end the procedure.

Note – For pulse dialling, the open contact shall be coded by a 2100 Hz tone and the closed contact by no signal at all.

Recommendation V.26

2400 BITS PER SECOND MODEM STANDARDIZED FOR USE ON 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Mar del Plata, 1968; amended at Geneva, 1972, 1976 and 1980, Malaga-Torremolinos, 1984)

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

1 The principal characteristics for this recommended modem for transmitting data at 2400 bits per second on 4-wire leased point-to-point and multipoint circuits conforming to Recommendation M.1020 [1] are as follows:

a) it is capable of operating in a full-duplex mode;

b) four-phase modulation with synchronous mode of operation;

c) inclusion of a backward (supervisory) channel at modulation rates up to 75 bauds in each direction of transmission, the use of these channels being optional.

2 Line signals

2.1 The carrier frequency is to be 1800 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Division of power between the forward and backward channels*

If simultaneous transmission of the forward and backward channels occurs in the same direction, a backward channel shall be 6 dB lower in power level than the data channel.

2.3 The data stream to be transmitted is divided into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element. At the receiver the dibits are decoded and the bits are reassembled in correct order. Two alternative arrangements of coding are listed in Table 1/V.26. The left-hand digit of the dibit is the one occurring first in the data stream.

TABLE 1/V.26

Dibit	Phase change (see Note)	
	Alternative A	Alternative B
00	0°	+45°
01	+90°	+135°
11	+180°	+225°
10	+270°	+315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

The meaning of phase change for alternatives A and B is illustrated by the line signal diagram in Figure 1/V.26.

2.4 *Synchronizing signal*

For the whole duration of the interval between the OFF to ON transitions of circuits 105 and 106, the line signal shall be that corresponding to the continuous transmission of dibit 11. This shall be known as the synchronizing signal.

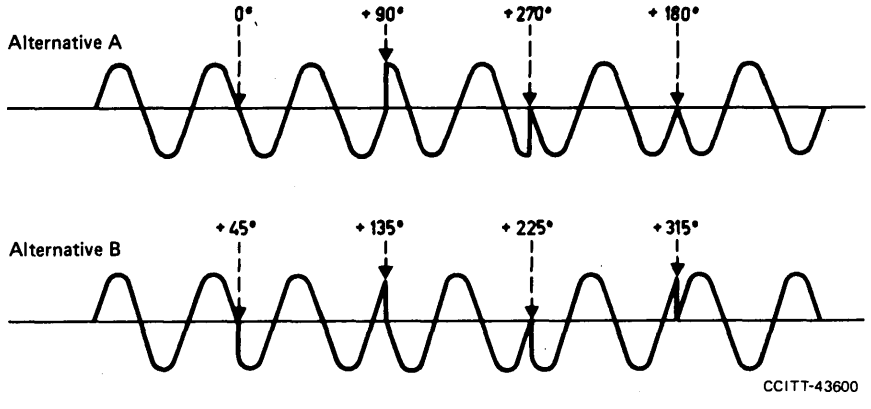


FIGURE 1/V.26

Note – Owing to several causes, the stability of timing recovery at the receiver is liable to be data-pattern sensitive. The presence of dibit 11 provides a stabilizing influence irrespective of the cause of lack of stability. Users are advised to include sufficient binary 1s in the data which will ensure that the dibit 11 will occur frequently. In certain cases, the use of a scrambling method may also facilitate timing recovery problems. However, prior agreement is required between users of a circuit.

3 Data signalling and modulation rates

The data signalling rate shall be 2400 bits per second ± 0.01%, i.e. the modulation rate is 1200 bauds ± 0.01%.

4 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance at the transmitter is ± 1 Hz and assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

5 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc., to be as recommended for backward channel in Recommendation V.23.

6 Interchange circuits

6.1 *List of interchange circuits concerned* (see Table 2/V.26)

6.2 *Threshold and response times of circuit 109*

A fall in level of the incoming line signal to −31 dBm or lower for more than 10 ± 5 ms will cause circuit 109 to be turned OFF. An increase in level to −26 dBm or higher will, within 10 ± 5 ms, turn this circuit ON. The condition of circuit 109 for levels between −26 dBm and −31 dBm is not specified except that the signal level detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition. These values shall be measured when the synchronizing signal as defined in § 2.4 above is being transmitted. It should be noted that the aforementioned times relate only to the defined function of circuit 109 and do not necessarily include the time for the modem to achieve bit synchronism.

Note – The signal levels specified above shall apply unless completion of Recommendation M.1020 [1] indicates otherwise.

TABLE 2/V.26

Interchange circuit		Forward (data) channel half-duplex or full-duplex (see Note)	
No.	Designation	Without backward channel	With backward channel
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105	Request to send	X	X
106	Ready for sending	X	X
107	Data set ready	X	X
108/1	Connect data set to line	X	X
109	Data channel received line signal detector	X	X
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
118	Transmitted backward channel data	–	X
119	Received backward channel data	–	X
120	Transmit backward channel line signal	–	X
121	Backward channel ready	–	X
122	Backward channel received line signal detector	–	X

Note — All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 8).

6.3 *Response times of circuits 106, 121 and 122*

Circuit 106		
OFF to ON	65-100 ms (see Note 1) (Provisional)	25-45 ms (see Note 2) (Provisional)
ON to OFF	⩽ 2 ms	
Circuit 121		
OFF to ON	80 ms to 160 ms	
ON to OFF	⩽ 2 ms	
Circuit 122		
OFF to ON	< 80 ms	
ON to OFF	15 ms to 80 ms	

Note 1 – These times shall be used when infrequent operation of circuit 105 is required, e.g. as in many cases of point-to-point usage. Further study is required to verify the range quoted.

Note 2 – These times shall be used when frequent operation of circuit 105 is required, e.g. in many cases of multipoint usage. Further study is required with a view to reducing these times.

6.4 *Threshold of circuit 122*

- greater than −34 dBm: circuit 122 ON
- less than −39 dBm: circuit 122 OFF

The condition of circuit 122 for levels between −34 dBm and −39 dBm is not specified except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

6.5 *Fault condition of interchange ciruits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

6.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

6.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

6.5.3 All other circuits not referred to above may use failure detection types 0 or 1.

7 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114 and receiver signal element timing, circuit 115. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment instead of in the data circuit-terminating equipment and be transferred to the modem via circuit 113.

8 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110 [2].

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the Series V application which minimizes the number of interchange circuits.

9

The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

Reference

[1] CCITT Recommendation *Characteristics of special quality international leased circuits, with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

Recommendation V.26 *bis*

2400/1200 BITS PER SECOND MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

(Geneva, 1972; amended at Geneva, 1976 and 1980, Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that there is a demand for data transmission at 2400 bit/s over the general switched telephone network;

(b) that a majority of connections over the general switched telephone network within some countries are capable of carrying data at 2400 bit/s;

(c) that a much lower proportion of international connections in the general switched telephone service are capable of carrying data at 2400 bit/s;

unanimously declares the view

(1) that transmission at 2400 bit/s should be allowed on the general switched telephone network. Reliable transmission cannot be guaranteed on every connection or routing and tests should be made between the most probable terminal points before a service is provided.

The CCITT expects that developments during the next few years in modern technology will bring about modems of more advanced design enabling reliable transmission to be given on a much higher proportion of connections.

Note – The provisions of this Recommendation are to be regarded as provisional in order to provide service where it is urgently required and between locations where it is expected that a reasonably satisfactory service can be given. The study of improved methods of transmission at 2400 bits/s or above over the general switched telephone network will be urgently continued with the aim of recommending a method of transmission which will enable a more reliable service to be given over a high proportion of the connections encountered in normal service.

(2) that the characteristics of the modems for this service shall provisionally be the following:

1 Principal characteristics

a) Use of a data signalling rate of 2400 bit/s with carrier frequency, modulation and coding according to Recommendation V.26, Alternative B (see Note below) on the communication channel. Administrations and users should note that the performance of this modem on international connections may not always be suitable for this service without prior testing and conditioning if required.

b) Reduced rate capability at 1200 bit/s.

c) Inclusion of a backward channel at modulation rates up to 75 bauds, use of this channel being optional.

Note – Attention is drawn to the fact that there are some old-type modems currently in operation for which the coding method in accordance with Recommendation V.26, Alternative A, is used.

2 Line signals at 2400 and 1200 bit/s

2.1 The carrier frequency is to be 1800 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Phase distortion limits*

The transmitted line signal spectrum should have linear phase characteristics (to be obtained by means of filters or equalizers or digital means). The deviation of the phase distortion characteristic should not exceed the limits specified in Figure 1/V.26 *bis*.

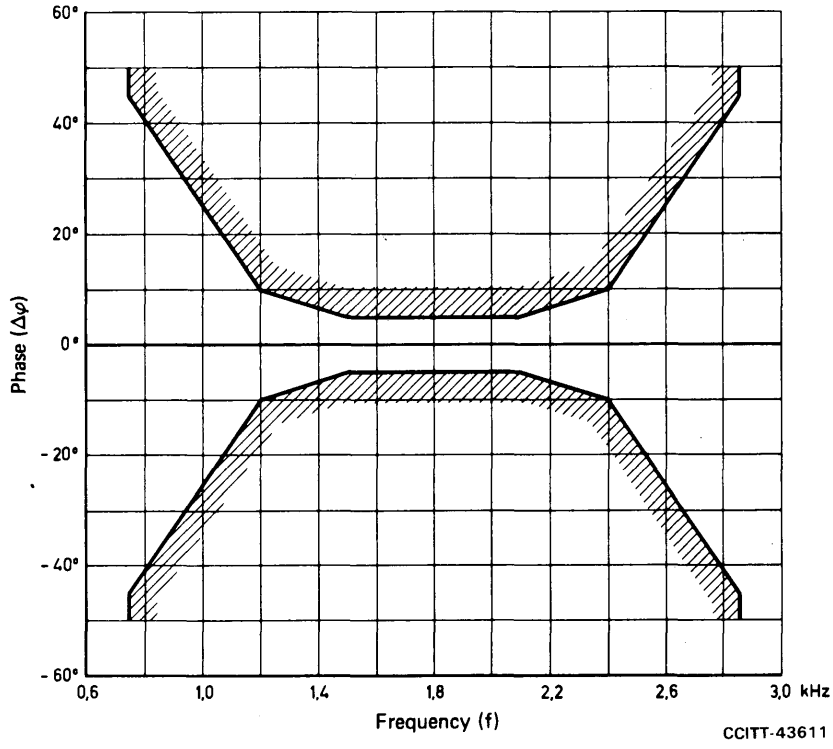


FIGURE 1/V.26 *bis*

Tolerance limit for phase distortion of the signal transmitted to the line

2.3 *Division of power between forward and backward channels*

Equal division of power between the forward and backward channels is recommended provisionally.

2.4 *Operation at 2400 bit/s*

2.4.1 The data stream to be transmitted is divided into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 1/V.26 *bis*). At the receiver the dibits are decoded and the bits are reassembled in correct order. The left-hand digit of the dibit is the one occurring first in the data stream.

The meaning of phase change is illustrated by the line signal diagram given in Figure 2/V.26 *bis*.

TABLE 1/V.26 *bis*

Dibit	Phase change (see Note)
00	+45°
01	+135°
11	+225°
10	+315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

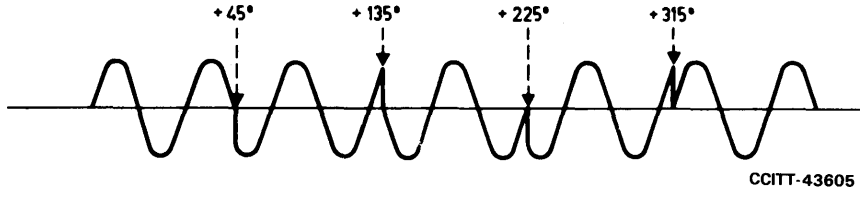


FIGURE 2/V.26 *bis*

2.4.2 *Synchronizing signal*

For the whole duration of the interval between the OFF to ON transitions of circuits 105 or 107 and 106, the line signal shall be that corresponding to the continuous transmission of dibit 11. This shall be known as the synchronizing signal (see § 5.2.2 below).

Note – Owing to several causes the stability of timing recovery at the receiver is liable to be data-pattern sensitive. The presence of dibit 11 provides a stabilizing influence irrespective of the cause of lack of stability. Users are advised to include sufficient binary 1s in the data which will ensure that the dibit 11 will occur frequently.

2.4.3 *Data signalling and modulation rates*

The data signalling rate shall be 2400 bit/s ± 0.01%, i.e. the modulation rate is 1200 bauds ± 0.01%.

2.5 *Operation at 1200 bit/s*

2.5.1 Coding and modulation used are 2-phase differential modulation with binary 0 for +90° and binary 1 for +270°.

2.5.2 The data signalling rate shall be 1200 bit/s ± 0.01%, the modulation rate remains at 1200 bauds ± 0.01%.

3 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance at the transmitter is ± 1 Hz and assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

4 Backward channel

4.1 *Modulation rate and characteristic frequencies for the backward channel*

The modulation rate and characteristic frequencies for the backward channel are as follows:

	F_z (symbol 1, mark)	F_A (symbol 0, space)
Modulation rate up to 75 bauds	390 Hz	450 Hz

In the absence of any signal on the backward channel interface, the condition Z signal is to be transmitted.

4.2 *Tolerances on the characteristic frequencies of the backward channel*

As the backward channel is a VF telegraph-type channel, the frequency tolerances should be as recommended in Recommendation R.35 [1] for frequency-shift voice-frequency telegraphy.

The ± 6 Hz frequency drift in the connection between the modems postulated in § 3 above would produce additional distortion in the backward channel. This should be taken into account in the design.

5 Interchange circuits

5.1 *List of essential interchange circuits*

The list of interchange circuits essential for the modems when used on the general switched telephone network, including terminals equipped for manual calling or answering or automatic calling or answering is given in Table 2/V.26 *bis*.

5.2 *Response times of circuits 106, 109, 121 and 122* (see Table 3/V.26 *bis*)

5.2.1 Circuit 109 response times are the times that elapse between the connection or removal of the test synchronizing signal to or from the modem receive line terminals and the appearance of the corresponding ON and OFF condition on circuit 109.

The level of the test synchronizing signal should fall within the level range between 3 dB above the actual OFF to ON threshold of the received line signal detector and the maximum admissible level of the received signal. At all levels within this range, the measured response times shall be within the specified limits.

5.2.2 Circuit 106 response times are from the connection to an ON or OFF condition on:

- circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106; or
- circuit 107 (where circuit 105 is not required to initiate the synchronizing signal) to the appearance of the corresponding ON or OFF condition on circuit 106.

5.3 *Threshold of data channel and backward channel received line signal detectors*

Level of received line signal at receive line terminals of modem for all types of connections, i.e. general switched telephone network or non-switched leased telephone circuits:

- greater than −43 dBm: circuits 109/122 ON
- less than −48 dBm: circuits 109/122 OFF

The condition of circuits 109 and 122 for levels between −43 dBm and −48 dBm is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

Where transmission conditions are known and allowed, it may be desirable at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

5.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

TABLE 2/V.26 *bis*

Interchange circuit		Forward (data) channel one-way system (see Note 1)				Forward (data) channel either-way system (see Note 1)	
No.	Designation	Without backward channel		With backward channel		Without backward channel	With backward channel
		Transmit end	Receive end	Transmit end	Receive end		
102	Signal ground or common return	X	X	X	X	X	X
103	Transmitted data	X		X		X	X
104	Received data		X		X	X	X
105	Request to send	X		X		X	X
106	Ready for sending	X		X		X	X
107	Data set ready	X	X	X	X	X	X
108/1 or 108/2 (see Note 2)	Connect data set to line / Data terminal ready	X	X	X	X	X	X
109	Data channel received line signal detector		X		X	X	X
111	Data signalling rate selector (DTE source)	X	X	X	X	X	X
113	Transmitter signal element timing (DTE source)	X		X		X	X
114	Transmitter signal element timing (DCE source)	X		X		X	X
115	Receiver signal element timing (DCE source)		X		X	X	X
118	Transmitted backward channel data				X		X
119	Received backward channel data			X			X
120	Transmit backward channel line signal						X
121	Backward channel ready				X		X
122	Backward channel received line signal detector			X			X
125	Calling indicator	X	X	X	X	X	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 7).

Note 2 – This circuit shall be capable of operation as circuit 108/1 or circuit 108/2 depending on its use.

TABLE 3/V.26 *bis*

Response times

Circuit 106		
OFF to ON	750 ms to 1400 ms (see Note 1)	a) 65 ms to 100 ms (see Note 2) b) 200 ms to 275 ms (see Note 2)
ON to OFF	⩽ 2 ms	
Circuit 109		
OFF to ON	300 ms to 700 ms (see Note 1)	5 ms to 15 ms (see Note 1)
ON to OFF	5 ms to 15 ms	
Circuit 121		
OFF to ON	80 ms to 160 ms	
ON to OFF	⩽ 2 ms	
Circuit 122		
OFF to ON	< 80 ms	
ON to OFF	15 ms to 80 ms	

Note 1 – For automatic calling and answering, the longer response times of circuits 106 and 109 are to be used during call establishment only.

Note 2 – The choice of response times depends upon the system application: a) limited protection given against line echoes; b) protection given against line echœs.

Note 3 – The above parameters and procedures, particularly in the case of automatic calling and answering are provisional and are the subject of further study. Especially the shorter response times for circuit 109 may need revision to prevent remnants of the synchronizing signal from appearing on circuit 104.

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

5.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

5.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114 and receiver signal element timing, circuit 115. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment instead of in the data circuit-terminating equipment and be transferred to the modem via circuit 113.

7 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

8 The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

9 When echo control device disabling is required, it is recommended that the procedures specified in Recommendation V.25 be followed.

10 Fixed compromise equalizer

A fixed compromise equalizer shall be incorporated into the receiver. The characteristics of this equalizer may be selected by Administrations but this should be the matter for further study.

Reference

[1] CCITT Recommendation *Standardization of FMVFT systems for a modulation rate of 50 bauds*, Vol. VII, Rec. R.35.

Recommendation V.26 *ter*

2400 BITS PER SECOND DUPLEX MODEM USING THE ECHO CANCELLATION TECHNIQUE STANDARDIZED FOR USE ON THE GENERAL SWITCHED TELEPHONE NETWORK AND ON POINT-TO-POINT 2-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that there is a demand for data transmission at 2400 bit/s in the duplex mode on the general switched telephone network (GSTN) and on point-to-point 2-wire leased telephone-type circuits;

(b) that there will be a demand to have compatibility with higher data signalling rate duplex modems in the fall-back mode;

(c) that in this case the echo cancellation technique (ECT) is foreseen,

unanimously declares

the view that the characteristics of the modems for this service shall provisionally be as follows:

1 Introduction

This modem is intended for use on connections on the GSTN and on point-to-point 2-wire leased telephone-type circuits (see Note 1). Its principal characterisics are as follows:

a) duplex mode of operation on the GSTN and point-to-point leased circuits,

b) half-duplex mode of operation (optional) on the GSTN and point-to-point leased circuits (Note 2),

c) channel separation by echo cancellation,

d) differential phase-shift modulation for each channel with synchronous line transmission at 1200 baud (nominal),

e) inclusion of a scrambler,

f) inclusion of a compromise or adaptive equalizer,

g) inclusion of test facilities,

h) operation with data terminal equipment (DTE) in the following modes:

2400 bit/s synchronous,

1200 bit/s synchronous (fall-back rate),

2400 bit/s start stop (optional),

1200 bit/s start stop (optional) (fall-back rate),

i) inclusion of an operating sequence intended to allow interworking with 2-wire duplex 4800 bit/s modem (which modem is for further study).

Note 1 – In certain countries the use of such a modem over the GSTN may not be allowed.

Note 2 – When the optional half-duplex mode of operation is used, provisions in § 7 shall supersede provisions given elsewhere in this Recommendation.

2 Line signals

2.1 *Carrier frequency*

The carrier frequency shall be 1800 ± 1 Hz. No separate pilot tones are provided.

2.2 *Data line signal level*

The power levels used will conform to Recommendation V.2.

2.3 *Equalizer*

If a fixed compromise equalizer is used, it shall be incorporated in the receiver. The characteristics of this equalizer may be selected by Administrations.

The possibility of producing compromise equalizer characteristics for international connections is for further study.

If an adaptive equalizer is used, it shall be able to converge on data signals at 2400 bit/s without a training sequence.

2.4 *Spectrum and group-delay characteristics*

A 100% raised cosine amplitude spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1200 Hz and 2400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1200 Hz and 2400 Hz.

The group-delay of the transmit filters shall be within ± 100 microseconds over the frequency range 1200-2400 Hz.

2.5 *Modulation*

2.5.1 *Data signalling rates*

The data signalling rate transmitted to line shall be 2400 bit/s or 1200 bit/s ± 0.01% with a modulation rate of 1200 baud ± 0.01%.

2.5.2 *Encoding of data bits*

2.5.2.1 *2400 bits per second*

At 2400 bit/s the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 1/V.26 *ter*). At the receiver, the dibits are decoded and reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.26 *ter*

Line encoding at 2400 bit/s

Dibit values	Phase change (see Note)
00	0°
01	90°
11	180°
10	270°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5.2.2 *1200 bits per second*

At 1200 bit/s each bit shall be encoded as a phase change relative to the phase of the preceding signal element (see Table 2/V.26 *ter*).

TABLE 2/V.26 *ter*

Line encoding at 1200 bit/s

Bit values	Phase change (see Note)
0	0°
1	180°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.6 *Received signal frequency tolerance*

The receiver shall be able to operate with frequency offsets in the signal received from the other modem of up to ± 7 Hz.

2.7 *Synchronizing signals*

Synchronizing signals are used in the operating sequence and in the half-duplex mode (see §§ 6.3 and 7). The synchronizing signals, for both data signalling rates, are divided into two segments as follows:

2.7.1 The composition of segment 1 is continuous 180° phase reversals for 32 symbol intervals.

2.7.2 Segment 2 is a pattern derived by scrambling binary ones with the scramblers defined in § 5. The length of the pattern is 64 bits (32 symbol intervals) for 2400 bit/s and 64 bit/s (64 symbol intervals) for 1200 bit/s. The patterns are defined in Table 3/V.26 *ter*. See also Appendix I.

TABLE 3/V.26 *ter*

Data signalling rate	Scrambler (see § 5)	Segment 2 phase changes (in degrees)
2400 bit/s	GPC	0, 180, 180, 180, 180, 0, 0, 0, 0, 180, 180, 270, 90, 180, 0, 0, 90, 180, 0 ...
2400 bit/s	GPA	0, 180, 180, 180, 180, 0, 0, 0, 0, 180, 180, 270, 90, 180, 0, 180, 180, 270, 0 ...
1200 bit/s	GPC	0, 0, 180, 180, 180, 180, 180, 180, 180, 180, 0, 0, 0, 0, 0, 0, 0, 0, 180, 180, 180, 180, 0, 0, 180, 180, 180, 0, 0, 0, 0, 0, 180, 180, 180 ...
1200 bit/s	GPA	0, 0, 180, 180, 180, 180, 180, 180, 180, 180, 0, 0, 0, 0, 0, 0, 0, 0, 180, 180, 180, 180, 180, 0, 0, 180, 180, 180, 0, 0, 180, 180, 180, 0, 180, 0 ...

3 Interchange circuits

3.1 *Essential and optional interchange circuits*

These are listed in Table 4/V.26 *ter*.

3.2 *Circuit 106 response times* (see Table 5/V.26 *ter*)

Circuit 106 response times are from the application of an ON or OFF condition on circuit 105. See also § 6.3 for conditions of circuit 106 during the operating sequence.

3.3 *Threshold and response times of circuit 109*

3.3.1 *Threshold*

The level of received line signal at the receive line terminals of the modem for all types of connections, i.e. the general switched telephone network or non-switched 2-wire leased telephone type circuits, is:

- greater than −43 dBm: circuit 109 ON
- less than −48 dBm: circuit 109 OFF

Where transmission conditions are known and allowed, it may be desirable at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

TABLE 4/V.26 *ter*

Interchange circuit (see Note 1)		Notes
No.	Designation	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	
106	Ready for sending	
107	Data set ready	
108/1 or	Connect data set to line	2
108/2	Data terminal ready	2
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	
112	Data signalling rate selector (DCE source)	3
113	Transmitter signal element timing (DTE source)	4
114	Transmitter signal element timing (DCE source)	5
115	Receiver signal element timing (DCE source)	5
125	Calling indicator	6
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.5).

Note 2 – This circuit shall be capable of operation as circuit 108/1 or circuit 108/2 depending on its use.

Note 3 – This circuit is optional.

Note 4 – When the modem is not operating in a synchronous mode at the interface, any signals on circuit 113 shall be disregarded and the DTE may not have a generator connected.

Note 5 – When the modem is not operating in a synchronous mode, this circuit shall be clamped to the OFF condition and the DTE may not terminate the circuit.

Note 6 – This circuit is for use with the general switched telephone network only.

TABLE 5/V.26 *ter*

	Constant carrier
Circuit 106	
OFF to ON	⩽ 2 ms
ON to OFF	⩽ 2 ms

In addition, for use over special quality leased circuits (see Recommendation M.1020) the response levels of the received line signal detector shall be:

- greater than −26 dBm: circuit 109 ON
- less than −31 dBm: circuit 109 OFF

The condition of circuit 109 between the ON and OFF levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for the ON to OFF transition.

3.3.2 *Response time*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104.

The ON to OFF response time of circuit 109 is 5 ms to 15 ms. See also § 6.3 for the condition of circuit 109 during the operating sequence.

Following a drop-out after the initial handshake, circuit 109 shall be turned ON 40 to 50 ms after the level of the receiver signal appearing at the line terminal of the modem exceeds the relevant threshold defined in § 3.3.1.

3.4 *Timing arrangement*

Clocks shall be included in the modem to provide the DTE with transmitter element timing (circuit 114) and receiver signal element timing (circuit 115). The transmitter element timing may be originated in the DTE and be transferred to the modem via the appropriate interchange circuit, circuit 113.

3.5 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.6 *Fault condition of interchange circuits*

(See § 7 of Recommendation V.28 for association of the receiver failure detection types.)

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Modes of operation

The modem can be configured for the following modes of operation:

Mode i) 2400 bit/s ± 0.01% synchronous

Mode ii) 2400 bit/s start-stop 8, 9, 10 or 11 bits per character (optional)

Mode iii) 1200 bit/s ± 0.01% synchronous

Mode iv) 1200 bit/s start-stop 8, 9, 10 or 11 bits per character (optional).

4.1 *Transmitter*

In the synchronous modes of operation, the modem shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or circuit 114. The data shall then be scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5.

When circuit 114 is used, the modem shall derive its line signal clock from the internal clock source or, alternatively, from the receive signal element timing.

In the start-stop modes, the modem shall accept a data stream of start-stop characters from the DTE at a nominal rate of 2400 or 1200 bit/s. The start-stop data shall be converted to a form suitable for transmission synchronously at 2400 or 1200 bit/s ± 0.01%, then scrambled in accordance with § 5 and then passed to the modulator for encoding in accordance with § 2.5. The modem shall derive its line signal clock from the internal clock source or, alternatively, from the receive signal element timing.

It shall be possible to condition the converter to accept the following character formats, viz:

a) a one-unit start element, followed by 7 data units, and a stop element of one unit in length (9-bit characters);

b) a one-unit start element, followed by 8 data units, and a stop element of one unit in length (10-bit characters);

c) a one-unit start element, followed by 9 data units, and a stop element of one unit in length (11-bit characters).

The converter may also accept characters consisting of:

d) a one-unit start element, followed by 6 data units, and a stop element of one unit in length (8-bit characters).

Note that character formats c) and d) do not conform to International Alphabet No. 5.

The character format selected shall be the same for both transmitter and receiver. The characters shall be in accordance with Recommendation V.4 regardless of whether they conform to International Alphabet No. 5. It shall be possible to transmit characters contiguously or with any additional continuous stop element of arbitrary length between characters.

Note – In each of the four formats, data units can be replaced by additional stop units. For example, format c) will allow 11-bit characters consisting of a one-unit start element, followed by 8 data units and a stop element of 2 units to be handled.

4.1.1 *Signalling rate range*

The intracharacter signalling rate (signalling rate of the start bit and information bits within each character) provided by the DTE on circuit 103 must be 2400 or 1200 bit/s +1%, −2.5%. In Mode ii), the character rate (the reciprocal of the time interval between successive start bits) provided by the DTE over circuit 103 must not exceed:

303 characters per second for 8-bit characters

269.3 characters per second for 9-bit characters

242.4 characters per second for 10-bit characters

220.3 characters per second for 11-bit characters.

The start-stop to synchronous converter in the modem transmitter shall as often as is necessary delete the stop bits of the incoming characters in order to attain the nominal transmission rate. No more than one stop bit shall be deleted for any 8 consecutive characters.

When the character rate provided by the DTE on circuit 103 is less than:

300 characters per second for 8-bit characters

266.6 characters per second for 9-bit characters

240 characters per second for 10-bit characters

218.2 characters per second for 11-bit characters,

the start-stop to synchronous converter in the modem is transmitting more bits per second than are provided by the DTE. The converter shall therefore insert extra stop bits in between the transmitted characters.

In Mode iv) the character rates are half those for Mode ii).

4.1.2 *Extended signalling rate range (optional)*

Certain DTEs and multiplexers are not within the +1% overspeed limit. Facilities may therefore be provided to enable the modem to accept data from a DTE having an intracharacter signalling rate of 2400 or 1200 bit/s +2.3%, −2.5%, with 8, 9, 10 or 11 bits per character by deletion of up to one stop bit in any four consecutive characters. A modem transmitter set to work with 2.3% maximum overspeed can handle data received from a DTE in accordance with § 4.1.1.

4.1.3 *Break signal*

If the converter detects M to $2M + 3$ bits all of "start" polarity, where M is the number of bits per character in the selected format, the converter shall transmit $2M + 3$ bits all of "start" polarity. If the converter detects more than $2M + 3$ bits all of "start" polarity, the converter shall transmit all these bits as "start" polarity.

Note – The DTE must transmit on circuit 103 at least $2M$ bits of "stop" polarity after the "start" polarity break signal before sending further data characters. This ensures that the receiving modem can regain character synchronism.

4.2 *Receiver*

In the synchronous modes of operation, the modem shall give synchronous data to the DTE on circuit 104 under control of circuit 115.

In the start-stop modes, the intracharacter signalling rate provided to the DTE over circuit 104 shall be in the range 2400 to 2455 bit/s for Mode ii), in the range 1200 to 1227 bit/s for Mode iv). The nominal length of the start and data elements for all characters shall be the same. The length of the stop element shall not be reduced by more than 12% for the basic signalling rate range (or 25% for the optional extended signalling rate range) to allow for overspeed in the transmitting terminal.

The use of the basic signalling rate range is preferred since it results in lower distortion. The choice of range shall be made at time of installation, and shall be the same for both transmitter and receiver. It is not intended to be under customer control.

4.2.1 *Break signal*

The $2M + 3$ or more bits of "start" polarity received from the transmitting modem shall be output on circuit 104. The modem shall then regain character synchronism from the following "stop" to "start" transition.

5 Scrambler and descrambler

Each transmission direction uses a different scrambler. The way to allocate the scramblers/descramblers is described in § 6.1.1.

A self-synchronizing scrambler/descrambler shall be included in the modem. According to the direction of transmission (see § 6.1) the generating polynominal is: GPC = $1 + x^{-18} + x^{-23}$ or GPA = $1 + x^{-5} + x^{-23}$.

At the transmitter the scrambler shall effectively divide the message polynomial (of which the input data sequence represents the coefficients in descending order) by the scrambler generating polynomial to generate the transmitted sequence; at the receiver the received polynomial (of which the received data sequence represents the coefficient in descending order) shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix I.

6 Operating sequence

6.1 *Scrambler/descrambler allocation and signalling rate selection*

6.1.1 *General switched telephone network (GSTN)*

On the general switched telephone network the modem at the calling data station shall use the scrambler with the GPC generating polynomial and the descrambler with the GPA generating polynomial (call mode). The modem at the answering data station shall use the scrambler with the GPA generating polynomial and the descrambler with the GPC generating polynomial (answer mode).

In some situations, however, for example, when calls are established on the GSTN by operators, bilateral agreement on call mode/answer mode allocation will be necessary.

The calling and answering modems automatically condition themselves to operate at the correct data signalling rate by exchanging rate patterns at the bit rate of 1200 bit/s during the operating sequences, as defined in § 6.3.1.

6.1.2 *Point-to-point leased circuits*

Scrambler/descrambler allocation, data signalling rate selection and call mode and answer mode designation on point-to-point leased circuits will be by bilateral agreement between Administrations or users.

6.1.3 *Rate patterns*

The rate pattern is a scrambled sequence of a particular repeated octet transmitted 32 times.

Out of the possible 256 binary numbers, the 34 following hexadecimal numbers are selected:

01 – 03 – 05 – 07 – 09 – 0B – 0D – 0F – 11 – 13 – 15 – 17 – 19 – 1B – 1D – 1F – 25 – 27 – 2B – 2D – 2F – 33 – 35 – 37 – 3B – 3D – 3F – 55 – 57 – 5B – 5F – 6F – 77 – 7F

Each of the binary octets (numbers listed above) may be replaced by one of its rotations.

The transmission of an octet begins by the least significant bit.

Table 6/V.26 *ter* shows the relationship between an octet value and one or two bit rates (see Note 2 of the table) enabled in a modem.

TABLE 6/V.26 *ter*

Rate pattern octet coding

Octet (see Note 1)		Bit rate (bit/s)		
Hexadecimal	Binary	1200	2400	4800 (see Note 2)
	LSB			
01	0 0 0 0 0 0 0 1	X		
03	0 0 0 0 0 0 1 1		X	
05	0 0 0 0 0 1 0 1			X
07	0 0 0 0 0 1 1 1	X	X	
09	0 0 0 0 1 0 0 1		X	X

Note 1 – In the case of an interface according to Recommendation V.24, only two rates can be selected by circuits 111 and 112. A new kind of interface under study may enlarge the possibilities.

Note 2 – These octets assignments are provisional.

6.2 *V.25 automatic answering sequence*

The V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted on point-to-point leased circuits or on national connections on the GSTN, where permitted by the Administration.

6.3 *Operating protocol*

The means of achieving automatic bit rate selection, initial echo cancellation and synchronism between the call mode and the answer mode modems on international GSTN connections and leased lines are shown in Figure 1/V.26 *ter*.

The automatic bit rate selection, initial echo cancellation and synchronizing signals are based on a half-duplex procedure. After this procedure, both modems shall continue to operate adaptive echo cancellation during duplex data transmission.

The operating sequence is divided into three sub-sequences: A, B and C (see Note).

Sequence A is the answering sequence according to Recommendation V.25.

Sequence B is the data bit rate selection sequence operated at 1200 bit/s.

Sequence C is the echo cancelling sequence operated at the selected bit rate.

At the end of these three sequences, the modem is conditioned to transmit and receive data.

Note – Manufacturers should note that the impedance of the modems as seen by the telephone line should not be varied throughout the duration of the connection.

6.3.1 *Description*

6.3.1.1 *Sequence A (answering sequence)*

6.3.1.1.1 *Call mode modem*

a) On connection to line it shall condition the scrambler and the descrambler in accordance with § 6.1.1.

b) In accordance with Recommendation V.25, after the detection of the 2100 Hz tone and a silent period of 75 ± 20 ms, the modem shall apply an ON condition to circuit 107.

6.3.1.1.2 *Answer mode modem*

a) On connection to line it shall condition the scrambler and the descrambler in accordance with § 6.1.1.

b) In accordance with Recommendation V.25, the modem is silent during 2.15 ± 0.35 seconds, sends a 2100 ± 15 Hz tone for 3.3 ± 0.7 seconds, and then remains silent for 75 ± 20 ms.

c) In accordance with Recommendation V.25, after the silent period, it shall apply an ON condition to circuit 107.

6.3.1.2 *Sequence B (data bit rate selection sequence)*

The call and the answer mode modems are conditioned to transmit and receive at 1200 bit/s in a half-duplex mode.

6.3.1.2.1 *Call mode modem*

a) The modem waits until it detects at least 4 consecutive error free octets of the rate pattern (see Note 1).

The calling modem selects the maximum rate compatible with the answering modem or the maximum rate it can transmit.

b) Then, it remains silent during 250 ± 5 ms.

c) After that it transmits the synchronization sequence followed by 256 bits of a rate pattern corresponding to the selected bit rate in accordance with § 6.1.3.

d) Then, it applies the appropriate condition to circuit 112 (if used).

6.3.1.2.2 *Answer mode modem*

a) The modem transmits the receiver synchronization signals defined in § 2.7 followed by 256 bits of the rate pattern which indicates the set of rates available for the answering modem in accordance with § 6.2.

b) The modem remains silent until it detects at least 4 consecutive error-free octets of a rate pattern.

If a rate pattern is not detected within 2 seconds following the end of the rate pattern transmitted by the answering modem, it shall resume the operating sequence at the beginning of sequence B.

If the rate pattern indicates a rate not available, the modem shall disconnect from the line.

If the rate pattern indicates a rate available, the modem applies the appropriate condition to circuit 112 (if used).

c) Then, it remains silent again during 250 ± 5 ms.

d) In accordance with Recommendation G.164, the modem transmits a 2100 ± 15 Hz tone for 500 ± 50 ms to disable echo suppressors, then remains silent for 75 ± 20 ms.

6.3.1.3 *Sequence C (echo cancelling procedure)*

The call and the answer mode modems are conditioned to transmit, to receive and to cancel the echo at the selected data bit rate.

6.3.1.3.1 *Call mode modem*

a) The modem remains silent until 64 consecutive received scrambled binary 0s are detected. The modem shall then transmit the echo cancellation sequence (see Notes 2 and 3) until a sufficient degree of echo cancellation is available locally.

b) At the end of this sequence the modem shall be silent during 25 ± 3 ms and then transmit the receiver synchronization signals followed by scrambled binary 0s.

c) After detection of scrambled binary 0s, refinement of echo cancellation and detection of consecutive received scrambled binary 0s (Note 4) during a period of 64 bits, the calling modem shall apply the ON condition to circuit 109 and transmit scrambled binary 1s during a fixed period of 128 bits.

d) Then, the circuit 106 is enabled to respond to the condition of circuit 105 (see Notes 5 and 6).

6.3.1.3.2 *Answer mode modem*

a) The modem transmits the echo cancellation sequence (see Note 2) until a sufficient degree of echo cancellation is available locally (see Note 3).

b) After this sequence, the modem is silent during 25 ± 3 ms and then transmits the receiver synchronization signals followed by scrambled binary 0s.

c) After detection of a signal transmitted by the calling modem during a period of 50 ± 5 ms, the answering modem remains silent.

d) After detection of 64 consecutive received scrambled binary 0s, the modem transmits the receiver synchronization signals followed by scrambled binary 0s.

e) After refinement of echo cancellation and the detection of a further 64 consecutive scrambled binary 0s whilst operating in duplex mode, the modem transmits scrambled binary 1s.

f) After detection of 64 consecutive received scrambled binary 1s the modem applies an ON condition on circuit 109 and enables circui 106 to respond to the condition of circuit 105 (see Notes 5 and 6).

Note 1 – If 4 consecutive error-free octets of the rate pattern are not detected the modem remains silent.

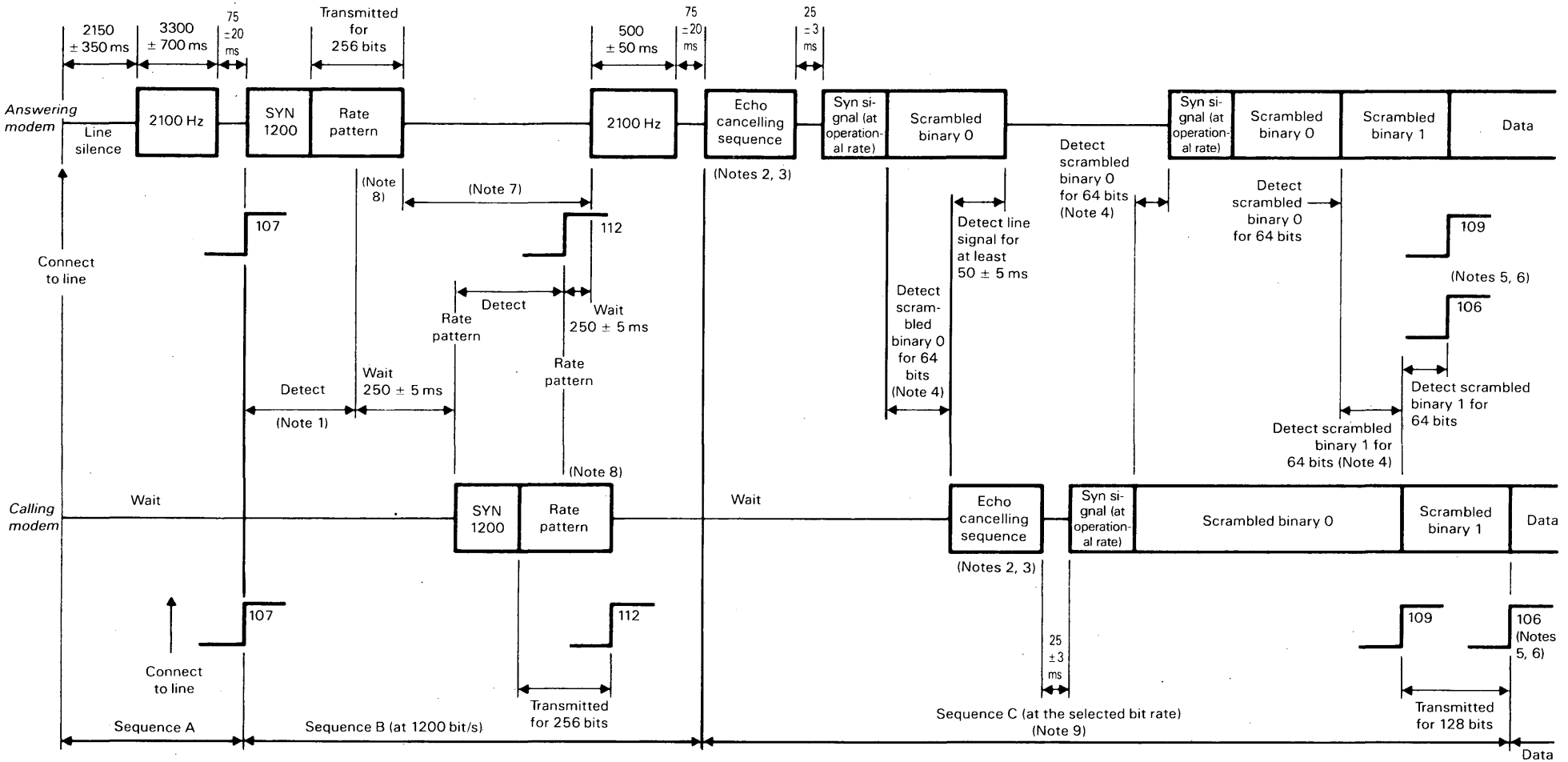
Note 2 – The echo cancellation sequence must not contain more than 32 consecutive unscrambled or scrambled binary 0s.

Note 3 – Manufacturers are cautioned that the time duration of the echo cancellation sequence has to be at least 650 ms when operating with network echo cancellers in accordance with Recommendation G.165.

Note 4 – The detection of scrambled binary 1s or 0s should start only after the receiver synchronization signals are completed.

Note 5 – When circuit 106 is in the OFF condition, circuit 103 shall be changed to the binary 1 condition.

Note 6 – Users may wish to note that if in the DTE a time-out exists between the ON conditions of circuit 107 and circuit 106, this time-out shall be greater than 15 seconds.



Notes 1 to 6 - See Notes 1 to 6 of § 6.3.

Note 7 - If 4 consecutive octets of rate pattern are not detected within 2 seconds, the modem resumes sequence B.

Note 8 - Rate pattern is defined in § 6.1.3.

Note 9 - Sequence C is defined for operation at 2400 bit/s and 1200 bit/s and is under study for the higher bit rate of 4800 bit/s.

FIGURE 1/V.26 *ter*

Operating sequences

7 Half-duplex mode of operation

This mode of operation is optional.

7.1 *Synchronizing signals*

The synchronizing signals for both data signalling rates are divided into segments.

7.1.1 *Segment 1*

The composition of segment 1 is continuous 180° phase reversals for 32 symbol intervals without protection against talker echo or for 256 symbol intervals with protection against talker echo.

7.1.2 *Segment 2*

As defined in § 2.7.2.

7.2 *Response times of circuits 106 and 109*

See Table 7/V.26 *ter*.

TABLE 7/V.26 *ter*

Response times				
Circuit 106	With protection against talker echo		Without protection against talker echo	
	2400 bit/s	1200 bit/s	2400 bit/s	1200 bit/s
OFF to ON	240 ± 10 ms	267 ± 10 ms	55 ± 2 ms	82 ± 2 ms
ON to OFF	⩽ 2 ms			
Circuit 109 OFF to ON	See § 7.2.1			
ON to OFF	5 to 15 ms			

7.2.1 *Circuit 109*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104. Circuit 109 is prevented from turning ON during reception of unmodulated carrier when the optional protection against talker echo is used.

7.2.2 *Circuit 106*

Circuit 106 response times are from the connection of an ON or OFF condition on:

- circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106; or
- circuit 107 (where circuit 105 is already ON) to the appearance of the corresponding ON or OFF condition on circuit 106 as defined in the operating sequence in § 7.4.

7.3 *Clamping of circuits 104 and 109*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations.

7.4 *Operating sequence*

The means of achieving automatic bit rate selection, and synchronism between the call mode and the answer mode modems on international GSTN connections and leased lines are shown in Figure 2/V.26 *ter.*

The operating sequence is divided in two sequences, A and B_1.

The sequence A is the answering sequence according to Recommendation V.25 defined in § 6.3.1.1 above.

The sequence B_1 is the data bit rate selection sequence operated at 1200 bit/s.

At the end of these two sequences, the modem may now transmit or receive data.

7.4.1 *Description of sequence B_1*

During the sequence B_1 circuits 106 and 109 are clamped to the OFF condition.

The call and the answer mode modems are conditioned to transmit and receive at 1200 bit/s in a half-duplex mode.

7.4.1.1 *Call mode modems*

a) The modem waits until it detects at least 4 consecutive error-free octets of the rate pattern (see Note 1, Figure 2/V.26 *ter*). The calling modem selects the maximum rate compatible with the answering modem or the maximum rate it can transmit.

b) Then, it remains silent during 250 ± 5 ms.

c) After that it transmits the synchronization sequence defined in § 7.1 followed by 256 bits of a rate pattern corresponding to the selected bit rate in accordance with § 6.1.3 (see Note 1, Figure 2/V.26 *ter*).

d) Then, it applies the appropriate condition to circuit 112 (if used).

e) The modem remains silent during 250 ± 5 ms, and then it enables circuit 106 to respond to circuit 105 and circuit 109 to operate as defined in § 7.2.1.

7.4.1.2 *Answer mode modem*

a) The modem transmits the receiver synchronization signals defined in § 7.1 followed by 256 bit of the rate pattern which indicates the set of rates available for the answering modem in accordance with § 6.1.3.

b) The modem remains silent until it detects at least 4 consecutive error-free octets of a rate pattern.

If a rate pattern is not detected within 2 seconds following the end of the rate pattern transmitted by the answering modem, it shall resume the operating sequence at the beginning of sequence B_1.

If the rate pattern indicates a rate not available, the modem shall disconnect from the line.

if the rate pattern indicates a rate available, the modem applies the appropriate condition to circuit 112 (if used).

c) Then, it remains silent again during 250 ± 5 ms.

d) After the silent period the modem enables circuit 109 to operate as defined in § 7.2.1.

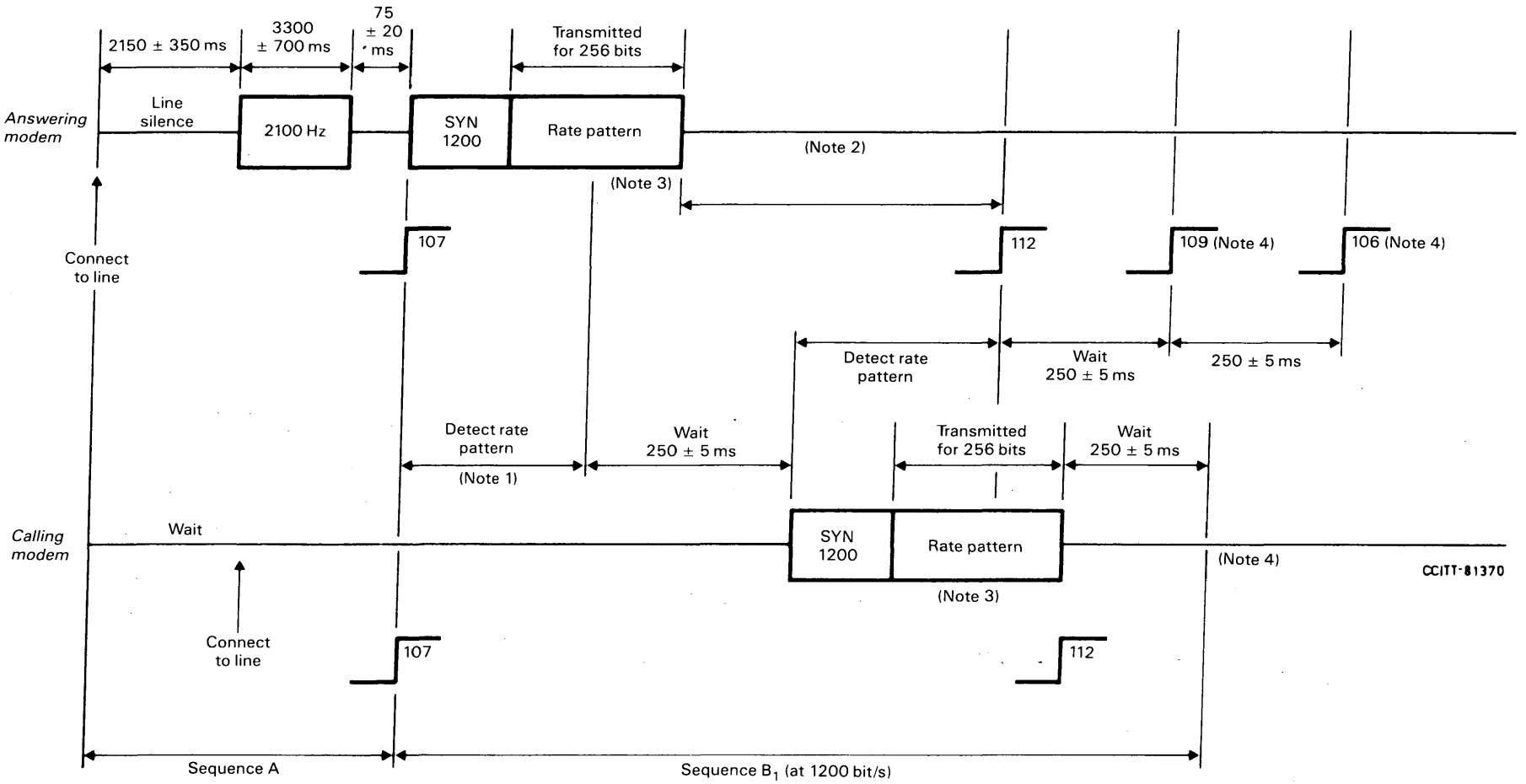
e) The modem waits 250 ± 5 ms prior to enabling circuit 106 to respond to circuit 105.

8 Testing facilities

Test loops 2 and 3 as defined in Recommendation V.54 shall be provided. Interface operation shall be as defined in Recommendation V.54.

8.1 *Remote loop 2*

Instigation and termination of remote loop 2 shall be in accordance with Recommendation V.54.



Note 1 - If 4 consecutive error free octets of the rate pattern are not detected the modem remains silent.

Note 2 - If 4 consecutive error free octets of the rate pattern are not detected within 2 seconds the modem resumes sequence B_1.

Note 3 - Rate pattern is defined in § 6.1.2.

Note 4 - The condition of circuit 106 shall respond to circuit 105, and the circuit 109 shall operate as defined in § 7.2.1.

FIGURE 2/V.26 *ter*

Operating sequences in half-duplex mode

APPENDIX I

(to Recommendation V.26 *ter*)

Detailed scrambling and descrambling process

I.1 *Scrambling*

The message polynomial is divided by the generating polynomial GPC = $1 + x^{-18} + x^{-23}$ or GPA = $1 + x^{-5} + x^{-23}$ (see Figure I-1/V.26 *ter* and I-2/V.26 *ter* respectively), according to the transmission direction. The coefficients of the quotient of this division taken in descending order from the data sequence D_s to be transmitted. The expression of this sequence is:

$D_s = D_i \oplus D_s\, x^{-18} \oplus D_s\, x^{-23}$, when the generating polynomial GPC is used;

$D_s = D_i \oplus D_s\, x^{-5} \oplus D_s\, x^{-23}$, when GPA is used.

D_i is the data sequence applied to the scrambler.

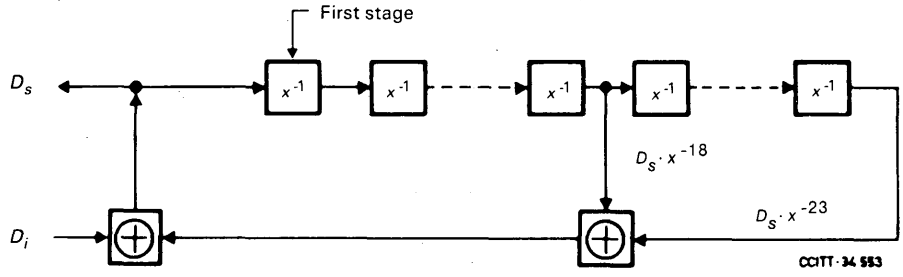


FIGURE I-1/V.26 *ter*

Scrambler with GPC generating polynomial

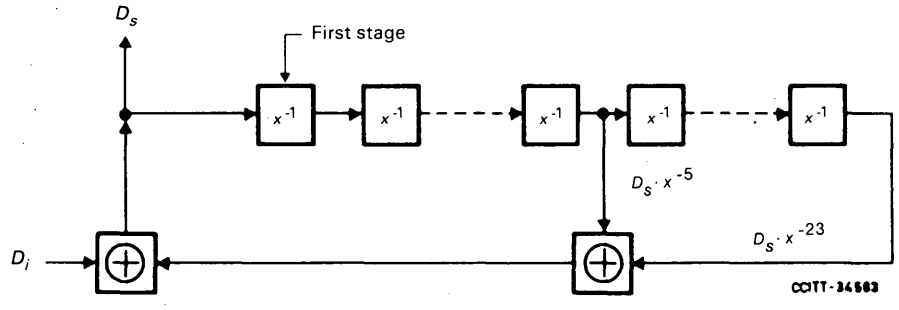


FIGURE I-2/V.26 *ter*

Scrambler with GPA generating polynomial

I.2 *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial GPC or GPA (see Figures I-3/V.26 *ter* and I-4/V.26 *ter* respectively) to form the recovered message polynomial. The coefficients of the recovered polynomial taken in descending order form the output data sequence D_o with the expression:

$$D_o = D_s (1 \oplus x^{-8} \oplus x^{-23}) \text{ for the GPC polynomial}$$

or

$$D_o = D_s (1 \oplus x^{-5} \oplus x^{-23}) \text{ for the GPA polynomial.}$$

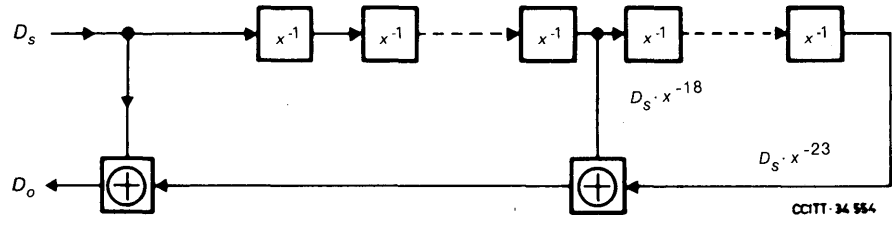


FIGURE I-3/V.26 *ter*

Descrambler with GPC polynomial

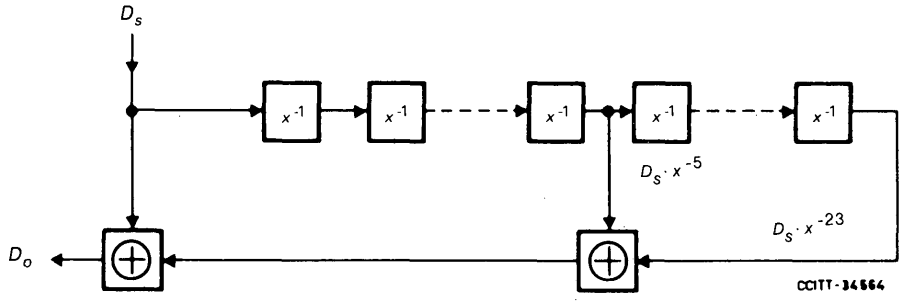


FIGURE I-4/V.26 *ter*

Descrambler with GPA polynomial

Note – The scrambler output patterns required to produce the synchronizing signal segment are as follows for both data rates:

GPC: 00 11 11 11 11 00 00 00 00 11 11 10 01 11 00 00 01 11 00
↑First bit

GPA: 00 11 11 11 11 00 00 00 00 11 11 10 01 11 00 11 11 10 00
↑First bit

Scrambler contents immediately preceding the output pattern above are as follows:

GPC: 10 01 11 11 11 11 11 11 00 00 01 1
↑

GPA: 01 10 00 00 11 10 00 00 11 10 00 0
First stage of scrambler ——————↑

4800 BITS PER SECOND MODEM WITH MANUAL EQUALIZER STANDARDIZED FOR USE ON LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1972; amended at Geneva, 1976 and 1980, Malaga-Torremolinos, 1984)

1 Introduction

This modem is intended to be used primarily on Recommendation M.1020 [1] circuits but this does not preclude the use of this modem over circuits of lower quality at the discretion of the Administration concerned.

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

The principal characteristics for this recommended modem for transmitting data at 4800 bits per second on leased circuits are as follows:

a) it is capable of operating in a full-duplex mode or half-duplex mode;

b) differential eight-phase modulation with synchronous mode of operation;

c) possibility of a backward (supervisory) channel at modulation rates up to 75 bauds in each direction of transmission, the use of these channels being optional;

d) inclusion of a manually adjustable equalizer.

2 Line signals

2.1 The carrier frequency is to be 1800 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Division of power between the forward and backward channels*

If simultaneous transmission of the forward and backward channels occurs in the same direction, a backward channel should be 6 dB lower in power level than the forward (data) channel.

2.3 The data stream to be transmitted is divided into groups of three consecutive bits (tribits). Each tribit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 1/V.27). At the receiver the tribits are decoded and the bits are reassembled in correct order. The left-hand digit of the tribit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.27

Tribit values			Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

3 Data signalling and modulation rates

The data signalling rate shall be 4800 bits per second ± 0.01%, i.e. the modulation rate is 1600 bauds ± 0.01%.

4 Received signal frequency tolerance

The carrier frequency tolerance allowance at the transmitter is ± 1 Hz and assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

5 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc. to be as recommended for backward channel in Recommendation V.23. This does not preclude the use of a higher speed backward channel with operational capability of 75 bauds or higher, bearing the same characteristic frequencies as the V.23 backward channel.

6 Interchange circuits

6.1 *List of essential interchange circuits* (see Table 2/V.27)

TABLE 2/V.27

Interchange circuit		Forward (data) channel half-duplex or full-duplex (see Note 1)	
No.	Designation	Without backward channel	With backward channel
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105 (see Note 2)	Request to send	X	X
106	Ready for sending	X	X
107	Data set ready	X	X
108/1	Connect data set to line	X	X
109	Data channel received line signal detector	X	X
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
118	Transmitted backward channel data		X
119	Received backward channel data		X
120	Transmit backward channel line signal		X
121	Backward channel ready		X
122	Backward channel received line signal detector		X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 6.6).

Note 2 – No essential for 4-wire full-duplex continuous carrier operation.

6.2 *Threshold and response times of circuit 109*

A fall in level of the incoming line signal to −31 dBm or lower for more than 10 ± 5 ms will cause circuit 109 to be turned OFF. An increase in level to −26 ± 1 dBm or higher will turn this circuit ON after a delay of:

a) 13 ± 3 ms for fast operations,

b) 100 ms to 1200 ms for slow operation,

where the choice of the delay for slow operation depends upon the application. Delays within the range of b) may be provided for 4-wire full-duplex continuous carrier operation.

6.3 *Response time for circuit 106*

The time between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106 shall be optionally 20 ± 3 ms or 50 ± 20 ms.

6.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

6.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

6.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

6.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

6.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6.6 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114 and receiver signal element timing, circuit 115. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment and be transferred to the modem via circuit 113.

8 Synchronizing signal

During the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106, synchronizing signals for properly conditioning the receiving modem must be generated by the transmitting modem. These signals are defined as:

a) signals to establish basic demodulator requirements;

b) signals to establish scrambler synchronization.

The actual composition of the synchronization signals is continuous 180 degrees phase reversals on line for 9 ± 1 ms followed by continuous 1s at the input to the transmit scrambler for b). Condition b) shall be sustained until the OFF to ON transition of circuit 106.

9 Line signal characteristics

A 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter.

10 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial:

$$1 + x^{-6} + x^{-7}$$

with additional guards against repeating patterns of 1, 2, 3, 4, 6, 9 and 12 bits, shall be included in the modem. Appendix I shows a suitable logical arrangement.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial, to generate the transmitted sequence, and at the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix I.

11 Equalizer

A manually adjustable equalizer with the capability of compensating for the amplitude and group delay distortion within the limits of Recommendation M.1020 [1] shall be provided in the receiver. The transmitter shall be able to send an equalization pattern while the receiver shall incorporate a means of indicating correct adjustment of the equalizer controls. The equalizer pattern is generated by applying continuous 1s to the input of the transmitter scrambler defined above.

12 Alternative equalization and scrambler techniques

This Recommendation does not preclude the use of alternative equalization techniques, for example manually adjustable transmit equalizers for use in multipoint polled networks and for point-to-point networks with an unattended location.

These techniques, and their incorporation in the modem, and a new scrambler, should be the subject of further study.

Note – For modems with automatic adaptive equalizers, see Recommendation V.27 *bis*.

13 The following information is provided to assist equipment manufacturers:

- the data modem should have no adjustment for send level or receive sensitivity under the control of the operator;
- no fall-back rate has been included because the convenient rate would be 3200 bit/s, not a permitted rate;
- circuit 108/2 has not been included in the list of interchange circuits because it was considered that the modem would not be suitable for switched network use until an automatic equalizer had been recommended.

APPENDIX I

(to Recommendation V.27)

Detailed scrambling and descrambling processes

I.1 *Scrambling*

The message polynomial is divided by the generating polynomial $1 + x^{-6} + x^{-7}$. (See Figure I-1/V.27.) The coefficients of the quotient of this division are taken in descending order from the data sequence to be transmitted.

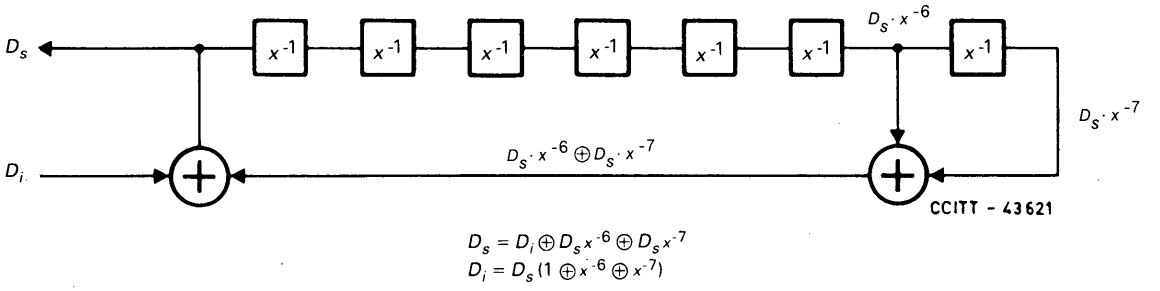
The transmitted bit sequence is continuously searched over a span of 45 bits for sequences of the form

$$p(x) = \sum_{i=0}^{32} a_i x^i$$

where

a_i = 1 or 0 and $a_i = a_{i+9}$ or a_{i+12}

If such a sequence occurs, the bit immediately following the sequence is inverted before transmission.



$D_S = D_i \oplus D_S x^{-6} \oplus D_S x^{-7}$

$D_i = D_S (1 \oplus x^{-6} \oplus x^{-7})$

FIGURE I-1/V.27

I.2 *Descrambling*

At the receiver the incoming bit sequence is continuously searched over a span of 45 bits for sequences of the form $p(x)$. If such a sequence occurs, the bit immediately following the sequence is inverted. The polynomial represented by the resultant sequence is then multiplied by the generating polynomial $1 + x^{-6} + x^{-7}$ to form the recovered message polynomial. The coefficients of the recovered polynomial, taken in descending order, form the output data sequence.

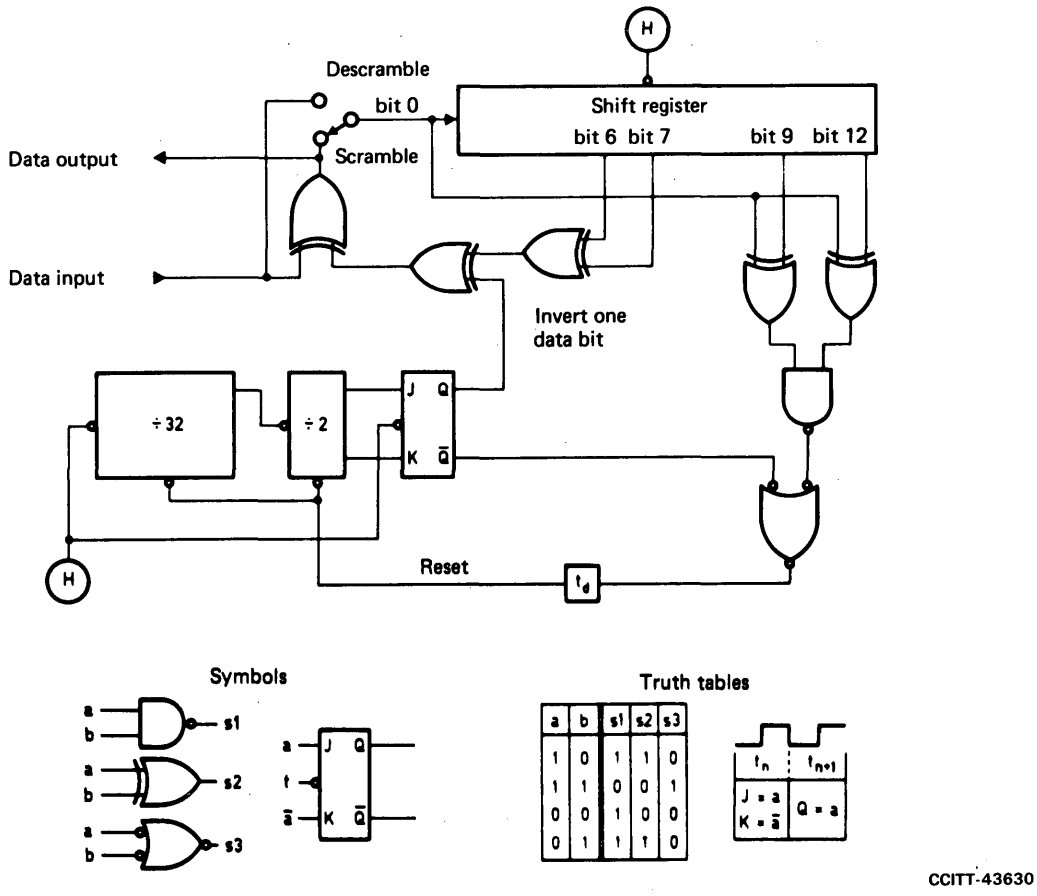
I.3 *Elements of scrambling process*

The factor $1 + x^{-6} + x^{-7}$ randomizes the transmitted data over a sequence length of 127 bits.

The equality $a_i = a_{i+9}$ in the guard polynomial $p(x)$ prevents repeated patterns of 1, 3 and 9 bits from occurring for more than 42 successive bits.

The equality $a_i = a_{i+12}$ in $p(x)$ prevents repeated patterns of 2, 4, 6 and 12 bits from occurring for more than 45 successive bits.

I.4 Figure I-2/V.27 is given as an indication only, since with another technique this logical arrangement might take another form.



Note 1 – Ⓗ represents the clock signal. The negative going transition is the active transition.

Note 2 – There is a delay time, due to physical circuits, between a negative going transition of Ⓗ and the end of the "0" state represented by t_d on the non-RESET wire; therefore the first coincidence between bit 0 and bit 9 or bit 12 is not taken into account by the counter.

Note 3 – The same voltage convention is used for data signals and logical circuits in the diagram.

FIGURE I-2/V.27

An example of scrambler and descrambler circuitry

Reference

[1] CCITT Recommendation *Characteristics of special quality international leased circuits, with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

Recommendation V.27 *bis*

4800/2400 BITS PER SECOND MODEM WITH AUTOMATIC EQUALIZER STANDARDIZED FOR USE ON LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

Introduction

This modem is intended to be used over any general leased circuits not necessarily conforming to Recommendation M.1020 [1]. A provision for a fast start-up sequence is made to allow the use of this modem for multipoint polling applications if the circuits used conform to Recommendation M.1020.

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems. This Recommendation does not eliminate the need for manually equalized modems according to Recommendation V.27 or application of other automatically equalized 4800 bits per second modems.

The provisions of this Recommendation are to be regarded as provisional in order to provide service where it is urgently required and between locations where it is expected that a reasonably satisfactory service can be given.

1 Principal characteristics

The principal characteristics for this recommended modem are very similar to the characteristics of a modem conforming to Recommendation V.27 with the exception of the equalizer used and these characteristics are as follows:

a) operates in a full-duplex or half-duplex mode over 4-wire leased circuits or in a half-duplex mode over 2-wire leased circuits;

b) at 4800 bits per second operation, modulation is 8-phase differentially encoded as described in Recommendation V.27;

c) reduced rate capability at 2400 bits per second with 4-phase differentially encoded modulation scheme as described in Recommendation V.26, Alternative A;

d) possibility of a backward (supervisory) channel at modulation rates up to 75 bauds in each direction of transmission, the provision and the use of these channels being optional;

e) inclusion of an automatic adaptive equalizer with a specific start-up sequence for Recommendation M.1020 [1] lines and an alternate start-up sequence for much lower grade lines.

2 Line signals at 4800 and 2400 bits per second operation

2.1 *Carrier frequency*

The carrier frequency is to be 1800 ± 1 Hz. No separate pilot tones are provided. The power levels used will conform to Recommendation V.2.

2.1.1 *Spectrum at 4800 bits per second*

A 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1000 Hz and 2600 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1000 Hz and 2600 Hz.

2.1.2 *Spectrum at 2400 bits per second*

A minimum of 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1200 Hz and 2400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1200 Hz and 2400 Hz.

2.2 *Division of power between the forward and backward channel*

If simultaneous transmission of the forward and backward channels occurs in the same direction, a backward channel should be 6 dB lower in power level than the forward (data) channel.

2.3 *Operation at 4800 bits per second*

2.3.1 *Data signalling and modulation rate*

The data signalling rate shall be 4800 bits per second ± 0.01%, i.e. the modulation rate is 1600 bauds ± 0.01%.

2.3.2 *Encoding data bits*

The data stream to be transmitted is divided into groups of three consecutive bits (tribits). Each tribit is encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.27 *bis*). At the receiver, the tribits are decoded and the bits are reassembled in correct order. The left-hand digit of the tribit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.27*bis*

Tribit values			Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.4 *Operation at 2400 bits per second*

2.4.1 *Data signalling and modulation rate*

The data signalling rate shall be 2400 bits per second ± 0.01%, i.e. the modulation rate is 1200 bauds ± 0.01%.

2.4.2 *Encoding data bits*

At 2400 bits per second the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 2/V.27 *bis*). At the receiver, the dibits are decoded and reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

2.5 *Operating sequences*

2.5.1 *Turn-ON sequence*

During the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106, synchronizing signals for proper conditioning of the receiving modem must be generated by the transmitting modem. These are signals to establish carrier detection, AGC if required, timing synchronization, equalizer convergence and descrambler synchronization.

TABLE 2/V.27*bis*

Dibit values	Phase change (see Note)
00	0°
01	90°
11	180°
10	270°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

Two sequences are defined, i.e.:

a) a short one for 4-wire circuits conforming to Recommendation M.1020 [1] operation,

b) a long one for 4-wire circuits which are much worse than Recommendation M.1020 [1] and for 2-wire circuits.

The sequences, for both data rates, are divided into three segments as in Table 3/V.27 *bis*.

TABLE 3/V.27*bis*

	Segment 1	Segment 2	Segment 3	Total of Segments 1, 2 and 3	
Type of line signal	Continuous 180° phase reversals	0°-180° 2-phase equalizer conditioning pattern	Continuous scrambled ONEs	Total "**Turn**-ON" sequence time	
				4800 bit/s	2400 bit/s
Number of symbol intervals (SI) [a]	a) 14 SI b) 50 SI	a) 58 SI b) 1074 SI	8 SI	a) 50 ms b) 708 ms	a) 67 ms b) 943 ms

[a] SI = symbol intervals. The durations of Segments 1, 2 and 3 are expressed in number of symbol intervals, these numbers being the same in fallback operation.

2.5.1.1 The composition of Segment 1 is continuous 180° phase reversals on line for 14 symbol intervals in the case of sequence a), for 50 symbol intervals in the case of sequence b).

2.5.1.2 Segment 2 is composed of an equalizer conditioning pattern which is derived from a pseudo-random sequence generated by the polynomial:

$$1 + x^{-6} + x^{-7}$$

2.5.1.2.1 For operation at 4800 bit/s the equalizer conditioning pattern is derived by using every third bit of the pseudo-random sequence defined in § 2.5.1.2. When the derived pattern contains a ZERO, 0° phase change is transmitted; when it contains a ONE, 180° phase change is transmitted. Segment 2 begins with 0°, 180°, 180°, 180°, 180°, 180°, 0°, ... according to the derived pattern and continues for 58 symbol intervals in the case of sequence a) and for 1074 symbol intervals in the case of sequence b). An example of the detailed sequence generation is described in Appendix I.

2.5.1.2.2 On leased circuits, considering that there exist modems which comply with § 2.5.1.2.1 at 4800 bit/s, but which differ in their "Turn-ON" sequences at 2400 bit/s, the following alternative equalizer conditioning patterns are defined:

i) In the first alternative, the equalizer conditioning pattern is identical to that defined in § 2.5.1.2.1.

ii) In the second alternative, the equalizer conditioning pattern is derived by using every second bit of the pseudo-random pattern defined in § 2.5.1.2. When the derived sequence contains a ZERO, 0° phase change is transmitted; when it contains a ONE, 180° phase change is transmitted. Segment 2 begins with 0°, 180°, 0°, 180°, 180°, 0°, 180°, ... according to the derived pattern and continues for 58 symbol intervals in the case of sequence a) and for 1074 symbol intervals in the case of sequence b).

2.5.1.3 Segment 3 commences transmission according to the encoding described in §§ 2.3 and 2.4 above with continuous data ONEs applied to the input of the data scrambler. Segment 3 is 8 symbol intervals. At the end of Segment 3, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

2.5.1.4 The phase change sequences for Segments 2 and 3 for 4800 bit/s and 2400 bit/s are shown in Table 4/V.27 *bis*.

TABLE 4/V.27 *bis* [a]

Data speed		Segment 2	Segment 3
4800 bit/s	Phase change PRS [b]	0° 180° 180° 180° 180° 180° 0° ..... 180° 180° 0° 0° 011 101 101 100 100 101 001 ..... 110 100 010 001	270° 225° 315° 90° 45° 45° 180° 180° 100 110 101 010 000 000 111 111
2400 bit/s alternative i)	Phase change PRS [b]	0° 180° 180° 180° 180° 180° 0° ..... 180° 180° 0° 0° 011 101 101 100 100 101 001 ..... 110 100 010 001	270° 90° 270° 270° 270° 270° 0° 0° 10 01 10 10 10 10 00 00
2400 bit/s alternative ii)	Phase change PRS [b]	0° 180° 0° 180° 180° 0° 180° ...180° 0° 180° 180° 180° 0° 01 11 01 10 11 00 10 ...10 00 10 10 11 00	0° 90° 90° 180° 270° 0° 180° 270° 00 01 01 11 10 00 11 10
	Duration	← 58 or 1074 symbol intervals → (Beginning and ending PRS and symbol sequences are the same for both durations)	← 8 symbol intervals →

[a] For a description of how the alternative sequences for Segments 2 and 3 may be generated, refer to the Note at the end of Appendix I.

[b] PRS is the pseudo-random sequence defined in § 2.5.1.2. The underlined bits determine the phase changes.

2.5.2 *Turn-OFF sequence*

The line signal emitted after the ON to OFF transition of circuit 105 is divided into two segments as shown in Table 5/V.27 *bis*.

TABLE 5/V.27 *bis*

	Segment A	Segment B	Total of Segments A and B
Type of line signal	Remaining data followed by continuous scrambled ONEs	No transmitted energy	Total "**Turn**-OFF" time
Duration	5 to 10 ms	20 ms	25 to 30 ms

If an OFF to ON transition of circuit 105 occurs during the Turn-OFF sequence, it will not be taken into account until the end of the Turn-OFF sequence.

In addition, in the case of half-duplex operation on two wires, if circuit 105 goes ON during the reception of the Segment A of the Turn-OFF sequence, optionally the transmission of the Turn-ON sequence shall be started within a time period of less than 20 ms after the end of reception of Segment A.

3 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance of the transmitter is ± 1 Hz and assuming a maximum drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

4 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc. to be as recommended for the backward channel in Recommendation V.23. This does not preclude the use of a higher speed backward channel with operational capability of 75 bauds or higher, bearing the same characteristic frequencies as the V.23 backward channel.

5 Interchange circuits

5.1 *List of essential interchange circuits* (Table 6/V.27 *bis*)

TABLE 6/V.27 *bis*

Interchange circuit		Forward (data) channel half-duplex or full-duplex (see Note)	
No.	Designation	Without backward channel	With backward channel
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105	Request to send	X	X
106	Ready for sending	X	X
107	Data set ready	X	X
108/1	Connect data set to line	X	X
109	Data channel received line signal detector	X	X
111	Data signal rate selector (DTE source)	X	X
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
118	Transmitted backward channel data		X
119	Received backward channel data		X
120	Transmit backward channel line signal		X
121	Backward channel ready		X
122	Backward channel received line signal detector		X

Note – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 6).

5.2 *Response times of circuits 106, 109, 121 and 122* (Table 7/V.27 *bis*)

TABLE 7/V.27*bis*

Response times

Circuit 106	4800 bits per second	2400 bits per second
OFF to ON	a) 50 ms b) 708 ms	a) 67 ms b) 944 ms
ON to OFF	⩽ 2 ms	
Circuit 109		
OFF to ON	See § 5.2.1	
ON to OFF	5 to 15 ms	
Circuit 121		
OFF to ON	80 to 160 ms	
ON to OFF	⩽ 2 ms	
Circuit 122		
OFF to ON	< 80 ms	
ON to OFF	15 to 80 ms	

Note – a) and b) refer to sequence a) and sequence b) as defined in § 2.5.1.

5.2.1 *Circuit 109*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104.

5.2.2 *Circuit 106*

Circuit 106 response times are from the connection of an ON or OFF condition on circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106.

5.3 *Threshold of data channel and backward channel received line signal detectors*

Levels of received line signal at receiver line terminals:

– *For use over ordinary quality leased circuits* (ref. Recommendation M.1040 [2])
  Threshold for circuits 109/122:
  – greater than −43 dBm: OFF to ON
  – less than −48 dBm: ON to OFF
– *For use over special quality leased circuits* (ref. Recommendation M.1020 [1])
  Threshold for circuit 109:
  – greater than −26 dBm: OFF to ON
  – less than −31 dBm: ON to OFF
  Threshold for circuit 122:
  – greater than −34 dBm: OFF to ON
  – less than −39 dBm: ON to OFF

The condition of circuits 109 and 122 for levels between the above levels is not specified except that the signal detectors shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

5.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

5.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

5.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangement

Clocks should be included in the modem to provide the data terminal equipment with transmitter element timing, circuit 114 and receiver signal element timing, circuit 115. The transmitter element timing may be originated in the data terminal equipment and be transferred to the modem via circuit 113.

8 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial:

$$1 + x^{-6} + x^{-7}$$

with additional guards against repeating patterns of 1, 2, 3, 4, 6, 8, 9 and 12 bits, shall be included in this modem. In Appendix I, Figure I-2/V.27 *bis* shows a suitable logical arrangement (see Note). The scrambler/descrambler is the same as that in Recommendation V.27 with the addition of circuitry to guard against repeating patterns of 8 bits.

Note – Figures I-1/V.27 *bis* and I-2/V.27 *bis* in Appendix I are given as an indication only, since with another technique these logical arrangements might take another form.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence, and at the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

9 Equalizer

An automatic adaptive equalizer shall be provided in the receiver. The receiver shall incorporate a means of detecting loss of equalization and be able to recover equalization from the normal data-modulated received line signal without initiating a new synchronizing signal from the distant transmitter.

10 Options

Since this modem is equipped with an automatic adaptive equalizer, and can operate on 2-wire lines, operation over the general switched network is possible. Thus, in the event of failure of the leased line, the general switched network may serve as a stand-by facility.

Options can be added to this modem in order to allow the use of the general switched network when the leased line fails. These options can also be added for use on 2-wire leased lines where echo protection is required.

Additional information for these options can be found in Recommendation V.27 *ter.*

11 The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

At 4800 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1100 Hz to 2500 Hz.

At 2400 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1300 Hz to 2300 Hz.

APPENDIX I

(to Recommendation V.27 *bis*)

A two phase equalizer training generator for 4800 bit/s

Rapid convergence for the equalizer with the least amount of circuitry is more readily accomplished by sending only an in-phase or out-of-phase carrier during training. This implies that the only tribits sent to the modulator will be 001 (0° phase) or 111 (180° phase). Refer to Figure I-1/V.27 *bis* for circuitry to generate the sequence and Figure I-3/V.27 *bis* for timing the sequence.

Let T1 be a timing signal equal to 1600 Hz (symbol clock), that is true (high) for one 4800-Hz period, and low for two 4800-Hz clock periods. T2 is the inversion of T1.

During T1 select the input to the scrambler, during T2 select the first stage of the scrambler. During the period when T2 is high, C forces the output high. This may be accomplished by circuitry shown in Figure I-2/V.27 *bis.*

If T1 is forced continually high and T2 is forced continually low, normal operation is restored.

In order to ensure consistent training, the same pattern should always be sent. To accomplish this, the data input to the scrambler should be in mark hold during the training, and the first seven stages of the scrambler should be loaded with 0011110 (right-hand-most first in time) on the first coincidence on T1 and the signal that will cause the mute should be removed from the transmitter output. [Generally this signal will be *Request To Send* (RTS)].

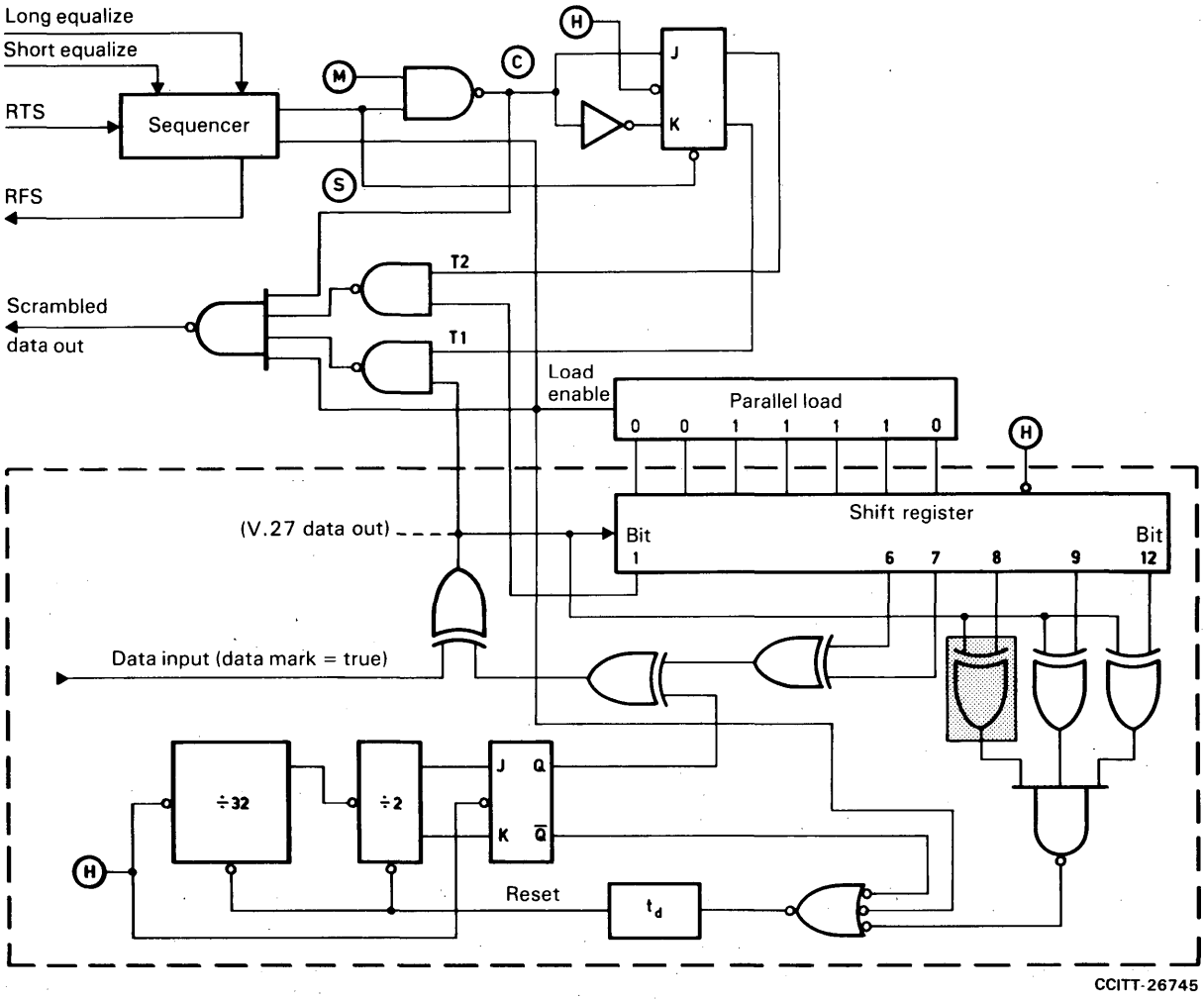
This particular starting point was chosen in order to ensure a pattern that has continuous 180° phase reversals at the beginning in order to ensure rapid clock acquisition, followed by a pattern that will ensure rapid equalizer convergence.

Within eight symbol intervals prior to the ON condition of *Ready For Sending* (RFS), the scrambler should be switched to normal operation, keeping the scrambler in mark hold until RFS, to synchronize the descrambler.

Note – At 2400 bits per second, a similar technique may be used with appropriate clocking changes, as shown in Table I-1/V.27 *bis.*

TABLE I-1/V.27*bis*

		Segment 2	Segment 3
Clock (H)	i)	3600 Hz	2400 Hz
	ii)	2400 Hz	2400 Hz
Clock (M)	i)	1200 Hz	1200 Hz
	ii)	1200 Hz	1200 Hz



Note 1 – The dotted line encloses the V.27 scrambler.

Note 2 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 3 – (H) is 3 times baud rate clock.

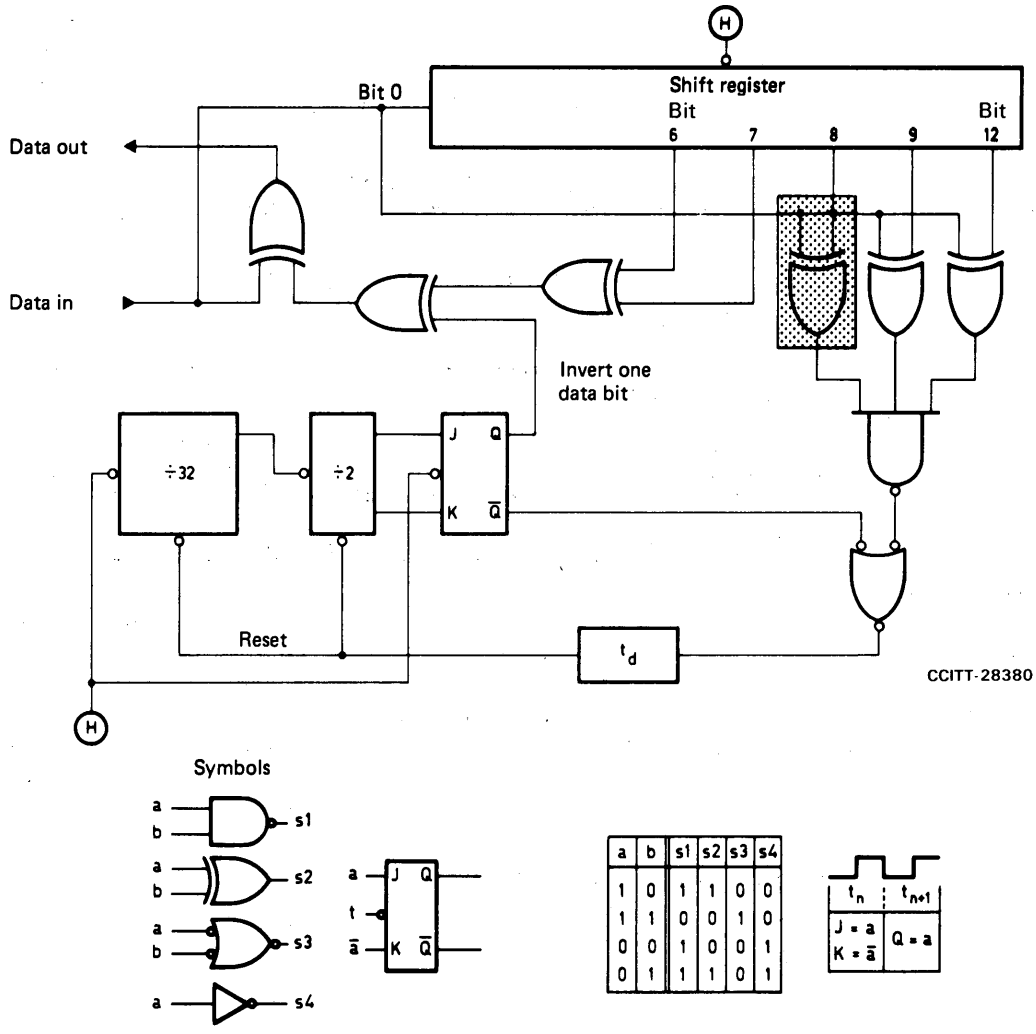
Note 4 – (M) is baud rate clock (1600 Hz).

Note 5 – Diagrams shown with positive logic.

Note 6 – Signals (C) and (S) are identified only to correlate with Figure I-3/V.27*bis*.

FIGURE I-1/V.27*bis*

An example of sequence generator and scrambler circuitry for 4800 bit/s



Note 1 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 2 – (H) represents clock signal. The negative going transition is the active transition.

Note 3 – There is a delay time due to physical circuits between a negative going transition of (H) and the end of the "0" state represented by t_d on the non-reset wire; therefore the first coincidence between bit 0 and bit 8 or bit 9 or bit 12 is not taken into account by the counter.

FIGURE I-2/V.27 *bis*

An example of descrambler circuitry

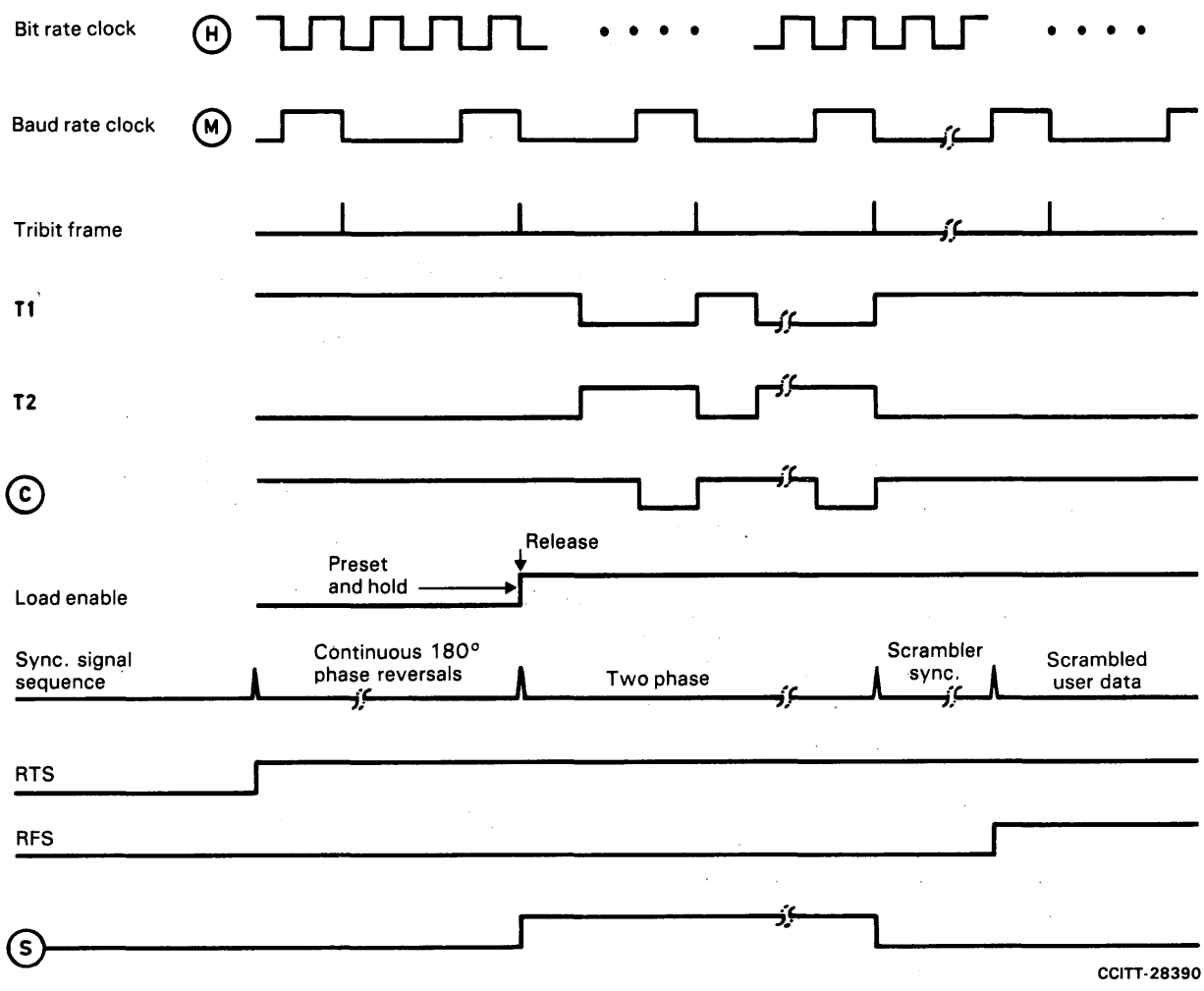


FIGURE I-3/V.27 *bis*

Synchronizing signal sequence for 4800 bit/s (see Figure I-1/V.27 *bis*)

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of ordinary quality international leased circuits*, Vol. IV, Rec. M.1040.

4800/2400 BITS PER SECOND MODEM STANDARDIZED FOR USE IN THE GENERAL SWITCHED TELEPHONE NETWORK

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that there is a demand for data transmission at 4800 bits per second over the general switched telephone network;

(b) that a majority of connections over the general switched telephone network within some countries are capable of carrying data at 4800 bits per second;

(c) that a lower proportion of international connections in the general switched telephone network are capable of carrying data at 4800 bits per second;

(d) that other international connections in the general switched telephone network may still support operations at 2400 bits per second using a built-in fallback capability;

unanimously declares the view

that transmission at 4800 bits per second should be allowed on the general switched telephone network. Reliable transmission cannot be guaranteed on every connection or routing and tests should be made between the most probable terminal points before a service is provided. The CCITT expects that developments during the next few years in modern technology will bring about modems of more advanced design enabling reliable transmission to be given on a much higher proportion of connections. The provisions of this Recommendation are to be regarded as provisional in order to provide service where it is urgently required and between locations where it is expected that a reasonably satisfactory service can be given;

that the characteristics of the modem for transmission at 4800 bits per second over the general switched telephone network shall provisionally be the following:

1 Principal characteristics

a) Use of data signalling rate of 4800 bits per second with 8-phase differentially encoded modulation as described in Recommendation V.27.

b) Reduced rate capability at 2400 bits per second with 4-phase differentially encoded modulation as described in Recommendation V.26, Alternative A.

c) Provision for a backward channel at modulation rates up to 75 bauds, use of this channel being optional.

d) Inclusion of an automatic adaptive equalizer.

2 Line signals at 4800 and 2400 bits per second operation

2.1 *Carrier frequency*

The carrier frequency is to be 1800 ± 1 Hz. No separate pilot tones are provided. The power levels used will conform to Recommendation V.2.

2.1.1 *Spectrum at 4800 bits per second*

The 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1000 Hz and 2600 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1000 Hz and 2600 Hz.

2.1.2 *Spectrum at 2400 bits per second*

A minimum of 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1200 Hz and 2400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1200 Hz and 2400 Hz.

2.2 *Division of power between the forward and backward channel*

Equal division between the forward and backward channels is recommended (if provided).

2.3 *Operation at 4800 bits per second*

2.3.1 *Data signalling and modulation rate*

The data signalling rate shall be 4800 bits per second ± 0.01%, i.e. the modulation rate is 1600 bauds ± 0.01%.

2.3.2 *Encoding data bits*

The data stream to be transmitted is divided into groups of three consecutive bits (tribits). Each tribit is encoded as a phase change relative to the phase of the preceding signal element (see Table 1/V.27 *ter*). At the receiver, the tribits are decoded and the bits are reassembled in correct order. The left-hand digit of the tribit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 1/V.27 *ter*

Tribit values			Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.4 *Operation at 2400 bits per second*

2.4.1 *Data signalling and modulation rate*

The data signalling rate shall be 2400 bits per second ± 0.01% i.e. the modulation rate is 1200 bauds ± 0.01%.

2.4.2 *Encoding data bits*

At 2400 bits per second the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 2/V.27 *ter*). At the receiver, the dibits are decoded and the bits are reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

TABLE 2/V.27 *ter*

Dibit values	Phase change (see Note)
00	0°
01	90°
11	180°
10	270°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

2.5 *Operating sequences*

2.5.1 *Turn-ON sequence*

During the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106, synchronizing signals for proper conditioning of the receiving modem must be generated by the transmitting modem. These are signals to establish carrier detect, AGC if required, timing synchronization, equalizer convergence and descrambler synchronization.

The synchronizing signals are defined in two separate sequences with the long sequence used once at the beginning of the established connection and the short sequence used for subsequent turn-around in which the equalizer training pattern is used to update and refine equalizer convergence.

Two sequences are defined, i.e.:

a) a short one for turn-around operation,

b) a longer one for initial establishment of connection.

The sequence b) is only used after the first OFF to ON transition of circuit 105 following the OFF to ON transition of circuit 107, or at the OFF to ON transition of circuit 107 if the circuit 105 is already ON. After every subsequent OFF to ON transition of circuit 105, the sequence a) is used.

The sequences, for both data rates, are divided into five segments as in Table 3/V.27 *ter*.

2.5.1.1 The composition of Segment 3 is continuous 180° phase reversals on line for 14 symbol intervals in the case of sequence a), for 50 symbol intervals in the case of sequence b).

2.5.1.2 Segment 4 is composed of an equalizer conditioning pattern which is derived from a pseudo-random sequence generated by the polynomial:

$$1 + x^{-6} + x^{-7}$$

For operation at both 4800 bit/s and 2400 bit/s, the equalizer conditioning pattern is derived by using every third bit of the pseudo-random sequence defined by the polynomial. When the derived pattern contains a ZERO, 0° phase change is transmitted; when it contains a ONE, 180° phase change is transmitted. Segment 4 begins with 0°, 180°, 180°, 180°, 180°, 180°, 0°, ... according to the derived pattern and continues for 58 symbol intervals in the case of sequence a) and for 1074 symbol intervals in the case of sequence b). An example of the detailed sequence generation is described in Appendix I.

2.5.1.3 Segment 5 commences transmission according to the encoding described in §§ 2.3 and 2.4 above with continuous data ONEs applied to the input of the data scrambler. Segment 5 is 8 symbol intervals. At the end of Segment 5, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

2.5.1.4 The phase change sequences for Segments 4 and 5 for 4800 bit/s and 2400 bit/s are shown in Table 4/V.27 *ter*.

TABLE 3/V.27 *ter*

	Segment 1	Segment 2	Segment 3	Segment 4	Segment 5	Total of Segments 1, 2, 3, 4 and 5	
Type of line signal	Unmodulated carrier	No transmitted energy	Continuous 180° phase reversals	0° - 180° 2-phase equalizer conditioning pattern	Continuous scrambled ONEs	Nominal total "**Turn**-ON" sequence time	
						4800 bit/s	2400 bit/s
Protection against talker echo	185 ms to 200 ms	20 ms to 25 ms	a) 14 SI b) 50 SI	a) 58 SI b) 1074 SI	8 SI	a) 265 ms b) 923 ms	a) 281 ms b) 1158 ms
Without any protection	0 ms	0 ms	a) 14 SI b) 50 SI	a) 58 SI b) 1074 SI	8 SI	a) 50 ms b) 708 ms	a) 66 ms b) 943 ms

SI = symbol intervals. The durations of Segments 3, 4 and 5 are expressed in number of symbol intervals, these numbers being the same in the fallback operation.

TABLE 4/V.27 *ter* [a]

Data speed		Segment 4	Segment 5
4800 bit/s	Phase change PRS[b]	0° 180° 180° 180° 180° 180° 0° ..... 180° 180° 0° 0° 011 101 101 100 100 101 001 ..... 110 100 010 001	270° 225° 315° 90° 45° 45° 180° 180° 100 110 101 010 000 000 111 111
2400 bit/s	Phase change PRS[b]	0° 180° 180° 180° 180° 180° 0° ..... 180° 180° 0° 0° 011 101 101 100 100 101 001 ..... 110 100 010 001	270° 90° 270° 270° 270° 270° 0° 0° 10 01 10 10 10 10 00 00
	Duration	← 58 or 1074 symbol intervals → (Beginning and ending PRS and symbol sequences are the same for both lengths.)	← 8 symbol intervals →

[a] For a description of how the alternative sequences for Segments 4 and 5 may be generated, refer to the Note at the end of Appendix I.

[b] PRS is the pseudo-random sequence defined in § 2.5.1.2. The underlined bits determine the phase changes.

2.5.2 *Turn-OFF sequence*

The line signal emitted after the ON to OFF transition of circuit 105 is divided into two segments as in Table 5/V.27 *ter.*

TABLE 5/V.27 *ter*

	Segment A	Segment B	Total **Turn**-OFF time
Type of line signals	Remaining data followed by continuous scrambled ONEs	No transmitted energy	Total of Segments A and B
With or without protection against talker echo	5 to 10 ms	20 ms	25 to 30 ms

If an OFF to ON transition of circuit 105 occurs during the Turn-OFF sequence, it will not be taken into account until the end of the Turn-OFF sequence.

In addition, if circuit 105 goes ON during the reception of the Segment A of the Turn-OFF sequence, optionally the transmission of the Turn-ON sequence shall be started within a time period of less than 20 ms after the end of reception of Segment A.

3 Received signal frequency tolerance

Noting that the carrier frequency tolerance allowance of the transmitter is ± 1 Hz and assuming a maximum drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

4 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc. to be as recommended for backward channel in Recommendation V.23. This does not preclude the use of a higher speed backward channel with operational capability of 75 bauds or higher, bearing the same characteristic frequencies as the V.23 backward channel.

5 Interchange circuits

5.1 *List of interchange circuits*

Interchange circuits essential for the modem when used on the general switched telephone network, including terminals equipped for manual calling or automatic calling or answering are as in Table 6/V.27 *ter.*

5.2 *Response times of circuits 106, 109, 121 and 122* (see Tables 7/V.27 *ter* and 8/V.27 *ter*)

5.2.1 *Circuit 109*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104. Circuit 109 is prevented from turning ON during reception of unmodulated carrier when the optional protection against talker echo is used.

5.2.2 *Circuit 106*

Circuit 106 response times are from the connection of an ON or OFF condition on:

- circuit 105 to the appearance of the corresponding ON or OFF condition on circuit 106; or,
- circuit 107 (where circuit 105 is already ON) to the appearance of the corresponding ON or OFF condition on circuit 106.

5.3 *Threshold of data channel and backward channel received line signal detectors*

Level of received line signal at the receive line terminals of the modem for all types of connections, i.e. the general switched telephone network or non-switched 2-wire leased telephone circuits:

- greater than −43 dBm: circuits 109/122 ON
- less than −48 dBm: circuits 109/122 OFF

The condition of circuits 109 and 122 for levels between −43 dBm and −48 dBm is not specified except that the signal detectors shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

Where transmission conditions are known and allowed, it may be desirable at the time of modem installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

TABLE 6/V.27 *ter*

Interchange circuit		Forward (data) channel one-way system (see Note 1)				Forward (data) channel either-way system (see Note 1)	
		Without backward channel		With backward channel			
No.	Designation	Transmit end	Receive end	Transmit end	Receive end	Without backward channel	With backward channel
102	Signal ground or common return	X	X	X	X	X	X
103	Transmitted data	X		X		X	X
104	Received data		X		X	X	X
105	Request to send	X		X		X	X
106	Ready for sending	X		X		X	X
107	Data set ready	X	X	X	X	X	X
108/1 or 108/2 (see Note 2)	Connect data set to line / Data terminal ready	X	X	X	X	X	X
109	Data channel received line signal detector		X		X	X	X
111	Data signalling rate selector (DTE source)	X	X	X	X	X	X
113	Transmitter signal element timing (DTE source)	X		X		X	X
114	Transmitter signal element timing (DCE source)	X		X		X	X
115	Receiver signal element timing (DCE source)		X		X	X	X
118	Transmitted backward channel data				X		X
119	Received backward channel data			X			X
120	Transmit backward channel line signal						X
121	Backward channel ready				X		X
122	Backward channel received line signal detector			X			X
125	Calling indicator	X	X	X	X	X	X

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 6).

Note 2 – This circuit shall be capable of operation as circuit 108/1 – *connect data set to line* or circuit 108/2 – *data terminal ready* depending on its use.

TABLE 7/V.27*ter*

Response times for operation at 4800 bits per second		
Circuit 106	With protection against talker echo	Without protection against talker echo
OFF to ON	a) 215 ± 10 ms + 50 ms b) 215 ± 10 ms + 708 ms	a) 50 ms b) 708 ms
ON to OFF	⩽ 2 ms	⩽ 2 ms
Circuit 109		
OFF to ON	See § 5.2.1	See § 5.2.1
ON to OFF	5 to 15 ms	5 to 15 ms
Circuit 121		
OFF to ON	80 to 160 ms	80 to 160 ms
ON to OFF	⩽ 2 ms	⩽ 2 ms
Circuit 122		
OFF to ON	< 80 ms	< 80 ms
ON to OFF	15 to 80 ms	15 to 80 ms

TABLE 8/V.27*ter*

Response times for operation of 2400 bits per second		
Circuit 106	With protection against talker echo	Without protection against talker echo
OFF to ON	a) 215 ± 10 ms + 67 ms b) 215 ± 10 ms + 944 ms	a) 67 ms b) 944 ms
ON to OFF	⩽ 2 ms	⩽ 2 ms
Circuit 109		
OFF to ON	See § 5.2.1	See § 5.2.1
ON to OFF	5 to 15 ms	5 to 15 ms

Note 1 – a) and b) refer to sequence a) and sequence b) as defined to § 2.5.1.

Note 2 – The parameters and procedures, particularly in the case of automatic calling and answering, are provisional and are the subject of further study.

5.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line, shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

5.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

5.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangement

Clocks should be included in the modem to provide the data terminal equipment with transmitter element timing, circuit 114 and receiver signal element timing, circuit 115. The transmitter element timing may be originated in the data terminal equipment and be transferred to the modem via circuit 113.

8 Equalizer

An automatic adaptive equalizer shall be provided in the receiver.

9 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial:

$$1 + x^{-6} + x^{-7}$$

with additional guards against repeating patterns of 1, 2, 3, 4, 6, 8, 9 and 12 bits, shall be included in this modem. Figure I-2/V.27 *ter* shows a suitable logical arrangement (see Note). The scrambler/descrambler is the same as that in Recommendation V.27 with the addition of circuitry to guard against repeating patterns of 8 bits.

Note – Figures I-1/V.27 *ter* and I-2/V.27 *ter* are given as an indication only, since with another technique these logical arrangements might take another form.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence, and at the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

10 When echo control device disabling is required, it is recommended that procedures specified in Recommendation V.25 be followed.

11 The following information is provided to assist equipment manufacturers:

The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.

At 4800 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1100 Hz to 2500 Hz.

At 2400 bits per second operation, the transmitter energy spectrum shall be shaped in such a way that when continuous data ONEs are applied to the input of the scrambler, the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 1300 Hz to 2300 Hz.

APPENDIX I

(to Recommendation V.27 *ter*)

A two-phase equalizer training generator for 4800 bit/s

Rapid convergence for the equalizer with the least amount of circuitry is more readily accomplished by sending only an in-phase or out-of-phase carrier during training. This implies that the only tribits sent to the modulator will be 001 (0° phase) or 111 (180° phase). Refer to Figure I-1/V.27 *ter* for circuitry to generate the sequence and Figure I-3/V.27 *ter* for timing the sequence.

Let T1 be a timing signal equal to 1600 Hz (symbol clock), that is true (high) for one 4800-Hz period, and low for two 4800-Hz clock periods. T2 is the inversion of T1.

During T1, select the input to the scrambler, during T2 select the first stage of the scrambler. During the period when T2 is high, C forces the output high. This may be accomplished by circuitry shown in Figure I-2/V.27 *ter*.

If T1 is forced continually high and T2 is forced continually low, normal operation is restored.

In order to ensure consistent training, the same pattern should always be sent. To accomplish this, the data input to the scrambler should be in mark hold during the training, and the first seven stages of the scrambler should be loaded with 0011110 (right-hand-most first in time) on the first coincidence on T1 and the signal that will cause the mute should be removed from the transmitter output. [Generally this signal will be *Request To Send* (RTS).]

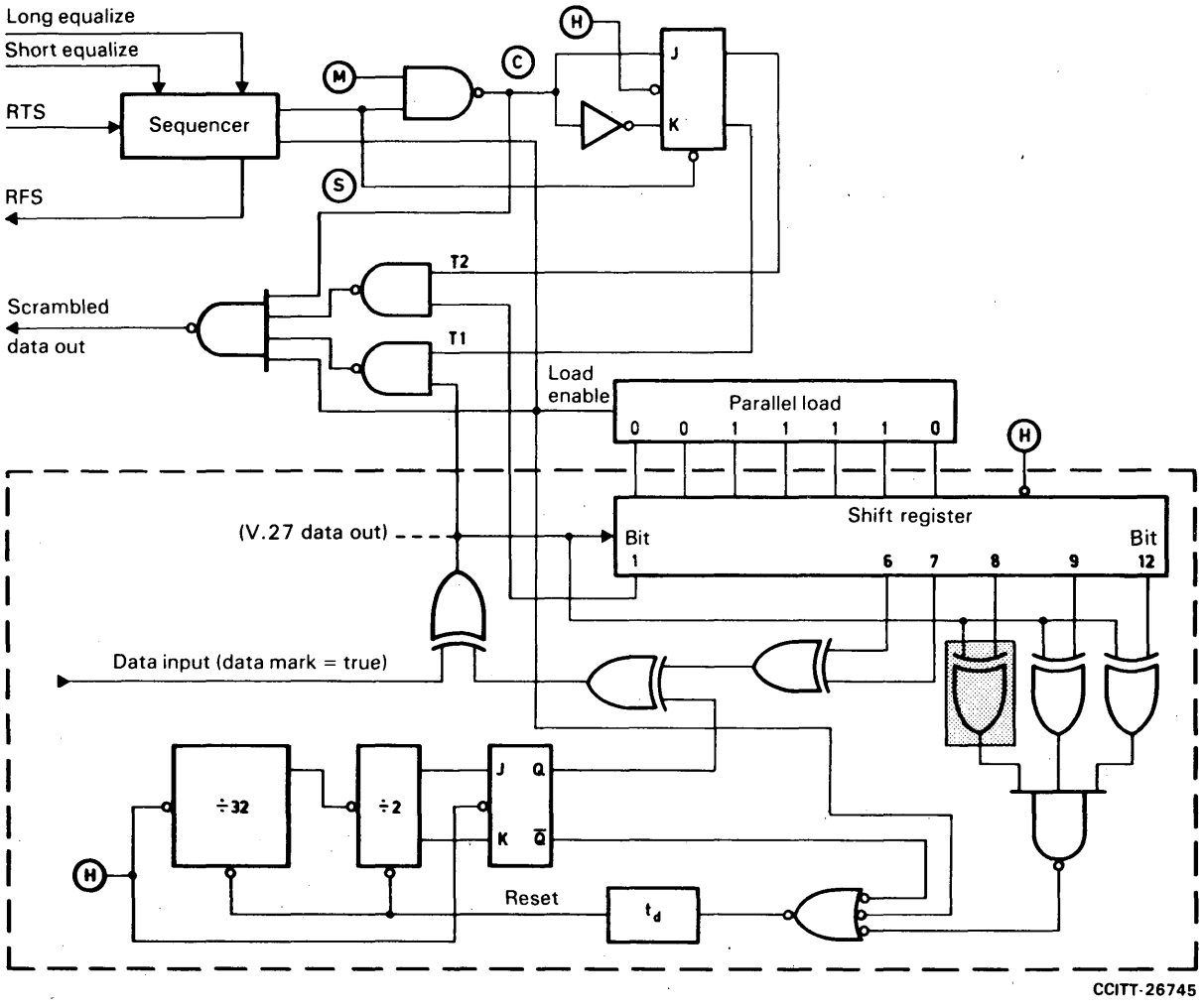
This particular starting point was chosen in order to ensure a pattern that has continuous 180° phase reversals at the beginning in order to ensure rapid clock acquisition, followed by a pattern that will ensure rapid equalizer convergence.

Within eight symbol intervals prior to the ON condition of *Ready For Sending* (RFS), the scrambler should be switched to normal operation, keeping the scrambler in mark hold until RFS to synchronize the descrambler.

Note – At 2400 bits per second, a similar technique may be used with appropriate clocking changes, as shown in Table I-1/V.27 *ter*.

TABLE I-1/V.27 *ter*

	Segment 4	Segment 5
Clock (H)	3600 Hz	2400 Hz
Clock (M)	1200 Hz	1200 Hz



Note 1 – The dotted line encloses the V.27 scrambler.

Note 2 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 3 – (H) is 3 times baud rate clock.

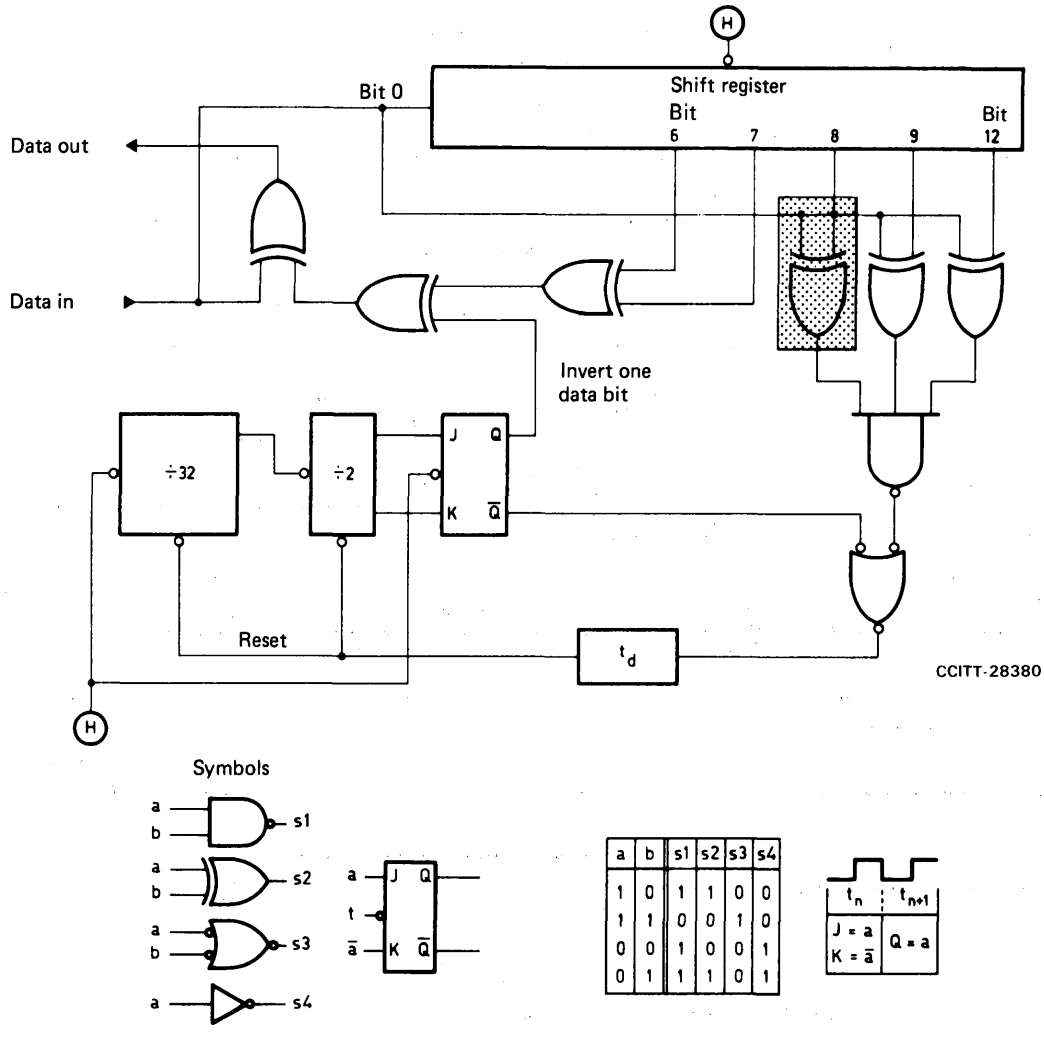
Note 4 – (M) is baud rate clock (1600 Hz).

Note 5 – Diagrams shown with positive logic.

Note 6 – Signals (C) and (S) are identified only to correlate with Figure I-3/V.27 *ter*.

FIGURE I-1/V.27 *ter*

An example of sequence generator and scrambler circuitry for 4800 bit/s



Note 1 – Shaded rectangle is for guarding against 8-bit repeating pattern.

Note 2 – (H) represents clock signal. The negative going transition is the active transition.

Note 3 – There is a delay time due to physical circuits between a negative going transition of a (H) and the end of the "0" state represented by t_d on the non-reset wire; therefore the first coincidence between bit 0 and bit 8 or bit 9 or bit 12 is not taken into account by the counter.

FIGURE I-2/V.27 *ter*

An example of descrambler circuitry

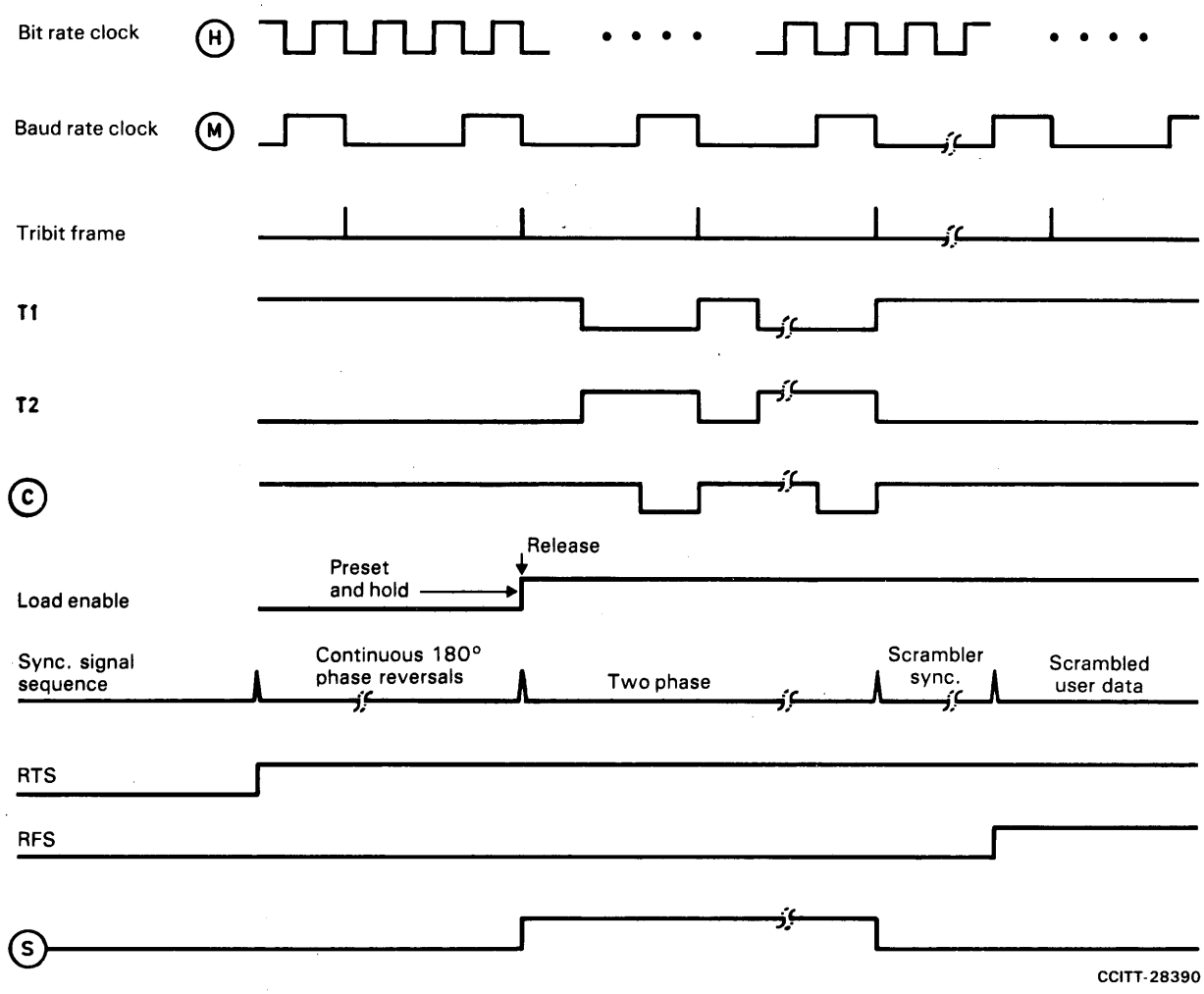


FIGURE I-3/V.27 *ter*

Synchronizing signal sequence for 4800 bit/s (see Figure I-1/V.27 *ter*)

ELECTRICAL CHARACTERISTICS FOR UNBALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS

(Geneva, 1972; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

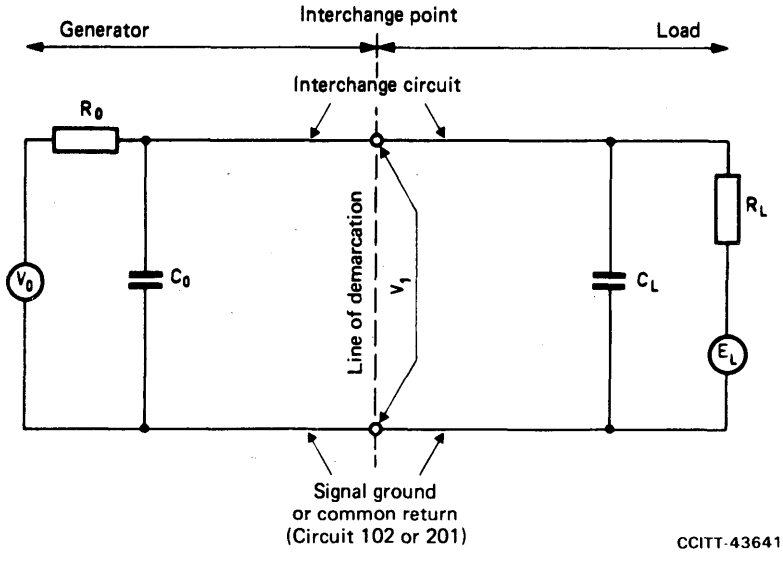
1 Scope

The electrical characteristics specified in this Recommendation apply generally to interchange circuits operating with data signalling rates below the limit of 20 000 bits per second.

2 Interchange equivalent circuit

Figure 1/V.28 shows the interchange equivalent circuit with the electrical parameters, which are defined below.

This equivalent circuit is independent of whether the generator is located in the data circuit-terminating equipment and the load in the data terminal equipment or vice versa.



V_0 is the open-circuit generator voltage.
R_0 is the total effective d.c. resistance associated with the generator, measured at the interchange point.
C_0 is the total effective capacitance associated with the generator, measured at the interchange point.
V_1 is the voltage at the interchange point with respect to signal ground or common return.
C_L is the total effective capacitance associated with the load, measured at the interchange point.
R_L is the total effective d.c. resistance associated with the load, measured at the interchange point.
E_L is the open-circuit load voltage (bias).

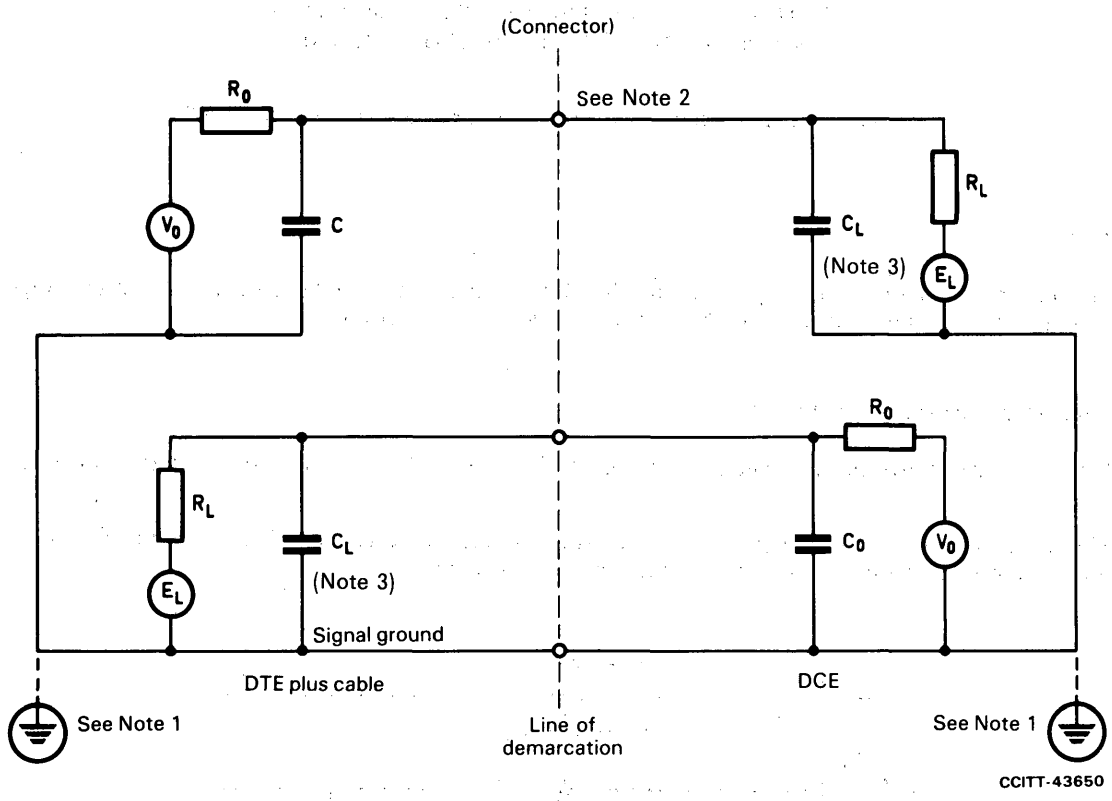
FIGURE 1/V.28

Interchange equivalent circuit

The impedance associated with the generator (load) includes any cable impedance on the generator (load) side of the interchange point.

The equipment at both sides of the interface may implement generators as well as receivers in any combination.

For data transmission applications, it is commonly accepted that the interface cabling is provided by the DTE. This introduces the line of demarcation between the DTE plus cable and the DCE. This line is also called the interchange point and is physically implemented in the form of a connector. The applications also require interchange circuits in both directions. This leads to an illustration as shown in Figure 2/V.28.



Note 1 – Signal ground may be further connected to external protective ground if national regulations require.

Note 2 – For data transmission over telephone-type facilities, ISO has specified a 25-pin connector and pin assignments in accordance with ISO 2110.

Note 3 – Many existing interchange circuit generators do not provide for meeting the maximum rise time requirement of Recommendation V.28, § 6 when driving a capacitance of greater than 2500 pF, the maximum permitted load capacitance (C_L), which includes the capacitance of the DTE supplied interface cable.

FIGURE 2/V.28

Practical representation of the interface

3 Load

The test conditions for measuring the load impedance are shown in Figure 3/V.28.

The impedance on the load side of an interchange circuit shall have a d.c. resistance (R_L) neither less than 3000 ohms nor more than 7000 ohms. With an applied voltage (E_m), 3 to 15 volts in magnitude, the measured input current (I) shall be within the following limits:

$$I_{\text{min., max.}} = \left| \frac{E_m \pm E_{L\,\text{max.}}}{R_{L\,\text{max., min.}}} \right|$$

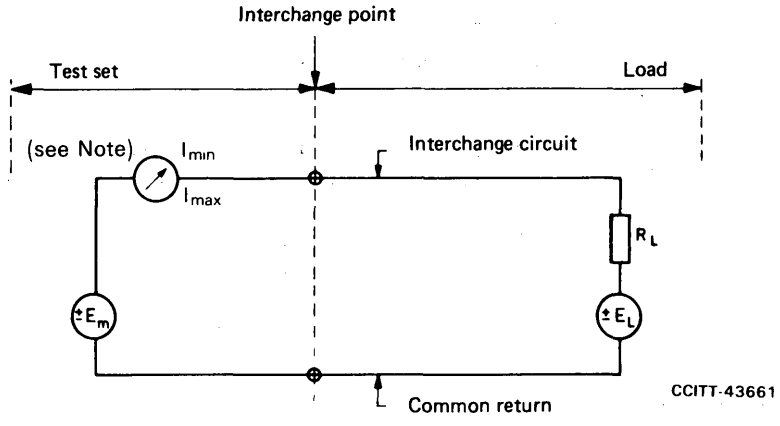
The open-circuit load voltage (E_L) shall not exceed 2 volts.

The effective shunt capacitance (C_L) of the load, measured at the interchange point, shall not exceed 2500 picofarads.

To avoid inducing voltage surges on interchange circuits the reactive component of the load impedance shall not be inductive.

Note – This is subject to further study.

The load on an interchange circuit shall not prejudice continuous operation with any input signals within the voltage limits specified in § 4. below.



Note – The internal resistance of the ammeter shall be much less than the load resistance (R_L).

FIGURE 3/V.28

Equivalent test circuit

4 Generator

The generator on an interchange circuit shall withstand an open circuit and a short circuit between itself and any other interchange circuit (including generators and loads) without sustaining damage to itself or its associated equipment.

The open circuit generator voltage (V_0) on any interchange circuit shall not exceed 25 volts in magnitude. The impedance (R_0 and C_0) on the generator side of an interchange circuit is not specified; however, the combination of V_0 and R_0 shall be selected so that a short circuit between any two interchange circuits shall not result in any case in a current in excess of one-half ampere.

Additionally, when the load open-circuit voltage (E_L) is zero, the voltage (V_1) at the interchange point shall not be less than 5 volts and not more than 15 volts in magnitude (either positive or negative polarity), for any load resistance (R_L) in the range between 3000 ohms and 7000 ohms.

The effective shunt capacitance (C_0) at the generator side of an interchange circuit is not specified. However, in addition to any load resistance (R_L) the generator shall be capable of driving all of the capacitance at the generator side (C_0), plus a load capacitance (C_L) of 2500 picofarads.

Note – Relay or switch contacts may be used to generate signals on an interchange circuit, with appropriate measures to ensure that signals so generated comply with the applicable clauses of § 6 below.

5 Significant levels (V_1)

For data interchange circuits, the signal shall be considered in the binary 1 condition when the voltage (V_1) on the interchange circuit measured at the interchange point is more negative than minus 3 volts. The signal shall be considered in the binary 0 condition when the voltage (V_1) is more positive than plus 3 volts.

For control and timing interchange circuits, the circuit shall be considered ON when the voltage (V_1) on the interchange circuit is more positive than plus 3 volts, and shall be considered OFF when the voltage (V_1) is more negative than minus 3 volts (see Table 1/V.28).

Note – In certain countries, in the case of direct connection to d.c. telegraph-type circuits only, the voltage polarities in Table 1/V.28 may be reversed.

The region between plus 3 volts and minus 3 volts is defined as the transition region. For an exception to this, see § 7 below.

TABLE 1/V.28

Correlation table

$V_i < -3$ volts	$V_i > +3$ volts
1	0
OFF	ON

6 Signal characteristics

The following limitations to the characteristics of signals transmitted across the interchange point, exclusive of external interference, shall be met at the interchange point when the interchange circuit is loaded with any receiving circuit which meets the characteristics specified in § 3 above.

These limitations apply to all (data, control and timing) interchange signals unless otherwise specified.

1) All interchange signals entering into the transition region shall proceed through this region to the opposite signal state and shall not re-enter this region until the next significant change of signal condition, except as indicated in 6) below.
2) There shall be no reversal of the direction of voltage change while the signal is in the transition region, except as indicated in 6) below.
3) For control interchange circuits, the time required for the signal to pass through the transition region during a change in state shall not exceed one millisecond.
4) For data and timing interchange circuits, the time required for the signal to pass through the transition region during a change in state shall not exceed 1 millisecond or 3 per cent of the nominal element period on the interchange circuit, whichever is the less.
5) To reduce crosstalk between interchange circuits the maximum instantaneous rate of voltage change will be limited. A provisional limit will be 30 volts per microsecond.
6) When electromechanical devices are used on interchange circuits, points 1) and 2) above do not apply to data interchange circuits.

7 Detection of generator power-off or circuit failure

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator power-off condition;
2) receiver not interconnected with a generator;
3) open-circuited interconnecting cable;
4) short-circuited interconnecting cable.

The power-off impedance of the generator side of these circuits shall not be less than 300 ohms when measured with an applied voltage (either positive or negative polarity) not greater than 2 volts in magnitude referenced to signal ground or common return.

The interpretation of a fault condition by a receiver (or load) is application dependent. Each application may use a combination of the following classification:

Type 0: No interpretation. A receiver or load does not have detection capability.

Type 1: Data circuits assume a binary 1 state. Control and timing circuits assume an OFF condition.

The association of the circuit failure detection to particular interchange circuits in accordance with the above types is a matter of the functional and procedural characteristics specification of the interface.

The interchange circuits monitoring circuit fault conditions in the general telephone network interfaces are indicated in Recommendation V.24.

9600 BITS PER SECOND MODEM STANDARDIZED FOR USE ON POINT-TO-POINT 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

1 Introduction

This modem is intended to be used primarily on special quality leased circuits, e.g. Recommendation M.1020 [1] or M.1025 [2] circuits but this does not preclude the use of this modem over circuits of lower quality at the discretion of the Administration concerned (see Notes 1 and 2).

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

The principal characteristics of this recommended modem for transmitting data at 9600 bits per second on leased circuits are as follows:

a) fallback rates of 7200 and 4800 bits per second;

b) capable of operating in a duplex or half-duplex mode with continuous or controlled carrier;

c) combined amplitude and phase modulation with synchronous mode of operation;

d) inclusion of an automatic adaptive equalizer;

e) optional inclusion of a multiplexer for combining data rates of 7200, 4800 and 2400 bits per second (see Note 3).

Note 1 – The principal use of this recommended modem is on 4-wire leased circuits. Other applications, such as stand-by operation on the switched network, should be points for further study.

The types of special quality circuits, e.g. M.1020 [1] or M.1025 [2] should be studied.

Note 2 – The values of some circuit characteristics, for example, noise and nonlinear distortion, are subject to further study.

Note 3 – When the multiplexer option is installed, provisions in § 12 may supersede provisions given in other sections.

Note 4 – Attention should be given to the selection of appropriate equalization techniques in the modem implementation, if acceptable performance on circuits conforming to Recommendation M.1025 is desired.

2 Line signals

2.1 The carrier frequency is to be 1700 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Signal space coding*

2.2.1 At 9600 bits per second, the scrambled data stream to be transmitted is divided into groups of four consecutive data bits (quadbits). The first bit (Q1) in time of each quadbit is used to determine the signal element amplitude to be transmitted. The second (Q2), third (Q3) and fourth (Q4) bits are encoded as a phase change relative to the phase of the immediately preceding element (see Table 1/V.29). The phase encoding is identical to Recommendation V.27.

The relative amplitude of the transmitted signal element is determined by the first bit (Q1) of the quadbit and the absolute phase of the signal element (see Table 2/V.29). The absolute phase is initially established by the synchronizing signal as explained in § 8 below.

Figure 1/V.29 shows the absolute phase diagram of transmitted signal elements at 9600 bits per second.

At the receiver the quadbits are decoded and the data bits are reassembled in correct order.

TABLE 1/V.29

Q2	Q3	Q4	Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note – The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

TABLE 2/V.29

Absolute phase	Q1	Relative signal element amplitude
0°, 90°, 180°, 270°	0	3
	1	5
45°, 135°, 225°, 315°	0	$\sqrt{2}$
	1	$3\sqrt{2}$

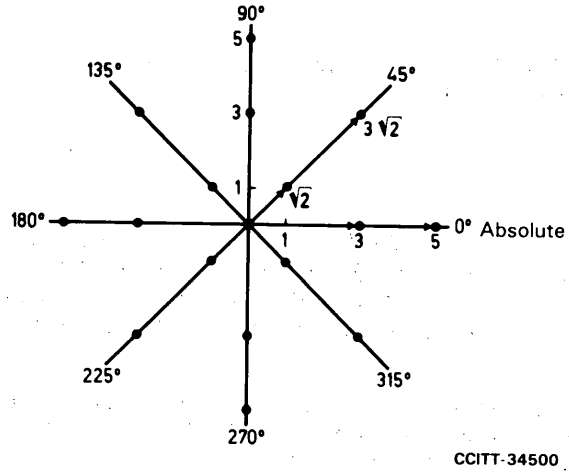


FIGURE 1/V.29

Signal space diagram at 9600 bit/s

2.2.2 At the fallback rate of 7200 bits per second, the scrambled data stream to be transmitted is divided into groups of three consecutive data bits. The first data bit in time determines Q2 of the modulator quadbit. The second and third data bits determine Q3 and Q4 respectively of the modulator quadbit. Q1 of the modulator quadbit is a data ZERO for each signal element. Signal elements are determined in accordance with § 2.2.1 above. Figure 2/V.29 shows the absolute phase diagram of the transmitted signal elements at 7200 bits per second.

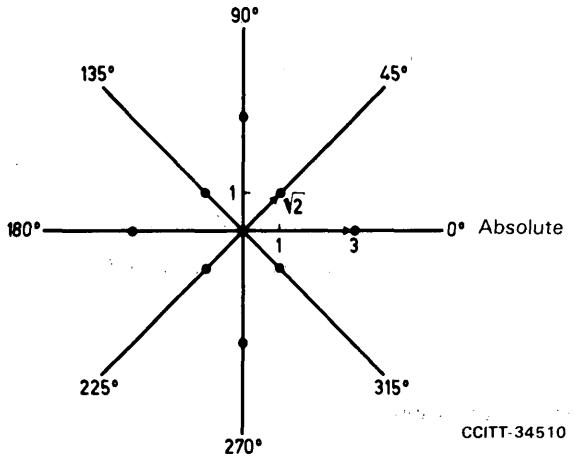


FIGURE 2/V.29

Signal space diagram at 7200 bit/s

2.2.3 At the fallback rate of 4800 bits per second (see Table 3/V.29), the scrambled data stream to be transmitted is divided into groups of two consecutive data bits. The first data bit in time determines Q2 of the modulator quadbit and the second data bit determines Q3 of the modulator quadbit. Q1 of the modulator quadbit is a data ZERO for each signal element. Q4 is determined by inverting the modulo 2 sum of Q2 + Q3. The signal element is then determined in accordance with § 2.2.1 above. Figure 3/V.29 shows the absolute phase diagram of transmitted signal elements at 4800 bits per second.

The phase changes are identical with Recommendation V.26 (alternative A) and the amplitude is constant with a relative value of 3.

TABLE 3/V.29

Data bits		Quadbits Q1	Q2	Q3	Q4	Phase change
0	0	0	0	0	1	0°
0	1	0	0	1	0	90°
1	1	0	1	1	1	180°
1	0	0	1	0	0	270°

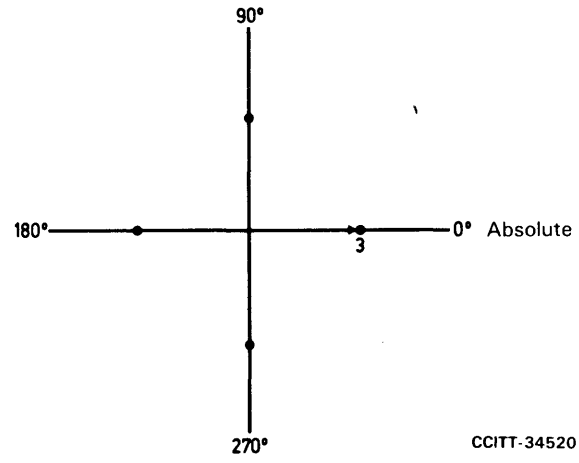


FIGURE 3/V.29

Signal space diagram at 4800 bit/s

3 Data signalling and modulation rates

The data signalling rates shall be 9600, 7200 and 4800 bits per second ± 0.01%. The modulation rate is 2400 bauds ± 0.01%.

4 Received signal frequency tolerance

The carrier frequency tolerance allowance at the transmitter is ± 1 Hz. Assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received signal frequency.

5 Interchange circuits

5.1 *List of interchange circuits* (Table 4/V.29)

5.2 *Threshold and response times of circuit 109*

5.2.1 *Threshold*

- greater than −26 dBm: circuit 109 ON;
- less than −31 dBm: circuit 109 OFF.

The condition of circuit 109 for levels between −26 dBm and −31 dBm is not specified except that the signal detector shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

5.2.2 *Response times*

- ON to OFF: 30 ± 9 ms;
- OFF to ON:
  1) for initial equalization, circuit 109 must be ON prior to user data appearing on circuit 104;
  2) for re-equalization during data transfer, circuit 109 will be maintained in the ON condition; during this period, circuit 104 may be clamped to the binary 1 condition;
  3) after a line signal interruption that lasts more than the ON to OFF response time:
     a) when no new equalization is needed, 15 ± 10 ms,
     b) when a new equalization is needed, circuit 109 must be ON prior to user data appearing on circuit 104.

TABLE 4/V.29

Interchange circuit (see Note 1)	
No.	Designation
102	Signal ground or common return
103	Transmitted data
104	Received data
105	Request to send
(see Note 2)	
106	Ready for sending
107	Data set ready
109	Data channel received line signal detector
111	Data signalling rate selector (DTE source)
(see Note 3)	
113	Transmitter signal element timing (DTE source)
114	Transmitter signal element timing (DCE source)
115	Receiver signal element timing (DCE source)
140	Loopback / Maintenance test
(see Note 4)	
141	Local loopback
(see Note 4)	
142	Test indicator

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 6).

Note 2 – Not essential for continuous carrier operation.

Note 3 – A manual selector shall be implemented which determines the two data signalling rates selected by circuit 111. The manual selector positions shall be designated 9600/7200, 9600/4800 and 7200/4800. The ON condition of circuit 111 selects the higher data signalling rate and the OFF condition of circuit 111 selects the lower data signalling rate.

Note 4 – Interchange circuits 140 and 141 are optional.

Response times of circuit 109 are the times that elapse between the connection or removal of a line signal to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuit 109.

Note – Circuit 109 ON to OFF response time should be suitably chosen within the specified limits to ensure that all valid data bits have appeared on circuit 104.

5.3 *Response time for circuit 106*

The time between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106 shall be optionally 15 ms ± 5 ms or 253.5 ms ± 0.5 ms.

The short delay is used when circuit 105 does not control the transmitter carrier. The long delay is used when circuit 105 controls transmitter carrier and a synchronizing signal is initiated by the OFF to ON transition of circuit 105.

The time between the ON to OFF transition of circuit 105 and the ON to OFF transition of circuit 106 shall be suitably chosen to ensure that all valid signal elements have been transmitted.

5.4 *Fault condition of interchange circuits*

(See Recommendations V.28, § 7 for association of the receiver failure detection types.)

5.4.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.4.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.4.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114, and receiver signal element timing, circuit 115. In this arrangement, the transmitter may either run as an independent timing source or with loopback timing (transmit timing slaved to receive timing). Loopback timing may be desirable in some network applications. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment and be transferred to the modem via interchange circuit 113.

8 Synchronizing signals

Transmission of synchronizing signals may be initiated by the modem or by the associated data terminal equipment. When circuit 105 is used to control the transmitter carrier the synchronizing signals are generated during the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106. When the receiving modem detects a circuit condition which requires resynchronizing, it shall turn circuit 106 OFF and generate a synchronizing signal.

The synchronizing signals for all data signalling rates are divided into four segments as in Table 5/V.29.

TABLE 5/V.29

	Segment 1	Segment 2	Segment 3	Segment 4	Total of Segments 1, 2, 3 and 4
Type of line signal	No transmitted energy	Alternations	Equalizer conditioning pattern	Scrambled all binary ONEs	Total synchronizing signal
Number of symbol intervals	48	128	384	48	608
Approximate time in ms [a]	20	53	160	20	253

[a] Approximate times are provided for information only. The segment duration is determined by the exact number of symbol intervals.

8.1 Segment 2 of the synchronizing signal consists of alterations between two signal elements. The first signal element (A) transmitted has a relative amplitude of 3 and defines the absolute phase reference of 180°. The second signal element (B) transmitted depends on the data signalling rate. Figure 4/V.29 shows the B signal element at each of the data signalling rates. Segment 2 alternates ABAB...ABAB for 128 symbol intervals.

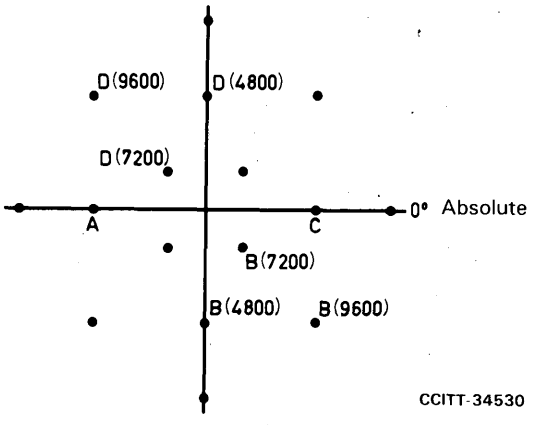


FIGURE 4/V.29

Signal space diagram showing synchronizing signal points

8.2 Segment 3 of the synchronizing signals transmits two signal elements according to an equalizer condition pattern. The first signal element (C) has a relative amplitude of 3 and absolute phase of 0°. The second signal element (D) transmitted depends on the data signalling rate. Figure 4/V.29 shows the D signal element at each of the data signalling rates. The equalizer conditioning pattern is a pseudo-random sequence generated by the polynomial:

$$1 + x^{-6} + x^{-7}$$

Each time the pseudo-random sequence contains a ZERO, point C is transmitted. Each time the pseudo-random sequence contains a ONE, the point D is transmitted. Segment 3 begins with the sequence CDCDCDC.... according to the pseudo-random sequence and continues for 384 symbol intervals. The detailed pseudo-random sequence generation is described in Appendix I.

8.3 Segment 4 commences transmission according to the encoding described in § 2.2 above with continuous binary ONEs applied to the input of the data scrambler. Segment 4 duration is 48 symbol intervals. At the end of Segment 4, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

9 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial $1 + x^{-18} + x^{-23}$, shall be included in the modem.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence. At the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix II.

10 Equalizer

An automatic adaptive equalizer shall be provided in the receiver.

The receiver shall incorporate a means of detecting loss of equalization and initiating a synchronizing signal sequence in its associated local transmitter.

The receiver shall incorporate a means of detecting a synchronizing signal sequence from the remote transmitter and initiating a synchronizing signal sequence in its associated local transmitter, which may be initiated at any time during the reception of the synchronizing signal sequence, regardless of the state of circuit 105.

Either modem can initiate the synchronizing signal sequence. The synchronizing signal is initiated when the receiver has detected a loss of equalization or when circuit 105 OFF to ON transition occurs in the carrier controlled mode, as described in § 5.3 above. Having initiated a synchronizing signal, the modem expects a synchronizing signal from the remote transmitter.

If the modem does not receive a synchronizing signal from the remote transmitter within a time interval equal to the maximum expected two-way propagation delay, it transmits another synchronizing signal. A time interval of 1.2 seconds is recommended.

If the modem fails to synchronize on the received signal sequence, it transmits another synchronizing signal.

If a modem receives a synchronizing signal when it had not initiated a synchronizing signal and the receiver properly synchronizes, it returns only one synchronizing sequence.

11

The following information is provided to assist equipment manufacturers:

- The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.
- The transmitter energy spectrum shall be shaped in such a way that with continuous binary ONEs applied to the input of the scrambler the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 700 Hz to 2700 Hz and the energy density at 500 Hz and 2900 Hz shall be attenuated 4.5 dB ± 2.5 dB with respect to the maximum energy density between 500 Hz and 2900 Hz.

12 Multiplexing (see Table 6/V.29)

A multiplexing option may be included to combine 7200, 4800 and 2400 bits per second data subchannels into a single aggregate bit stream for transmission. Identification of the individual data subchannels is accomplished by assignment to the modulator quadbit as defined in § 2.2 above.

12.1 *List of interchange circuits concerned with multiplexer ports* (see Table 7/V.29)

12.2 *Transmit buffers*

In the transmitter of each multiplexer port, there shall be a data buffer of suitable capacity. In this way, both phase variations and, within certain limits, frequency deviations are absorbed. The buffer shall be initialized when the OFF to ON transition of circuit 105 occurs and may be repositioned in the event of the buffer overflow.

Note – The buffer may be initialized upon the DCE sending a synchronizing signal.

12.3 *Transmit port timing arrangements*

Table 8/V.29 shows all possible combinations of port and main DCE transmit timing clock arrangements.

12.4 *Port simulated circuit 105 to circuit 109 operation (optional)*

When implemented, simulated circuit 105 to circuit 109 operation shall be provided on an individual port basis, non-interruptive to other ports. This operation shall communicate circuit 105 status at the transmitter to circuit 109 status at the receiver as may be required in some applications. The entire DCE shall operate in a continuous carrier mode in this case.

TABLE 6/V.29

Aggregate data rate	Multiplex configuration	Sub-channel data rate	Multiplex channel	Modulator bits			
				Q1	Q2	Q3	Q4
9600 bit/s	1	9600	A	X	X	X	X
	2	7200 2400	A B	X	X	X	 X
	3	4800 4800	A B	X	 X	X	 X
	4	4800 2400 2400	A B C	X	 X	X	 X
	5	2400 2400 2400 2400	A B C D	X	 X	 X	 X
7200 bit/s	6	7200	A		X	X	X
	7	4800 2400	A B		X	X	 X
	8	2400 2400 2400	A B C		X	 X	 X
4800 bit/s	9	4800	A		X	X	
	10	2400 2400	A B		X	 X	

Note – When more than one modulator bit is assigned to a sub-channel, the first bit in time of the sub-channel is assigned to the first bit in time (Q1) of the modulator.

TABLE 7/V.29

Interchange circuits (see Note 1)		Port A	Ports B, C, D
No.	Designation		
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105	Request to send	X (see Note 2)	X (see Note 2)
106	Ready for sending	X (see Note 3)	X (see Note 3)
107	Data set ready	X	X
109	Data channel received line signal detector	X	X
111	Data signalling rate selector (DTE source)	X (see Note 4)	
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
140	Loopback / Maintenance test	X (see Note 5)	X (see Note 5)
141	Local loopback	X (see Notes 5 and 6)	
142	Test indicator	X (see Note 7)	X (see Note 7)

Note 1 — All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate recommendation for electrical characteristics (see § 6).

Note 2 — Circuit 105 is not necessary for continuous carrier transmission. The transmitted line signal will not be controlled by this interchange circuit. If needed, circuit 105 (when the multiplexer is present) is used to control circuit 109 at the remote DCE. See § 12.4 below.

Note 3 — During the synchronization process of the main DCE, the OFF condition of circuit 106 is signalled at all port interfaces.

Note 4 — Circuit 111 is optionally present on Port A. If present, circuit 111 is activated in multiplexer configurations 1, 6 and 9 in the same way as if no multiplexer were present.

Note 5 — Circuits 140 and 141 are optional.

Note 6 — Circuit 141 is present only on Port A. When used in multiplexer configurations other than configurations 1, 6 or 9, the looping occurs on all ports.

Note 7 — Circuit 142 is present on all ports of the multiplexer, but may be activated on an individual port basis for individual port tests. All are activated simultaneously for entire DCE tests.

TABLE 8/V.29

Source of port transmitter signal element timing (used to clock in circuit 103)	Source of DCE internal transmitter element timing (internal transmit clock)	Port transmit buffer
114 (DCE source)	Internal (Independent timing)	Not required
	External [a] (Circuit 113 of selected port)	Not required
	Receiver timing (Loopback timing)	Not required
113 (DTE [a] source)	Internal (Independent timing)	Required
	External [a] (Circuit 113 of selected port)	Required for all ports except port supplying circuit 113 to DCE
	Receiver timing (Loopback timing)	Required

[a] In these applications a source could also be another DCE.

12.5 *Response times for circuit 106*

Circuit 105 to circuit 106 delays on individual ports of the multiplexer are not necessarily those specified in § 5.3. Other suitable delays may be needed to handle simulated circuit 105 to circuit 109 operations.

APPENDIX I

(to Recommendation V.29)

Details of the pseudo-random sequence generator

The equalizer conditioning pattern is determined by a pseudo-random sequence generated by the polynomial $1 + x^{-6} + x^{-7}$. Figure I-1/V.29 shows a suitable implementation.

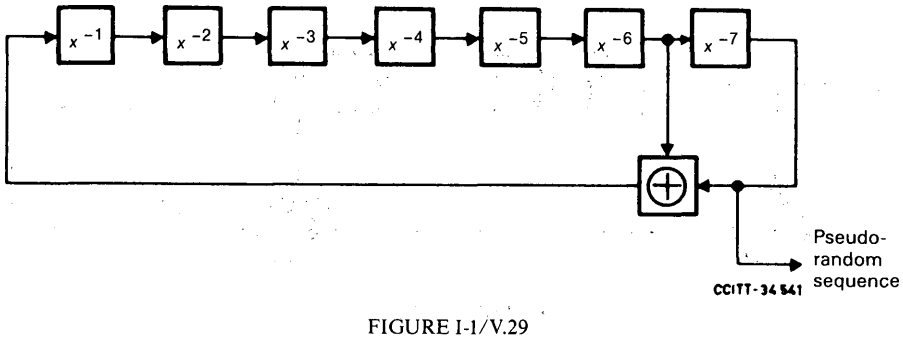


FIGURE I-1/V.29

The initial condition of the generator is 0101010. The generator clock is at the symbol rate (2400 symbols per second). The first four conditions of the generator are:

- initial condition: 0101010
- after first shift: 1010101
- after second shift: 1101010
- after third shift: 1110101

APPENDIX II

(to Recommendation V.29)

Detailed scrambling and descrambling process

II.1 *Scrambling*

The message polynomial is divided by the generating polynomial $1 + x^{-18} + x^{-23}$ (see Figure II-1/V.29). The coefficients of the quotient of this division taken in descending order form the data sequence to be transmitted. In order to ensure that proper starting sequence is generated, the shift register is fed with "0" during segments 1, 2 and 3. During segment 4 and normal data transmission it is fed with scrambled data D_s (input data D_i being "1" during segment 4).

$$D_s = D_i \oplus D_s x^{-18} \oplus D_s x^{-23}$$

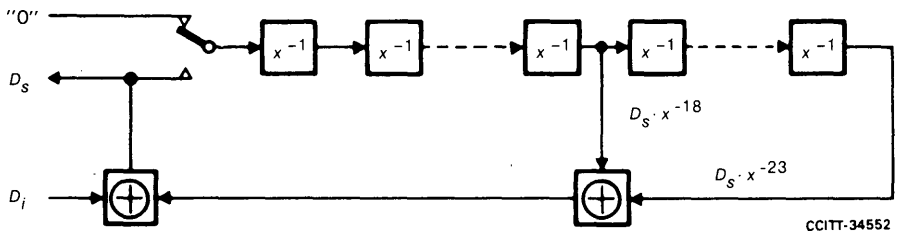


FIGURE II-1/V.29

II.2 *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial (Figure II-2/V.29) to form the recovered message polynomial. The coefficients of the recovered polynomial, taken in descending order, form the output data sequence D_o.

$$D_o = D_i = D_s (1 \oplus x^{-18} \oplus x^{-23})$$

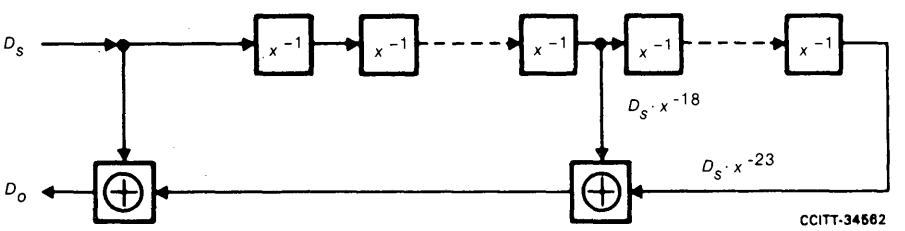


FIGURE II-2/V.29

II.3 *Elements of the scrambling process*

The polynomial $1 + x^{-18} + x^{-23}$ generates a pseudo-random sequence of length $2^{23} - 1 = 8{,}388{,}607$. This long sequence does not require the use of a guard polynomial to prevent the occurrence of repeat patterns and is particularly simple to implement with integrated circuits.

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with basic bandwidth conditioning*, Vol. IV, Rec. M.1025.

Recommendation V.31

ELECTRICAL CHARACTERISTICS FOR SINGLE-CURRENT INTERCHANGE CIRCUITS CONTROLLED BY CONTACT CLOSURE

(Geneva, 1972)

1 General

In general, the electrical characteristics specified in this Recommendation apply to interchange circuits operating at data signalling rates up to 75 bit/s.

Each interchange circuit consists of two conductors (go and return leads) which are electrically insulated from each other and from all other interchange circuits. A common return lead can be assigned to several interchange circuits of a group.

2 Equivalent circuit of interface

Figure 1/V.31 shows the equivalent interchange circuit, together with the electrical characteristics laid down in this Recommendation. Some electrical characteristics vary depending upon whether the signal receive side is located in the data circuit-terminating equipment or in the data side is located in the data circuit-terminating equipment or in the data terminal equipment. This fact is specially referred to below.

3 Signal source

The signal source must be isolated from ground or earth irrespective of whether it is located within the data circuit-terminating equipment or within the data terminal equipment.

If the signal receive side is in the data circuit-terminating equipment, the open-contact insulation resistance measured from either leg to ground or to any other interchange circuit shall not fall below 5 megohms and the capacitance measured between the same points shall not exceed 1000 picofardas.

Irrespective of the above, the following specifications apply to the signal source.

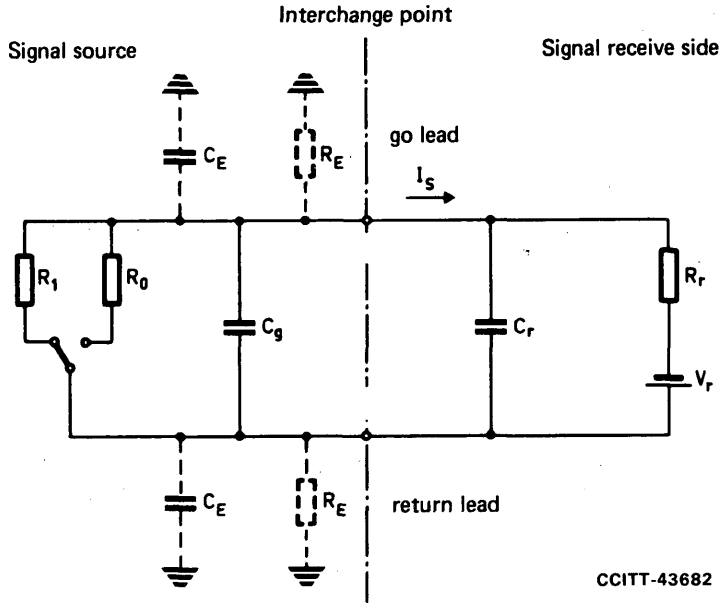
3.1 *Internal resistance of signal source R_1, R_0*

The d.c. resistance of the closed contact R_1, including the resistance of the interface cable, measured at the interface (see Figure 1/V.31), should not exceed 10 ohms within the current and voltage ranges of the signal receive side.

The d.c. resistance of the open contact R_0 including the insulation resistance of the interface cable should not fall below 250 kilohms when measured at the interface (see Figure 1/V.31) within the voltage range of the signal receive side.

3.2 *Capacitance of signal source C_g*

The capacitance of the signal source C_g including that of the interface cable, measured at the interface (see Figure 1/V.31), should not exceed 2500 picofards.



R_1 = internal resistance of the signal source in the closed contact condition
R_0 = internal resistance of the signal source in the open contact condition
C_g = capacitance of signal source
C_r = capacitance of signal receive side
V_r = open circuit voltage of signal receive side
I_S = current in interchange circuit
R_r = internal resistance of signal receive side
R_E = insulation resistance of signal source if the latter is in the data terminal equipment
C_E = ground capacitance of signal source if the latter is in the data terminal equipment

FIGURE 1/V.31

Equivalent circuit of interface

4 Signal receive side

4.1 *Signal receive side in the data circuit-terminating equipment*

The signal receive side in the data circuit-terminating equipment can be floating or connected to ground at any single point.

4.1.1 *Open circuit voltage of the signal receive side V_r*

The open circuit voltage V_r on the signal receive side of the data-circuit terminating equipment, measured at the interface (see Figure 1/V.31), should not fall below 3 volts and should not exceed 12 volts.

4.1.2 *Current at interface I_s*

The current I_s supplied by the signal receive side in the data circuit-terminating equipment should not fall below 0.1 milliamp and should not exceed 15 milliamps, when measured at the interface (see Figure 1/V.31) in the closed contact condition, i.e. with an internal resistance of the signal source of $R_1 \leqslant 10$ ohms.

Note – Irrespective of the current I_s in the closed contact conditions, i.e. with an internal resistance of the signal source of $R_1 \leqslant 10$ ohms, the voltage at the interface should not exceed 150 millivolts, when measured between go and return leads.

4.1.3 *Internal resistance of signal receive side R_r*

The internal resistance R_r of the signal receive side of the data circuit-terminating equipment results from the limits for the open circuit voltage V_r of the signal receive side and the current I_s at the interface, which are specified under §§ 4.1.1 and 4.1.2 above.

Even if R_r has an inductive component, the voltage at the interface should not exceed the maximum of 12 volts specified under § 4.1.1 above.

Note – This item is subject to further study.

4.1.4 *Capacitance of signal receive side C_r*

The capacitance of C_r of the signal receive side in the data circuit-terminating equipment, including the capacitance of the cable up to the interface (see Figure 1/V.31), is not specified. It is only necessary to ensure that the signal receive side works satisfactorily, allowing for the capacitance of the signal source C_g.

4.2 *Signal receive side in the data terminal equipment*

The signal receive side in the data terminal equipment can be connected to ground at any single point.

4.2.1 *Open circuit voltage of the signal receive side V_r*

The open circuit voltage V_r of the signal receive side of the data terminal equipment, measured at the interface (see Figure 1/V.31), should not fall below 3 volts and should not exceed 52.8 volts.

4.2.2 *Current at the interface I_s*

The current I_s, supplied by the signal receive side in the data terminal equipment, should not fall below 10 milliamps and not exceed 50 milliamps, when measured at the interface (see Figure 1/V.31) in the closed contact condition, i.e. with an internal resistance of the signal source of $R_1 \leqslant 10$ ohms.

4.2.3 *Internal resistance of signal receive side R_r*

The internal resistance R_r of the signal receive side in the data terminal equipment is obtained from the limits for the open circuit voltage V_r of the signal receive side and the current I_s at the interface, which are specified under §§ 4.2.1 and 4.2.2 above.

Even if R_r has an inductive component, the voltage at the interface should not exceed the maximum of 52.8 volts, specified under § 4.2.1.

Note – This item is subject to further study.

4.2.4 *Capacitance of signal receive side C_r*

The capacitance of C_r of the signal receive side in the data terminal equipment including the capacitance of the cable is not specified. It is only necessary to ensure that the signal receive side works satisfactorily, allowing for the capacitance of the signal source C_g.

5 Signal allocation

Table 1/V.31 shows allocations of digital signals for data, control and timing circuits.

TABLE 1/V.31

	Closed contact $R_1 \leqslant 10\Omega$	Open contact $R_0 \geqslant 250$ kΩ
Data circuits	"1" condition	"0" condition
Control and timing circuits	ON condition	OFF condition

ELECTRICAL CHARACTERISTICS FOR SINGLE-CURRENT INTERCHANGE CIRCUITS USING OPTOCOUPLERS

(Malaga-Torremolinos, 1984)

1 General

In general, the electrical characteristics specified in this Recommendation apply to interchange circuits operating at data signalling rates up to 75 bit/s, which have been covered in Recommendation V.31, and also to interchange circuits operating at data signalling rates up to 1200 bit/s.

The electrical characteristics are specified to provide compatibility with existing equipment according to Recommendation V.31 which meet the voltage and current values given in Table 1/V.31 *bis*. The resistance values defined in Recommendation V.31 are converted into current and voltage values to meet the optocouplers requirements.

Each interchange circuit consists of two conductors (go and return leads) which are electrically insulated from each other and from all other interchange circuits. A common return lead can be assigned to several interchange circuits of a group.

2 Equivalent circuit of interface

Figure 1/V.31 *bis* shows the equivalent interchange circuit, together with the electrical characteristics laid down in this Recommendation. Some electrical characteristics vary depending upon whether the signal receive side is located in the data circuit-terminating equipment (DCE) or in the data terminal equipment (DTE). This fact is specially referred to below.

3 Signal source

The signal source must be isolated from ground or earth irrespective of whether it is located within the data circuit-terminating equipment or within the data terminal equipment.

If the signal receive side is in the data circuit-terminating equipment, the insulation resistance in the ON or OFF condition measured from either leg to ground or to any other interchange circuit shall not fall below 5 megohms and the capacitance measured between the same points shall not exceed 1000 picofarads.

Irrespective of the above, the following specifications apply to the signal source.

3.1 *Internal resistance of signal source R_1, R_0*

The d.c. resistance of the signal source in the ON (or 1) condition R_1 depends on V_s, V_r and I_1 (see Figure 1/V.31 *bis*). The d.c. resistance of the signal source in the OFF (or 0) condition R_0 depends on V_r and I_0 (see Figure 1/V.31 *bis*).

3.2 *Current at the interface I_0*

The current I_0, which represents the reverse current of the optocouplers in the OFF condition, should not exceed 10 μA (see Figure 1/V.31 *bis*).

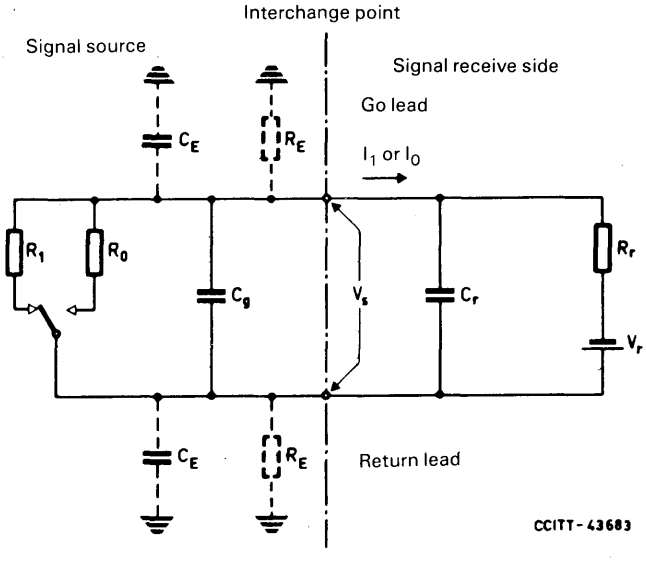
3.3 *Capacitance of signal source*

The capacitance of the signal source C_g including that of the interface cable, measured at the interface (see Figure 1/V.31 *bis*), should not exceed 2500 pF.

4 Signal receive side

4.1 *Signal receive side in the DCE*

The signal receive side in the DCE can be floating or connected to ground at any single point.



R_1 Internal resistance of the signal source in the ON (or 1) condition.
R_0 Internal resistance of the signal source in the OFF (or 0) condition.
C_g Capacitance of signal source.
C_r Capacitance of signal receive side.
V_r Open circuit voltage of signal receive side.
I_1 Current in interchange circuit in the ON (or 1) condition.
I_0 Current in the interchange circuit in the OFF (or 0) condition.
R_r Internal resistance of signal receive side.
R_E Insulation resistance of signal source if the latter is in the data terminal equipment.
C_E Ground capacitance of signal source if the latter is in the data terminal equipment.
V_s Voltage between the two leads of the interchange circuit in the ON (or 1) condition.

FIGURE 1/V.31 *bis*

Equivalent circuit of interface

4.1.1 *Open circuit voltage of the signal receive side V_r*

The open circuit voltage V_r on the signal receive side of the DCE, measured at the interface (see Figure 1/V.31 *bis*), should not fall below 3 V and should not exceed 25 V. The polarity of V_r has to be chosen for the current direction DTE to DCE in the go lead and DCE to DTE in the return lead.

4.1.2 *Current at the interface I_1*

The current I_1 supplied by the receive side in the DCE should not fall below 0.1 mA and should not exceed 5 mA, when measured at the interface in the ON (or 1) condition.

4.1.3 *Voltage at the interface V_s*

The voltage at the interface V_s, measured between the go and return leads in the ON (or 1) condition, should not exceed 1 V.

4.1.4 *Internal resistance of signal receive side R_r*

The internal resistance R_r of the signal receive side of the DCE results from the limits for the open circuit voltage V_r of the signal receive side and the current I_1 at the interface, which are specified under §§ 4.1.1 and 4.1.2 above.

Even if R_r has an inductive component, the voltage at the interface should not exceed the maximum of 25 V specified under § 4.1.1 above.

4.1.5 *Capacitance of signal receive side C_r*

The capacitance of C_r, of the signal receive side in the DCE, including the capacitance of the cable up to the interface (see Figure 1/V.31 *bis*), is not specified. It is only necessary to ensure that the signal receive side works satisfactorily, allowing for the capacitance of the signal source C_g.

4.2 *Signal receive side in the DTE*

The signal receive side in the DTE can be connected to ground at any single point.

4.2.1 *Open circuit voltage of the signal receive side V_r*

The open circuit voltage V_r of the signal receive side of the DTE, measured at the interface (see Figure 1/V.31 *bis*), should not fall below 3 V and should not exceed 25 V. The polarity of V_r has to be chosen for the current direction DTE to DCE in the go lead and DCE to DTE in the return lead.

4.2.2 *Current at the interface I_1*

The current I_1, supplied by the signal receive side in the DTE, should not fall below 0.1 mA and should not exceed 15 mA, when measured at the interface (see Figure 1/V.31 *bis*), in the ON (or 1) condition.

4.2.3 *Voltage at the interface V_s*

The voltage at the interface V_s, measured between the go and return leads in the ON (or 1) condition, should not exceed 1.5 V.

4.2.4 *Internal resistance of signal receive side R_r*

The internal resistance R_r of the signal receive side of the DTE results from the limits for the open circuit voltage V_r of the signal receive side and the current I_1 at the interface, which are specified under §§ 4.2.1 and 4.2.2 above.

4.2.5 *Capacitance of signal receive side C_r*

The capacitance of C_r of the signal receive side in the DTE including the capacitance of the cable is not specified. It is only necessary to ensure that the signal receive side works satisfactorily, allowing for the capacitance of the signal source C_g.

5 Signal allocation

Table 1/V.31 *bis* shows allocations of digital signals for data, control and timing circuits.

TABLE 1/V.31 *bis*

	0.1 mA $\leqslant I_1 \leqslant$ 5 mA (15 mA) $V_s \leqslant$ 1 V (1.5 V)	$I_0 \leqslant$ 10 μA
Data circuits	1 condition	0 condition
Control and timing circuits	ON condition	OFF condition

A FAMILY OF 2-WIRE, DUPLEX MODEMS OPERATING AT DATA SIGNALLING RATES OF UP TO 9600 BIT/S FOR USE ON THE GENERAL SWITCHED TELEPHONE NETWORK AND ON LEASED TELEPHONE-TYPE CIRCUITS

(Malaga-Torremolinos, 1984)

1 Introduction

This family of modems is intended for use on connections on general switched telephone networks (GSTNs) (see Note 1) and on point-to-point leased telephone-type circuits. The principal characteristics of the modems are as follows:

a) Duplex mode of operation on GSTN and 2-wire point-to-point leased circuits.

b) Channel separation by echo cancellation techniques.

c) Quadrature amplitude modulation for each channel with synchronous line transmission at 2400 bauds.

d) Any combination of the following data signalling rates may be implemented in the modems:

9600 bit/s synchronous,

4800 bit/s synchronous,

2400 bit/s synchronous (for further study).

e) At 9600 bit/s, two alternative modulation schemes, one using 16 carrier states and one using trellis coding with 32 carrier states, are provided for in this Recommendation. However, modems providing the 9600 bit/s data signalling rate shall be capable of interworking using the 16-state alternative.

f) Exchange of rate sequences during start-up to establish the data rate, coding and any other special facilities.

g) Asynchronous mode of operation (for further study) (see Note 2).

Note 1 – On international GSTN connections that utilize circuits that are in accord with Recommendation G.235 (16-channel terminal equipments), it may be necessary to employ a greater degree of equalization within the modem than would be required for use on most national GSTN connections.

Note 2 – Protocol of asynchronous to synchronous conversion will be derived from one already used in Recommendations V.22, V.22 *bis* and V.26 *ter*. A corresponding proposal, not yet fully finalized, may be found in Question 3/XVII.

2 Line signals

2.1 *Carrier frequency*

The carrier frequency is to be 1800 ± 1 Hz. No separate pilot tones are to be provided. The receiver must be able to operate with received frequency offsets of up to ± 7 Hz.

2.2 *Transmitted spectrum*

The transmitted power level must conform to Recommendation V.2. With continuous binary ones applied to the input of the scrambler, the transmitted energy density at 600 Hz and 3000 Hz should be attenuated 4.5 ± 2.5 dB with respect to the maximum energy density between 600 Hz and 3000 Hz.

2.3 *Modulation rate*

The modulation rate shall be 2400 bauds ± 0.01%.

2.4 *Coding*

2.4.1 *Signal element coding for 9600 bit/s*

Two alternatives are defined:

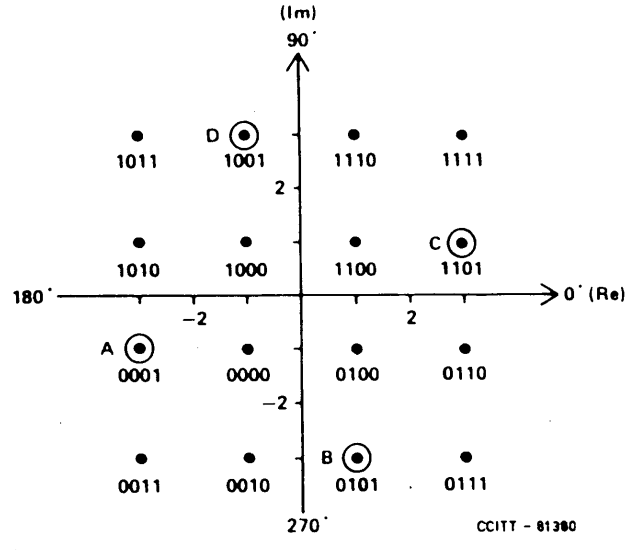
2.4.1.1 *Nonredundant coding*

The scrambled data stream to be transmitted is divided into groups of 4 consecutive data bits. The first two bits in time $Q1_n$ and $Q2_n$ in each group, where the subscript n designates the sequence number of the group, are differentially encoded into $Y1_n$ and $Y2_n$ according to Table 1/V.32. Bits $Y1_n$, $Y2_n$, $Q3_n$ and $Q4_n$ are then mapped into the coordinates of the signal state to be transmitted according to the signal space diagram shown in Figure 1/V.32 and as listed in Table 3/V.32.

TABLE 1/V.32

Differential quadrant coding for 4800 bit/s and for nonredundant coding at 9600 bit/s

Inputs		Previous outputs		Phase quadrant change	Outputs		Signal state for 4800 bit/s
$Q1_n$	$Q2_n$	$Y1_{n-1}$	$Y2_{n-1}$		$Y1_n$	$Y2_n$	
0	0	0	0	+ 90°	0	1	B
0	0	0	1		1	1	C
0	0	1	0		0	0	A
0	0	1	1		1	0	D
0	1	0	0	0°	0	0	A
0	1	0	1		0	1	B
0	1	1	0		1	0	D
0	1	1	1		1	1	C
1	0	0	0	+180°	1	1	C
1	0	0	1		1	0	D
1	0	1	0		0	1	B
1	0	1	1		0	0	A
1	1	0	0	+270°	1	0	D
1	1	0	1		0	0	A
1	1	1	0		1	1	C
1	1	1	1		0	1	B



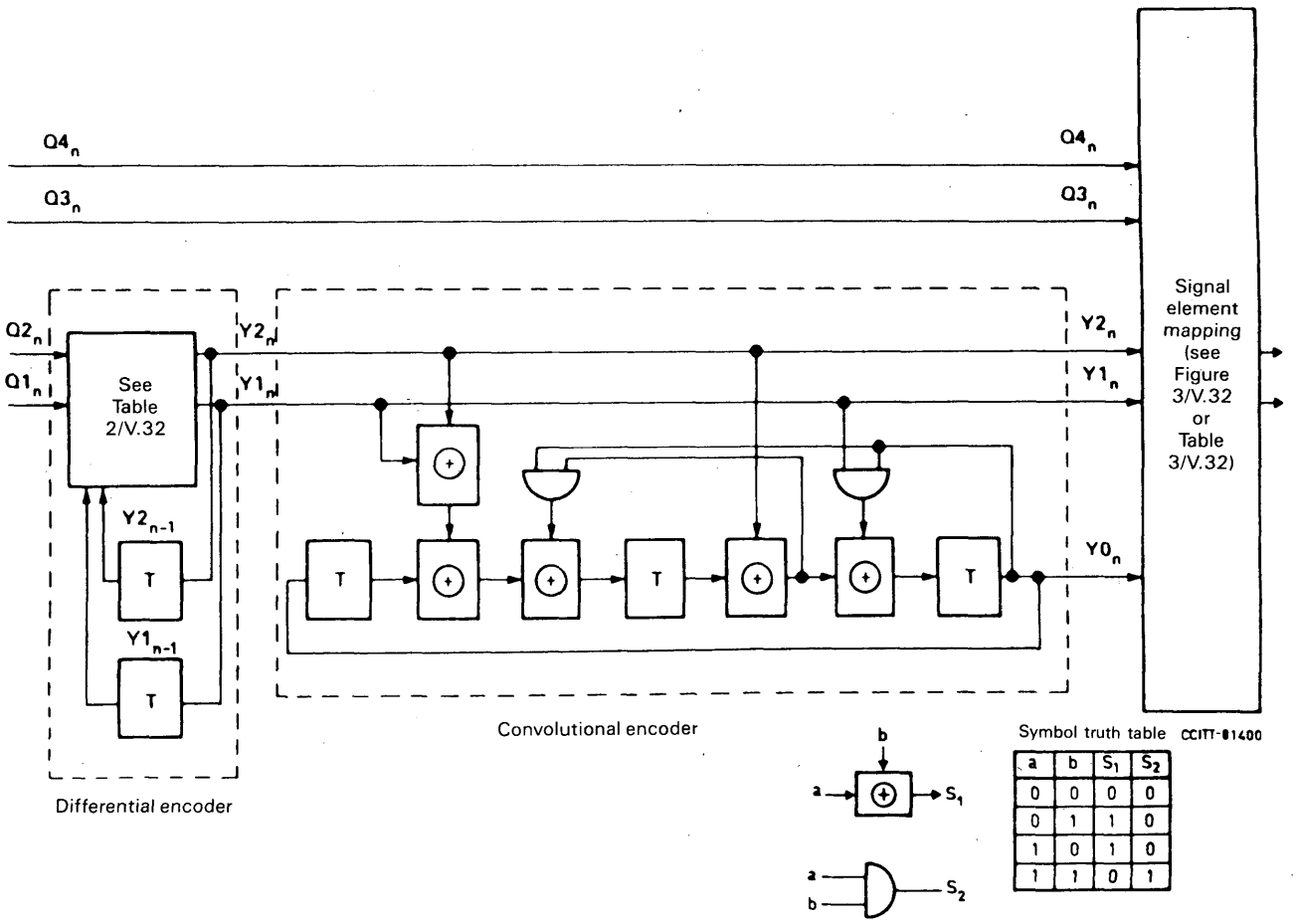
The binary numbers denote $Y1_n\ Y2_n\ Q3_n\ Q4_n$

FIGURE 1/V.32

16-point signal structure with nonredundant coding for 9600 bit/s and subset A B C D of states used at 4800 bit/s and for training

2.4.1.2 *Trellis coding*

The scrambled data stream to be transmitted is divided into groups of 4 consecutive data bits. As shown in Figure 2/V.32, the first two bits in time $Q1_n$ and $Q2_n$ in each group, where the subscript n designates the sequence number of the group, are first differentially encoded into $Y1_n$ and $Y2_n$ according to Table 2/V.32. The two differentially encoded bits $Y1_n$ and $Y2_n$ are used as input to a systematic convolutional encoder which generates a redundant bit $Y0_n$. This redundant bit and the 4 information-carrying bits $Y1_n$, $Y2_n$, $Q3_n$ and $Q4_n$ are then mapped into the coordinates of the signal element to be transmitted according to the signal space diagram shown in Figure 3/V.32 and as listed in Table 3/V.32.



a	b	S_1	S_2
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FIGURE 2/V.32

Trellis coding at 9600 bit/s

TABLE 2/V.32

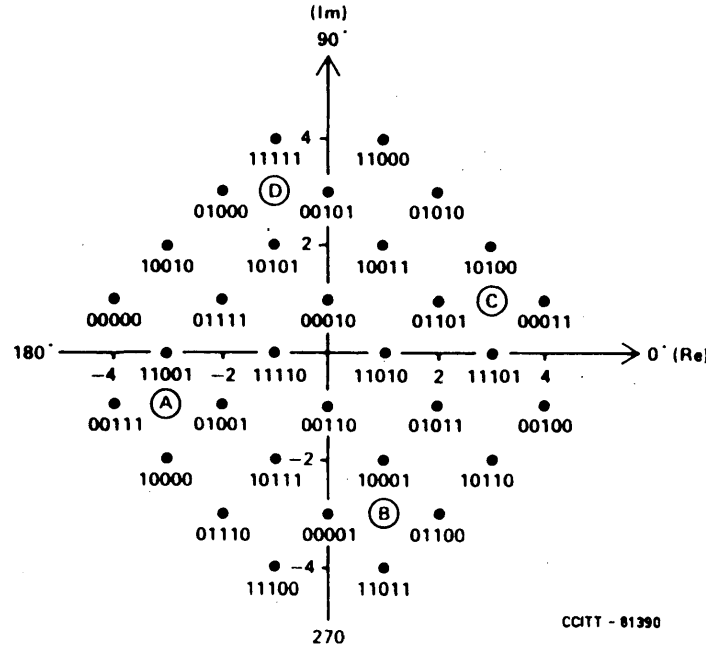
Differential encoding for use with trellis coded alternative at 9600 bit/s

Inputs		Previous outputs		Outputs	
$Q1_n$	$Q2_n$	$Y1_{n-1}$	$Y2_{n-1}$	$Y1_n$	$Y2_n$
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	1	0	1

TABLE 3/V.32

The two alternative signal-state mappings for 9600 bit/s

Coded inputs (see Table 1/V.32 or Table 2/V.32 with Figure 2/V.32)					Nonredundant coding		Trellis coding	
(Y0)	Y1	Y2	Q3	Q4	Re	Im	Re	Im
0	0	0	0	0	−1	−1	−4	1
	0	0	0	1	−3	−1	0	−3
	0	0	1	0	−1	−3	0	1
	0	0	1	1	−3	−3	4	1
	0	1	0	0	1	−1	4	−1
	0	1	0	1	1	−3	0	3
	0	1	1	0	3	−1	0	−1
	0	1	1	1	3	−3	−4	−1
	1	0	0	0	−1	1	−2	3
	1	0	0	1	−1	3	−2	−1
	1	0	1	0	−3	1	2	3
	1	0	1	1	−3	3	2	−1
	1	1	0	0	1	1	2	−3
	1	1	0	1	3	1	2	1
	1	1	1	0	1	3	−2	−3
	1	1	1	1	3	3	−2	1
1	0	0	0	0			−3	−2
	0	0	0	1			1	−2
	0	0	1	0			−3	2
	0	0	1	1			1	2
	0	1	0	0			3	2
	0	1	0	1			−1	2
	0	1	1	0			3	−2
	0	1	1	1			−1	−2
	1	0	0	0			1	4
	1	0	0	1			−3	0
	1	0	1	0			1	0
	1	0	1	1			1	−4
	1	1	0	0			−1	−4
	1	1	0	1			3	0
	1	1	1	0			−1	0
	1	1	1	1			−1	4



The binary numbers denote $Y0_n\ Y1_n\ Y2_n\ Q3_n\ Q4_n$

FIGURE 3/V.32

32-point signal structure with trellis coding for 9600 bit/s and states A B C D used at 4800 bit/s and for training

2.4.2 *Signal element coding for 4800 bit/s*

The scrambled data stream to be transmitted is divided into groups of 2 consecutive data bits. These bits, denoted $Q1_n$ and $Q2_n$, where $Q1_n$ is the first in time, and the subscript n designates the sequence number of the group, are differentially encoded into $Y1_n$ and $Y2_n$ according to Table 1/V.32. Figure 1/V.32 shows the subset A, B, C and D of signal states used for 4800 bit/s transmission.

2.4.3 *Signal element coding for 2400 bit/s*

(For further study.)

3 Interchange circuits

3.1 *List of interchange circuits*

These are listed in Table 4/V.32 below.

TABLE 4/V.32

Interchange circuit (see Note 1)		Notes
No.	Description	
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	
106	Ready for sending	
107	Data set ready	
108/1 or	Connect data set to line	2
108/2	Data terminal ready	2
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	3
112	Data signalling rate selector (DCE source)	3
113	Transmitter signal element timing (DTE source)	
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
125	Calling indicator	4
140	Loopback/maintenance test	
141	Local loopback	
142	Test indicator	

Note 1 – All interchange circuits which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.8).

Note 2 – This circuit shall be capable of operation as circuit 108/1 or circuit 108/2 depending on its use. Operation of circuits 107 and 108/1 shall be in accordance with § 4.4 of Recommendation V.24.

Note 3 – This circuit is not essential when only one data signalling rate is implemented in the modem.

Note 4 – This circuit is for use with the general switched telephone network only.

3.2 *Transmit data*

The modems shall accept synchronous data from the DTE on circuit 103 under control of circuit 113 or 114.

3.3 *Receive data*

The modems shall pass synchronous data to the DTE on circuit 104 under the control of circuit 115.

3.4 *Timing arrangements*

Clocks shall be included in the modems to provide the DTE with transmitter signal element timing on circuit 114 and receiver signal element timing on circuit 115. The transmitter timing may originate in the DTE and be transferred to the modem via circuit 113. In some applications it may be necessary to slave the transmitter timing to the receiver timing inside the modem.

3.5 *Data rate control*

Data rate selection may be by switch (or similar means) or alternatively by circuit 111. In cases where three different data signalling rates are implemented in a modem, a manual selector may be provided which determines the two data signalling rates selected by circuit 111.

The ON condition of circuit 111 selects the higher data signalling rate and the OFF condition of circuit 111 selects the lower data signalling rate.

3.6 *Circuit 106*

After the start-up and retrain sequences, circuit 106 must follow the state of circuit 105 within 2 ms.

3.7 *Circuit 109*

OFF to ON and ON to OFF transitions of circuit 109 should occur solely in accordance with the operating sequences defined in § 5. Thresholds and response times are inapplicable because a line signal detector cannot be expected to distinguish wanted received signals from unwanted talker echoes.

3.8 *Electrical characteristics of interchange circuits*

3.8.1 Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-Series application which minimizes the number of interchange circuits.

3.9 *Fault condition on interchange circuits*

See § 7 of Recommendation V.28 for association of the receiver failure detection types.

3.9.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.9.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.9.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Scrambler and descrambler

A self-sychronizing scrambler/descrambler shall be included in the modem. Each transmission direction uses a different scrambler. The method of allocating the scramblers/descramblers is described in § 4.1. According to the direction of transmission, the generating polynomial is:

Call mode modem generating polynomial: (GPC) $= 1 + x^{-18} + x^{-23}$, or

Answer mode modem generating polynomial: (GPA) $= 1 + x^{-5} + x^{-23}$

At the transmitter, the scrambler shall effectively divide the message data sequence by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. At the receiver the received data sequence shall be multiplied by the scrambler generating polynomial to recover the message sequence.

4.1 *Scrambler/descrambler allocation*

4.1.1 *General switched telephone network (GSTN)*

On the general switched telephone network, the modem at the calling data station (call mode) shall use the scrambler with the GPC generating polynomial and the descrambler with the GPA generating polynomial. The modem at the answering data station (answer mode) shall use the scrambler with the GPA generating polynomial and the descrambler with the GPC generating polynomial. In some situations, however, such as when calls are established on the GSTN by operators, bilateral agreement on call mode/answer mode allocation will be necessary.

4.1.2 *Point-to-point leased circuits*

Scrambler/descrambler allocation and call mode and answer mode designation on point-to-point leased circuits will be by bilateral agreement between Administrations or users.

5 Operating procedures

5.1 *Recommendation V.25 automatic answering sequence*

The Recommendation V.25 automatic answering sequence shall be transmitted from the answer mode modem on international GSTN connections. The transmission of the sequence may be omitted on point-to-point leased circuits or on national connections on the GSTN where permitted by Administrations. In this event, the answer mode modem shall initiate transmission as in the retrain procedure specified in § 5.5.

5.2 *Receiver conditioning signal*

The receiver conditioning signal shall be used in the start-up and retrain procedures defined in §§ 5.4 and 5.5 below. The signal consists of three segments:

5.2.1 Segment 1, denoted by S in Figures 4/V.32 and 5/V.32, consists of alternations between states A and B as shown in Figure 1/V.32, for a duration of 256 symbol intervals.

5.2.2 Segment 2, denoted by $\overline{S}$ in Figures 4/V.32 and 5/V.32, consists of alternations between states C and D as shown in Figure 1/V.32, for a duration of 16 symbol intervals.

The transition from segment 1 to segment 2 provides a well-defined event in the signal that may be used for generating a time reference in the receiver.

5.2.3 Segment 3, denoted by TRN in Figures 4/V.32 and 5/V.32, is a sequence derived by scrambling binary ones at a data rate of 4800 bit/s with the scrambler defined in § 4. During the transmission of this segment, the differential quadrant encoding shall be disabled. The initial state of the scrambler shall be all zeros, and a binary one applied to the input for the duration of segment 3. Successive dibits are encoded onto transmitted signal states.

The first 256 transmitted signal states are determined from the state of the first bit occurring (in time) in each dibit. When this bit is ZERO, signal state A is transmitted; when this bit is ONE, signal state C is transmitted. Depending on whether the modem is in call or answer mode, the scrambler output patterns and corresponding signal states will then begin as below, where the bits and the signal states are shown in time sequence from left to right.

Call mode modem:

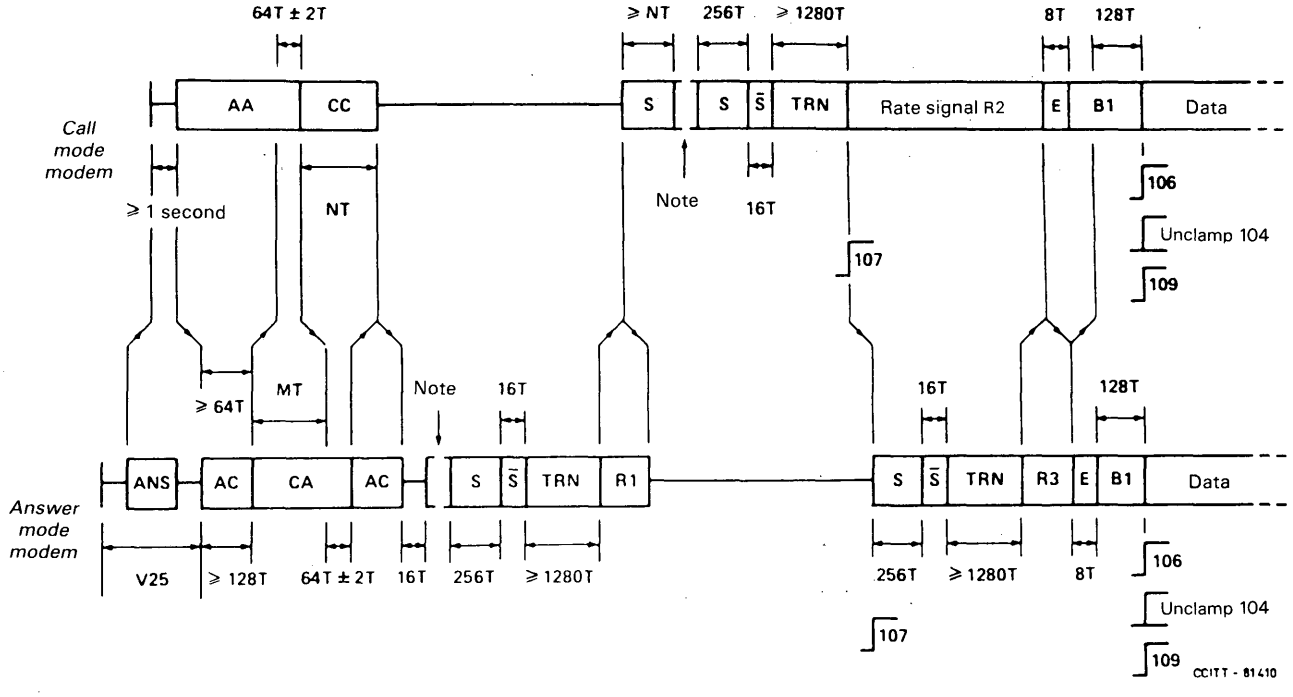
GPC: 11 11 11 11 11 11 11 11 11 00 00 01 11 11 11
C C C C C C C C C A A A C C C

Answer mode modem:

GPA: 11 11 10 00 00 11 11 10 00 00 11 10 01 11 11
C C C A A C C C A A C C A C C

Immediately after 256 such symbols, successive scrambled dibits are encoded onto transmitted signal states in accordance with Table 5/V.32 directly without differential encoding for the remainder of segment 3. The duration of segment 3 shall be at least 1280 and not exceed 8192 [1] symbol intervals.

Segment 3 is intended for training the adaptive equaliser in the receiving modem and the echo canceller in the transmitting modem.



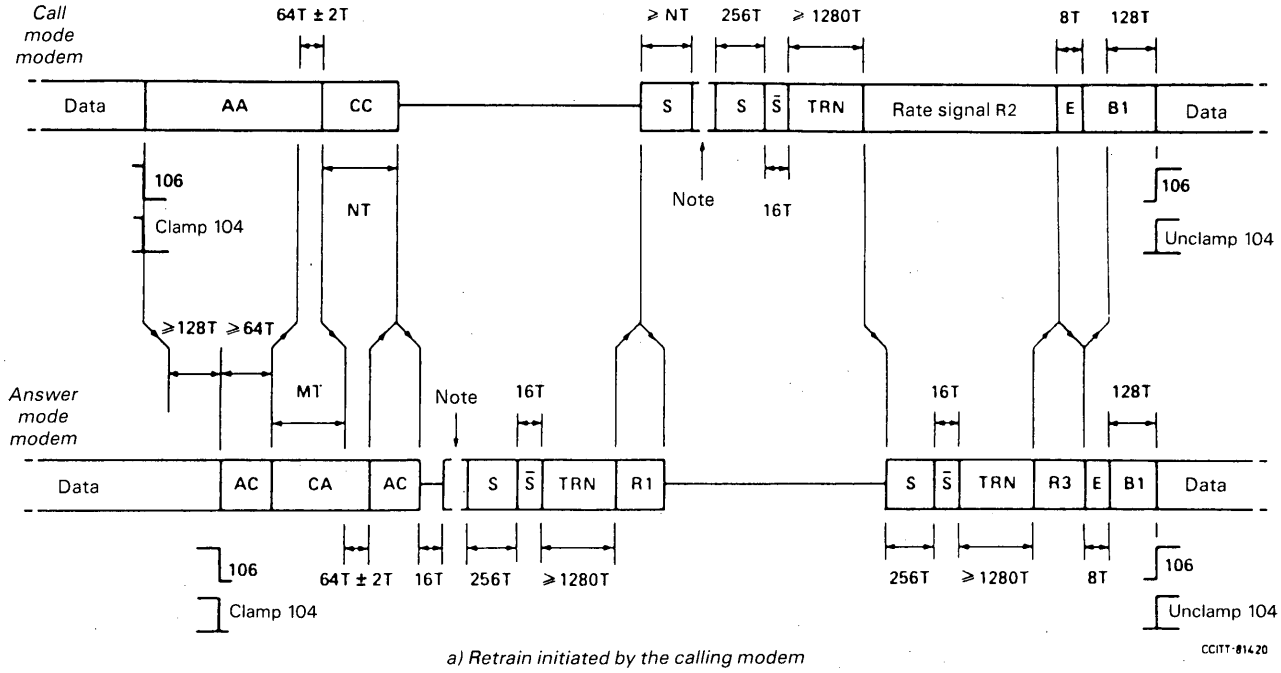
AC Signal states ACAC..AC for an even number of symbol intervals T; similarly with CA, AA and CC.
MT, NT Round-trip delays observed from answer and call modems respectively, including 64T ± 2T modem turn round delay.
S, S̄ Signal states ABAB..AB, CDCD..CD.
TRN Scrambled ones at 4800 bit/s with dibits encoded directly to states A, B, C and D as defined in § 5.2, c).
R1, R2, R3 Each a repeated 16-bit rate sequence at 4800 bit/s scrambled and differentially encoded as in Table 1/V.32.
E A single 16-bit sequence marking and following the end of a whole number of 16-bit rate sequences in R2 and R3.
B1 Binary ones scrambled and encoded as for the subsequent transmission of data.

Note — The inclusion of a special echo canceller training sequence at this point is optional (see § 5.4, Note 3).

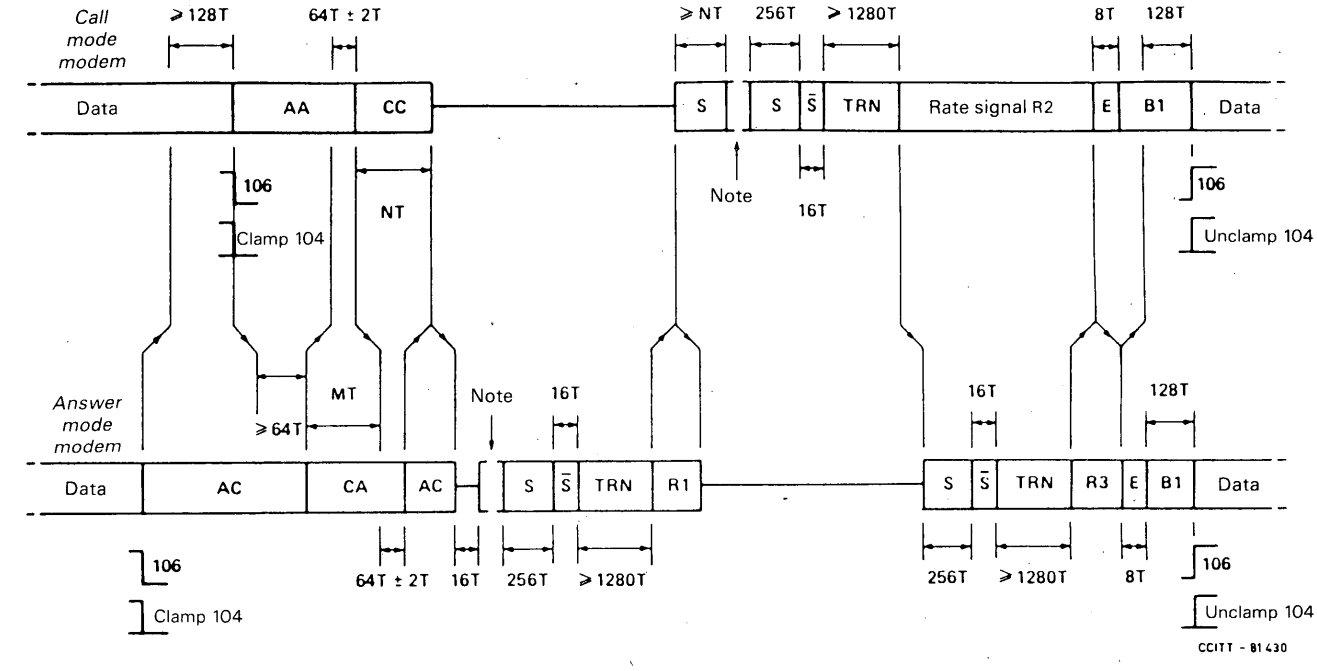
FIGURE 4/V.32

Start-up procedure

[1] The maximum duration of 8192 symbol intervals is for further study.



a) Retrain initiated by the calling modem



b) Retrain initiated by the answering modem

AC Signal states ACAC..AC for an even number of symbol intervals T; similarly with CA, AA and CC.
MT, NT Round-trip delays observed from answer and call modems respectively, including 64T ± 2T symbol intervals modem turn round delay.
S, $\bar{S}$ Signal states ABAB..AB, CDCD..CD.
TRN Scrambled ones at 4800 bit/s with dibits encoded directly to states A, B, C and D as defined in § 5.2, c).
R1, R2, R3 Each a repeated 16-bit rate sequence at 4800 bit/s scrambled and differentially encoded as in Table 1/V.32.
E A single 16-bit sequence marking and following the end of a whole number of 16-bit rate sequences in R2 and R3.
B1 Binary ones scrambled and encoded as for the subsequent transmission of data.

Note — The inclusion of a special echo canceller training sequence at this point is optional (see § 5.4, Note 3).

FIGURE 5/V.32

TABLE 5/V.32

Encoding for TRN segment after the first 256 symbols

Dibit	Signal state
00	A
01	B
11	C
10	D

Note – Signal states A, B, C and D are shown in Figure 1/V.32.

5.3 *Rate signal*

The rate signal consists of a whole number of repeated 16-bit binary sequences, as defined in Table 6/V.32, scrambled and transmitted at 4800 bit/s with dibits differentially encoded as in Table 1/V.32. The differential encoder shall be initialized using the final symbol of the transmitted TRN segment.

The first two bits and each successive dibit of the rate sequence shall be encoded to form the transmitted signal states.

The first transmitted octet, B0-B7, is fully defined in Table 6/V.32 and shall be interpreted by all Recommendation V.32 modems; the second octet, B8-B15, includes some codes defined in the table, some to be defined later and others to be left undefined for use by manufacturers.

TABLE 6/V.32

Coding of the 16-bit rate sequence

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	10	11	12	13	14	15	B0	B1	B2	B3	B4	etc.
0	0	0	0	–	–	–	1	–	–	–	1	–	–	–	1	0	0	0	0	–	

B0-3, B7, 11, 15	For synchronizing on a received rate signal
B4	1 denotes ability to receive data at 2400 bit/s
B5	1 denotes ability to receive data at 4800 bit/s
B6	1 denotes ability to receive data at 9600 bit/s
B4-6	0 0 0 calls for a GSTN cleardown
B8	1 denotes availability of trellis coding/decoding at the highest data rate indicated in B4-6
B9-14	0 0 1 0 0 0 denotes absence of special operational modes

Note – The remaining codes may be allocated within Recommendation V.32 in the future.

5.3.1 *Detecting a rate signal*

The minimum requirement for detection is the receipt of two consecutive identical 16-bit sequences each with bits B0-3, B7, 11 and 15 conforming to Table 6/V.32.

5.3.2 *Ending the rate signal*

In order to mark the end of transmission of any rate signal other than R1 (Figure 4/V.32), the modem shall first complete the transmission of the current 16-bit rate sequence, and then transmit one 16-bit sequence E, coded as shown in Table 7/V.32.

TABLE 7/V.32

Coding of signal E

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	10	11	12	13	14	15
1	1	1	1	–	–	–	1	–	–	–	1	–	–	–	1
B4-14	As in Table 6/V.32, except that the only data rate and coding to be indicated shall relate to the transmission of scrambled binary ones immediately following signal E														

5.4 *Start-up procedure*

The procedure for achieving synchronism between the calling modem and the answering modem on international GSTN connections is shown in Figure 4/V.32. The procedure includes the estimating of round-trip delay from each modem, the training of echo cancellers and receivers initially with half-duplex transmissions, and the exchanging of rate signals for automatic bit-rate and mode selection.

5.4.1 *Call mode modem*

After receiving the answer tone for a period of at least 1 s as specified in Recommendation V.25, the modem shall be connected to line (see Note 1 below) and shall condition the scrambler and descrambler in accordance with § 4.1.

The modem shall repetitively transmit carrier state A as shown in Figure 1/V.32.

The modem shall be conditioned to detect (see Note 2 below) one of two incoming tones at frequencies 600 ± 7 Hz and 3000 ± 7 Hz, and subsequently to detect a phase reversal in that tone.

On detection of one such phase reversal, the modem shall be conditioned to detect a second phase reversal in the same tone, start a counter/timer and change to repetitively transmitting state C as shown in Figure 1/V.32. The time delay between the reception of this phase reversal at the line terminals and the transmitted AA to CC transition appearing at the line terminals shall be 64 ± 2 symbol periods.

On detection of a second phase reversal in the same incoming tone, the modem shall stop the counter/timer and cease transmitting.

When the modem detects an incoming S sequence (see § 5.2), it shall proceed to train its receiver, and then seek to detect at least two consecutive identical 16-bit rate sequences as defined in Table 6/V.32.

On detection of the rate signal (R1), the modem shall transmit an S sequence for a period equal to the round-trip delay already estimated by the counter/timer.

After this period has expired (see Note 3 below), the modem shall transmit the receiver conditioning signal as defined in § 5.2, starting with an S sequence for 256 symbol intervals.

Transmission of the TRN segment of the receiver conditioning signal may be extended in order to ensure a satisfactory level of echo cancellation (see Note 4 below).

After the TRN segment, the modem shall apply an ON condition to circuit 107 and transmit a rate signal (R2) in accordance with § 5.3 to indicate the available data rates and whether trellis coding and/or other special operational modes are available. R2 should take account of the previously received rate signal R1. It is recommended that R2 should also take account of the likely receiver performance with the particular GSTN connection. If it appears that satisfactory performance cannot be attained at any of the available data rates, then R2 should be used to call for a GSTN cleardown in accordance with Table 6/V.32.

Transmission of R2 shall continue until an incoming rate signal R3 is detected. The modem shall then, after completing its current 16-bit rate sequence, transmit a single 16-bit sequence E in accordance with § 5.3.2 indicating the data rate, coding and any special operational modes called for in R3. If, however, R3 is calling for a GSTN cleardown in accordance with Table 6/V.32, then the call modem shall disconnect from line and effect a cleardown.

The modem shall then transmit continuous scrambled binary ones at the data rate and with the coding called for in R3, and apply the appropriate condition to circuit 112. If trellis coding according to § 2.4.1.2 is to be used, the initial states of the delay elements of the convolution encoder shown in Figure 2/V.32 should be set to zero.

On detecting an incoming 16-bit E sequence as defined in § 5.3.2, the modem shall condition itself to receive data at the rate and with the coding indicated by the incoming E sequence. After a delay of 128 symbol intervals, it shall apply an ON condition to circuit 109, and unclamp circuit 104.

The modem shall then enable circuit 106 to respond to the condition of circuit 105 and be ready to transmit data.

5.4.2 *Answer mode modem*

On connection to line, the modem shall condition the scrambler and descrambler in accordance with § 4.1, and transmit the Recommendation V.25 answer sequence. Means, defined in Recommendation V.25, of disabling network echo cancellers and/or truncating the answer tone may be employed.

After the Recommendation V.25 answer sequence, the modem shall transmit alternate carrier states A and C as shown in Figure 1/V.32.

After alternate states A and C have been transmitted for an even number of symbol intervals greater than or equal to 128 *and* an incoming tone has been detected at 1800 ± 7 Hz for 64 symbol periods (see Note 5 below), the modem shall be conditioned to detect a phase reversal in the incoming tone, start a counter/timer, and change to transmitting alternate carrier states C and A for an even number of symbol intervals.

On detecting a phase reversal in the incoming tone, the modem shall stop the counter/timer and, after transmitting a state A, revert to transmitting alternate states A and C. The time delay between the reception of this phase reversal at the line terminals and the transmitted CA to AC transition appearing at the line terminals shall be 64 ± 2 symbol periods.

When an amplitude drop is detected in the incoming tone, the modem shall cease transmitting for a period of 16 symbol intervals and then (see Note 3) transmit the receiver conditioning signal as defined in § 5.2.

Transmission of the TRN segment of the receiver conditioning signal may be extended in order to ensure a satisfactory level of echo cancellation (see Note 4).

After the TRN segment, the modem shall transmit a rate signal (R1) in accordance with § 5.3 to indicate the data rates, coding and any special operational modes available in the answer modem and associated DTE.

On detection of an incoming S sequence, the modem shall cease transmitting.

The modem shall wait for a period equal to the round-trip delay already estimated by the counter/timer and then, if an incoming S sequence persists, or when an S sequence reappears (see *Note 3*), the modem shall proceed to train its receiver.

After training its receiver, the modem shall seek to detect at least two consecutive identical incoming 16-bit rate sequences as defined in § 5.3.

On detection of a rate signal (R2), the modem shall apply an ON condition to circuit 107 and transmit a second receiver conditioning signal as defined in § 5.2.

After the TRN segment, the modem shall transmit a second rate signal (R3) in order to indicate the data rate, coding and any special operational modes to be used. R3 shall take account of the received rate signal R2. It is recommended that R3 should also take account of the likely performance of the answer modem receiver with the particular GSTN connection established. If R2 is calling for a GSTN cleardown (see Table 6/V.32) and/or if it appears that satisfactory performance cannot be attained by the answer modem at any of the available data rates, then R3 should call for a GSTN cleardown, in accordance with Table 6/V.32.

When the modem detects an incoming 16-bit E sequence as defined in § 5.3.2, it shall condition itself to receive data at the rate and with the coding indicated by the E sequence.

The modem shall complete the current 16-bit rate sequence and then transmit a single 16-bit E sequence indicating the data rate and coding to be used in the subsequent transmission of scrambled binary ones. If trellis coding according to § 2.4.1.2 is to be used, then the initial states of the delay elements of the convolution encoder shown in Figure 3/V.32 should be set to zero.

The modem shall transmit scrambled binary ones for 128 symbol intervals, then enable circuit 106 to respond to the condition of circuit 105 and be ready to transmit data.

The modem shall also apply an ON condition to circuit 109 and unclamp circuit 104.

Note 1 – Once an incoming tone is detected at 600 ± 7 Hz or 3000 ± 7 Hz, the calling modem should proceed with the start-up sequence even if no 2100 Hz tone has been detected.

Note 2 – In some cases, the incoming tones may be preceded by a special pattern which may last up to 294 ms (see Appendix I).

Note 3 – The TRN segment in the receiver conditioning signal is suitable for training the echo canceller in the transmitting modem. Alternatively, it is acceptable to precede the receiver conditioning signal by a sequence which can be used specifically for training the echo canceller, but which need not be defined in detail in this Recommendation. The echo cancellation sequence (if used) must maintain energy transmitted to line to hold echo suppressors disabled, must not imitate segments 1 or 2 of the receiver conditioning signal defined in § 5.2, and its duration must not exceed 8192[2)] symbol intervals.

Note 4 – Manufacturers are cautioned that a period of 650 ms is needed for training any network echo cancellers conforming to Recommendation G.165, that may be encountered on GSTN connections.

Note 5 – The answering modem may disconnect from the line if the 1800 ± 7 Hz tone is not detected following transmission of the segment AC. However, to assure compatibility with manual originating data stations, it shall not disconnect for at least 3 seconds after the segment AC has been transmitted.

5.5 *Retrain procedure*

A retrain may be initiated during data transmission if either modem incorporates a means of detecting unsatisfactory signal reception. Figure 5a/V.32 shows a retrain event initiated by the calling modem and Figure 5b/V.32 shows a retrain event initiated by the answering modem. The procedure is as follows:

5.5.1 *Call mode modem*

Following detection of unsatisfactory signal reception or detection of one of two tones at frequencies 600 ± 7 Hz and 3000 ± 7 Hz for more than 128 symbol intervals, the modem shall turn OFF circuit 106, clamp circuit 104 to binary one and repetitively transmit carrier state A as shown in Figure 1/V.32. It shall then proceed in accordance with § 5.4.1 beginning with the third paragraph (see Note in § 5.5.2).

5.5.2 *Answer mode modem*

Following detection of unsatisfactory signal reception or detection of a tone of frequency 1800 ± 7 Hz for more than 128 symbol intervals, the modem shall turn OFF circuit 106, clamp circuit 104 to binary one and transmit alternate carrier states A and C for an even number of symbol intervals not less than 64. It shall then proceed in accordance with § 5.4.2 beginning with the third paragraph (see Note).

Note – During a retrain, circuits 109 and 107 should remain ON.

(The need for a shorter duplex retrain procedure to provide for rapid training of the modem receivers is for further study.)

6 Testing facilities

Test loops 2 and 3 as defined in Recommendation V.54 should be provided. Provision for test loop 2 shall be as specified for point-to-point circuits.

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2) The maximum duration of 8192 symbol intervals is for further study.

APPENDIX I

(to Recommendation V.32)

Interworking procedure for echo cancelling modems

Considering

– that the V.26 *ter* modem at 2400 bit/s and the V.32 modems at 9600 bit/s and 4800 bit/s are based on the same technique, referred to as echo cancellation;

– that the 1800 Hz carrier frequency is the same for the two modems;

– that there may be a need for a modem, referred to as multimode, able to interwork with V.26 *ter* and V.32 modems;

– that the determination of round-trip delay may be useful in some cases,

the handshaking operating sequence defined in the following paragraphs is provided for the information of manufacturers.

I.1 *Interworking of echo cancelling modems*

The V.32 modems at 9600 bit/s and 4800 bit/s and the V.26 *ter* modems at 2400 bit/s could interwork with a dedicated multimode modem implementing both V.32 and V.26 *ter* capabilities, as illustrated in Table I-1/V.32.

I.1.1 *Operation of the calling multimode modem*

The modem will recognize:

– A V.26 *ter* modem by detecting the 1200 baud synchronization signals followed by a rate pattern and then will proceed as defined in V.26 *ter* (see Figure I-1/V.32).

– V.32 modems by the detection of one of two incoming tones at frequencies 600 ± 7 Hz and 3000 ± 7 Hz (see Figure I-2/V.32). It will then proceed as defined in § 5.4.1.

– A multimode modem by the detection of a special rate pattern assigned to the multimode modem. It will transmit, as shown in Figure I-3/V.32, repetitively carrier state A or the synchronizing signals followed by the rate pattern, according to the selected mode of operation: V.32 or V.26 *ter* respectively.

I.1.2 *Operation of the answering multimode modem*

After the V.25 sequence, the modem will transmit the 1200 baud synchronizing signals followed by its special rate pattern, and then alternate carrier states A and C as defined in Recommendation V.32.

It will recognize during the transmission of these alternate carrier states A and C:

– a V.26 *ter* modem by the detection of the 1200 baud synchronizing signals followed by a rate pattern. It will stop transmitting alternate carrier states A and C and proceed according to Recommendation V.26 *ter* (see Figure I-4/V.32);

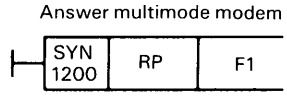
– V.32 modems by recognizing a tone at 1800 ± 7 Hz and will then proceed as defined in Recommendation V.32 (see Figure I-5/V.32).

The case of multimode modems on both answering and calling sides has been considered in § I.1.1.

TABLE I-1/V.32

Handshaking compatibility

Calling \ Answering	V.26 *ter*	V.32	M (Multimode)
V.26 *ter*	SYN 1200 / SYN 1200	F1 Disconnect / No energy	SYN 1200 then F1 (Note) / SYN 1200
V.32	F2 Wait at least T1 = 300 ms / SYN 1200 disconnect	F1 / F2	SYN 1200 then F1 (Note)
M (Multimode)	SYN 1200 / SYN 1200	F1 / Detected transmit F2	SYN 1200 then F1 (Note) / F2 or SYN 1200



CCITT - 85680

F1 : tones at 600 ± 7 Hz and 3000 ± 7 Hz generated by alternately transmitting carrier states A and C.
F2: tone at 1800 ± 7 Hz generated by repetitively transmitting carrier state A.

Note — The modem M is distinguished by a special rate pattern.

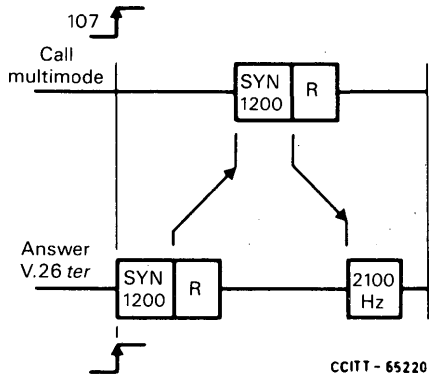


FIGURE I-1/V.32

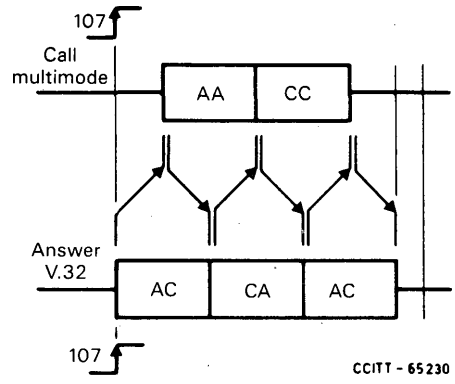


FIGURE I-2/V.32

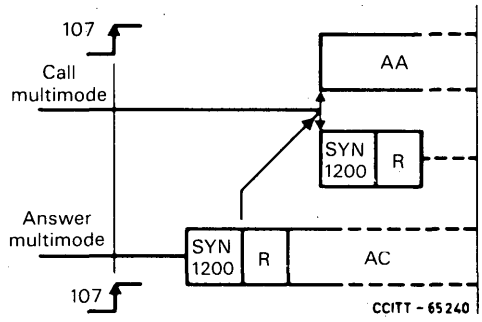


FIGURE I-3/V.32

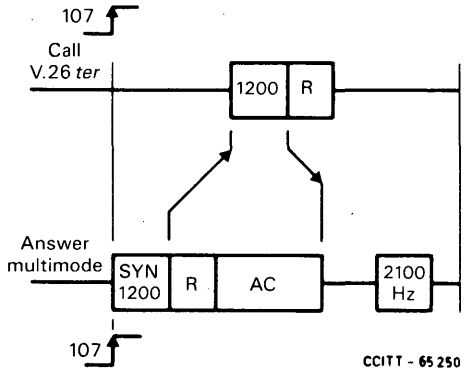


FIGURE I-4/V.32

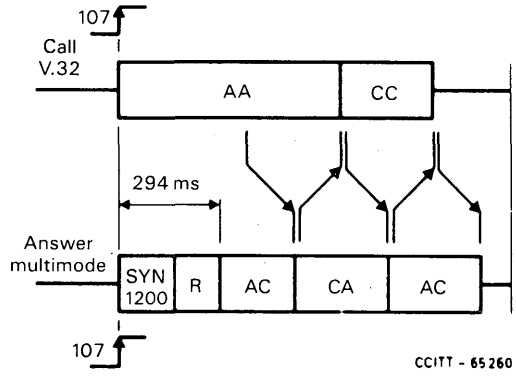


FIGURE I-5/V.32

SECTION 3

WIDEBAND MODEMS

Recommendation V.35

DATA TRANSMISSION AT 48 KILOBITS PER SECOND USING 60-108 kHz GROUP BAND CIRCUITS

(Mar del Plata, 1968; amended at Geneva, 1972 and 1976)

On leased circuits, considering that there exist and will come into being other modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

This is a particular system using a group reference pilot at 104.08 kHz.

Principal recommended characteristics to be used for simultaneous both-way operation are the following:

1 Input/output

Rectangular polar serial binary data.

2 Transmission rates

Preferred mode is synchronous at 48 000 ± 1 bit/s, with the following exceptions permissible:

a) Synchronous at 40 800 ± 1 bit/s when it is an operational necessity, or

b) Non-synchronous transmission of essentially random binary facsimile with element durations in the range 21 microseconds to 200 milliseconds.

Note – Operation at half data signalling rate shall be possible when the line characteristics do not permit the above data signalling rates.

3 Scrambler/descrambler

Synchronous data should be scrambled to avoid restrictions on the data input format. Such restrictions would be imposed by the need to have sufficient transitions for receiver clock stability, without short repetitive sequences of data signals which would result in high level discrete frequency components in the line signal. Synchronous data should be scrambled and descrambled by means of the logical arrangements described in Appendix I.

4 Modulation technique

The baseband signal (see § 5 below) should be translated to the 60 – 104 kHz band as an asymmetric sideband suppressed carrier AM signal with a carrier frequency of 100 kHz. A pilot carrier will be necessary to permit homochronous demodulation. To simplify the problem of recovery of the pilot carrier for demodulation the serial binary data signal should be modified as stated in § 5 below. The transmitted signal should correspond with the following:

a) The data carrier frequency should be 100 000 ± 2 Hz.

b) The nominal level of a frequency translated suppressed carrier 48 kbit/s encoded data baseband signal in the 60-104 kHz band should be equivalent to −5 dBm0.

c) A pilot carrier at −9 ± 0.5 dB relative to the nominal level of the signal in b) should be added such that the pilot carrier would be in phase, to within ± 0.04 radian, with a frequency translated continuous binary 1 input to the modulator.

d) The modulator should be linear, and the characteristics of the transmit bandpass filter should be such that the relative attenuation distortion and the relative envelope delay distortion in the range 64 to 101.5 kHz are less than 0.2 dB and 4 microseconds respectively.

5 Baseband signal

5.1 The scrambled synchronous or random non-synchronous serial binary data signal should be modified by the following transform:

$$\frac{pT_1}{1 + pT_1}$$ to remove the low-frequency components,

where

p is the complex frequency operator, and

T_1 is $25/2\pi$ times the minimum binary element duration, i.e. 83 microseconds.

The value of T_1 shall have an accuracy of ± 2%.

In this form the signal is referred to as the baseband signal.

5.2 The baseband signal resulting from the transformation should not suffer impairment greater than that resulting from relative attenuation distortion or relative envelope delay distortion of 1.5 dB or 4 microseconds respectively, *and*

i) distortion due to modification of the baseband signal by the transform

$$\frac{pT_2}{1 + pT_2}$$

where T_2 is 3.18 milliseconds; *or*

ii) distortion due to modification of the baseband signal by the transform

$$\left[\frac{pT_3}{1 + pT_3}\right]^2$$

where T_3 is 6.36 milliseconds.

5.3 The frequency range for §§ 5.1 and 5.2 is 0 to 36 kHz.

6 Voice channel

A service speech channel provided as an integral part of this system should correspond to channel 1 of a 12-channel system, i.e. as a lower sideband SSB signal in the 104-108 kHz band.

a) The characteristics of this channel may be less stringent than those of a telephone circuit in accordance with Recommendation G.232 [1].

b) This voice channel is optional.

7 Group reference pilots

7.1 Provision should be made for facilitating the injection of a group reference pilot of 104.08 kHz from a source external to the modem.

7.2 The protection of the group reference pilot should conform to Recommendation H.52 [2].

8 Adjacent channel interference

8.1 When transmitting scrambled synchronous serial binary data at 48 kbit/s on the data channel, the out-of-band energy in a 3-kHz band centered at any frequency in the range 1.5 to 58.5 kHz or 105.5 to 178.5 kHz should not exceed −60 dBm0.

8.2 When a signal at 0 dBm0 at any frequency in the range 0 to 60 or 104 to 180 kHz is applied to the carrier input terminals, the resulting crosstalk measured in the demodulated data baseband should not exceed a level equivalent to −40 dBm0.

9 Line characteristics

The characteristics of a channel over which this equipment can be expected to operate satisfactorily should be as given in reference [3].

10 Interface

10.1 The interchange circuits should be as shown in Table 1/V.35.

TABLE 1/V.35

Number	Function
102	Signal ground or common return
103 ø	Transmitted data
104 ø	Received data
105	Request to send
106	Ready for sending
107	Data set ready
109	Data channel receive line signal detector
114 ø	Transmitter signal element timing
115 ø	Receiver signal element timing

10.2 The electrical characteristics of the interchange circuits marked ø should be as described in Appendix II; the circuits not marked should conform to Recommendation V.28.

APPENDIX I

(to Recommendation V.35)

Scrambling process

I.1 *Definitions*

I.1.1 **applied data bit**

The data bit which has been applied to the scrambler but has not affected the transmission at the time of consideration.

I.1.2 **next transmitted bit**

The bit which will be transmitted as a result of scrambling the applied data bit.

I.1.3 **earlier transmitted bits**

Those bits which have been transmitted earlier than the next transmitted bit. They are numbered sequentially in reverse time order, i.e. the first earlier transmitted bit is that immediately preceding the next transmitted bit.

I.1.4 **adverse state**

The presence of any one of certain repetitive patterns in the earlier transmitted bits.

I.2 *Scrambling process*

The binary value of the next transmitted bit shall be such as to produce odd parity when considered together with the twentieth and third earlier transmitted bits and the applied data bit unless an adverse state is apparent, in which case the binary value of the next transmitted bit shall be such as to produce even instead of odd parity.

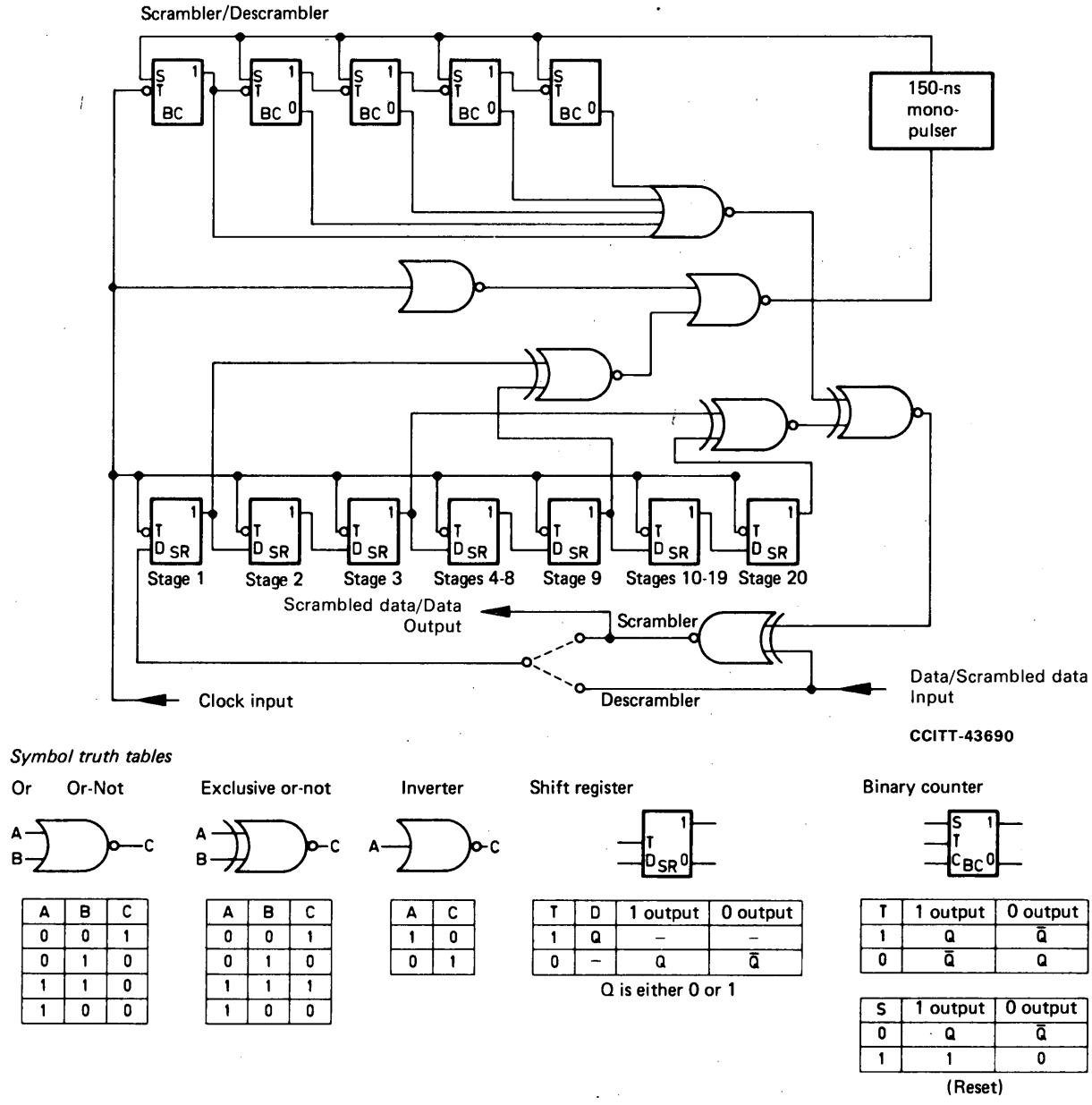
An adverse state shall be apparent only if the binary values of the p^{th} and $(p + 8)^{th}$ earlier transmitted bits have not differed from one another when p represents all the integers from 1 to q inclusive. The value of q shall be such that, for $p = (q + 1)$, the p^{th} and $(p + 8)^{th}$ earlier transmitted bits had opposite binary values and $q = (31 + 32\ r)$, r being 0 or any positive integer.

At the time of commencement, i.e. when no earlier bits have been transmitted, an arbitrary 20-bit pattern may be assumed to represent the earlier transmitted bits. At this time also it may be assumed that the p^{th} and $(p + 8)^{th}$ earlier transmitted bits have had the same binary value when p represents all the integers up to any arbitrary value. Similar assumptions may be made for the descrambling process at commencement.

Note 1 – From this it can be seen that received data cannot necessarily be descrambled correctly until at least 20 bits have been correctly received and any pair of these bits, separated from each other by seven other bits, have differed in binary value from one another.

Note 2 – It is not possible to devise a satisfactory test pattern to check the operation of the Adverse State Detector (ASD) because of the large number of possible states in which the 20-stage shift register can be at the commencement of testing. For those modems in which it is possible to bypass the scrambler and the descrambler and to strap the scrambler to function as a descrambler, the following method may be used. A 1 : 1 test pattern is transmitted with the ASD of the scrambler bypassed. If the ASD of the descrambler is functioning correctly the descrambled test pattern will contain a single element error every 32 bits, i.e. 90 000 errors per minute for a modem operating at 48 kbit/s indicates that the descrambler is functioning correctly. The operation of the ASD of the scrambler may be checked in a similar manner with the scrambler strapped as a descrambler and the descrambler bypassed.

I.3 Figure I-1/V.35 is given as an indication only, since with another technique this logical arrangement might take another form.



A	B	C
0	0	1
0	1	0
1	1	0
1	0	0

A	B	C
0	0	1
0	1	0
1	1	1
1	0	0

A	C
1	0
0	1

T	D	1 output	0 output
1	Q	–	–
0	–	Q	$\bar{Q}$

T	1 output	0 output
1	Q	$\bar{Q}$
0	$\bar{Q}$	Q

S	1 output	0 output
0	Q	$\bar{Q}$
1	1	0

Note – Negative-going transitions of clocks (i.e. 1 to 0 transitions) coincide with data transitions. This is self-synchronizing.

FIGURE I-1/V.35

An example of scrambler and descrambler circuitry

APPENDIX II

(to Recommendation V.35)

Electrical characteristics for balanced double-current interchange circuits

II.1 *Scope*

The electrical characteristics specified here apply to interchange circuits to Recommendation V.35.

II.2 *Cable*

The interface cable should be a balanced twisted multi-pair type with a characteristic impedance between 80 and 120 ohms at the fundamental frequency of the timing waveform at the associated terminator.

II.3 *Generator*

This circuit should comply with the following requirements:

a) source impedance in the range 50 to 150 ohms;

b) resistance between short-circuited terminals and circuit 102: 150 ± 15 ohms (the tolerance is subject to further study);

c) when terminated by a 100-ohm resistive load the terminal-to-terminal voltage should be 0.55 volt ± 20% so that the A terminal is positive to the B terminal when binary 0 is transmitted, and the conditions are reversed to transmit binary 1;

d) the rise time between the 10% and 90% points of any change of state when terminated as in c) should be less than 1% of the nominal duration of a signal element or 40 nanoseconds, whichever is the greater;

e) the arithmetic mean of the voltage of the A terminal with respect to circuit 102, and the B terminal with respect to circuit 102 (d.c. line offset), should not exceed 0.6 volt when terminated as in c).

II.4 *Load*

The load should comply with the following:

a) input impedance in the range 100 ± 10 ohms, substantially resistive in the frequency range of operation;

b) resistance to circuit 102 of 150 ± 15 ohms, measured from short-circuited terminals (the tolerance on this resistance is subject to further study).

II.5 *Electrical safety*

A generator or load should not be damaged by connection to earth potential, short-circuiting, or cross-connection to other interchange circuits.

II.6 *Performance in the presence of noise*

A generator, as in § II.3 above, connected via a cable as in § II.2 above to a load, as in § II.4 above, should operate without error in the presence of longitudinal noise or d.c. common return potential differences (circuit 102 offset) as follows:

a) with ± 2 volts (peak) noise present longitudinally, i.e. algebraically added to both load input terminals simultaneously with respect to the common return, *or*

b) with ± 4 volts circuit 102 offset;

c) if circuit 102 offset and longitudinal noise are present simultaneously, satisfactory operation should be achieved when:

$$\frac{\text{circuit 102 offset}}{2} + \text{longitudinal noise (peak)} = 2 \text{ volts or less.}$$

Note – It has been proposed to perform a test under inclusion of a cable length corresponding to the actual operation. This point is for further study.

References

[1] CCITT Recommendation *12-channel terminal equipments*, Vol. III, Rec. G.232.

[2] CCITT Recommendation *Transmission of wide-spectrum signals (data, facsimile, etc.) on wideband group links*, Vol. III, Rec. H.52.

[3] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals*, Vol. III, Rec. H.14, § 2.

Recommendation V.36

MODEMS FOR SYNCHRONOUS DATA TRANSMISSION USING 60-108 kHz GROUP BAND CIRCUITS

(Geneva, 1976; amended at Geneva, 1980 and Malaga-Torremolinos, 1984)

On leased circuits, considering that there exist and will come into being other modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

The only group reference pilot frequency which can be used in conjunction with this modem is 104.08 kHz.

1 Scope

The family of modems covered by this Recommendation should be applicable to the following uses:

a) transmission of data between customers on leased circuits;

b) transmission of a multiplex aggregate bit stream for public data networks;

c) extension of a PCM channel at 64 kbit/s over analogue facilities;

d) transmission of a common channel signalling system for telephony and/or public data networks;

e) extension of Single-Channel-Per-Carrier (SCPC) circuit from a satellite earth station;

f) transmission of a multiplex aggregate bit stream for telegraph and data signals.

Principal recommended characteristics to be used for simultaneous both-way synchronous operation are the following:

2 Data signalling rates

2.1 *Application a)*

The recommended data signalling rate (equals the customer signalling rate) for international use is synchronous at 48 kbit/s. For certain national applications or with bilateral agreement between Administrations, the following data signalling rates are applicable: 56, 64 and 72 kbit/s.

2.2 *Applications b), c) and d)*

For these applications, the recommended data signalling rate is synchronous at 64 kbit/s.

For those synchronous networks requiring the end-to-end transmission of both the 8 kHz and 64 kHz timing together with the data at 64 kbit/s, a data signalling rate of 72 kbit/s on the line is suggested.

The corresponding data format should be obtained by inserting one extra bit E just before the first bit of each octet of the 64 kbit/s data stream. The bits E convey alignment and housekeeping information, according to the pattern shown in Figure 1/V.36.

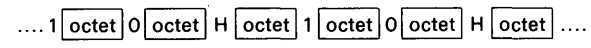


FIGURE 1/V.36

The use of the housekeeping bits H is determined with bilateral agreement between Administrations. When not used, these bits should be assigned the value 1. A framing strategy is not specified in this Recommendation.

When the transmission of the 8 kHz timing is not required, the data signalling rate on the line may be 64 kbit/s.

2.3 *Application e)*

The recommended data signalling rate (equals the customer signalling rate) for international use is synchronous at 48 kbit/s. For certain national applications or with bilateral agreement between Administrations the data signalling rate of 56 kbit/s is applicable.

2.4 *Application f)*

The recommended data signalling rate is synchronous at 64 kbit/s.

2.5 The permitted tolerance for all the data signalling rates mentioned above is $\pm 5 \times 10^{-5}$ bit/s.

Note – There are equipments in service which will only work successfully with a maximum tolerance of the data signalling rate of $\pm$ 1 bit/s.

3 Scrambler/descrambler

In order to be bit sequence independent and to avoid high amplitude spectral components on the line, the data should be scrambled and descrambled by means of the logical arrangements described in Appendix I.

4 Baseband signal

The equivalent baseband signal shaping process is based upon the binary coded partial response pulse, often referred to as class IV, whose time and spectral function are defined by:

$$g(t) = \frac{2}{\pi} \cdot \frac{\operatorname{Sin} \frac{\pi}{T} t}{\left(\frac{t}{T}\right)^2 - 1}$$

and

$$G(f) = \begin{cases} 2\,T j \operatorname{Sin} 2\pi\, Tf\,, & |f| \leqslant \dfrac{1}{2\,T} \\ 0\,, & |f| > \dfrac{1}{2\,T} \end{cases}$$

respectively, where $1/T$ denotes the data signalling rate.

This shaping process should be effected in such a way that the decoding can be achieved by full wave rectification of the demodulated line signal.

The reference to equivalent baseband signals recognizes that the modem implementation may be such that the binary signal at the input and output of the modem is converted to and from the line signal without appearing as an actual baseband signal.

5 Line signal in 60-108 kHz band (at the line output of the modem)

5.1 In the 60-108 kHz band the line signal should correspond to a single sideband signal with its carrier frequency at 100 kHz ± 2 Hz.

5.2 The relationship between the binary signals at the real or hypothetical output of the scrambler and the transmitted line signal states shall be in accordance with the amplitude modulation case of Recommendation V.1, i.e., tone ON for binary 1 and tone OFF for binary 0.

In a practical case this means that the voltage or no voltage conditions which will result from the full wave rectification of the demodulated line signal will correspond with the binary 1 and binary 0 signals respectively at the output of the scrambler.

5.3 The amplitude of the theoretical line signal spectrum, corresponding to binary symbol 1 appearing at the output of the scrambler, is to be sinusoidal, with zeros and maxima at the frequencies listed below:

Data signalling rate (kbit/s)	Zeros at (kHz)	Maxima at (kHz)
64	68 and 100	84
48	76 and 100	88
56	72 and 100	86
72	64 and 100	82

5.4 In the 60-108 kHz band, amplitude distortion of the real spectrum relative to the theoretical spectrum as defined under § 5.3 above is not to exceed ± 1 dB; the group delay distortion is not to exceed 8 microseconds. These two requirements are to be met for each frequency band centred on one of the maxima mentioned in § 5.3 and whose width is equal to 80% of the frequency band used.

5.5 The nominal level of the line data signal should be −6 dBm0. The actual level should be within ± 1 dB of the nominal level.

5.6 A pilot carrier at the same frequency as the modulated carrier at the transmitter and with a level of −9 ± 0.5 dB relative to the actual level mentioned under § 5.5 above, should be added to the line signal. The relative phase between the modulated carrier and the pilot carrier at the transmitter should be time invariant.

6 Group reference pilot

6.1 Provision should be made for facilitating the injection of a group reference pilot of 104.08 kHz from a source external to the modem.

6.2 The protection of the group reference pilot should conform to Recommendation H.52 [1].

7 Voice channel

7.1 The service speech channel is an integral part of the applications a) and e) of this system and is used on an optional basis. The channel corresponds to channel 1 of a 12-channel SSB-AM system in the 104-108 kHz band (virtual carrier at 108 kHz). It can transmit continuous voice at a mean level of maximum −15 dBm0 or pulsed signalling tones according to the individual specifications.

To avoid overloading of the system by peak signals a limiter shall be used with cut-off levels above +3 dBm0.

To avoid stability problems the channel shall be connected to 4-wire equipment only.

For operator-to-operator signalling Recommendation Q.1 [2] shall be followed, but instead of 500/20 Hz a non-interrupted tone of 2280 Hz at a level of −10 dBm0 shall be used.

For other signalling purposes [application e)] the R1 or R2 inband signalling, described in Recommendations Q.322 [3], Q.323 [4] and Q.454 [5], Q.455 [6] respectively, is preferred.

The transmit filter shall be such that any frequency applied to the transmit input terminals at a level of −15 dBm0 will not cause a level exceeding:

a) −73 dBm0p in the adjacent group,

b) −61 dBm0 in the vicinity (± 25 Hz) of the pilot 104.08 kHz,

c) −55 dBm0 in the data band between 64 and 101 kHz,

d) the values specified in Recommendation Q.414 [7] to protect the nearest low level signalling path.

The voice band is sufficiently protected if the same filter is used in the receive direction of the channel. The attenuation/frequency characteristic, measured between the voice-frequency input and the group band output or the group band input and the voice-frequency output, with respect to the value at 800 Hz is limited by:

−1 dB over the 300-3400 Hz band,

+2 dB between 540 and 2280 Hz.

7.2 The voice channel is inapplicable to applications b), c), d) and f). It is used on an optional basis for applications a) and e).

Note – When the modem is installed at the repeater station, the voice channel should be extended to the renter's premises.

8 Adjacent channel interference

In the bands 36-60 kHz and 108-132 kHz, the adjacent channel interference should conform to Recommendation H.52 [1].

9 Line characteristics

The modem is intended to operate satisfactorily over group links according to reference [8] at data signalling rates of 48 up to 64 kbit/s.

For group links, comprising more than three group sections, or where a data signalling rate of 72 kbit/s is required, the characteristics given in reference [8] are not adequate.

Furthermore, compliance of a group link with reference [8] does not necessarily guarantee proper operation of the modem, nor does noncompliance imply improper operation.

In Annex A a method is presented to calculate the suitability of a group link for data transmission using a modem according to this Recommendation.

When an automatic adaptive equalizer is included in the modem, proper operation over a circuit of similar construction as the hypothetical reference circuit as specified in reference [9] will be possible at data signalling rates up to 64 kbits.

Note 1 – Reference [9] specifies a maximum number of 8 through-group filters, but this figure is subject to further study and possible amendment.

Note 2 – The modem may allow operation at 72 kbit/s over a circuit having a maximum of 5 through-group filters. This value is left for further study.

10 Interface

10.1 *Interface for applications a), e) and f) indicated in § 1*

10.1.1 *List of interchange circuits* (See Table 1/V.36)

TABLE 1/V.36

Interchange circuit (see Note 1)		Remark
102	Signal ground or common return	See Note 2
102a	DTE common return	See Note 3
102b	DCE common return	See Note 3
103	Transmitted data	
104	Received data	
105	Request to send	
106	Ready for sending	
107	Data set ready	
109	Data channel received line signal detector	
113	Transmitter signal element timing (DTE source)	
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
140	Loopback/Maintenance test	See Note 2
141	Local loopback	See Note 2
142	Test indicator	See Note 2

Note 1 – When the modem is installed at the repeater station, this interface should appear at the customer's premises without restrictions regarding the data signalling rate and the provision of the voice channel. The method to achieve this is subject to national regulations.

Note 2 – Equipment may be in service that does not implement these circuits.

Note 3 – Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 are used.

10.1.2 *Electrical characteristics*

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended together with the use of the connector and pin assignment plan specified by ISO 4902.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

ii) In the case of circuits 105, 106, 107 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1 or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies with receivers configured as specified by Recommendation V.10 for category 2.

Note – For an interim period the electrical interface characteristics of Recommendation V.35 may be optionally used, together with the connector and pin assignment plan specified in ISO 2593.

10.2 *Interface for applications b), c) and d) indicated in § 1*

For applications b), c) and d) the interface may comply with the functional requirements given in reference [10] for the 64 kbit/s interface. In these cases, the electrical characteristics may comply with reference [11].

If an end-to-end transmission of the 8 kHz timing signal is not used, an 8 kHz timing signal across the interface will not be supplied nor utilized by the modem.

Alternatively the interface according to § 10.1 may be used for these applications.

11 Threshold and response time of circuit 109

11.1 *Threshold*

For a data line signal level greater than −13 dBm0, circuit 109 is ON. For data line signal level less than −18 dBm0, circuit 109 is OFF.

Note – The corresponding levels for the pilot carrier are −22 dBm0 and −27 dBm0 respectively.

The condition of circuit 109 for levels between the above levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition. To measure the thresholds of the detector, a modulated data signal with its pilot carrier at the level specified in § 5.6 should be used.

11.2 *Response time*

From OFF to ON: 15 ms to 150 ms,

From ON to OFF: 5 ms to 15 ms.

The response times of circuit 109 are the time intervals between the appearance or disappearance of the line signal at the reception input terminal of the modem and the occurrence of the corresponding ON or OFF condition on circuit 109.

The line signal level should be within the range from 3 dB above the actual threshold of the line signal detector at reception and the maximum permissible level of the signal at reception.

12 Error performance

12.1 For a hypothetical reference circuit, 2500 km in length, with characteristics in accordance with Recommendation H.14 [8], and with not more than two through-group connection equipments, the performance objective in terms of error rate should be not worse than 1 error per 10^7 bits transmitted. This is based on an assumed Gaussian noise power of 4 pW per km/per 4 kHz band psophometrically weighted (this figure corresponds to 4 pW0p/km).

13 Additional information for the designer

13.1 *Input level variation*

The step-change in the input level is, under normal conditions, smaller than ± 0.1 dB. The gradual input level change is smaller than ± 6 dB and includes the tolerance of the transmitter output level.

13.2 *Interference from adjacent group bands*

A sinusoidal signal of +10 dBm0 in the frequency bands of 36-60 kHz and 108-132 kHz can appear together with the data line signal at the input of the receiver.

ANNEX A

(to Recommendation V.36)

Line characteristics

For proper operation of the modem, the line characteristic of a group link shall comply with:

$$\varepsilon = \sqrt{\frac{c^2}{a^2 + b^2} - \frac{1}{2}} < 0.08$$

where

$$a = \frac{2}{T} \int_{f_t - \frac{1}{2T}}^{f_t} |G(f)|^2 \cdot |H(f)| \cos [\theta(f) + 2\pi f \tilde{\tau}] \, df,$$

$$b = \frac{2}{T} \int_{f_t - \frac{1}{2T}}^{f_t} |G(f)|^2 \cdot |H(f)| \sin [\theta(f) + 2\pi f \tilde{\tau}] \, df,$$

$$c^2 = \frac{2}{T} \int_{f_t - \frac{1}{2T}}^{f_t} |G(f)|^2 \cdot |H(f)|^2 \, df,$$

$|H(f)|$ is the attenuation characteristic of the link,

$\theta(f)$ is the phase characteristic of the link,

$G(f)$ is the spectral function of the transmitted line signal $= 2jT \sin \{2\pi (f_t - f)T\}$,

$\tilde{\tau}$ represents a constant time delay which should be chosen in such a way as to minimize ε, and

f_t is 100 kHz.

APPENDIX I

(to Recommendation V.36)

Scrambling process

I.1 *Definitions*

I.1.1 **applied data bit**

The data bit which has been applied to the scrambler but has not affected the transmission at the time of consideration.

I.1.2 **next transmitted bit**

The bit which will be transmitted as a result of scrambling the applied data bit.

I.1.3 **earlier transmitted bits**

Those bits which have been transmitted earlier than the next transmitted bit. They are numbered sequentially in reverse time order, i.e. the first earlier transmitted bit is that immediately preceding the next transmitted bit.

I.1.4 **adverse state**

The presence of any one of certain repetitive patterns in the earlier transmitted bits.

I.2 *Scrambling process*

The binary value of the next transmitted bit shall be such as to produce odd parity when considered together with the twentieth and third earlier transmitted bits and the applied data bit unless an adverse state is apparent, in which case the binary value of the next transmitted bit shall be such as to produce even instead of odd parity.

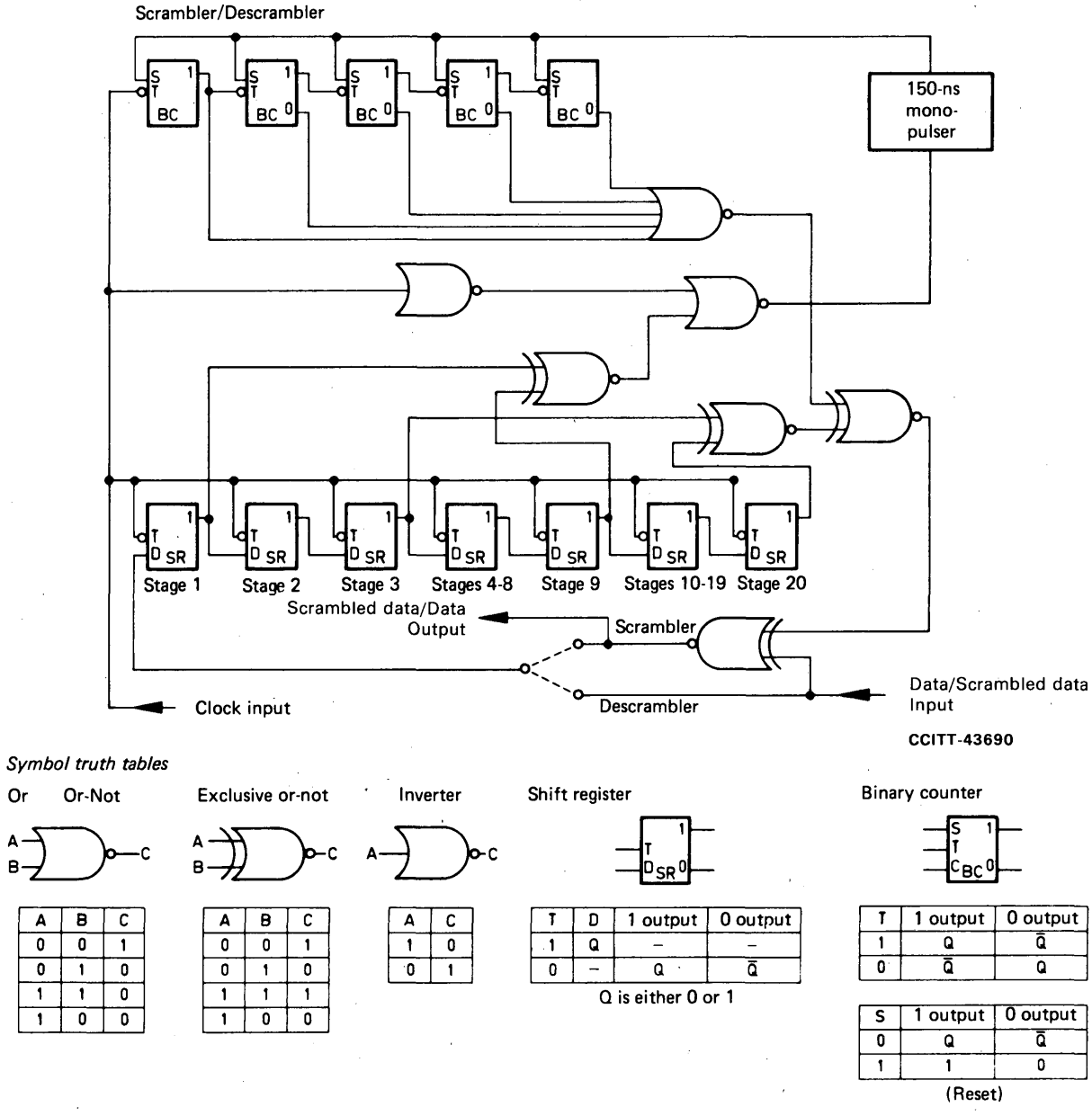
An adverse state shall be apparent only if the binary values of the p^{th} and $(p+8)^{th}$ earlier transmitted bits have not differed from one another when p represents all the integers from 1 to q inclusive. The value of q shall be such that, for $p = (q + 1)$, the p^{th} and $(p+8)^{th}$ earlier transmitted bits had opposite binary values and $q = (31 + 32\ r)$, r being 0 or any positive integer.

At the time of commencement, i.e. when no earlier bits have been transmitted, an arbitrary 20-bit pattern may be assumed to represent the earlier transmitted bits. At this time also it may be assumed that the p^{th} and $(p+8)^{th}$ earlier transmitted bits have had the same binary value when p represents all the integers up to any arbitrary value. Similar assumptions may be made for the descrambling process at commencement.

Note 1 – From this it can be seen that received data cannot necessarily be descrambled correctly until at least 20 bits have been correctly received and any pair of these bits, separated from each other by seven other bits, have differed in binary value from one another.

Note 2 – It is not possible to devise a satisfactory test pattern to check the operation of the Adverse State Detector (ASD) because of the large number of possible states in which the 20 state shift register can be at the commencement of testing. For those modems in which it is possible to bypass the scrambler and the descrambler and to strap the scrambler to function as a descrambler, the following method may be used. A 1 : 1 test pattern is transmitted with the ASD of the scrambler bypassed. If the ASD of the descrambler is functioning correctly the descrambled test pattern will contain a single element error every 32 bits, i.e. 90 000 errors per minute for a modem operating at 48 kbit/s indicates that the descrambler is functioning correctly. The operation of the ASD of the scrambler may be checked in a similar manner with the scrambler strapped as a descrambler and the descrambler bypassed.

I.3 Figure I-1/V.36 is given as an indication only, since with another technique this logical arrangement might take another form.



A	B	C
0	0	1
0	1	0
1	1	0
1	0	0

A	B	C
0	0	1
0	1	0
1	1	1
1	0	0

A	C
1	0
0	1

T	D	1 output	0 output
1	Q	–	–
0	–	Q	$\bar{Q}$

T	1 output	0 output
1	Q	$\bar{Q}$
0	$\bar{Q}$	Q

S	1 output	0 output
0	Q	$\bar{Q}$
1	1	0

Note – Negative-going transitions of clocks (i.e. 1 to 0 transitions) coincide with data transitions. This is self-synchronizing.

FIGURE I-1/V.36

An example of scrambler and descrambler circuitry

References

[1] CCITT Recommendation *Transmission of wide-spectrum signals (data, facsimile, etc.) on wideband group links*, Vol. III, Rec. H.52.

[2] CCITT Recommendation *Signal receivers for manual working*, Vol. VI, Rec. Q.1.

[3] CCITT Recommendation *Multifrequency signal sender*, Vol. VI, Rec. Q.322.

[4] CCITT Recommendation *Multifrequency signal receiving equipment*, Vol. VI, Rec. Q.323.

[5] CCITT Recommendation *The sending part of the multifrequency signalling equipment*, Vol. VI, Rec. Q.454.

[6] CCITT Recommendation *The receiving part of the multifrequency signalling equipment*, Vol. VI, Rec. Q.455.

[7] CCITT Recommendation *Signal sender*, Vol. VI, Rec. Q.414.

[8] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals*, Vol. III, Rec. H.14, § 2.

[9] *Ibid.*, § 3.

[10] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces*, Vol. III, Rec. G.703, § 1.

[11] *Ibid.*, § 1.2.

Recommendation V.37

SYNCHRONOUS DATA TRANSMISSION AT A DATA SIGNALLING RATE HIGHER THAN 72 kbit/s USING 60-108 kHz GROUP BAND CIRCUITS

(Geneva, 1980; amended at Malaga-Torremolinos, 1984)

1 Introduction

On leased circuits, considering that there exist and will come into being other modems with features designed to meet the requirements of Administrations and users, this Recommendation in no way restricts the use of any other modems.

The only group reference pilot frequency which can be used in conjunction with this modem is 104.08 kHz.

The modem is intended to be used on group band circuits not necessarily conforming to [1].

Principal characteristics:

a) transmission of any type of high-speed synchronous data in duplex constant carrier mode on 4-wire (60-108 kHz) group band circuits;

b) primary data signalling rates up to 144 kbit/s;

c) inclusion of an automatic adaptive equalizer;

d) class IV partial response pulse amplitude single sideband signalling and modulation;

e) optional inclusion of an overhead-free multiplexer combining existing data signalling rates;

f) optional voice channel.

2 Data signalling rates

2.1 The recommended synchronous data signalling rates are 96 kbit/s, 112 kbit/s, 128 kbit/s and 144 kbit/s. For some applications with agreement from the Administration, data signalling rates up to 168 kbit/s are applicable. (See the Note to § 7.)

2.2 The permitted tolerance for all data signalling rates is $\pm 5 \times 10^{-5}$.

3 Scrambler/descrambler

In order to be bit sequence independent, to avoid high amplitude spectral components on the line, and to allow the automatic equalizer to remain converged, the data should be scrambled and descrambled by means of the logical arrangements described in Appendix I.

4 Encoding method

The binary bit stream A, delivered by the scrambler, to be transmitted is divided into consecutive groups of 2 bits A_1 and A_2 (dibits), A_1 being the first in time delivered by the scrambler.

An amplitude level B is assigned to each dibit (A) as shown in Table 1/V.37.

TABLE 1/V.37

A_1	A_2	Equivalent B amplitude level
0	0	0
0	1	+ 1
1	1	+ 2
1	0	+ 3

A pre-encoder circuit converts the stream B into another quaternary stream C which conforms to the relation:

$$C_i = B_i \oplus C_{i-2}$$

where

$\oplus$ represents the modulo 4 sum

and the subscript i represents the i^{th} element of B or C.

The resulting quaternary stream C can be processed to form a baseband signal.

5 Baseband signal shaping

The equivalent baseband signal shaping process is based upon the binary coded partial response pulse, often referred to as class IV, whose time and spectral function are defined by:

$$g(t) = \frac{2}{\pi} \cdot \frac{\operatorname{Sin} \frac{\pi}{T} t}{\left(\frac{t}{T}\right)^2 - 1}$$

and

$$G(f) = \begin{cases} 2\,T j \sin 2\pi\,Tf\,, & |f| \leqslant \dfrac{1}{2\,T} \\ 0\,, & |f| > \dfrac{1}{2\,T} \end{cases}$$

respectively, where $1/T$ denotes the modulation rate.

The reference to equivalent baseband signals recognizes that the modem implementation may be such that the binary signal at the input and output of the modem is converted to and from the line signal without appearing as an actual baseband signal.

The baseband signal formed by the processes described above will present 7 levels (see Table 2/V.37).

The baseband signal shaping is performed in the transmitter.

TABLE 2/V.37

Level	Bit value	
	A_1	A_2
+ 3	1	0
+ 2	1	1
+ 1	0	1
0	0	0
− 1	1	0
− 2	1	1
− 3	0	1

6 Line signal in the 60-108 kHz band (at the line output of the modem)

6.1 In the 60-108 kHz band, the line signal should correspond to a single sideband signal with its carrier frequency pilot and timing pilot at frequencies as specified in Table 3/V.37.

6.2 The amplitude of the theoretical line signal spectrum, corresponding to a quaternary symbol (+1) appearing at the output of the encoder, is sinusoidal. The zeros and maxima of the theoretical line spectrum are shown in Table 3/V.37.

TABLE 3/V.37

Data rate (kbit/s)	Zeros at (kHz)	Maxima at (kHz)	Pilot carrier frequency	Timing pilot frequency
144	64 and 100	82	100 kHz	64 kHz
128	68 and 100	84	100 kHz	68 kHz
112	72 and 100	86	100 kHz	72 kHz
96	76 and 100	88	100 kHz	76 kHz
168 (optional)	62 and 104	83	104 kHz	62 kHz

6.3 In the 60-108 kHz band, amplitude distortion of the real spectrum relative to the theoretical spectrum as defined under § 6.2 above is not to exceed ± 1 dB; the group-delay distortion is not to exceed 15 μs. These two requirements are to be met for each frequency band centred on one of the maxima mentioned in § 6.2 and whose width is equal to 80% of the frequency band used.

6.4 The nominal level of the line data signal should be −6 dBm0. The actual level should be within ± 1 dB of the nominal level.

6.5 A pilot carrier at the same frequency as the modulated carrier (100 kHz ± 2 Hz) at the transmitter and with a level of −9 ± 0.5 dB relative to the actual level mentioned under § 6.4 above, should be added to the line signal. The relative phase between the modulated carrier and the pilot carrier at the transmitter should be time invariant.

Note – For the optional data signalling rate of 168 kbit/s, the pilot carrier should be 104 kHz ± 2 Hz.

6.6 A timing pilot at a frequency difference from the carrier equal to half the modulation rate at the transmitter with a level of −12 ± 0.5 dB relative to the actual level mentioned under § 6.4 above, should be added to the line signal.

The relationship between the timing pilot and the pilot carrier should remain time invariant at the transmitter.

7 Group reference pilot

7.1 Provision should be made for facilitating the injection of a group reference pilot of 104.08 kHz from an external source.

7.2 The protection of the group reference pilot should conform to Recommendation H.52 [2].

Note – Group reference pilot must be removed from the channel for operation at 168 kbit/s.

8 Optional voice channel

The service speech channel may be an integral part of the application of this system and is used on an optional basis. The channel corresponds to channel 1 of a 12 channel SSB-AM system in the 104-108 kHz band (virtual carrier at 108 kHz). It can transmit continuous voice at a mean level of maximum −15 dBm0 or pulsed signalling tones according to the individual specifications.

To avoid overloading of the system by peak signals, a limiter shall be used with cut-off levels above +3 dBm0.

To avoid stability problems, the channel shall be connected to 4-wire equipment only.

The transmit filter shall be such that any frequency applied to the transmit input terminals at a level of −15 dBm0 will not cause a level exceeding:

a) −73 dBm0p in the adjacent group;

b) −61 dBm0 in the vicinity (± 25 Hz) of the pilot 104.08 kHz;

c) −55 dBm0 in the data band between 64 and 101 kHz. When the 168 kbit/s data signalling rate is used this requirement applies between 62 and 104 kHz.

The voiceband is sufficiently protected if the same filter is used in the receive direction of the channel. The attenuation/frequency characteristic, measured between the voice-frequency input and the group band output or the group input and the voice-frequency output, with respect to the value at 800 Hz is limited by:

−1 dB over the 300-3400 Hz band,

+2 dB between 540 and 2280 Hz.

Note – When the modem is installed at the repeater station, the voice channel should be extended to the customer's premises.

9 Adjacent channel interference

In the bands 36-60 kHz and 108-132 kHz the adjacent channel interference should conform to Recommendation H.52 [2].

10 Line characteristics

The modem will allow proper operation of data signalling rates up to 128 kbit/s over a circuit of similar construction as the Hypothetical Reference Circuit as specified in reference [3].

Note 1 – Reference [3] specifies a maximum number of 8 through-group filters, but this figure is subject to further study and possible amendment.

Note 2 – The modem will allow operation over a circuit having a maximum number of 5 through-group filters at 144 kbit/s.

Note 3 – The line characteristics for operation at 168 kbit/s are not specified.

11 Synchronizing signals

Transmission of synchronizing signals is initiated by the modem. When the receiving modem detects a condition which requires resynchronizing, it shall turn circuit 106 OFF and generate synchronizing signals.

The synchronizing signals for all data signalling rates are divided into three segments as indicated in Table 4/V.37.

TABLE 4/V.37

	Segment 1	Segment 2	Segment 3	Total of Segments 1, 2 and 3	
Type of line signals	Only carrier and timing pilots	Carrier and timing pilots and alternation of levels (± 2)	Carrier and timing pilots and scrambled all binary ONEs	Data signalling rates (kbit/s)	Approximate time (s)
Number of symbol intervals	10240	4096	262144	96	5.76
				112	4.93
				128	4.32
				144	3.84
				168	3.29

11.1 Segment 1 transmits the carrier pilot, the timing pilot and data signal corresponding with the dibits (0, 0) applied at the input of the encoder.

11.2 Segment 2 consists of the carrier pilot, the timing pilot and an alternation between two signal levels (+2) and (−2) corresponding with the dibits (1, 1) applied at the input of the encoder.

11.3 Segment 3 consists of the carrier pilot, the timing pilot and scrambled all binary ONEs.

At the beginning of this segment:

- the scrambler shift register must be set to all 0s (see Appendix I);
- the adverse state detector counter must be set to all 1s (see Appendix I);
- the pre-encoder must be set to all 0s.

The equivalent baseband signal processed at the beginning of Segment 3 consists of a succession of 15 levels (0) followed by levels (+1), (0), (−1), (+1), (0), (−1), (+1), (0), (−1), (+1), (+1), (−1) . . . .

11.4 Circuit 106 is turned ON at the end of Segment 3 and the user's data may appear at the input of the scrambler.

12 Optional multiplexing

Multiplexing options shall be separately available to combine nominally available group band data rates of 48, 56, 64 or 72 kbit/s into a single aggregate bit stream for transmission as shown in Table 3/V.37. These multiplexers should be of a synchronous, overhead-free, bit interleave design. Using modem internal processing signals, multiplexers shall require no framing, allowing each subchannel to be a full one-half of the composite bit rate.

The two port multiplexer uses the bits from port A and B for bits A_1 and A_2 respectively of the dibits defined in § 4.

12.1 *Transmit buffers*

In the transmitter of each multiplex port, there shall be a data buffer of suitable capacity. In this way, both phase variations and, within certain limits, frequency deviations are absorbed. The buffer shall be initialized when an OFF to ON condition of circuit 105 occurs and may be repositioned in the event of a buffer overflow.

Note – The buffer may reinitialize upon a DCE resynchronization signal.

12.2 *Transmit port timing arrangements*

Table 5/V.37 shows all possible combinations of port and main DCE transmit timing clock arrangements.

13 Digital interface requirements

13.1 *List of interchange circuits* (see Table 6/V.37)

The interchange circuit table is valid for the main channel or the subchannel interfaces.

13.2 *Electrical characteristics*

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended together with the use of the connector and pin assignment plan specified by ISO 4902.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

ii) In the case of circuits 105, 106, 107 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1, or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies, with receivers configured as specified by Recommendation V.10 for category 2.

Note – For an interim period the electrical interface characteristics of Recommendation V.35 may be optionally used, together with the connector and pin assignment plan specified in ISO 2593.

TABLE 5/V.37

Source of port transmitter signal element timing (used to clock in circuit 103)	Source of DCE internal transmitter element timing (internal transmit clock)	Port transmit buffer
114 (DCE source)	Internal (Independent timing)	Not required
	External[a] (Circuit 113 of selected port)	Not required
	Receiver timing (Loopback timing)	Not required
113 (DTE[a] source)	Internal (Independent timing)	Required
	External[a] (Circuit 113 of selected port)	Required for all ports except port supplying circuit 113 to DCE
	Receiver timing (Loopback timing)	Required

[a] In these applications a source could also be another DCE.

TABLE 6/V.37

Interchange circuit (see Note 1)		Remark
102	Signal ground or common return	See Note 2
102a	DTE common return	See Note 3
102b	DCE common return	See Note 3
103	Transmitted data	
104	Received data	
105	Request to send	See Note 4
106	Ready for sending	See Notes 4 and 5
107	Data set ready	
109	Data channel received line signal detector	
113	Transmitter signal element timing (DTE source)	See Note 4
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
128	Receiver signal element timing (DTE source)	
140	Loop-back/Maintenance test	
141	Local loop-back	See Note 4
142	Test indicator	See Note 6

Note 1 – When the modem is installed at the repeater station, this interface should appear at the customer's premises without restrictions regarding the data signalling rate and the provision of the voice channel. The method to achieve this is subject to national regulations.

Note 2 – The provision of this conductor is optional.

Note 3 – Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 are used.

Note 4 – Not essential in subchannel.

Note 5 – During the synchronization process of the main modem, the OFF condition of circuit 106 is signalled at all port interfaces.

Note 6 — Circuit 142 is present on all ports of the multiplexer, but may be activated on an individual port basis for individual port tests. All are activated simultaneously for entire modem tests.

14 Optional PCM interface alternative

The recommended data signalling rate is synchronous at 64 kbit/s.

For those synchronous networks requiring the end-to-end transmission of both the 8 kHz and 64 kHz timing together with the data at 64 kbit/s, an internal data signalling rate of 72 kbit/s is suggested.

The corresponding data format shall be obtained by inserting one extra bit (E) just before the first bit of each octet of the 64 kbit/s data stream.

The bits E convey alignment and housekeeping information, according to the pattern shown in Figure 1/V.37.

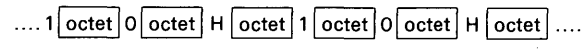


FIGURE 1/V.37

The use of the housekeeping bits H is determined with bilateral agreement between Administrations. When not used these bits should be assigned the value 1. A framing strategy is not specified in this Recommmendation.

When the transmission of the 8 kHz timing is not required, the data signalling rate may be 64 kbit/s.

The interfaces shall comply with the functional requirements given in Recommendation G.703 [4] for the 64 kbit/s interface. The electrical characteristics may comply with reference [5].

If an end-to-end transmission of an 8 kHz timing signal is not used, an 8 kHz timing across the interface will not be supplied nor utilized by the modem.

15 Threshold and response times of circuit 109

15.1 *Threshold*

For a data line signal level greater than −13 dBm0, circuit 109 is ON. For a data line signal level less than −18 dBm0, circuit 109 is OFF.

Note – The corresponding levels for the pilot carrier are −22 dBm0 and −27 dBm0 respectively.

The condition of circuit 109 for levels between the above levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition. To measure the thresholds of the detector, a modulated data signal with its carrier and timing pilots at the levels specified in §§ 6.5 and 6.6 above should be used.

15.2 *Response times*

ON to OFF: 15 to 50 ms.

OFF to ON:

1) For initial equalization, circuit 109 must be ON prior to user data appearing on circuit 104.
2) For re-equalization during data transfer, circuit 109 will be maintained in the ON condition. During this period, circuit 104 may be clamped to the binary 1 condition.
3) After a line signal interruption that lasts more than the ON to OFF response time:
   a) when no new equalization is needed, the exact figure is under study;
   b) when a new equalization is needed, circuit 109 must be ON prior to user data appearing in circuit 104.

The response times of circuit 109 are the time intervals between the appearance or disappearance of the line signal at the reception input terminals of the modem and the occurrence of the corresponding ON or OFF condition on circuit 109.

The line signal level should be within the range from 3 dB above the actual threshold of the line signal detector at reception and the maximum permissible level of the signal at reception.

16 Response times of circuit 106

ON to OFF response time less than or equal to 2 ms

OFF to ON response time less than or equal to 2 ms.

17 Equalizer

An automatic adaptive equalizer shall be provided in the receiver.

The receiver shall incorporate a means of detecting loss of equalization and initiating a synchronizing signal sequence in its associated local transmitter.

The receiver shall incorporate a means of detecting a synchronizing signal sequence from the remote transmitter and initiating a synchronizing signal sequence in its associated local transmitter, which may be initiated at any time during the reception of the synchronizing signal sequence.

Either modem can initiate the synchronizing signal sequence. The synchronizing signal is initiated when the receiver has detected a loss of equalization. Having initiated a synchronizing signal, the modem expects a synchronizing signal from the remote transmitter.

If the modem does not receive a synchronizing signal from the remote transmitter within a time interval equal to the maximum expected two-way propagation delay plus twice the synchronizing signal detection time, it transmits another synchronizing signal.

If the modem fails to synchronize on the received signal sequence, it transmits another synchronizing signal.

If a modem receives a synchronizing signal when it has not initiated a synchronizing signal and the receiver properly synchronizes, it returns only one synchronizing sequence.

18 Additional information for the designer

18.1 *Input level variation*

The step-change in the input level is, under normal conditions, smaller than ± 0.1 dB. The gradual input level change is smaller than ± 6 dB and includes the tolerance of the transmitter output level.

18.2 *Interference from adjacent group bands*

A sinusoidal signal of +10 dBm0 in the frequency bands of 36-60 kHz and 108-132 kHz can appear together with the data line signal at the input of the receiver.

APPENDIX I

(to Recommendation V.37)

Scrambling process

I.1 *Definitions*

I.1.1 **applied data bit**

The data bit which has been applied to the scrambler but has not affected the transmission at the time of consideration.

I.1.2 **next transmitted bit**

The bit which will be transmitted as a result of scrambling the applied data bit.

I.1.3 **earlier transmitted bits**

Those bits which have been transmitted earlier than the next transmitted bit. They are numbered sequentially in reverse time order, i.e. the first earlier transmitted bit is that immediately preceding the next transmitted bit.

I.1.4 **adverse state**

The presence of any one of certain repetitive patterns in the earlier transmitted bits.

I.2 *Scrambling process*

The binary value of the next transmitted bit shall be such as to produce odd parity when considered together with the twentieth and third earlier transmitted bits and the applied data bit unless an adverse state is apparent, in which case the binary value of the next transmitted bit shall be such as to produce even instead of odd parity.

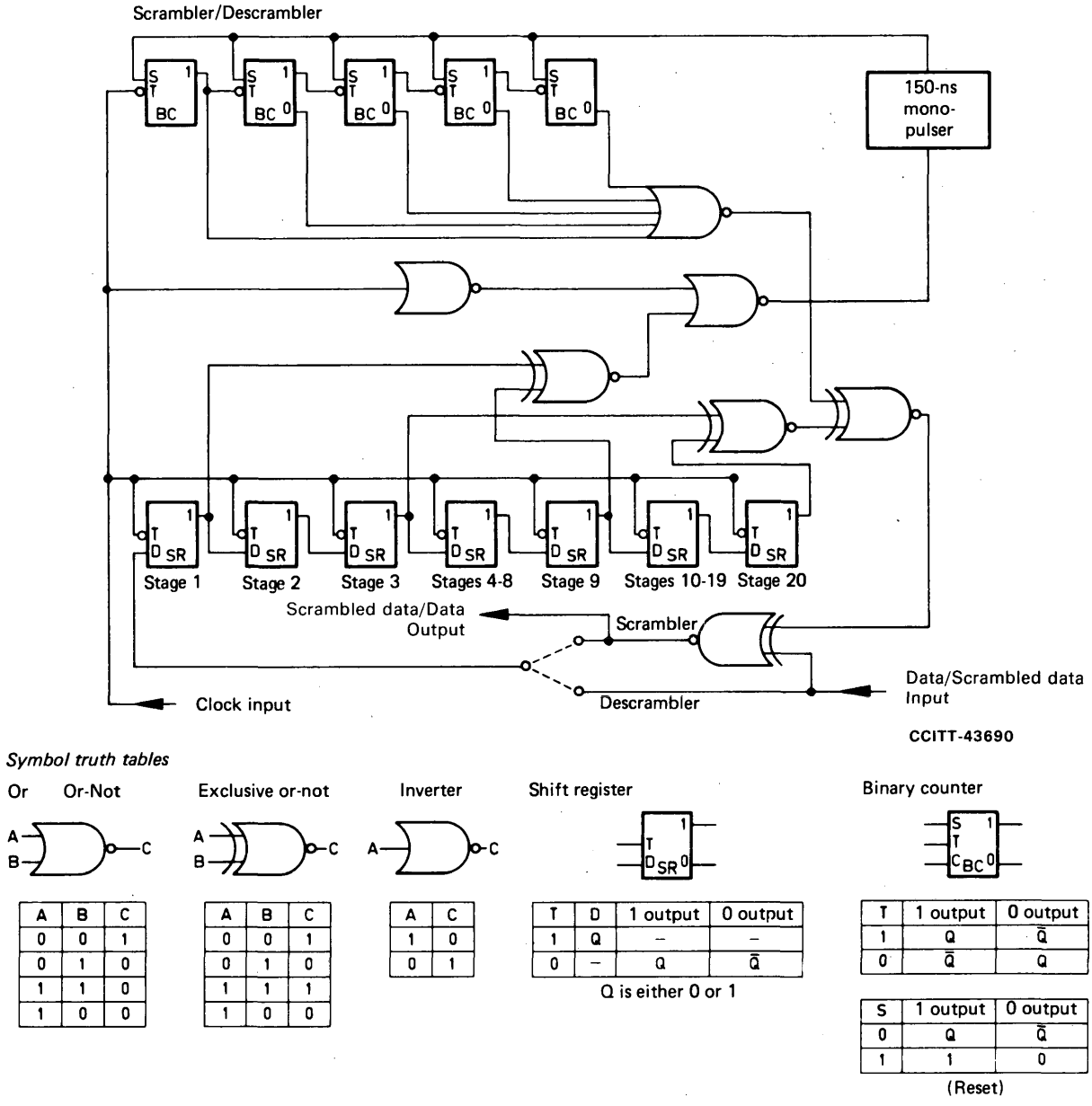
An adverse state shall be apparent only if the binary values of the p^{th} and $(p + 8)^{th}$ earlier transmitted bits have not differed from one another when p represents all the integers from 1 to q inclusive. The value of q shall be such that, for $p = (q + 1)$, the p^{th} and $(p + 8)^{th}$ earlier transmitted bits had opposite binary values and $q = (31 + 32\ r)$, r being 0 or any positive integer.

At the time of commencement, i.e. when no earlier bits have been transmitted, an arbitrary 20-bit pattern may be assumed to represent the earlier transmitted bits. At this time also it may be assumed that the p^{th} and $(p + 8)^{th}$ earlier transmitted bits have had the same binary value when p represents all the integers up to any arbitrary value. Similar assumptions may be made for the descrambling process at commencement.

Note 1 – From this it can be seen that received data cannot necessarily be descrambled correctly until at least 20 bits have been correctly received and any pair of these bits, separated from each other by seven other bits have differed in binary value from one another.

Note 2 – It is not possible to devise a satisfactory test pattern to check the operation of the Adverse State Detector (ASD) because of the large number of possible states in which the 20 state shift register can be at the commencement of testing. For those modems in which it is possible to bypass the scrambler and the descrambler and to strap the scrambler to function as a descrambler, the following method may be used. A 1 : 1 test pattern is transmitted with the ASD of the scrambler bypassed. If the ASD of the descrambler is functioning correctly the descrambled test pattern will contain a single element error every 32 bits, i.e. 180 000 errors per minute for a modem operating at 96 kbit/s indicates that the descrambler is functioning correctly. The operation of the ASD of the scrambler may be checked in a similar manner with the scrambler strapped as a descrambler and the descrambler bypassed.

I.3 Figure I-1/V.37 is given as an indication only, since with another technique this logical arrangement might take another form.



A	B	C
0	0	1
0	1	0
1	1	0
1	0	0

A	B	C
0	0	1
0	1	0
1	1	1
1	0	0

A	C
1	0
0	1

T	D	1 output	0 output
1	Q	–	–
0	–	Q	$\bar{Q}$

T	1 output	0 output
1	Q	$\bar{Q}$
0	$\bar{Q}$	Q

S	1 output	0 output
0	Q	$\bar{Q}$
1	1	0

Note – Negative-going transitions of clocks (i.e. 1 to 0 transitions) coincide with data transitions. This is self-synchronizing.

FIGURE I-1/V.37

An example of scrambler and descrambler circuitry

References

[1] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals*, Vol. III, Fascicle III.4, Rec. H.14, § 2.

[2] CCITT Recommendation *Transmission of wide-spectrum signals (data, facsimile, etc.) on wideband group links*, Vol. III, Fascicle III.4, Rec. H.52.

[3] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals*, Vol. III, Fascicle III.4, Rec. H.14, § 3.

[4] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces*, Vol. III, Fascicle III.3, Rec. G.703, § 1.

[5] *Ibid.*, § 1.2.

SECTION 4

ERROR CONTROL

Recommendation V.40

ERROR INDICATION WITH ELECTROMECHANICAL EQUIPMENT

(Mar del Plata, 1968)

If use is made of a code providing for the introduction into each character signal of an extra unit for the parity check, it is possible with electromechanical equipment to detect errors not only in the transmission channel but also in part of the mechanical translation or transmission equipment.

It might be possible therefore, when an error is detected in a character signal, to arrange for an error indication to be given on the position where the error is found.

This indication could take the form of an extra perforation in the tapes of the perforated tape equipment or a special printout with direct printing equipment.

Such devices would however be either very costly or only partially effective (for example, many character signals of the International Alphabet No. 5 do not correspond to any printout so that for these characters the normal sign cannot be replaced by an "error" sign).

For these reasons, the CCITT *unanimously recommends*

that use of an alarm or error-counting device is the best method if a local indication is required for an error detected in a character signal.

Recommendation V.41

CODE-INDEPENDENT ERROR-CONTROL SYSTEM

(Mar del Plata, 1968, amended at Geneva, 1972)

1 General

This Recommendation is primarily intended for error control when implemented as an intermediate equipment which may be provided either with data terminal equipment or with the data circuit-terminating equipment. The appropriate interfaces are shown in Figures 1/V.41 and 2/V.41. The system is not primarily intended for use with multi-access computing systems. The Recommendation does not exclude the use of any other error-control system that may be better adapted to special needs.

The modems used must provide simultaneous forward and backward channels. The system uses synchronous transmission on the forward channel and asynchronous transmission on the backward channel. When modems to Recommendation V.23 are used with data signalling rates of 1200 or 600 bit/s in the general switched telephone network, Recommendation V.5 applies, the error-control equipment being classed as communication equipment. The margin of the synchronous receiver should be at least ± 45%.

The system employs block transmission of information in fixed units of 240, 480, 960 or 3840[1] bits and is therefore most suited to the transmission of medium or long data messages, but a fast starting procedure is incorporated to improve the transmission efficiency for shorter messages.

Error control is achieved by means of automatic repetition of a block upon request (ARQ) from the data receiver. If storage is provided at the receiver, detected errors can be removed before the system output (clean copy). Storage for at least two data blocks must be provided at the transmitter.

The forward bit stream is divided into blocks each consisting of four service bits, the information bits, and 16 error-detection (or check) bits in that order, the check bits being generated in a cyclic encoder. Thus each block transmitted to line contains 260, 500, 980 or 3860[1] bits.

The system will detect:

a) all odd numbers of errors within a block;

b) any error burst not exceeding 16 bits in length and a large percentage of other error patterns.

Assuming a distribution of errors as recorded in reference [1], the error-rate improvement factor has been indicated by a computer simulation to be of the order of 50 000 for a block size of 260 bits.

The fixed block system employed limits the use of the system to those lines having a loop propagation time not greater than the figures given in Table 1/V.41. Allowances of 40 ms for total modem delay and 50 ms for the detection of the RQ signal have been made.

TABLE 1/V.41

Maximum permissible line loop propagation times (ms)

Block size (bits) \ Data signalling rate (bit/s)	200	600	1200	2400	3600	4800
260	1210	343	127	18	–	–
500	2410	743	327	118	49	14
980	4810	1543	727	318	182	114
3860	19210	6343	3127	1518	982	714

2 Encoding and checking process

The service bits and information bits, taken in conjunction, correspond to the coefficients of a message polynomial having terms from x^{n-1} (n = total number of bits in a block or sequence) down to x^{16}. This polynomial is divided, modulo 2, by the generating polynomial $x^{16} + x^{12} + x^5 + 1$. The check bits correspond to the coefficients of the terms from x^{15} to x^0 in the remainder polynomial found at the completion of this division. The complete block, consisting of the service and information bits followed by the check bits, corresponds to the coefficients of a polynomial which is integrally divisible in modulo 2 fashion by the generating polynomial.

At the transmitter the service bits and information bits are subjected to an encoding process equivalent to a division by the generator polynomial. The resulting remainder is transmitted to line immediately after the information bits, commencing with the highest order bits.

At the receiver, the incoming block is subjected to a decoding process equivalent to a division by the generator polynomial which in the absence of errors will result in a zero remainder. If the division results in other than a zero remainder, errors are indicated.

---

[1] This block length is suitable for circuits provided by means of geostationary orbit satellites.

The above processes may conveniently be carried out by a 16-stage cyclic shift register with appropriate feedback gates (see Figures I-1/V.41 and I-2/V.41) which is set to the all 0 position before starting to process each block; at the receiver the all 0 condition after processing a block indicates error-free reception.

Use of scramblers – Where self-synchronizing scramblers (i.e. scramblers which effectively divide the message polynomial by the scrambler polynomial at the transmitter and multiply the received polynomial by the scrambler polynomial at the receiver) are used, in order to ensure satisfactory performance of the error-detecting system, the scrambler polynomial and the Recommendation V.41 generating polynomial must have no common factors. Where this condition cannot be maintained, the scrambling process must precede the error detection encoding process and the descrambler process must follow the error detection decoding process. Where additive (i.e. non-self-synchronizing) scramblers are used, this precaution need not be observed.

3 The service bits

3.1 *Block sequence indication*

The four service bits at the beginning of each block transmitted to the line indicate the block sequence and convey control information external to the message information. One of these control functions is to ensure that the information block order can be checked during repetitions, thus ensuring that information is not lost, gained or transposed. Three block sequence indicators A, B and C are used cyclically in that order.

Once a sequence indicator has been attached to an information block it remains with that block until the block is received correctly. Examination of the sequence indication is an additional part of the checking process.

3.2 *Allocation of service bits*

The allocation of the 16 possible combinations of the four service bits is given in Tables 2/V.41 and 3/V.41. Table 2/V.41 lists essential and therefore mandatory combinations and Table 3/V.41 optional combinations.

TABLE 2/V.41

Essential combinations

Group	Combination	Function
a	0011	Block A sequence indicator
b	1001	Block B sequence indicator
c	1100	Block C sequence indicator
d	0101	Synchronizing sequence prefix

Note – The digit on the left occurs first.

TABLE 3/V.41

Optional combinations

Group	Combination	Function
e	0110	Hold block
f	1000	End of transmission (this block contains no data)
g	0001	Start of message 1 (five-unit codes)
h	1010	Start of message 2 (six-unit codes)
j	1011	Start of message 3 (seven-unit codes)
k	0010	Start of message 4 (eight-unit codes)
l	0100	End of message (this block contains no data)
m	0111	Data link escape (general control block)
n	1101	To be allocated by bilateral agreement
p	1110	
q	1111	
r	0000	

3.3 *Control functions*

Synchronization is the only essential control function catered for in the service bits.

The optional *Data link escape* (general control) block contains data which are special in some way agreed to by the users.

Additional optional functions are *Start of message 1* (or for five-unit codes), *Start of message 2* (or for six-unit codes), *Start of message 3* (or for seven-unit codes), *Start of message 4* (or for eight-unit codes), *End of message*, and *End of transmission.*

Four additional service bit combinations are available for allocation by bilateral agreement.

The message information part of the non-data blocks (*Hold, End of transmission* and *End of message*) is of no significance, but such blocks will still be checked at the receiver.

When the optional facilities groups g to k are not used, the first data block following the OFF to ON transition of *Ready for sending* is automatically prefixed *Block A sequence indicator, group a.* Data blocks BCABC, etc. then follow sequentially unless one (or more) of the other types of block are inserted.

When the optional facilities groups g to k are used, the first data block is prefixed by one of the *Start of message indicators* 1, 2, 3 or 4 (groups g to k), depending on the number of bits per character which will be used during transmission. Data blocks ABCAB, etc. then follow. Should an interruption to a leased type connection occur during transmission or should an operator interrupt the transmission to change to the speech mode, the transmission will be resumed with the sequence indicator following that of the last block to be accepted before the interruption. A *Start of message* indicator should not be used after such an interruption.

In the case of switched connections, special measures may be necessary to ensure that an interrupted message is not continued by a new message without appropriate indication.

4 Correction procedure

A binary 1 condition on the backward channel (the supervisory channel) indicates the need for repetition of information (RQ). Conversely, a binary 0 implies acceptance of the transmitted information. The rules governing the transmission and reception of these conditions are given in the following and §§ 5 and 6 below.

4.1 *Data transmitter sequence*

Starting and resynchronizing conditions are given in §§ 5 and 6 below, only normal operations being dealt with here.

Data are transmitted block by block, but the contents of each transmitted block together with its service bits are held in store at the transmitter until correct reception has been ensured. Storage for at least two blocks must be provided.

During transmission of a block the condition of the backward channel (circuit 119) is monitored for a period of 45-50 milliseconds immediately prior to transmission of the last check bit. If any RQ is found within this period the block is rendered invalid by inverting this last bit. The transmitter then recommences transmission from the beginning of the previous block by reference to the store. During the retransmission of the block which follows the detection of the RQ signal, the state of the backward channel is ignored.

4.2 *Receiver procedure*

In normal operation a binary 0 is maintained on the backward channel as long as blocks are received with correct check bits and permissible service combinations. Any data contained in these blocks are passed to the receiver output. If a clean copy output is required, data storage for at least one block should be provided since a block cannot be checked until it has been completely received.

When a block has been received which does not meet the error check condition, binary 1 is transmitted on the backward channel and the expected service bit combination is noted in the receiver.

Usually, the first received data block in the repetition cycle having correct check bits also will have an acceptable service bit combination and any data within it will be processed. Occasionally the first block which checks correctly may bear an abnormal service bit combination due to a line transmission error in the backward channel (causing either a mutilated or imitated binary 0 signal). In either case the data in this first block are

discarded. In the case that the block checks correctly but the service bit combination indicates the block preceding the expected block, a binary 0 should be applied to the backward channel.

If the next block checks correctly and bears an acceptable service bit combination, its data should be processed and normal operation resumed. In the case that the service bit combination indicates an invalid block, a binary 1 should be applied; moreover, if the service bit combination indicates the block following the expected block, it is implied that a binary 0 has been imitated for the whole of the 45 ms period specified in § 4.1 above and an alarm must be given since it is not possible to recover from this (rare) condition automatically.

5 Starting procedures

5.1 *Transmitter procedures and synchronizing pattern*

During the delay between *Request to send* and *Ready for sending*, line idle conditions (binary 1) are emitted by the modem. The first data signals, after the modem is ready for sending, are the synchronizing sequence prefix (0101), followed by the synchronizing filler, followed by the synchronizing pattern. The filler may be of any length provided it includes at least 28 transitions and does not include the synchronizing pattern. The synchronizing pattern is 0101000010100101 starting from the left-hand digit (see Appendix I for a possible derivation). The 28 transitions are provided for bit synchronization purposes. These synchronizing signals are followed by *Block A* or a *Start of message* block (groups g to k in Table 3/V.41). During the whole of this sequence from the beginning of the synchronizing prefix the transmitter ignores the condition of the backward channel, acting as though binary 0 were present. The condition of the backward channel then assumes its normal significance (see § 4 above). Should this be binary 1 during the examination period of the second block, this block must be completed with the last bit inverted and the starting procedure must be recommenced from the beginning of the synchronizing sequence prefix.

5.2 *Receiver procedures*

Binary 1 is emitted on the backward channel at the receiving terminal until the synchronizing pattern (0101000010100101) is detected, at which time binary 0 is emitted and block timing is established. The only acceptable service bit combinations to follow the synchronizing pattern are the *Block A* sequence indicator or a *Start of message* indicator (when used). If other service bit combinations are received, binary 1 is returned and the search for the synchronizing pattern is resumed.

6 Resynchronization procedure

6.1 *Recovery of synchronization*

Should the receiver fail to recognize an acceptable block within a reasonable time, then it must examine the incoming bit stream continuously to find the synchronization pattern. When this pattern is found, block timing is re-established and the binary 0 condition applied to the backward channel; the procedure is identical to the starting procedure except that the expected service bit combination is that following the last sequence indicator to have been accepted.

6.2 *Emission of synchronization pattern*

If the normal repetition cycle has continued for a number of times consecutively (typically 4 or 8) the transmitter must assume that resynchronization is necessary. The normal repetition cycle is replaced by a three-block cycle including a synchronization block and the two blocks previously repeated. The synchronization block contains the synchronization sequence prefix, filler and pattern as described in § 5.1 above.

Note – A short filler should result in quicker resynchronization, particularly when long blocks are used. However, the short filler has the disadvantage that correct synchronization can be lost if the prefix is imitated or disturbed by noise or should the synchronization pattern be disturbed. The use of the longer filler, making the block the same length as the data block, overcomes this difficulty. There is the option to choose either length, both lengths being compatible.

6.3 *Use of synchronization block for delay in transmission*

The information flow may be suspended by the insertion of a synchronizing "block". In the case of the short filler it is essential that the receiving terminal should recognize the synchronizing prefix and change itself immediately into the synchronizing search mode, otherwise synchronization will be lost. In the case of the filler

which produces a normal block length it is desirable to change into the search mode without abandoning block timing, a backward binary 0 being returned at the end of the block if the prefix is recognized and the check bits correspond to the synchronization pattern.

It may happen that the transmitter emits a resynchronization cycle before the receiver has changed into the synchronization search condition. The procedure at the receiver is identical to that just described for the use of a synchronization block for suspending the information flow.

7 Interfaces

7.1 *Modem interfaces*

In the normal case where the modems are not an integral part of the data terminal, the modem interfaces are as shown at points A-A in Figures 1/V.41 and 2/V.41. Where synchronous modems are employed, the appropriate signal element timing circuits will also be included in these interfaces.

7.2 *Data terminal interfaces*

Where the error control equipment (including stores) is not an integral part of the data terminal, the error control equipments are interposed between the data terminals and the modem. The data terminal interfaces are then as indicated at B-B and C-C in Figures 1/V.41 and 2/V.41 respectively. A signal element timing circuit is included in each of these interfaces.

7.2.1 In the case of the transmitting terminal all the interchange circuits perform their usual functions but *ready-for-sending* also takes advantage of the final paragraph of its definition in Recommendation V.24 and performs in the following manner:

Ready-for-sending circuit (see Figure 1/V.41)

This circuit, in conjunction with the signal element timing circuit, will inform the data terminal equipment when data are required in response to the *request-to-send* circuit. The *ready-for-sending* circuit will go to the ON condition when data are required and to the OFF condition when data are not required (in general this will be during the service and check bit transmissions and any repetition). This circuit will not go to the ON condition until the *request-to-send* circuit has gone to the ON condition. All transitions of this circuit will coincide with the signal element timing transition from ON to OFF. The transition from ON to OFF will thus coincide with the signal element timing transition from ON to OFF during the 240th, 480th, 960th or 3840th bit of the information within a block, as appropriate.

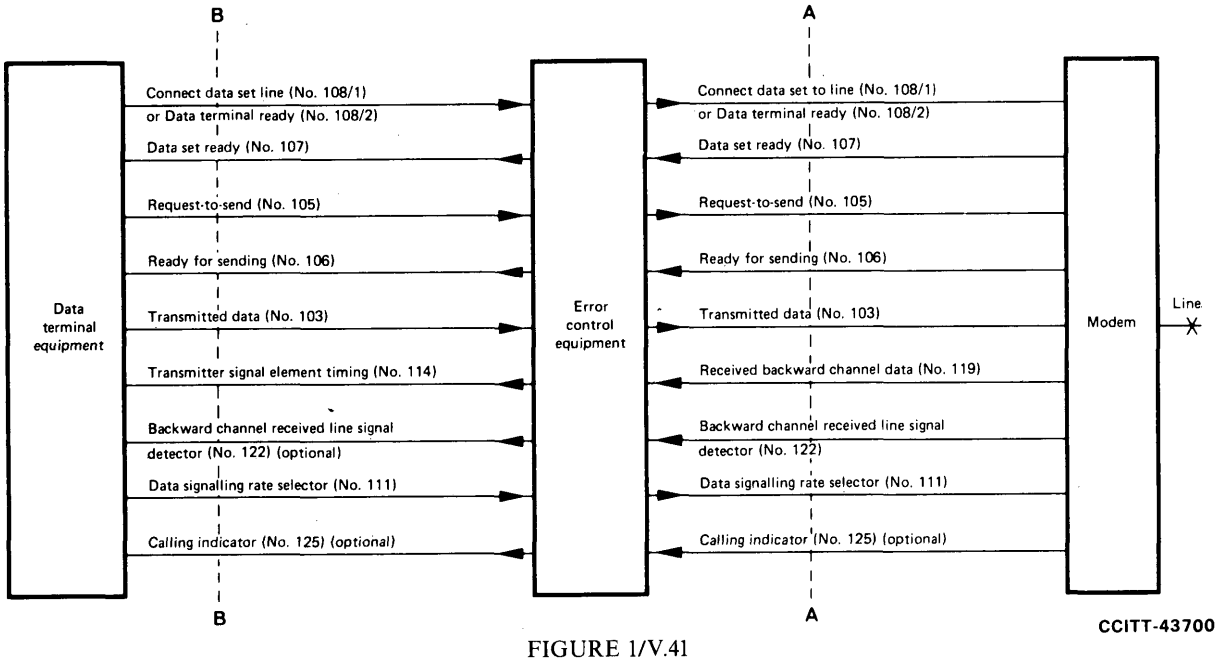


FIGURE 1/V.41

Interchange circuits – Transmitting terminal

7.2.2 In the case of the receiving terminal two new circuits are introduced, but since two (or more) of the modem interface circuits are not used in this interface, the number of circuits is not increased. Circuit 118 – *Transmitted backward channel data* is not available at this interface.

A *Ready for receiving* function must be provided to inform the error control equipment of the status of the data terminal. This function may be performed by circuit 108, in which case a connection on the switched telephone network will be released when the circuit goes from ON to OFF. Alternatively, a separate function control circuit may be provided in order to retain the line connection for short periods when the data terminal is unable to accept data. This new circuit may be assumed to take the place of circuit 120 and functions in the following manner:

Ready-for-receiving (see Figure 2/V.41)

Direction: to error control equipment from data terminal equipment

The data terminal equipment shall maintain the ON condition on this circuit when the data terminal equipment is ready to receive data. Since the error control equipment will receive data in blocks, the data terminal equipment must be capable of receiving data also in blocks. Therefore, the data terminal equipment shall change this circuit to the ON condition only if the data terminal equipment is capable of accepting a block of data (240, 480, 960 or 3840 elements) and shall return to the OFF condition if the data terminal equipment cannot accept another block within 15 element intervals after the end of the previous block of transferred data.

Note – If this *Ready for receiving* circuit is OFF at the end of this 15-element period, an RQ condition will be generated.

The other new circuit performs the function of responding to the ready-for-receiving function and is therefore analogous to circuit 121 – *Backward channel ready.* This new circuit functions as below:

Received-data-present (see Figure 2/V.41)

Direction: from error control equipment to data terminal equipment

This circuit, in conjunction with the signal element timing circuit, will inform the data terminal equipment when data are going to be output in response to the receive data terminal's connect data set to line (and separate *Ready for receiving* circuit when provided) and the incoming data from the distant end being adjudged correct. The *Received data present* circuit will go to the ON condition when data are going to be output and to the OFF condition at all other times. All transitions of this circuit will coincide with the signal element timing transition from ON to OFF. The transition from ON to OFF will thus coincide with the signal element timing transition from ON to OFF during the 240th, 480th, 960th or 3840th bit of information within a block as appropriate.

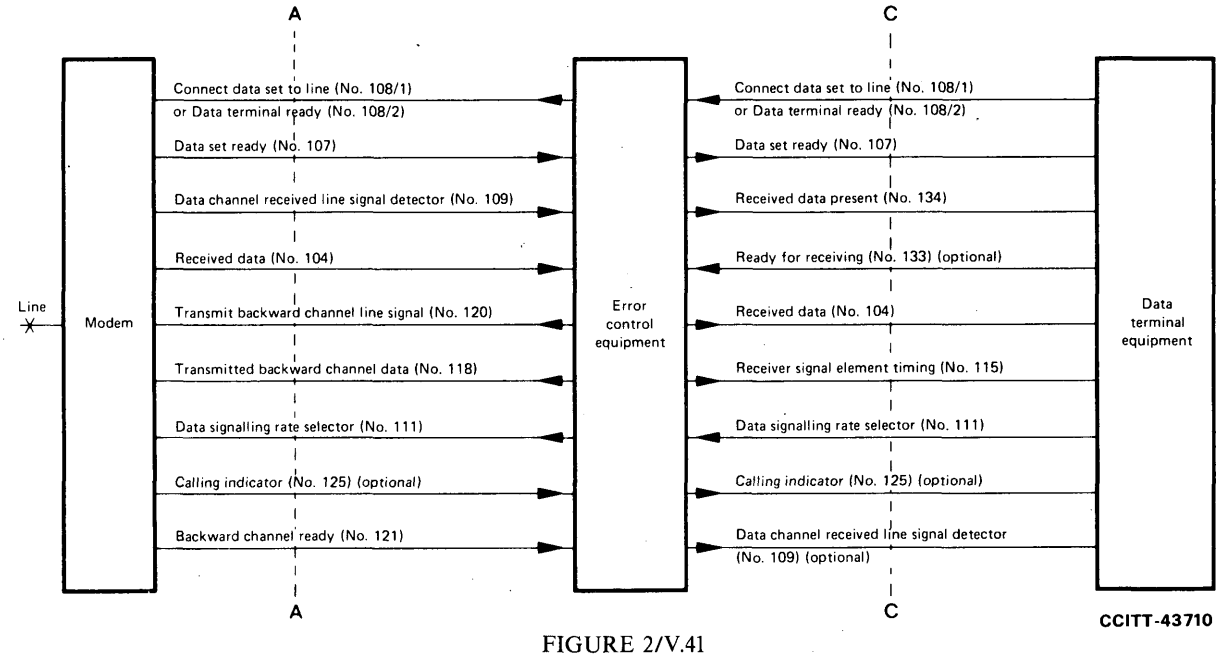


FIGURE 2/V.41

Interchange circuits – Receiving terminal

7.2.3 Additional interchange circuits may be provided at the data terminal interface by bilateral agreement of the users. These additional circuits may be used to introduce service bit control functions other than those provided as a basic necessity. Such circuits should not interfere with the operation of the recommended circuits.

8 Use of service functions

Data link escape is included in Table 3/V.41 as an optional indicator and its use is left to be agreed between operators. It may, for instance, be used to signal to a receiving station that the sending station wishes to speak over the connection. In this case the receiving equipment would operate a bell or similar calling device and transfer the line from the modem to a telephone. Alternatively, it may cause a short message to be printed on a teleprinter for the attention of an operator.

End of transmission is envisaged as giving a positive indication to the receiver that the transmission has ended and that the connection may be released. This is an alternative to the data terminal equipment interpreting the received data to know when to release the connection.

The optional start of message indicators together with the end of message indicator may be used to route messages to different destinations or terminal equipment at the receiving end, which may include the selection of equipment appropriate to the code used.

The hold block need not be used at a transmitter since synchronization sequences may be used as packing between data blocks in the event of data not being ready at the transmitting data terminal equipment, but if required a hold block may be used for this purpose.

APPENDIX I

(to Recommendation V.41)

Encoding and decoding realization for cyclic code system

I.1 *Encoding*

Figure I-1/V.41 shows an arrangement for encoding using the shift register. To encode, the storage stages are set to zero, gates A and B are enabled, gate C is inhibited and k service and information bits are clocked into the input. They will appear simultaneously at the output.

After the bits have been entered, gates A and B are inhibited and gate C is enabled, and the register is clocked a further 16 counts. During these counts the required check bits will appear in succession at the output.

Generation of the synchronizing pattern may be achieved by making $k = 4$, the four bits being 0101. Clocking is suspended for the duration of the synchronizing filler.

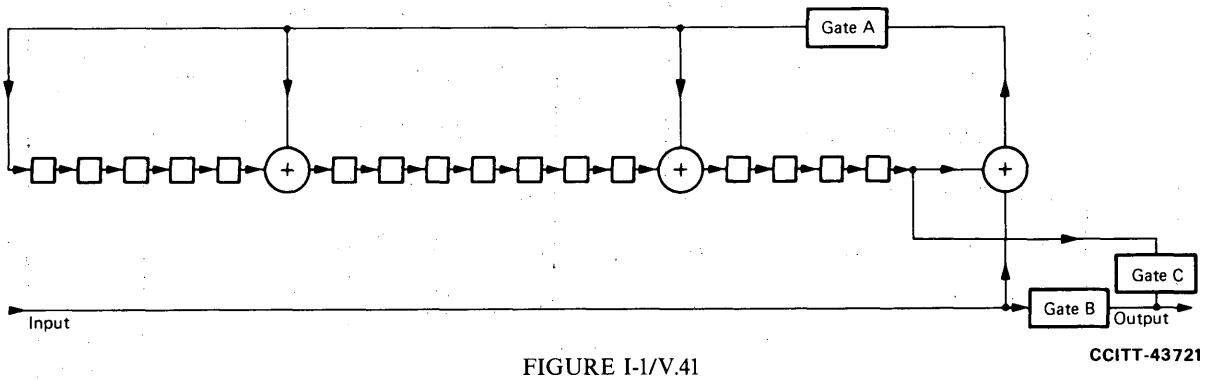


FIGURE I-1/V.41

Encoder

I.2 *Decoding*

Figure I-2/V.41 shows an arrangement for decoding using the shift register. To decode, gates A, B and E are enabled, gate D is inhibited and the storage stages are set to zero.

The *k* information or prefix bits are then clocked into the input and after *k* counts gate B is inhibited, the 16 check bits are then clocked into the input and the contents of the storage stages are then examined. For an error-free block the contents will be zero. A non-zero content indicates an erroneous block.

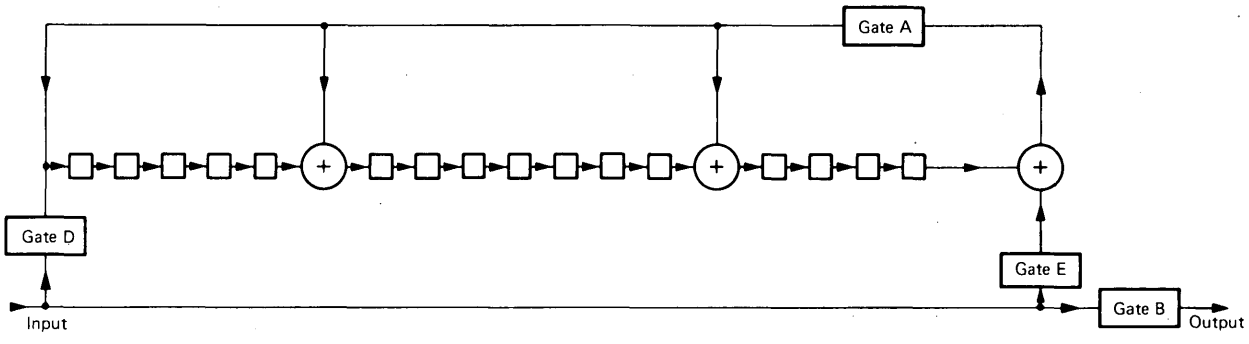


FIGURE I-2/V.41

Decoder

I.3 *Synchronizing at receiver*

For block synchronizing gate D is enabled (Figure I-2/V.41 and gates A, B and E are inhibited and the register is examined in successive bit intervals for the required 16-bit pattern. When the pattern is recognized the register and bit counter are set to zero and decoding proceeds normally.

Reference

[1] *Measurements on switched and leased telephone lines transmitting data at speeds of 250, 800 and 1000 bauds*, Blue Book, Vol. VIII, Supplement No. 22, ITU, Geneva, 1964.

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SECTION 5

TRANSMISSION QUALITY AND MAINTENANCE

Recommendation V.50

STANDARD LIMITS FOR TRANSMISSION QUALITY OF DATA TRANSMISSION

(Mar del Plata, 1968)

One of the most important factors affecting data transmission quality – similarly to telegraph transmission quality – is the distortion in time of the significant instants (known as "telegraph distortion" [1]; the degree of signal distortion must be kept within certain limits, the ultimate objective being that the degree of distortion on received signals should be compatible with the margin of the receiving equipment.

This distortion on received signals arises from the composition of:

a) the sending distortion;

b) the distortion introduced by the transmission channel.

Hence, limits must be fixed for the degree of sending distortion and for the degree of distortion due to the transmission channel.

The limits contemplated for the transmission channel are specified in Recommendation V.53; these limits, which are not yet final, are recalled below:

Channel with modem V.21: 20-25%

Channels with modem V.23:

600 bauds – leased circuits: 20-30%

1200 bauds – leased circuits: 25-35%

600 bauds – switched circuit: 25-30%

1200 bauds – switched circuit: 30-35%

(when this mode of operation is possible)

These figures are expressed provisionally in maximum degrees of individual distortion and apply to the circuit including the modems. The limits for the degree of sending distortion must be fixed so that a reasonable margin is left for the receiving equipment, making allowance for the distortion introduced by the circuit.

In view of the foregoing, the CCITT *unanimously issues the recommendation that*:

1 with regard to the *quality of transmission signals* (signals at point A – Figure 1/V.51), it is preferable, given the wide range of possible modulation rates, to adopt a single standard for each type of modem.

2 when a Recommendation V.21 modem is used, the duration of a unit element should be at least 90% of the duration of the unit element at 200 bauds [i.e. (1/200) × (90/100) second, or 4.5 milliseconds].

3 when a Recommendation V.23 modem is used, the duration of a unit element should be at least 95% of the duration of the unit element either at 1200 bauds [(1/1200) × (95/100) second, or 0.791 millisecond] or at 600 bauds [(1/600) × (95/100) second, or 1.583 millisecond].

4 if a system sends signals of which the sending distortion is systematically well below the limits specified above for the category concerned, the permissible margin for receivers of that system may be reduced.

5 the values indicated above could be revised when a more accurate plan for transmission quality has been drawn up.

Note – The receive margin limits will be studied in liaison with the ISO.

Reference

[1] CCITT Definition: *Telegraph distortion*, Volume X, Fascicle X.1 (Terms and Definitions).

Recommendation V.51

ORGANIZATION OF THE MAINTENANCE OF INTERNATIONAL TELEPHONE-TYPE CIRCUITS USED FOR DATA TRANSMISSION

(Mar del Plata, 1968)

(For the text of this Recommendation, see Recommendation M.729, Volume IV, Fascicle IV.1.)

Recommendation V.52

CHARACTERISTICS OF DISTORTION AND ERROR-RATE MEASURING APPARATUS FOR DATA TRANSMISSION

(Mar del Plata, 1968; amended at Geneva, 1972)

The CCITT,

considering

that distortion and error-rate measurements are of interest in data transmission and that measuring instruments must have compatible characteristics for international inter-operation,

unanimously declares the following view:

1 Modulation rates

1.1 The nominal *modulation rates* of the measuring apparatus to be used in the tests are: 50, 75, 100, 200, 600, 1200, 1800, 2000, 2400, 3000, 3600 and 4800 bauds.

1.2 The accuracy of these rates should in no case deviate from the nominal value by more than ± 0.01%.

1.3 To obtain these rates a time-base external to the instrument may be used.

2 Emission of test signals

2.1 In order to test circuits for data transmission on an international basis it is necessary to standardize the test patterns to be used. Such a pattern should be a pseudo-random one having the following characteristics:

- it should contain all or at least the majority of eight-bit sequences likely to be met in the transmission of actual data;
- it should contain sequences of zeros and ones as long as possible compatible with ease of generation;
- the pattern should be of sufficient length such that at modulation rates higher than 1200 bauds its duration is significant compared with line noise disturbances.

Accordingly a 511-bit test pattern is recommended. The pattern may be generated in a nine-stage shift-register whose fifth and ninth stage outputs are added together in a modulo-two addition stage, and the result is fed back to the input of the first stage. The modulo-two adder would be such that the output produces a 0 output when the two inputs are similar and 1 output when the two outputs are dissimilar.

Table 1/V.52 shows the state of each stage of such register during the transmission of the first 15 bits. The pattern over a longer period is as follows:

111111111000001111011111000101110011100, etc.

It is clear from Table 1/V.52 that this pattern is the sequence of bits in stage 9 of the shift register but it also represents the sequence in any other stage shifted in time. The choice of stage to be connected to the output is therefore a matter of circuit convenience.

2.2 Other test signals recommended are: permanent space, permanent mark, 1 : 1, 3 : 1, 1 : 3, 7 : 1 and 1 : 7, all of which may be sent over the line for an unlimited time.

2.3 A tolerance of ± 1% is the maximum permissible for the transmitter distortion of the test signals.

2.4 The form of signals shall be as prescribed in Recommendation V.28.

3 Synchronization of transmitting with receiving apparatus

The receiving measuring set shall be synchronized with the transitions of the test signals received; these signals to be the recommended 511-bit sequence.

4 Measurement of distortion

4.1 The apparatus should measure the degrees of early and late individual distortion.

4.2 The receiver should measure bias distortion on reversals (1 : 1 signals), with a ± 2% measurement accuracy.

4.3 The tolerance of the measurement of the individual distortion of pseudo-random signals shall be ± 3%.

4.4 The impedence of the receiving apparatus shall be as recommended in Recommendation V.28.

4.5 Provisionally, the margin of the measuring receiver should be measured in terms of the "margin of a synchronous receiver" ([1]), under the following measurement conditions: the signals entering the receiving measuring set shall be those defined in § 2 above, with the transitions in one direction only subject to a delay equal to Δ% of the theoretical duration of a significant unit. The modulation rate may be fixed at the nominal value, and at a value in the range: nominal value ± 0.01%. The receiving measuring set should not indicate any error after the synchronizing period as long as Δ is less than 90%; this applies to both directions of the transitions subject to the delay Δ. Under these conditions the margin of the measuring apparatus shall be said to be over 90%.

5 Measurement of error rate

Both bit error-rate and block error-rate measurements should be possible with the apparatus.

Information on the error rate for sequences of 511 bits should be given in a form similar to that for the bit error rate, the two measurements being made simultaneously.

TABLE 1/V.52

Shift register stages during pseudo-random pattern generation

1	2	3	4	5	6	7	8	9	Output
1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1
1	1	0	0	0	0	0	1	1	1
1	1	1	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0
1	0	1	1	1	1	0	0	0	0
1	1	0	1	1	1	1	0	0	0
1	1	1	0	1	1	1	1	0	0
1	1	1	1	0	1	1	1	1	1

Reference

[1] CCITT Definition: *Margin of a synchronous receiver*, Vol. X, (Terms and Definitions).

LIMITS FOR THE MAINTENANCE OF TELEPHONE-TYPE CIRCUITS USED FOR DATA TRANSMISSION

(Mar del Plata, 1968)

For data transmission maintenance purposes, the following limits are recommended for the essential parameters indicating the quality of a transmission channel.

1 Telegraph distortion limits

Limits for the *degree of distortion on a transmission channel* between the interfaces (i.e. including the modems) vary with the data transmission system. The following values are recommended, these same limits applying to the backward channel:

System with Recommendation V.21 modem:20-25%

Systems with Recommendation V.23 modem:

600 bauds – leased circuits: 20-30%

1200 bauds – leased circuits: 25-35%

600 bauds – switched circuit: 25-30%

1200 bauds – switched circuit: 30-35%

(when this mode of operation is possible).

These figures express provisionally maximum degrees of individual distortion. They will be converted into degrees of isochronous distortion once a method for determining the reference ideal instant has been studied, specifying a synchronization procedure for the distortion-measuring receiver.

2 Limits for error rates

2.1 *Bit error rate*

The limits in Table 1/V.53 are recommended; when they are exceeded the maintenance services should consider the transmission channel defective. The period of measurement is about 15 minutes (more precisely, the period corresponding to the transmission of the total number of sequences which is closest to 15 minutes).

TABLE 1/V.53

Modulation rate (bauds)	Connection	Maximum bit error rate
1200	switched (when possible)	10^{-3}
1200	leased	$5 \cdot 10^{-5}$
600	switched	10^{-3}
600	leased	$5 \cdot 10^{-5}$
200	switched	10^{-4}
200	leased	$5 \cdot 10^{-5}$

Note – These values are not intended for use in planning circuits, but for the information of maintenance services.

2.2 *Block error rate*

Information on the error rate for sequences of 511 bits would be given in a form similar to that for the bit error rate, the two measurements being made simultaneously. However, no limit for the sequence error rate can be recommended for the time being.

Note – To enable Administrations to appreciate the value of sequence error-rate measurement, Table 2/V.53 shows the *maximum and minimum theoretic values* of error rates for sequences of 511 bits corresponding to different values of bit error rate.

These theoretic values do not depend on the modulation rate. For the purposes of this table, a modulation rate of 1200 bauds has been taken as an example.

Modulation rate: 1200 bauds
Period of measurement: 15 minutes = 900 seconds
Number of bits transmitted: 1 080 000
Length of sequence: 511 bits
Number of sequences transmitted: 2113

TABLE 2/V.53

Bit error rate	Number of erroneous bits	Erroneous sequences			
		Maximum number[a]	Maximum rate in %	Minimum number[b]	Minimum rate in %
$2 \cdot 10^{-3}$	2160	2113	100	5	0.24
10^{-3} [c]	1080	1080	51.1	3	0.15
$5 \cdot 10^{-4}$	540	540	25.5	2	0.10
10^{-4}	108	108	5.1	1	0.05
$5 \cdot 10^{-5}$	54	54	2.5	1	0.05

[a] The *maximum* number of erroneous sequences corresponds to a *uniform* distribution of erroneous bits (one bit per sequence).
[b] The *minimum* number of erroneous sequences corresponds to a *grouped* distribution of erroneous bits (sets of 511 bits affecting the sequences).
[c] It will be seen that for a bit error rate of 10^{-3}, the sequence error rate can vary between 0.15% and 51.1%. (This shows the value of sequence error-rate measurement, not only for users, but also for Administrations, which can thus obtain useful information on the causes of bit and sequence error.)

3 Limit of uniform-spectrum random noise

See Recommendation G.153 [1].

4 Limits for impulsive noise

4.1 Bearing in mind the following two points:

- that Recommendation V.2 demands a maximum data signal level of −10 dBm0 for a simplex transmission and −13 dBm0 for duplex transmission,
- that there has been considerable experience of using the threshold −18 dBm0 and −22 dBm0,

the threshold settings should be −18 dBm0 for telephone-type circuits and −21 dBm0 for the special quality circuits mentioned in Recommendation M.1020 [2], the standard measuring instrument (see Recommendation O.71, [3]) being adjustable to thresholds 3 dB apart (see Note 1).

4.2 For counting the number of impulses, the instrument shall be used in the "flat" bandwidth condition (see Note 2).

On a leased circuit, the admissible limit should be 70 impulse counts per hour; but in realizing that error rate measurements are conducted for periods of 15 minutes each, the recommended maintenance limit should be 18 counts in 15 minutes for leased circuits (see Note 3). The measurements should be made during peak hours.

At the time of measurement the line should be terminated at both ends by impedances of 600 ohms. The modem may be used for this purpose if it complies with this impedance.

4.3 For the general switched telephone network, there should be no recommended maintenance limits for impulse counts, but the instrument might be useful as a diagnostic aid at the discretion of the Administrations. This is because the impulse count results taken on any one connection vary considerably with time and even greater differences appear between various connections.

4.4 The correlation between the bit error rate and the number of impulse counts thus determined has not yet been established.

Note 1 – Levels should be expressed in dBm0, because

a) the difference between the various national transmission plans is taken into account, and

b) the level value is related to the value of the data signal level to a close degree.

Note 2 – Owing to lack of experience, no external filter should be used for present maintenance purposes. However, the study of the use of external filters should continue. By means of additional filters the instrument may provide other optional bandwidths (see the Recommendation cited in [4]).

Note 3 – These values are given as an indication. The question of the duration of the measurement and permissible maximum standards for impulsive noise forms the subject of future studies.

References

[1] CCITT Recommendation *Characteristics appropriate to international circuits more than 2500 km in length*, Vol. III, Rec. G.153.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

[3] CCITT Recommendation *Specification for an impulsive noise measuring instrument for telephone-type circuits*, Vol. IV, Rec. O.71.

[4] *Ibid.*, § 3.5.2.

Recommendation V.54

LOOP TEST DEVICES FOR MODEMS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

1 Introduction

The CCITT,

considering

the increasing use being made of data transmission systems, the volume of the information circulating on data transmission networks, the savings to be made by reducing interruption time on such links, the importance of being able to determine responsibilities in maintenance questions for networks, of necessity involving several parties, and the advantages of standardization in this field,

unanimously declares the following:

The locating of faults can be facilitated in many cases by looping procedures in modems. These loops allow local or remote measurements, analogue or digital, to be carried out optionally by the Administrations and/or users concerned.

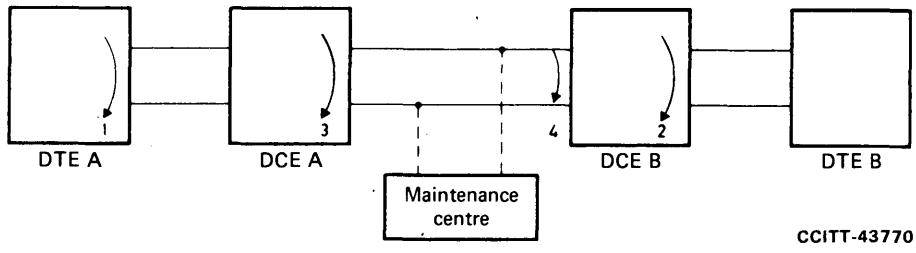
2 Scope

This Recommendation specifies modem loop testing procedures for the following cases:

- for synchronous mode of operation over point-to-point leased circuit, multipoint, tandem and general switched telephone network (GSTN) connections;
- for start-stop mode of operation over point-to-point leased circuit and GSTN connections.

3 Definition of the loops

Four loops are defined (numbered 1 to 4) and their locations as seen from DTE A are shown in Figure 1/V.54. A symmetrical set of four loops could exist as seen from DTE B.



DTE Data terminal equipment
DCE Data circuit-terminating equipment

FIGURE 1/V.54

3.1 *Loop 1*

This loop is used as a basic test on the operation of the DTE, by returning transmitted signals to the DTE for checking. The loop should be set up inside the DTE as close as possible to the interface.

While the DTE is in the loop 1 test condition:

- transmitted data (circuit 103) are connected to received data (circuit 104) within the DTE;
- circuit 108/1 or 108/2 must be in the same condition as it was before the test;
- circuit 105 must be in the OFF condition;
- circuit 125 should continue to be monitored by the DTE so that an incoming call can be given priority over a routine loop test.

Interchange circuit 103 as presented to the DCE must be in the binary 1 condition.

The conditions of the other interchange circuits are not specified but they should if possible permit normal working. The transmitter timing information, in particular if it comes from the DCE, will continue to be sent (see Recommendation V.24, § 4.6.2).

Note – When circuits 108 and 105 are not used by the DTE (for applications on leased lines, for example) the DCE will not be informed of the test condition. This is considered acceptable provided that the remote station is not disturbed.

3.2 *Loop 3*

This is a local loop established in analogue mode as close as possible to the line to check the satisfactory working of the DCE. The loop should include the maximum number of circuits used in normal working (in particular the signal conversion function, if possible) which may in some cases necessitate the inclusion of devices for attenuating signals, for example.

The establishment of the loop presents no difficulty when using a 4-wire line, except in certain cases in which parts of the line equalization system are removed from service.

For certain 2-wire lines the loop may be obtained by simple unbalance of the hybrid transformer.

While the DCE is in the loop 3 test condition:

- the transmission line is suitably terminated, as required by national regulations;
- all interchange circuits are operated normally, except in the case of 2-wire half-duplex operation where the mandatory clamping involving circuits 105 and 109 (as specified in Recommendation V.24, § 4.3.2 a) is disabled;
- circuit 125 should continue to be monitored by the DTE so that an incoming call can be given priority over a routine loop test, after abandoning the loop 3 condition;
- no signal is transmitted to line on the data channel.

Since most interchange circuits operate normally, a diagram of interchange circuit operation sequence is not presented.

Note 1 – In certain switched networks the loop 3 procedure may clear the connection due to national regulations. During the loop 3 condition, however, the DCE must not be switched to the line, if not already connected.

Note 2 – In 4-wire point-to-point connections circuit 105 may be continuously ON. If in such cases synchronous modems are used, no test data should be transmitted until circuits 106, 109 and 142 are in the ON condition.

3.3 *Loop 2*

Loop 2 is designed to permit station A or the network to check the satisfactory working of the line (or part of the line) and of the DCE B. It can only be used with a duplex DCE; the application to the backward channel is left for further study. Pseudo loop 2 may be defined for a half-duplex DCE and will be specified in the Recommendation relating to the DCE concerned.

The establishment of the loop will be effective when the control is applied, regardless of the condition of circuit 108 presented by the DTE associated with the DCE in which the loop is set up.

While the DCE B is in the loop 2 test condition:

- circuit 104 is connected internally in the DCE to circuit 103 (see Note 1);
- circuit 104 to the DTE is maintained in the binary 1 condition;
- circuit 109 is connected internally in the DCE to circuit 105 (see Note 1);
- circuit 109 to the DTE is maintained in the OFF condition;
- circuit 106 to the DTE is maintained in the OFF condition;
- circuit 107 to the DTE is maintained in the OFF condition;
- circuit 115 is connected internally in the DCE to circuit 113 if provided (see Note 1);
- circuit 115 and circuit 114, if provided, to the DTE continue to function.

Note 1 – For the internal DCE connections, the electrical signal characteristics may either be that of the interchange circuits or that of the logic level used inside the DCE.

Note 2 – In certain applications, it may not be desirable to connect circuit 115 to circuit 113. In these cases a flexible buffer between circuits 104 and 103 might be recommended. Alternatively, changes in the transmit clock may be done in a phase-continuous manner.

3.4 *Loop 4*

This loop arrangement is only considered in the case of 4-wire lines. Loop 4 is designed for the maintenance of lines by Administrations using analogue-type measurements. When receiving and transmitting pairs are connected in tandem, such a connection cannot be measured as a data circuit (conformity with a line characteristic curve, for example).

In the loop position the two pairs are disconnected from the DCE and are connected to each other through a symmetrical attenuator designed to prevent any oscillation of the circuit (the loop, therefore, does not include any of the amplifiers and/or distortion correctors used in the DCE). The value of the attenuator will be fixed by each Administration in compliance with Recommendation G.122 [1].

Loop 4 may be established inside the DCE or in a separate unit.

When loop 4 is inside the DCE, and while in the test condition, the DCE presents circuits 107 and 109 to the DTE in the OFF condition and circuit 142 is in the ON condition. When loop 4 is in a separate unit, these conditions are desirable but not mandatory.

4 Loop control

Two (non-exclusive) types of control might be possible on the DCE:

- manual control by a switch on the equipment;
- automatic control through the DCE-DTE interface or upon recognition of a loop initiation signal in the received data.

Manual control would always have priority over automatic control and in particular it should be capable of returning the DCE to the normal operating condition.

Interchange circuit 142 shall be used to inform the DTE of a loop condition in the local DCE, even in the case of manual control (but see Note 3 to Table 1/V.54). To avoid ambiguity in interpretation of circuit 142 only one loop should be established at any one time in the DCE.

4.1 *Manual control*

See Table 1/V.54.

TABLE 1/V.54

Interface signalling for manual control of loops

Loop	Control switch on	Signal to DTE A		Signal to DTE B		Notes
		Circuit 107	Circuit 142	Circuit 107	Circuit 142	
2	DCE B	*)	*)	OFF	ON	Note 1
3	DCE A	ON	ON	*)	*)	Note 2
4	DCE B	*)	*)	OFF	ON	Note 3

*) Not applicable.

Note 1 – Data station A is in the normal operating condition. The loop is established by a switch on DCE B.

Note 2 – In DCE A, the condition of circuit 107 will be determined by the condition of circuit 108. When circuit 108 is not provided on the interface, circuit 107 is ON. The normal case is considered in the table.

Note 3 – When loop 4 is in a unit separate from the DCE, the signals to DTE B are desirable but not mandatory due to the difficulty of implementation. When the loop is implemented within the DCE, loop establishment shall always be possible by a switch on the DCE.

Note 4 – The conditions represented by ON in the table may also activate a visual indicator on the DCE.

4.2 *Automatic control through the DTE/DCE interface* (see Table 2/V.54)

Automatic control through the interface is achieved by using circuit 140, 141 and 142 as defined in Recommendation V.24. Circuit 140 is used to control loop 2 and circuit 141 is used to control loop 3. The turning ON of circuit 142 indicates the test mode is established. If circuit 107 is ON, the associated terminal is concerned and subsequent data transmitted on circuit 103 will be looped back on circuit 104. If circuit 107 is OFF, the associated terminal is not concerned.

Note 1 – Automatic control of loop 4 is considered of no use either locally or in the remote station and therefore is not provided.

Note 2 – As an alternative to activation of loop 3 via circuit 141, it could be activated via the four-phase procedure defined in § 4.2 here.

TABLE 2/V.54

Interface signalling for automatic control of loops

Loop	Control signals from DTE A		Signals to DTE A		Signals to DTE B		Notes
	Circuit 140	Circuit 141	Circuit 107	Circuit 142	Circuit 107	Circuit 142	
2	ON	OFF	ON	ON	OFF	ON	Notes 1 and 2
3	OFF	ON	ON	ON	*)	*)	Note 2

*) Not applicable.

Note 1 – There is a risk of head-on collision of controls from the two ends.
Note 2 – In DCE A, the condition of circuit 107 will be determined by the condition of circuit 108. When circuit 108 is not provided on the interface, circuit 107 is ON. The normal case is considered in the table.

Normally circuit 103 can only be used to transmit data or the test sequence, so long as the conditions of circuits 106, 140, 141 and 142 are as indicated in Table 3/V.54.

TABLE 3/V.54

Circuit 103	Circuit 106	Circuit 140	Circuit 141	Circuit 142
Data	ON	OFF	OFF	OFF
Loop 2 test sequence	ON	ON	OFF	ON
Loop 3 test sequence	ON	OFF	ON	ON

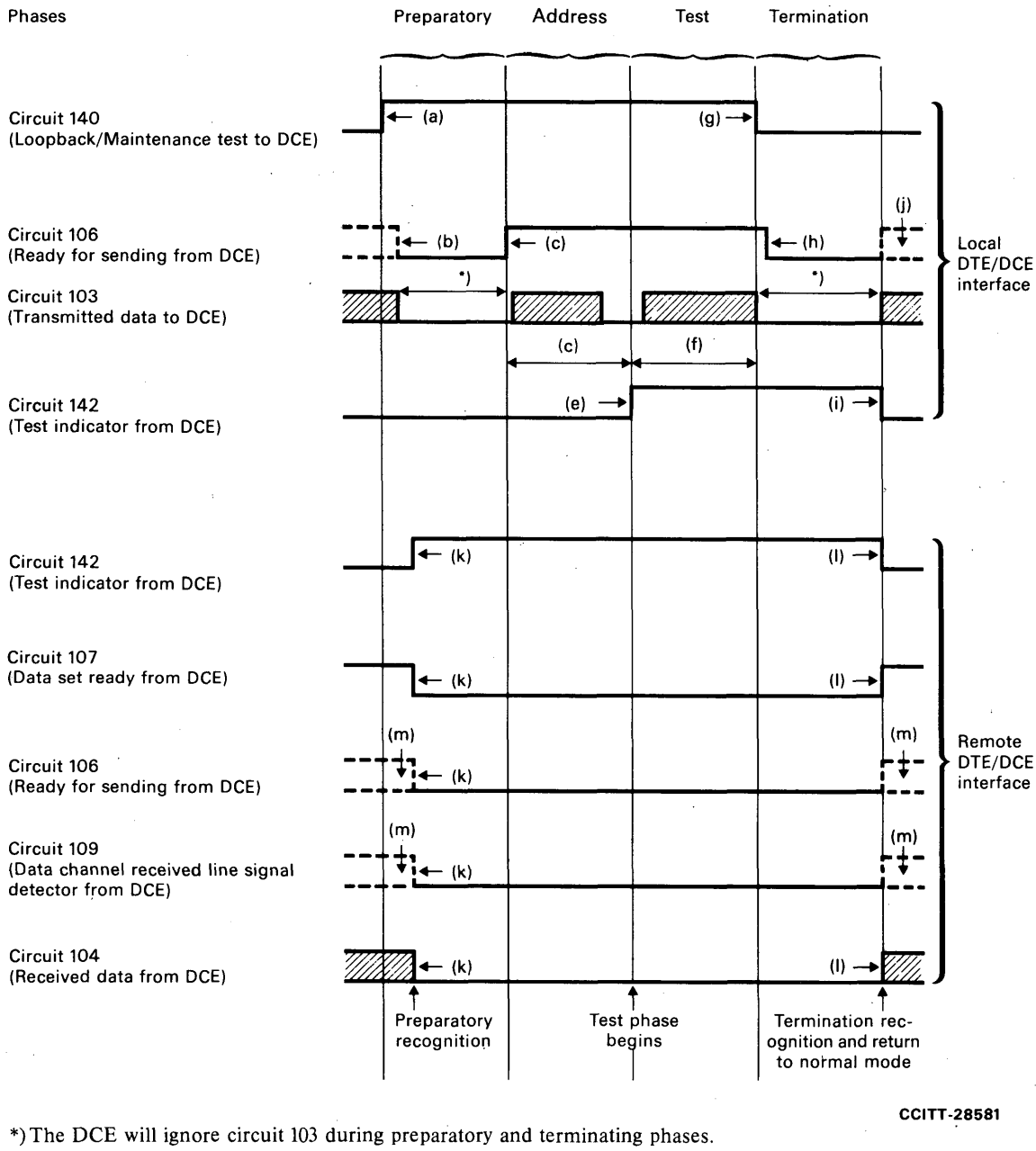
For inter-DCE signalling a four-phase action/reaction sequence should be used. The state of interchange circuits principally involved during this sequence is shown in Figure 2/V.54.

Automatic control with synchronous DCEs is decribed for:

- simple multipoint circuits (see § 5);
- point-to-point duplex circuits (see § 6);
- tadem circuits (see § 7).

Automatic control with asynchronous DCEs is decribed for:

- point-to-point duplex circuits (see § 8).



*) The DCE will ignore circuit 103 during preparatory and terminating phases.

Significant level reference — Binary 0 = ON, Binary 1 = OFF

Note – This sequence may be used for point-to-point duplex circuits. The address phase is not essential for point-to-point applications.

FIGURE 2/V.54

State of interchange circuits during the four-phase action/reaction sequence

Central site

(a) Circuit 140 goes ON (to DCE), requesting a maintenance sequence.

(b) Circuit 106 goes OFF (from DCE), very shortly thereafter, if not already OFF.

(c) Circuit 106 goes ON (from DCE), after a delay, which signifies that the DCE can accept address information.

(d) Circuit 103 is active (to DCE), transmitting the address.

(e) Circuit 142 goes ON (from DCE), after a delay, signifying that the maintenance address has been acted upon and if a loop establishment has been requested, circuit 103 may now be used for the test message.

(f) Circuit 103 is active (to DCE), containing a test message or any other data as required by the maintenance routine being performed.

(g) Circuit 140 goes OFF (to DCE), requesting termination of the maintenance sequence and a return to normal operation.

(h) Circuit 106 goes OFF (from DCE), very shortly thereafter.

(i) Circuit 142 goes OFF (from DCE), after a delay, signifying that the terminating phase is complete and the system is returned to normal operation.

(j) Circuit 106 may be ON or OFF after the maintenance sequence.

During the maintenance the state of circuit 105 would be disregarded.

Remote site

(k) Circuit 142 goes ON (from DCE), indicating test mode to the remote DTE.

Circuit 107 goes OFF. Circuits 106 and 109 go OFF if not already OFF.

Circuit 104 is clamped to binary 1 condition. Before preparatory recognition spurious bits may appear on circuit 104.

(l) Circuit 142 is turned OFF, circuit 107 is turned ON, the clamping of circuit 104 by circuit 142 ON condition is removed, signifying that termination recognition has taken place at the remote DCE, and that it has returned to the normal mode.

(m) Circuits 106 and 109 may be ON or OFF, prior to and after the maintenance sequence.

5 Inter-DCE signalling for simple multipoint circuits with synchronous DCEs

Note 1 – Modems in accordance with Recommendation V.22 are excluded from this procedure.

Note 2 – Considering the fact that there already exist or will exist modems implementing other signalling techniques than the one defined in this Recommendation and that these signalling techniques have been designed according to special conditions formulated by Administrations or users, this Recommendation does not limit the use of such signalling techniques.

A state diagram of the preparatory, address, test and termination phase is shown in Figure A-2/V.54.

5.1 *Preparatory phase*

During the preparatory phase DCE A will transmit a pattern of 2048 ± 100 bits produced by scrambling a binary 0 with the polynominal $1 + x^{-4} + x^{-7}$. No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler. Before transmitting the preparatory pattern, DCE A has to establish a data channel, if not already available.

The criteria for the recognition of this pattern by DCE B are not part of this Recommendation. The criteria that are implemented should offer a very high protection against false recognition due to simulation by user data and some protection against failure to recognize the preparatory pattern due to a high bit error rate. In order to provide protection against false recognition caused by user HDLC frames, the bit sequence consisting of seven consecutive binary 1s, which is at present in the preparatory pattern, must be included in the recognition criteria.

DCE B will start Timer T1 (if implemented) upon recognition of the preparatory phase.

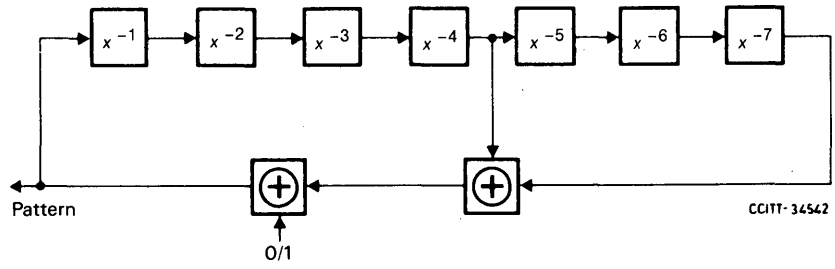


FIGURE 3/V.54

Example of scrambler implementation

5.2 *Address phase*

5.2.1 *Address signalling*

During the address phase the DTE will transmit an address sequence consisting of an address octet that is repeated at least 16 times. The sequence may be preceded and succeeded by other octets as required by the user link level protocol. Synchronous DCEs will transmit these octets in contiguous eight bit groups.

Table 4/V.54 contains a set of possible address octets and the constraints on their use.

TABLE 4/V.54

Single-octet address set

Hexadecimal code	Note	Hexadecimal code	Note	Hexadecimal code	Note
01	1	19	1	37	1
03	2	1B	2	3B	1
05	2	1D	2	3D	1
07	1	1F	1, 4	3F	2, 4
09	2	25	1	55	2
0B	3	27	2	57	1
0D	1	2B	2	5B	1
0F	2	2D	2	5F	2, 4
11	2	2F	1	6F	2
13	1	33	2	77	2
17	2	35	2	7F	1, 4

Note 1 – Odd parity.

Note 2 – Even parity.

Note 3 – Sync (1/6) with odd parity.

Note 4 – Not to be used in ISO 3309 (HDLC) frame structures.

When an extension of the address set is required, a similar set consisting of two-octet addresses can be generated.

Note – The set contained in Table 4/V.54 may be regarded as a subset of the extended set, i.e. one consisting of those two-octet addresses whose two octets are identical.

The DCE will recognize its address when it is detected in at least five contiguous octets received. No octet synchronization is required.

When the DCE detects an address sequence (five identical contiguous octets), not containing its address, it will disable the address detection function, thus avoiding false recognition of its own address due to simulation by subsequent test messages.

5.2.2 *Acknowledgement signalling*

DCE B, upon recognition of the address signal containing its address, will transmit a pattern of 1948 ± 100 bits produced by scrambling a binary 1 with the polynomial $1 + x^{-4} + x^{-7}$. No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler.

Before transmitting the acknowledgement pattern, DCE B has to ensure that the data channel to DCE A is available. Since the loop 2 test is in a synchronous DCE, DCE B will use its receiver signal element timing for this data channel.

The criteria for the recognition of this pattern by DCE A are not part of this Recommendation. The criteria that are implemented should offer good protection against failure to recognize the acknowledgement signal due to a high bit error rate.

DCE B, after transmission of the acknowledgement pattern, will enter the test phase.

DCE A, upon recognition of the acknowledgement pattern, will time out for a 2148 ± 100 bit period and will then turn ON circuit 142, thus entering the test phase.

DCE A, upon recognition of the acknowledgement pattern, will not take any action if it is in the normal data mode.

5.3 *Test phase*

Signals transmitted during the test phase are not specified in this Recommendation.

5.4 *Termination phase*

During the termination phase, DCE A will transmit a pattern of 8192 ± 100 bits produced by scrambling a binary 1 with the polynomial $1 + x^{-4} + x^{-7}$, followed by 64 binary 1s.

No particular starting pattern is specified. Transmission will be at the normal DCE data signalling rate. The pattern will be transmitted as though it were introduced to the DCE via circuit 103. Figure 3/V.54 shows an example of a suitable implementation of the scrambler.

DCE B will terminate the test mode in any of the following situations:

- recognition of the termination pattern;
- carrier loss with a duration longer than 1 s;
- expiration of the optional Timer T1.

The criteria for the recognition of this pattern by DCE B are not part of this Recommendation. The criteria that are implemented should offer good protection against false recognition due to simulation by test data and good protection against failure to recognize the termination pattern due to a high bit error rate.

DCE B will normally leave the termination phase during the reception of the binary 1 pattern that concludes the termination pattern.

DCE B upon recognition of the termination pattern will not take any action if it is in the normal data mode.

Note – The length of the time interval of the optional Timer T1 is not specified in this Recommendation.

6 Simplified inter-DCE signalling for use in point-to-point circuits with synchronous DCEs

For point-to-point circuits which require control of one loop 2 only, the four-phase sequence may be simplified by deleting the address signalling. The procedure is then as follows (see Figure A-3/V.54):

- Preparatory phase: in accordance with § 5.1.
- Address phase: acknowledgement signalling only in accordance with § 5.2.2 upon recognition of the preparatory pattern.
- Test phase: signals transmitted during the test phase are not specified in this Recommendation.
- Termination phase: in accordance with § 5.4.

7 Inter-DCE signalling for tandem circuits with synchronous DCEs

For tandem circuits the four-phase sequence may be used to control the loops shown in Figure 4/V.54.

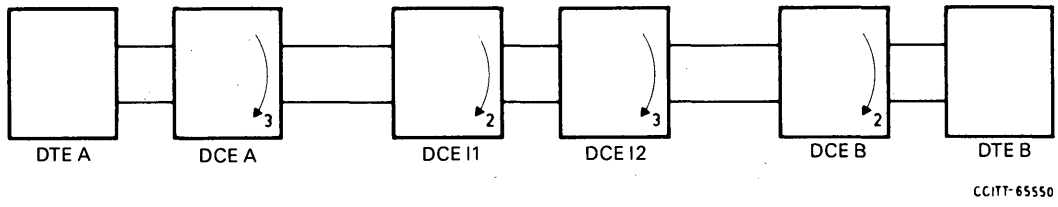
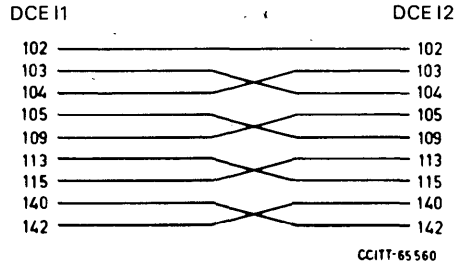


FIGURE 4/V.54

The inter-DCE signalling procedures apply to synchronous modems only, with or without multiplexer features. The interchange circuits of the DCEs at the intermediate site are connected as shown in Figure 5/V.54.



Note 1 - The ON condition on circuit 142 shall not clamp the interchange circuits 107, 109 and 104 in DCE I1.

Note 2 - Signalling the ON condition from circuit 142 to 140 shall not start transmission of the preparatory pattern from DCE I2, but activate the address monitor.

Note 3 - Only those interchange circuits essential for establishing the loops are shown.

FIGURE 5/V.54

A state diagram of the four-phase sequence is shown in Figure A-4/V.54. The procedure is as follows:

- Preparatory phase: in accordance with § 5.1.

  When DCE I1 recognizes the preparatory pattern it will signal this condition via the ON condition on circuit 142 to circuit 140 of DCE I2, which will activate its address monitor.

  The preparatory pattern is transmitted via circuit 103 of DCE I2 to DCE B.
- Address phase: in accordance with § 5.2.
- Test phase: signals transmitted during the test phase are not specified in this Recommendation.
- Termination phase: in accordance with § 5.4.

When a loop has been established in the intermediate site, the part of the link "behind" the loop is in fact inactivated.

When the loop that has been established is a loop 3 in DCE I2, the carrier towards DCE B will be removed from the line. When this condition lasts for more than one second, DCE B will regard the test condition as terminated and return to normal mode (i.e. with data carrier lost). As this situation was preceded by a 142 ON condition, the remote DTE may regard this as a normal situation. When the loop 3 condition in DCE I2 is terminated, which will normally be after the reception of the full termination pattern, the remote DTE will not receive garbled signals after DCE B has recovered the carrier.

When the loop that has been established is a loop 2 in DCE I1 all patterns will pass to DCE B. Thus DCE B will also receive the termination pattern and leave the test mode at the prescribed time. DCE I2 will leave the test mode upon detecting the OFF condition on circuit 140.

Note – When the connection of DCE I1 and DCE I2 is established via a multiplexer without remote signalling capabilities for interchange circuits 109 and 142, DCE I2 may optionally derive the required information from the patterns present on interchange circuit 103.

8 Inter-DCE signalling for point-to-point connections with asynchronous DCEs

For point-to-point duplex circuits with asynchronous DCEs for start-stop operation only, the four-phase sequence may be simplified by deleting the address signalling. Instead of the pseudo-random patterns used for synchronous transmission a simple signalling method shown in Figure 6/V.54 shall be used.

8.1 *Preparatory phase*

During the preparatory phase DCE A will transmit a SPACE-MARK-SPACE pattern. The duration of each interval shall be 320-400 ms.

8.2 *Address phase*

DCE B, upon recognition of the preparatory pattern, will establish loop 2 and transmit the acknowledgement signal consisting of a carrier OFF period of 100-150 ms.

DCE A will turn ON circuit 142 and enter the test phase after it has detected the OFF to ON transition of the carrier signal.

8.3 *Test phase*

Signals transmitted during the test phase are not specified in this Recommendation.

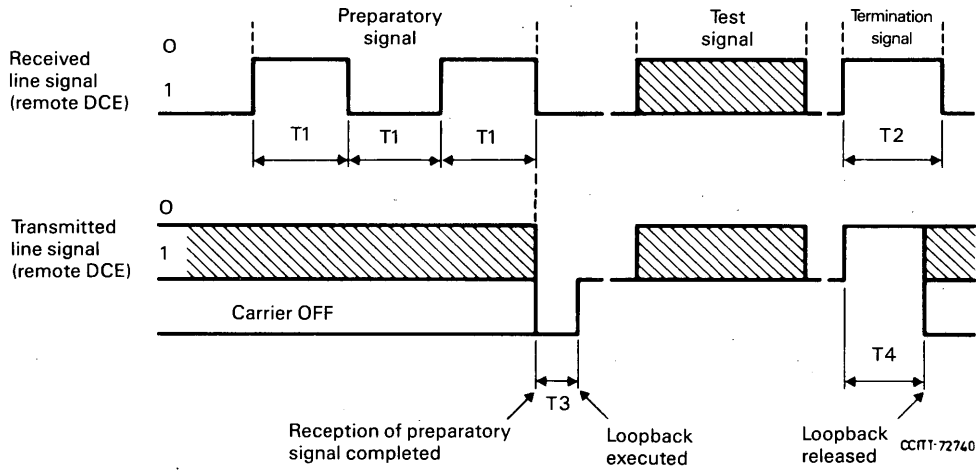
8.4 *Termination phase*

During the termination phase DCE A will transmit a signal consisting of binary 0 (SPACE) for at least 550 ms.

DCE B will terminate the test mode in any of the following situations:

- recognition of the termination signal for 480-550 ms;
- carrier loss with a duration longer than 1s.

DCE B upon recognition of the termination signal will not take any action if it is in the normal data mode.



Time duration
T1 : 320 - 400 ms
T2 : ⩾ 550 ms
T3 : 100 - 150 ms
T4 : 480 - 550 ms

Note 1 - Line signals that are transmitted before reception of preparatory signal is completed, and after loopback is released, depend upon the data signals transmitted by the DTE on circuit 103.

Note 2 - Binary 0 (SPACE) and binary 1 (MARK) correspond to the frequencies F_A and F_Z respectively.

FIGURE 6/V.54

Loop 2 signalling method in asynchronous modems

ANNEX A

(to Recommendation V.54)

State diagrams

A.1 *Introduction*

Procedures as outlined in §§ 5, 6 and 7 of Recommendation V.54 are further explained in this Annex by means of state diagrams.

In order to facilitate understanding of these diagrams the following information is provided.

A.2 *Location*

The loop device is considered to be functionally located between the DTE and the remaining part of the DCE.

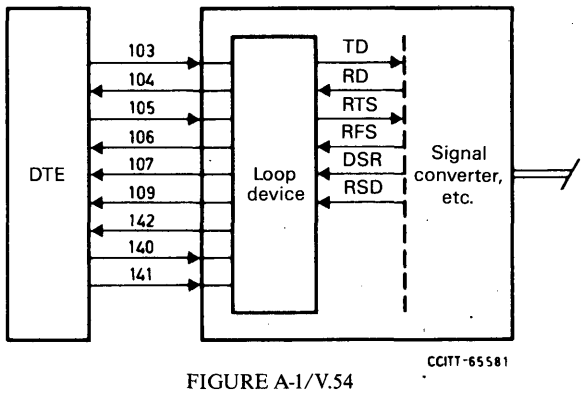


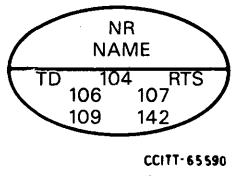
FIGURE A-1/V.54

During the data phase (i.e. no test loops applied), the following relations exist:

TD	(transmitted data)	= 103;
RD	(received data)	= 104;
RTS	(request to send)	= 105;
RFS	(ready for sending)	= 106;
DSR	(data set ready)	= 107;
RSD	(data channel received line signal detector)	= 109.

A.3 *Legend*

A.3.1 *States*



NR	State Number, with:
	LC = Loop Condition
	TL = Timing Loop;
NAME	State name;
TD	Signal on circuit TD to signal converter;
104	Signal on circuit 104 to DTE;
RTS	Signal on circuit RTS to signal converter;
106	Signal on circuit 106 to DTE;
107	Signal on circuit 107 to DTE;
109	Signal on circuit 109 to DTE;
142	Signal on circuit 142 to DTE.

A.3.2 *Signals*

"1" Steady binary one;

OFF Continuous OFF (="1");

ON Continuous ON (="0");

PREP Preparatory pattern;

ACK Acknowledgement pattern;

TERM Termination pattern;

103 Follows circuit 103 from DTE;

RD Follows circuit RD from signal converter;

105 Follows circuit 105 from DTE;

RFS Follows circuit RFS from signal converter;

DSR Follows circuit DSR from signal converter;

RSD Follows circuit RSD from signal converter.

A.3.3 *Events*

14n ON OFF to ON transition on circuit 14n;

14n OFF ON to OFF transition on circuit 14n;

Peripheral Valid in peripheral DCE;

intermed. Valid in intermediate DCE;

nnnn After nnnn bit intervals;

XXX rec. Recognition of pattern XXX;

Own address Recognition of unique DCE address sequence;

Other address Recognition of other address sequence;

RSD OFF 1s Circuit RSD OFF for 1 second.

A.4 *Examples*

In the lower half of the state symbols, the condition of all interchange circuits that originate in the loop device are given in the order:

- TD (to signal converter);
- 104 (to DTE);
- RTS (to signal converter);
- 106 (to DTE);
- 107 (to DTE);
- 109 (to DTE); and
- 142 (to DTE).

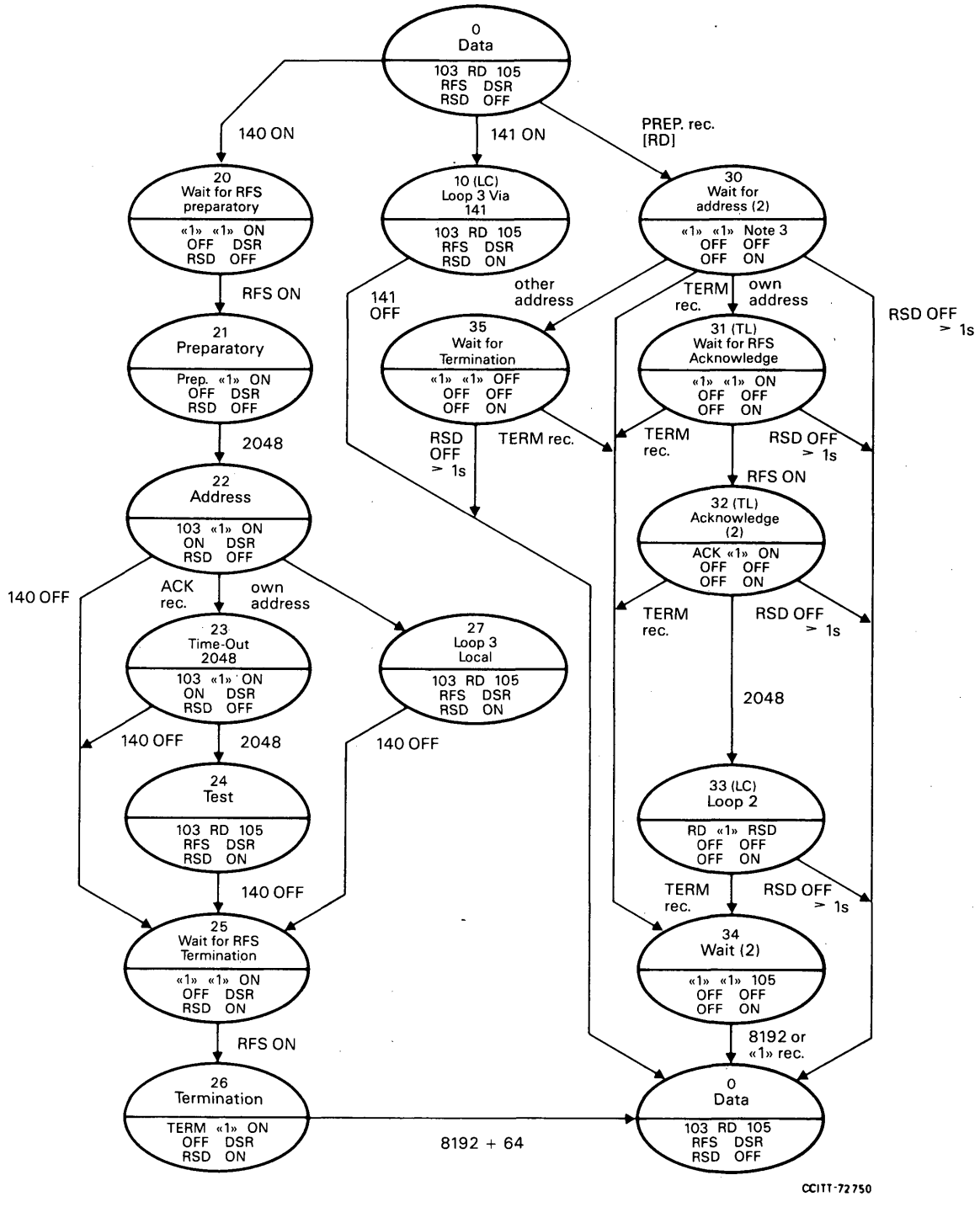
For example:

"RD" in the first position means that circuit TD to the signal converter is connected inside the loop device to RD from the signal converter.

"ACK" in the second position means that the acknowledgement pattern is transmitted on circuit 104.

"OFF" in the third position means that circuit RTS to the signal converter is kept in the OFF condition.

"RFS" in the fourth position means that circuit 106 to the DTE follows circuit RFS from the signal converter.



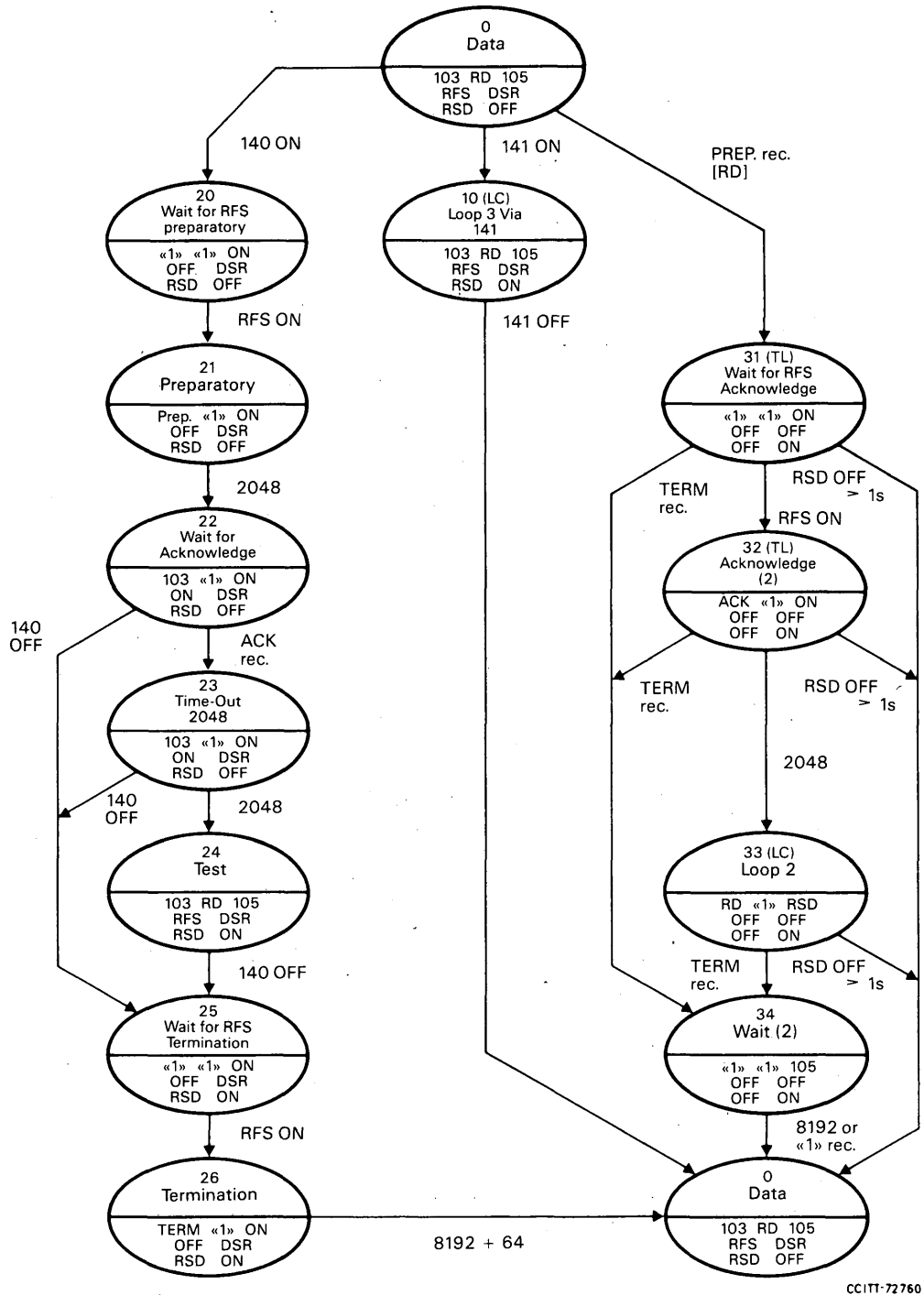
Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 30.

Note 3 - The condition of circuit RTS in state 30 may depend on the actual configuration. Normally circuit RTS will remain unchanged when moving from state 0 to state 30.

FIGURE A-2/V.54

State diagram for simple multipoint circuits

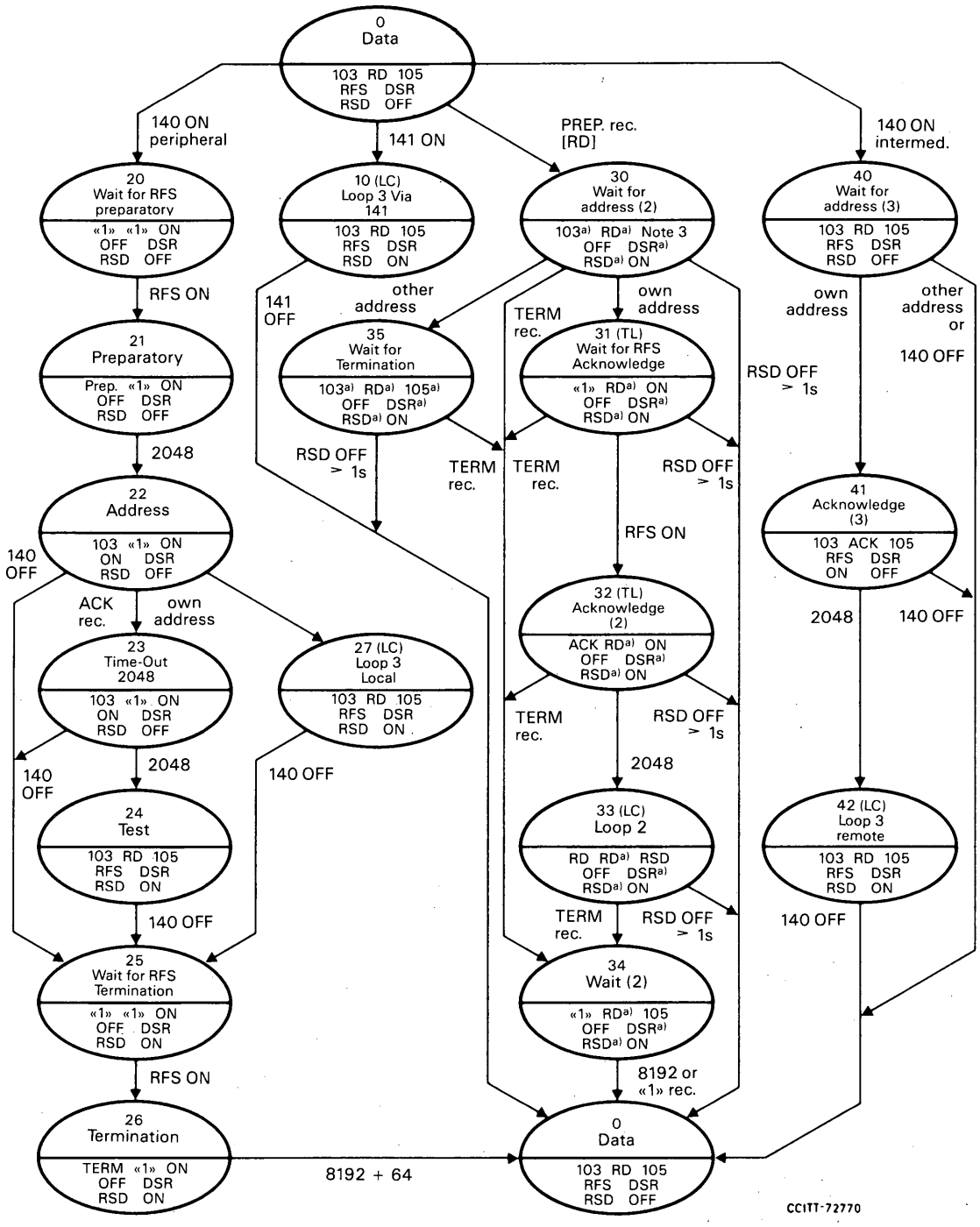


Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 31.

FIGURE A-3/V.54

State diagram for point-to-point circuits



a) Not clamped in intermediate DCE; clamped («1» or OFF) in peripheral DCE.

Note 1 - In the event of a momentary ON condition of circuit 140, a complete preparatory pattern followed by a complete termination pattern is transmitted.

Note 2 - In case the optional timer T1 is implemented, read «RSD OFF > 1s or T1 expired» instead of «RSD OFF > 1s». T1 is started in state 30.

Note 3 - The condition of circuit RTS in state 30 may depend on the actual configuration. Normally circuit RTS will remain unchanged when moving from state 0 to state 30.

Note 4 - Where interconnection of circuit 109 in DCE I1 to circuit 105 in DCE I2 is possible, during Loop 2 the same condition as in peripheral DCE B is permitted on the interface.

FIGURE A-4/V.54

State diagram for tandem circuits

Reference

[1] CCITT Recommendation *Influence of national systems on stability, talker echo and listener echo in international connections*, Vol. III, Rec. G.122.

Recommendation V.55

SPECIFICATION FOR AN IMPULSIVE NOISE MEASURING INSTRUMENT FOR TELEPHONE-TYPE CIRCUITS

(For the text of this Recommendation, see Recommendation O.71, Volume IV, Fascicle IV.4.)

Recommendation V.56

COMPARATIVE TESTS OF MODEMS FOR USE OVER TELEPHONE-TYPE CIRCUITS

(Geneva, 1972; amended at Geneva, 1976 and 1980, Malaga-Torremolinos, 1984)

To facilitate the work of Administrations in making comparative tests of modems for use over telephone-type circuits offered by different manufacturers, it is recommended that the tests should be made in the laboratory under the following operating conditions:

1 List of test parameters (see Table 1/V.56)

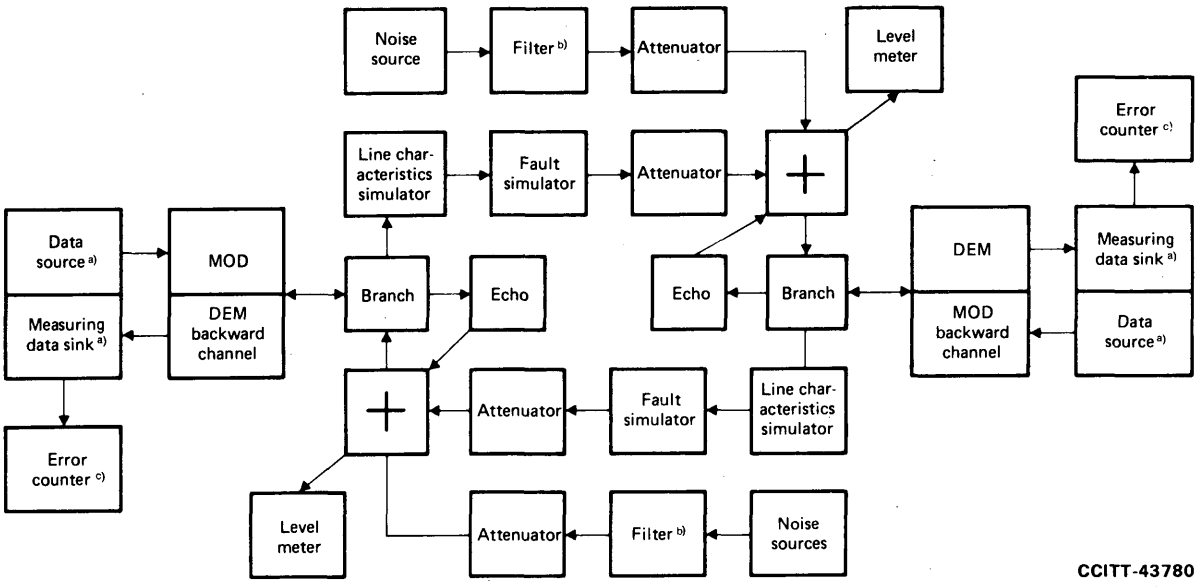
TABLE 1/V.56

Test parameters

Ref. No.	Parameter	Four-wire point-to-point	Two-wire switched network	
			Serial modems	Parallel modems
1	Total attenuation or receiving signal level	X	X	
2	Attenuation distortion	X	X	
3	Envelope or group delay distortion	X	X	
4	Frequency shift (or offset)	X	X	
5	Sudden changes of attenuation	X	X	
6	Interruptions	X	X	
7	Phase hits	X	X	
8	Phase jitter	X	X	
9	Harmonic distortion	X	X	X
10	Listener echo		X	
11	"White" noise	X	X	
12	Impulsive noise	X	X	
13	Single tone interference		X	

2 Block diagram for standard test measuring set-up

It is proposed that comparative tests be made using either all or parts of the measuring set-up shown in Figure 1/V.56.



a) 511-bit pseudo random text.
b) 300-3400-Hz band pass filter; the filter is left out if impulsive noise in the form of a square wave is used.
c) For bit and block error count, see Recommendation V.52.

FIGURE 1/V.56

Measuring set-up for the standard tests of modems

3 Test parameters

3.1 *Parameters of the line characteristics simulator*

3.1.1 *Symmetric line distortion*

See Tables 2/V.56 and 3/V.56. The tolerances for all values are ± 5%.

TABLE 2/V.56

Frequency (Hz)	Attenuation distortion (dB)		
	Mode 1 (see Note 1)	Mode 2 (see Note 2)	Mode 3 (see Note 5)
300	6	12	K_1 b)
500	3	8	0.35 K_1
800	1	2 a)	0
≈ 1600	0	0	0
2500	Unspecified	8	0.2 K_1
2800	3	Unspecified	0.3 K_1
3000	6	12	0.4 K_1

a) To be clarified.

b) K_1 is a multiplier with values 1, 2, 3, 4, 5, 6 and 7.

TABLE 3/V.56

Frequency (Hz)	Group-delay distortion (ms)		
	Mode 1 (see Note 1)	Mode 2 (see Note 2)	Mode 3 (see Note 5)
500	3	4.5	1.20 K_1 [a]
600	1.5	3	0.90 K_1
1000	0.5	1.5	0.32 K_1
≈ 1800	0	0	0
2600	0.5	1.5	0.12 K_1
2800	3	3	0.23 K_1
2900	Unspecified	4	0.31 K_1
3000	Unspecified	Unspecified	0.40 K_1

[a] K_1 is a multiplier with values 1, 2, 3, 4, 5, 6 and 7.

3.1.2 *Asymmetric line distortion*

See Tables 4/V.56 and 5/V.56. The tolerances for all values are ± 5%.

TABLE 4/V.56

Frequency (Hz)	Attenuation distortion (dB)		
	Mode 1 (see Note 1)	Mode 2 (see Note 2)	Mode 3 (see Note 5)
800	0	0	0
2000	0.75	Unspecified	Unspecified
2500	Unspecified	8	8 K_2[a]
2800	3	Unspecified	Unspecified
3000	6	12	12 K_2

[a] K_2 is a multiplier with values 0.4, 0.8, 1.2 and 1.6.

TABLE 5/V.56

Frequency (Hz)	Group-delay distortion (ms)		
	Mode 1 (see Note 1)	Mode 2 (see Note 2)	Mode 3 (see Note 5)
500	0	0	0
1900	Unspecified	Unspecified	0.075
2600	0.5	1.5	Unspecified
2800	3	3	0.225 K_3[a]
2900	Unspecified	4	Unspecified
3000	Unspecified	Unspecified	0.30 K_3

[a] K_3 is a multiplier with values 0.5, 1, 2, 4 and 8. All values of Mode 3 are provisional.

3.1.3 *Ripple distortion*

The ripple distortion is within the tolerance scheme of Recommendation M.1020 [1]. See Tables 6/V.56 and 7/V.56. The tolerances for all values are ± 5% ± 0.1 ms.

TABLE 6/V.56

Frequency (Hz)	Group-delay distortion (ms)
	Mode 1
500	2.0
600	1.3
1000	0 (see Note 3)
1400	0.5 (see Note 4)
1800	0 (see Note 3)
2200	0.5 (see Note 4)
2600	0.3 (see Note 3)
2800	2.0

TABLE 7/V.56

Frequency (Hz)	Group-delay distortion (ms)
	Mode 2
500	2.0
600	0.8
800	0.8 (see Note 4)
1000	0 (see Note 3)
1200	0.5 (see Note 4)
1400	0 (see Note 3)
1600	0.5 (see Note 4)
1800	0 (see Note 3)
2000	0.5 (see Note 4)
2200	0 (see Note 3)
2400	0.5 (see Note 4)
2600	0.3 (see Note 3)
2800	2.0

Notes to Tables 2/V.56 to 7/V.56

Note 1 – Mode 1 is in conformity with Recommendation M.1020 [1].

Note 2 – Mode 2 is in conformity with Recommendation M.1025 [2].

Note 3 – Ripple valley values (minima).

Note 4 – Ripple peak values (maxima).

Note 5 – Mode 3 is in conformity with the relevant European specifications.

3.2 *Parameters of the fault simulator*

a) Phase hits: with external control of timing (e.g. 0.25; 1; 100 Hz) adjustable continuously or in steps up to 165 degrees.

b) Frequency shifts e.g. ± 5 Hz, ± 6 Hz or ± 10 Hz by means of channel converters.

c) Peak-to-peak phase jitter from 0.2 degree to 30 degrees continuously from 50 to 300 Hz, sinusoidal waveform.

d) Sudden changes of attenuation: with external control of timing (e.g. 0.1; 0.25; 1; 100 Hz) adjustable continuously or in steps up to total attenuation.

e) Interruptions: with fixed duration of 1 ms and repetition period of 1s and/or with single interruptions with variable duration.

3.3 *Noise sources* (this subject needs further study)

a) White noise.

b) Impulsive noise: with adjustable level and adjustable pulse duration between 100 µs and 1 ms and with repetition period of 1 second.

c) Statistically distributed noise by recording or by simulation which is information to assist in standardizing a "Random noise simulator" which would encourage the utilization of block error counts.

d) Single tone interference: with adjustable level of an additional signal frequency, variable between 300 and 3100 Hz.

e) Harmonic distortion:

i) using a calibrating signal frequency of 700 Hz with the same r.m.s. level as the data signal and with its adjustable harmonic levels: a_{H2}, a_{H3} and a_{H4}, and

ii) using a calibrating signal frequency of 700 Hz with the same peak-to-peak level as the data signal and with its adjustable harmonic levels: a_{H2}, a_{H3} and a_{H4}.

3.4 *Listener echo*

Listener echo: with the variable echo attenuation between 0 and 20 dB and variable echo time delay τ_E between 0 and 20 ms (worst case relevant).

4 Measuring procedure

4.1 *Measurement of the bit error rate* (p_S) *as a function of the signal-to-noise ratio* (S/N) *in the case of white noise*

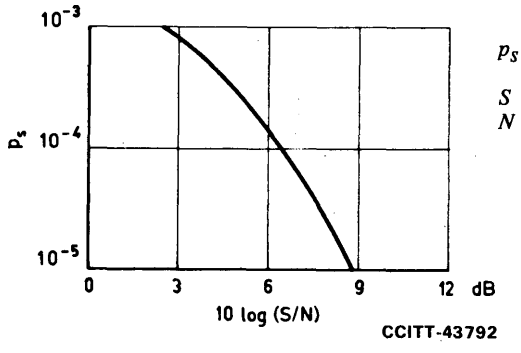
The receiving level at the summation point should be −30 dBm for switched line comparisons and −20 dBm for leased line comparisons.

For a comparison, the value of S/N ratio at defined p_S values can be ascertained (e.g. $3 \cdot 10^{-4}$ or 10^{-5}).

4.2 *Measurement of the number of the bit error per second* (F/t) *as a function of the different faults and noise parameters* (X)

The receiving level at the summation point should be −30 dBm for switched line comparisons and −20 dBm for leased line comparisons.

For a comparison, the value of F/t for different defined fault and noise parameters, or the value of the different parameters at the limit of the error-free region, can be ascertained.

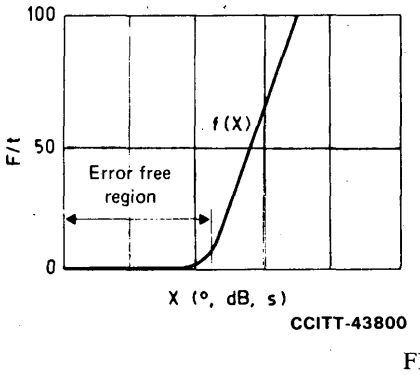


$p_S = f(S/N) = \frac{\text{error bits}}{\text{transmitted bits}}$

S = signal level
N = noise level

FIGURE 2/V.56

Example of bit error rate as a function of the signal-to-noise ratio



$F/t = f(X)$

X = $\Phi_S, \Phi_j, a_S, t_i, a_p, a_t, a_H$

Φ_S = f(degree of the phase hits)
Φ_j = degree of phase jitter
a_S = relative level of the sudden changes of attenuation
t_i = duration of interruptions
a_p = impulsive noise level (dBm)
a_t = single tone level (dBm)
$a_{H_2}, a_{H_3}, a_{H_4}$ = level of the harmonics below H_1 (dB)

FIGURE 3/V.56

Example of bit error per second as a function of the value of different fault and noise parameters

5 Comparative tests of modems (Table 8/V.56)

TABLE 8/V.56

Eighteen selected tests according to §§ 1, 2, 3 and 4

Test	Test parameters according to Table 1/V.56	Test parameters according to §	Measuring procedure according to §
A	11	3.3a)	4.1
B	2, 3, 11	3.1.1 mode 1, 3.3a)	4.1
C	2, 3, 11	3.1.1 mode 2, 3.3a)	4.1
D	2, 3, 11	3.1.2 mode 1, 3.3a)	4.1
E	2, 3, 11	3.1.2 mode 2, 3.3a)	4.1
F	2, 3, 4, 11	3.1.1 mode 1, 3.2b) (± 6 Hz), 3.3a)	4.1
G	2, 3, 4, 11	3.1.1 mode 2, 3.2b) (± 10 Hz), 3.3a)	4.1
H	2, 3, 7	3.1.1 mode 1, 3.2a)	4.2
J	2, 3, 7	3.1.1 mode 2, 3.2a)	4.2
K	8	3.2c)	4.2
L	2, 3, 5	3.1.1 mode 1, 3.2d)	4.2
M	2, 3, 5	3.1.1 mode 2, 3.2d)	4.2
N	6	3.2e)	4.2
P	12	3.3b)	4.2
R	13	3.3d)	4.2
S	9	3.3e) ii)	4.1
T	10, 11	3.4, 3.3a)	4.1
U	Statistic noise	3.3c)	4.1 (for block errors)

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning*, Vol. IV, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with basic bandwidth conditioning*, Vol. IV, Rec. M.1025.

COMPREHENSIVE DATA TEST SET FOR HIGH DATA SIGNALLING RATES

(Geneva, 1972; amended at Geneva, 1980, Malaga-Torremolinos, 1984)

The CCITT,

considering

that the characteristics for measuring instruments recommended in Recommendation V.52 are not suitable for use with modems conforming to Recommendations for group band modems and that error rate measurements, and in some cases distortion measurements, are of interest in data transmission when these modems are used,

unanimously declares the view that

for tests at high data signalling rates the following provisions shall apply:

1 Data signalling rates

1.1 The nominal data signalling rates of the measuring apparatus shall be 20 400, 24 000, 40 800, 48 000, 56 000, 64 000, 72 000, 96 000, 112 000, 128 000, 144 000 and 168 000 bit/s.

1.2 The accuracy of these rates shall be ± 0.002% if timing is not derived from the modem under test or that recommended in the Recommendations for group band modems if timing is derived from the modem under test.

1.3 To obtain these rates a time-base external to the instrument may be used. To accommodate higher rates, which may be standardized in the future, it should be possible for error measurements to be made at rates up to 2 Mbit/s using timing derived from the system under test.

2 Emission of test signals

2.1 In order to test circuits for data transmission on an international basis it is necessary to standardize the test patterns to be used. The test signals recommended are those recommended in Recommendation V.52 plus an additional pseudo-random pattern which should have the following characteristics:

- it contains the majority of bit sequences likely to be met in the transmission of actual data;
- it contains long sequences of zeros and ones compatible with ease of generation;
- it has the possibility of generating the pattern as a line signal with the coder of a group band modem by applying a steady state, binary 1, to its input.

2.2 A tolerance of ± 1% is the maximum permissible for the "transmitter distortion" [1] of the test signals.

2.3 The form of the signals shall be as prescribed in the Recommendations for group band modems.

Accordingly a 1 048 575-bit test pattern is recommended. This pattern may be generated in a 20-stage shift register of which the 20th and 3rd stage outputs are modulo-two added together and fed back to the input of the first stage.

Note – For bit error rate measurements on 64 kbit/s digital circuits, an alternative test pattern of length $2^{11}-1 = 2047$ bits may be used.

3 Synchronization of the receiving measuring apparatus

Two modes shall be possible:

a) Synchronization by means of a timing signal derived from the modem when the modem is working in the synchronous mode.

b) Synchronization from the transitions of the test signals received when the modem is operating in the nonsynchronous mode.

4 Measurement of distortion

4.1 The apparatus should measure the degrees of early and late individual distortion when operating in the mode in which its synchronizing is derived from transitions in the received test signals.

4.2 The tolerance of measurement of individual distortion of pseudo-random signals should be ± 3%.

4.3 The apparatus should measure bias distortion of received reversal (1 : 1) signals with ± 2% accuracy.

4.4 The characteristics of the receiving circuit of the apparatus shall be as prescribed in the Recommendations for group band modems.

4.5 The margin of the apparatus should be measured in terms of the "margin of a synchronous receiver" [2], under the following measurement conditions: The signals entering the receiving measuring set should be those defined in § 2 above, with the transitions in one direction only subject to a delay equal to Δ% of the theoretical duration of a significant interval. The modulation rate may be fixed at the nominal value, and a value in the range: nominal value ± 0.002%. The receiving measuring set should not indicate any data error after the synchronizing period as long as Δ% is less than 90%; this applies to both directions of the transitions subject to the delay Δ. Under these conditions the margin of the measuring apparatus shall be said to be over 90%.

5 Measurement of error rate

Both bit error-rate and block error-rate measurements should be possible with the apparatus simultaneously.

For the purpose of block error measurements a block length of 32 768 (i.e. 2^{15}) should be used.

Note – Designers of testing apparatus may find it convenient also to incorporate means for using a block length equal to a full pseudo-random pattern of 1 048 575 bits. This longer block length might be more suitable for testing systems operating at higher data signalling rates than recommended in the group band modem Recommendations.

References

[1] CCITT Definition: *Transmitter distortion*, Vol. X, (Terms and Definitions).

[2] CCITT Definitions: *Margin of a synchronous receiver*, Vol. X, (Terms and Definitions).

SECTION 6

INTERWORKING WITH OTHER NETWORKS

Recommendation V.100

INTERCONNECTION BETWEEN PUBLIC DATA NETWORKS (PDNs) AND THE PUBLIC SWITCHED TELEPHONE NETWORK (PSTN)

(Malaga-Torremolinos, 1984)

The CCITT,

considering that

(a) a data station may have an ingoing or outgoing access to a packet switched public data network (PSPDN) via the national[1] PSTN;

(b) the transmission characteristics of the data station may not be known at the PSPDN access level;

(c) in this case, the transmission characteristics have to be negotiated between modems before establishing the connection;

(d) half-duplex modems as well as full duplex modems may be used;

proposes

that Administrations may optionally introduce the following handshaking procedures including the types of modems to be supported.

[1] International access to a PSPDN via PSTN is not envisaged.

1 Procedure description

According to the type of modem (see Table 1/V.100), a half-duplex or a duplex procedure is used.

TABLE 1/V.100

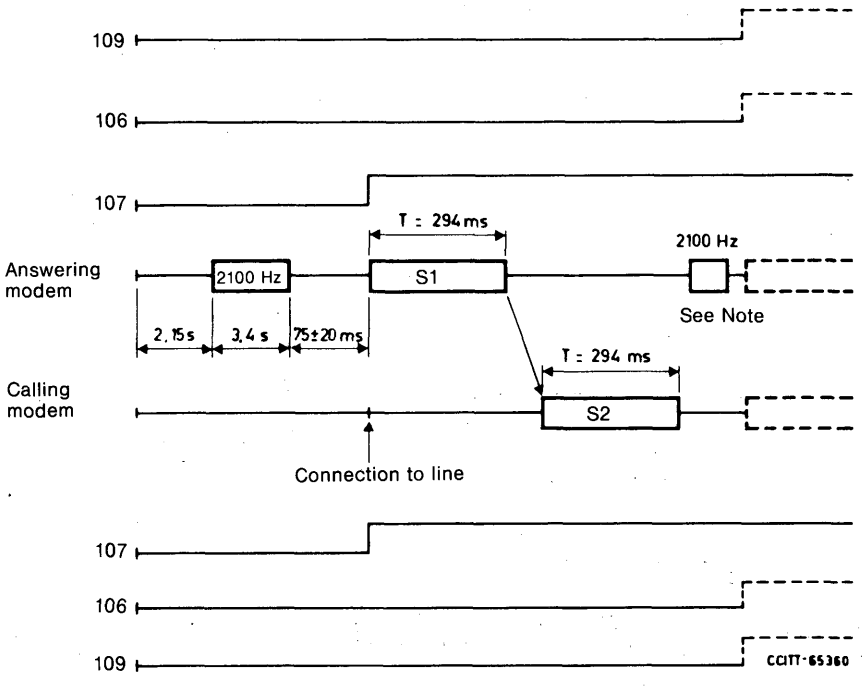
S2 and S1 signals

Categories	Data rate (bit/s)	Recommendation	Procedure	S2 (Calling DCE)	S1 (Answering DCE)
Duplex asynchronous	300 1200	V.21 V.22	Duplex Duplex	980 Hz 1200 Hz	1650 Hz 1800 + 2250 Hz
Duplex synchronous (FDM)	1200 2400	V.22 V.22 *bis*	Duplex Duplex	1200 Hz 1200 Hz	1800 + 2250 Hz 1800 + 2250 Hz
Duplex synchronous (ECT) [a]	2400 4800 9600	V.26 *ter* V.32 V.32	Half-duplex Duplex Duplex	(See V.26 *ter*) (See V.32) (See V.32)	(See V.26 *ter*) (See V.32) (See V.32)
Half-duplex synchronous	2400 4800 9600	V.27 *ter* (fallback mode) V.27 *ter* (Under study)	Half-duplex Half-duplex Half-duplex	None 1400 Hz 1100 Hz	None 2200 Hz 2300 Hz
Asymmetric asynchronous	75/1200	V.23	Duplex	390 Hz	1300 Hz

[a] ECT = echo cancellation technique.

1.1 *Half-dulex procedure*

See Figure 1/V.100.



Note – The 2100 Hz tone is transmitted to disable the echo suppressors in case of duplex transmission (see Recommendation V.26 *ter).* For half-duplex transmission, this tone is not mandatory.

FIGURE 1/V.100

Half-duplex procedure

1.1.1 *Answer mode modem*

a) Following the transmission of the answer sequence in accordance with Recommendation V.25, the modem shall apply an ON condition to circuit 107, and then transmit a segment S1 in accordance with Table 1/V.100 for 294 ms. Interchange circuits 106 and 109 are in the OFF condition during the procedure.

b) The modem remains silent until it detects S2 (defined in Table 1/V.100) or the synchronizing signals of a V.27 *ter* modem in the fallback mode.

c) Then the modem conditions itself to the selected mode or disconnects.

If no response is detected within 2 seconds following the end of the S1 transmission, the modem resumes transmitting S1.

If S2 indicates a capability not available, the modem shall disconnect from the line.

If S2 indicates a capability available, the modem conditions itself to this mode.

d) After the end of reception of S2, in the case of a duplex modem (see V.26 *ter*), in accordance with Recommendation G.164, the modem transmits a 2100 ± 15 Hz tone for 500 ± 50 ms to disable echo suppressors, then remains silent for 75 ± 20 ms.

Note – In the case of half-duplex modems, the transmission of the 2100 Hz tone is not needed.

1.1.2 *Call mode modem*

a) After connection to line, the modem shall apply an ON condition to circuit 107 (interchange circuits 106 and 109 are in the OFF condition during the procedure). The modem keeps silent during at least 400 ms.

During this period, it detects S1.

The calling modem selects a mode of interworking in accordance with S1 or its nominal one.

b) Then, it transmits S2 in accordance with Table 1/V.100 or the synchronizing signals of a V.27 *ter* modem in the fallback mode at 2400 bit/s.

c) Then, it conditions itself to the selected capability.

1.2 *Duplex procedure*

See Figure 2/V.100.

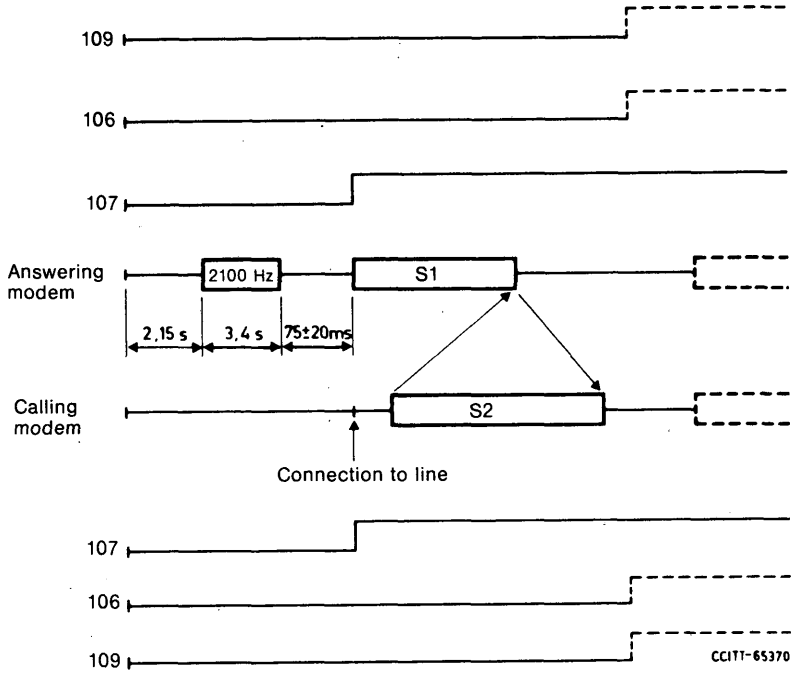


FIGURE 2/V.100
Duplex procedure

1.2.1 *Answer mode modem*

a) Following the transmission of the answer sequence in accordance with Recommendation V.25, the modem shall apply an ON condition to circuit 107 (interchange circuits 106 and 109 are in the OFF condition during the procedure.

b) Then, the modem transmits a segment S1 in accordance with Table 1/V.100 at least 40 ± 10 ms and until it has detected the end of transmission of S2.

Note – During this period, some exchanges may occur between the two modems according to the Series V Recommendation concerned (see Recommendation V.32).

If no response is detected within a time period (under study), the modem shall disconnect from line.

If S2 indicates a capability not available, the modem shall disconnect from the line.

If S2 indicates a capability available, the modem conditions itself to this mode.

1.2.2 *Call mode modem*

a) In accordance with Recommendation V.25, after detection of the 2100 Hz tone and a silent period of 75 ± 20 ms, the modem shall apply an ON condition to circuit 107 (interchange circuits 106 and 109 are in the OFF condition during the procedure).

b) The modem detects S1.

The calling modem selects a mode of interworking in accordance with S1 or its nominal one.

c) Then, it transmits S2 in accordance with Table 1/V.100.

Note – If the modem has only one possibility, it may transmit S2 after being connected to line.

d) Then, it conditions itself to the selected capability.

2 Combined half and duplex procedure

This section describes the interworking between a DCE having the capability of handling the two procedures [referrd to as two procedures (TP)modem] and DCEs having only one procedure.

2.1 *Interworking with half-duplex procedure*

2.1.1 *TP modem in the answering mode*

See Figure 3/V.100.

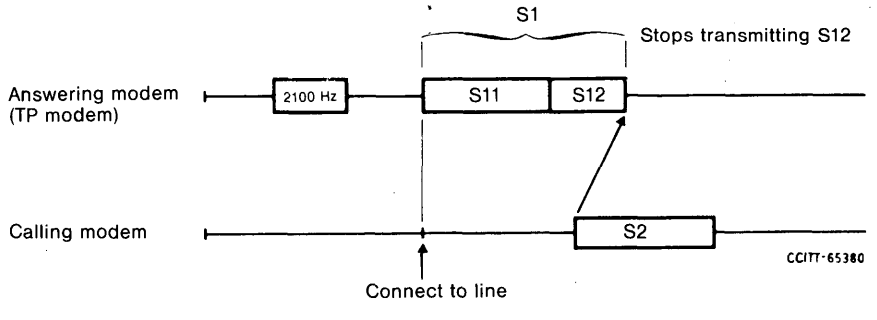


FIGURE 3/V.100
TP modem answer mode

2.1.1.1 *Answer TP modem*

a) After the V.25 sequence, the modem will transmit S1 which is composed of two segments S11 and S12 (as described in Appendix I to Recommendation V.32).

S11 is a modulated signal transmitted during 294 ms in a 600-3000 Hz bandwidth, S12 is a tone out of the 600-3000 Hz band.

b) After the transmission of S12, the modem is waiting for S2. When it detects S2, it stops transmitting S12 and proceeds with the half-duplex procedure.

2.1.1.2 *Calling modem*

The calling modem shall proceed with the half-duplex procedure taking into account that S12 is an out-of-band signal.

2.1.2 *TP modem in the calling mode*

See Figure 4/V.100.

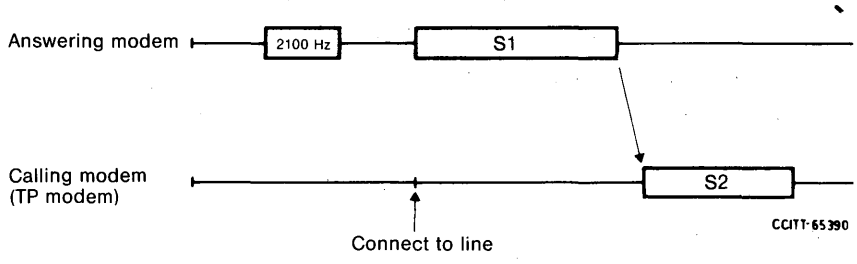


FIGURE 4/V.100

TP modem callmode

2.1.2.1 *Answering modem*

The answering modem shall proceed with the half-duplex procedure.

2.1.2.2 *Calling TP modem*

The calling TP modem after the V.25 sequence and connection to line remains silent. It detects S1 and shall proceed with the half duplex procedure.

2.2 *Interworking with duplex procedure*

2.2.1 *TP modem in the answering mode*

See Figure 5/V.100.

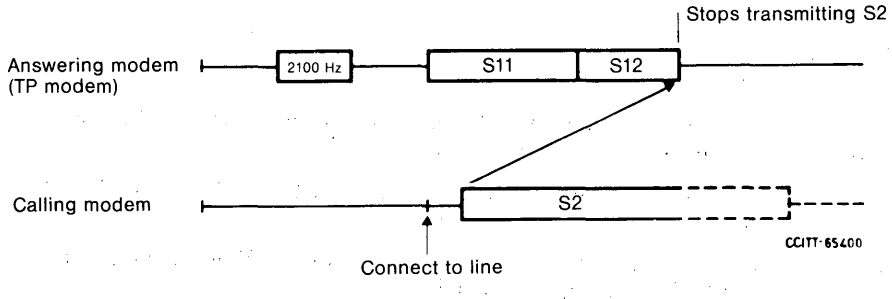


FIGURE 5/V.100

TP modem answer mode

2.2.1.1 *Answering TP modem*

The modem proceeds as in § 2.1.1.1 except that after detection of S2, it shall follow the duplex procedure.

2.2.1.2 *Calling modem*

The calling modem shall proceed with the duplex procedure.

2.2.2 *TP modem in the calling mode*

See Figure 6/V.100.

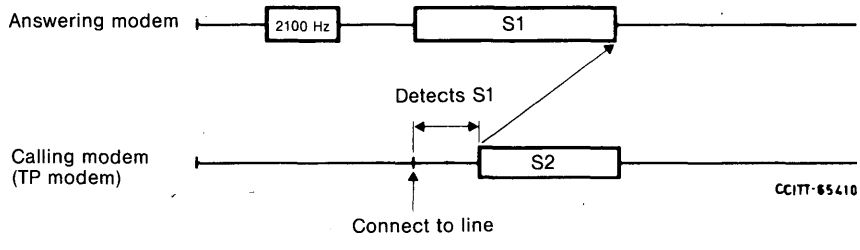


FIGURE 6/V.100

TP modem call mode

2.2.2.1 *Answering modem*

The answering modem shall proceed with the duplex procedure.

2.2.2.2 *Calling TP modem*

The calling TP modem after the V.25 sequence and connection to line remains silent. It detects S1 and shall proceed with the duplex procedure.

Recommendation V.110 [1]

SUPPORT OF DATA TERMINAL EQUIPMENTS (DTEs) WITH V-SERIES TYPE INTERFACES BY AN INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

(Malaga-Torremolinos, 1984)

The CCITT,

considering

(a) that the ISDN will offer the universal interfaces to connect subscriber terminals according to the reference configuration described in Recommendation I.411,

(b) that during the evolution of ISDN however there will exist for a considerable period DTEs with V-series type interfaces which have to be connected to the ISDN,

(c) that the D-channel signalling protocol is described in Recommendations I.430, I.441/Q.921 and I.451/Q.931,

unanimously declares the view

(1) that the scope of this Recommendation shall cover the connection of terminals with interfaces for modems conforming to current Series V Recommendations on the ISDN operating in accordance with circuit switched or leased circuit services;

(2) that the following circuit switched services shall be supported:

- alternate voice/data, (and/or)
- automatic calling and/or automatic answering;

(3) that the reference configurations of § 1 shall apply;

(4) that the terminal adaptor (TA) functions necessary to support the connection of DTEs with V-series type interfaces on an ISDN, shall include the following:

- conversion of electrical and mechanical interface characteristics;
- bit rate adaptation;
- end-to-end synchronization of entry to and exit from the data transfer phase;
- call establishment and disestablishment based on either manual or automatic calling and/or automatic answering.

1 Reference configurations

Figures 1/V.110 and 2/V.110 show examples of some of the many possible functional groupings. These figures are included simply as an aid to describing the TA in later sections.

1.1 *Customer access configuration*

Figure 1/V.110 shows several possible functional groupings that could be used for the connection of DTEs with V-series type interfaces to an ISDN.

Note – The connection of modems to the analogue side of the A/D converter in the TE1 functional grouping (e.g. a digital telephone) is not addressed in this Recommendation. While this type of connection may be useful to users during the transition period to an ISDN, and is allowed, it is not the subject of this Recommendation nor does it appear to be an appropriate subject for standardization.

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[1] This Recommendation is also included in the Recommendations of the I series under the number I.463.

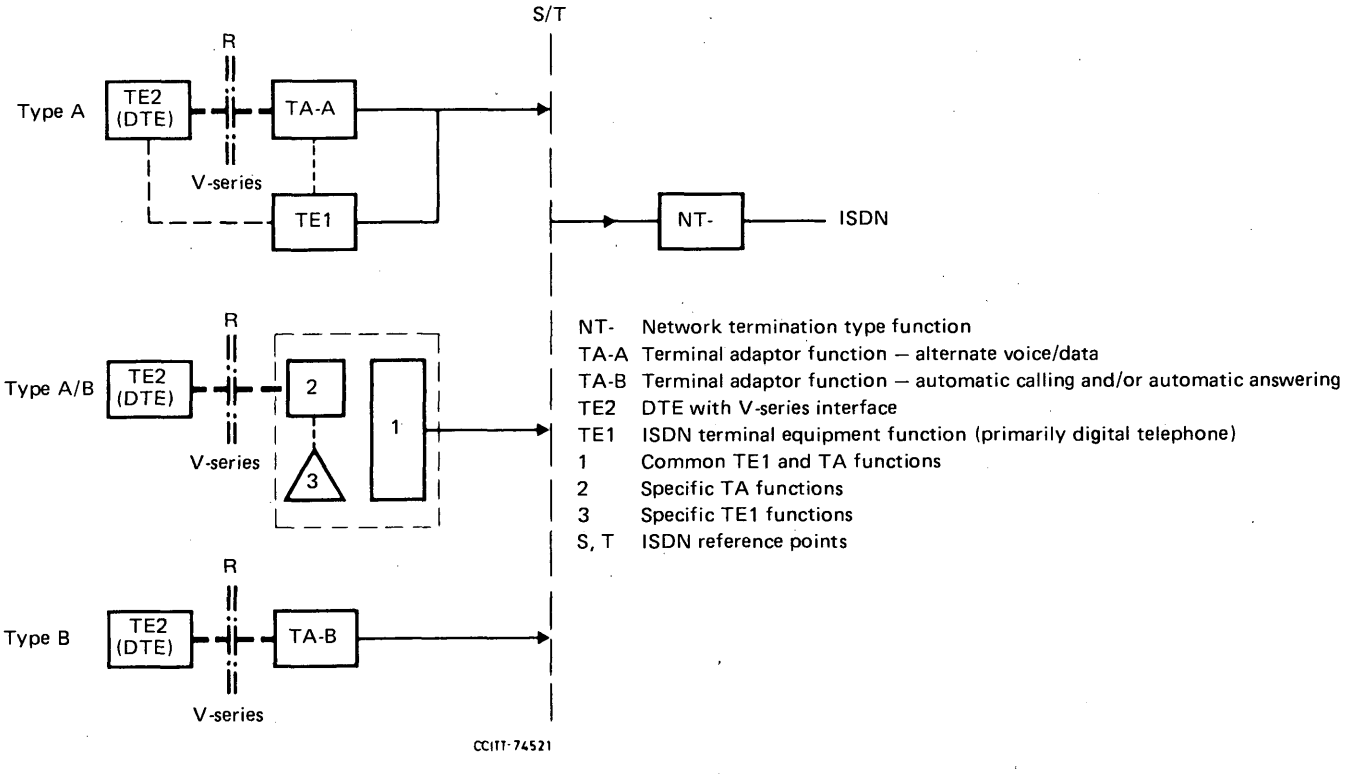


FIGURE 1/V.110

Customer access – reference connections

1.1.1 The TA-A provides manual call control functions associated with alternate voice/data, circuit switched service. The following functions are included:

a) conversion of electrical, mechanical, functional and procedural characteristics of the V-series type interface(s) to those required by an ISDN at reference points S and/or T as discussed in § 3.5;

b) bit rate adaptation of V-series data signalling rates to the 64 kbit/s B channel rate as described in §§ 2.1 and 2.2;

c) end-to-end synchronization of entry to and exit from the data transfer phase as described in § 4.

1.1.2 The TA-B provides, in addition to those functions provided by a TA-A, the mapping functions necessary to convert automatic calling and/or automatic answering procedures of Recommendations V.25 and V.25 *bis* to an ISDN's D channel signalling protocols. The provision of TA-B functions is for further study.

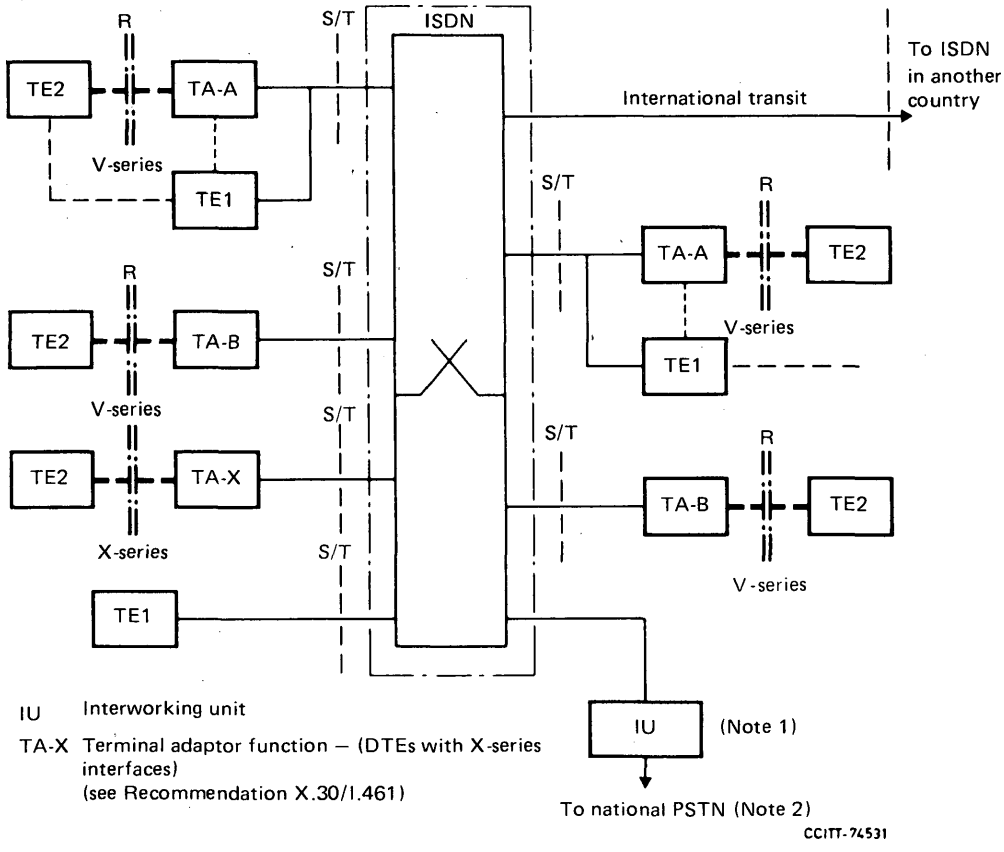
1.2 *Types of end-to-end connections*

The terminal adaptor functions described in this Recommendation take into account the end-to-end connection types shown in Figure 2/V.110. The figure shows the interoperation cases considered in this Recommendation, as follows:

V. ___ TE-2 – – – V. ___ TE-2
V. ___ TE-2 – – – X.21 TE-2
V. ___ TE-2 – – – TE-1

Interworking with TEs on other ISDNs is considered for the same cases.

1.2.1 Interworking with PSTNs may be provided on the basis of a trunk interconnection using interworking units (IUs) (Note 1 of Figure 2/V.110). The reference connections illustrated in Figure 2/V.110 do not envision a direct connection between an ISDN in one country and a public switched telephone network (PSTN) in another country via a network provided Interworking Unit in the first country. However access to non-ISDN countries could be through the normal PSTN international connections.



Note 1 – The functions of this interworking unit are for further study.

Note 2 – For access to national non-ISDN terminals or international access to PSTNs of non-ISDN countries (see § 1.2.1).

FIGURE 2/V.110

Network reference connections

2 Line signals at S and T reference points

The TA signals at ISDN reference points S or T shall be in conformance with the characteristics of an ISDN's, "Basic user/network interface" as described in Recommendation I.430 (Layer 1 specification), I.441/Q.921 (Layer 2 specification) and I.451/Q.931 (Layer 3 specification).

2.1 *Bit rate adaptation of data signalling rates up to 19.2 kbit/s*

2.1.1 *General approach*

The bit rate adaptation functions within the TA are shown in Figure 3/V.110. The function RA1 converts the user data signalling rate to an appropriate intermediate rate expressed by $2^K \times 8$ kbit/s (where $K = 0$, 1 or 2). RA2 performs the second conversion from the intermediate rates to 64 kbit/s. The data signalling rates of 48 and 56 kbit/s are converted directly into the 64 kbit/s B channel rate.

2.1.2 *Adaptation of V-series data signalling rates to the intermediate rates*

The intermediate rate used with each of the V-series data signalling rates are shown in Table 1/V.110.

Note – The specific V-series data signalling rate(s) to be supported by an ISDN are for further study.

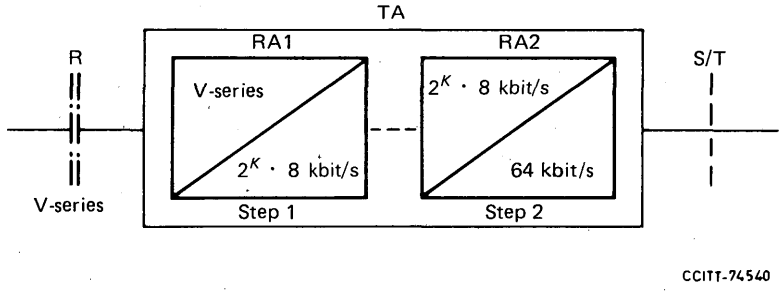


FIGURE 3/V.110

Two step bit rate adaptation

TABLE 1/V.110

First step rate adaptation

Data signalling rate (bit/s)	Intermediate rate		
	8 kbit/s	16 kbit/s	32 kbit/s
600	X		
1 200	X		
2 400	X		
4 800	X		
7 200		X	
9 600		X	
12 000			X
14 400			X
19 200			X

2.1.2.1 *Frame structure*

The frame structure is shown in Table 2/V.110 and is described in the following paragraphs.

As shown in Table 2/V.110, the conversion of the V-series rates to the intermediate rates uses one 80 bit frame. The octet zero contains all binary 0, whilst octet 5 consists of a binary 1 followed by seven E bits (see § 2.1.2.4). Octets 1-4 and 6-9 contain a binary 1 in bit number one, a status bit (S or X bit) in bit number 8 and six *data* bits (D bits) in bit positions 2-7. The order of bit transmission is from left to right and top to bottom.

2.1.2.2 *Frame synchronization*

The 17 bit frame alignment pattern consists of all 8 bits (set to binary 0) of octet zero and bit one (set to binary 1) of the following nine octets (see also § 2.1.3).

2.1.2.3 *Status bits (S1, S3, S4, S6, S8, S9 and X)*

The bits S and X are used to convey channel control information associated with the data bits. The mechanism for proper assignment of the control information from the transmitting signal rate adapter interface via these bits to the receiving signal rate adapter interface is shown in Table 3/V.110 and described in § 4.

TABLE 2/V.110

Frame structure

Octet number	Bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1	D2	D3	D4	D5	D6	S1
2	1	D7	D8	D9	D10	D11	D12	X
3	1	D13	D14	D15	D16	D17	D18	S3
4	1	D19	D20	D21	D22	D23	D24	S4
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D25	D26	D27	D28	D29	D30	S6
7	1	D31	D32	D33	D34	D35	D36	X
8	1	D37	D38	D39	D40	D41	D42	S8
9	1	D43	D44	D45	D46	D47	D48	S9

TABLE 3/V.110

General mapping scheme

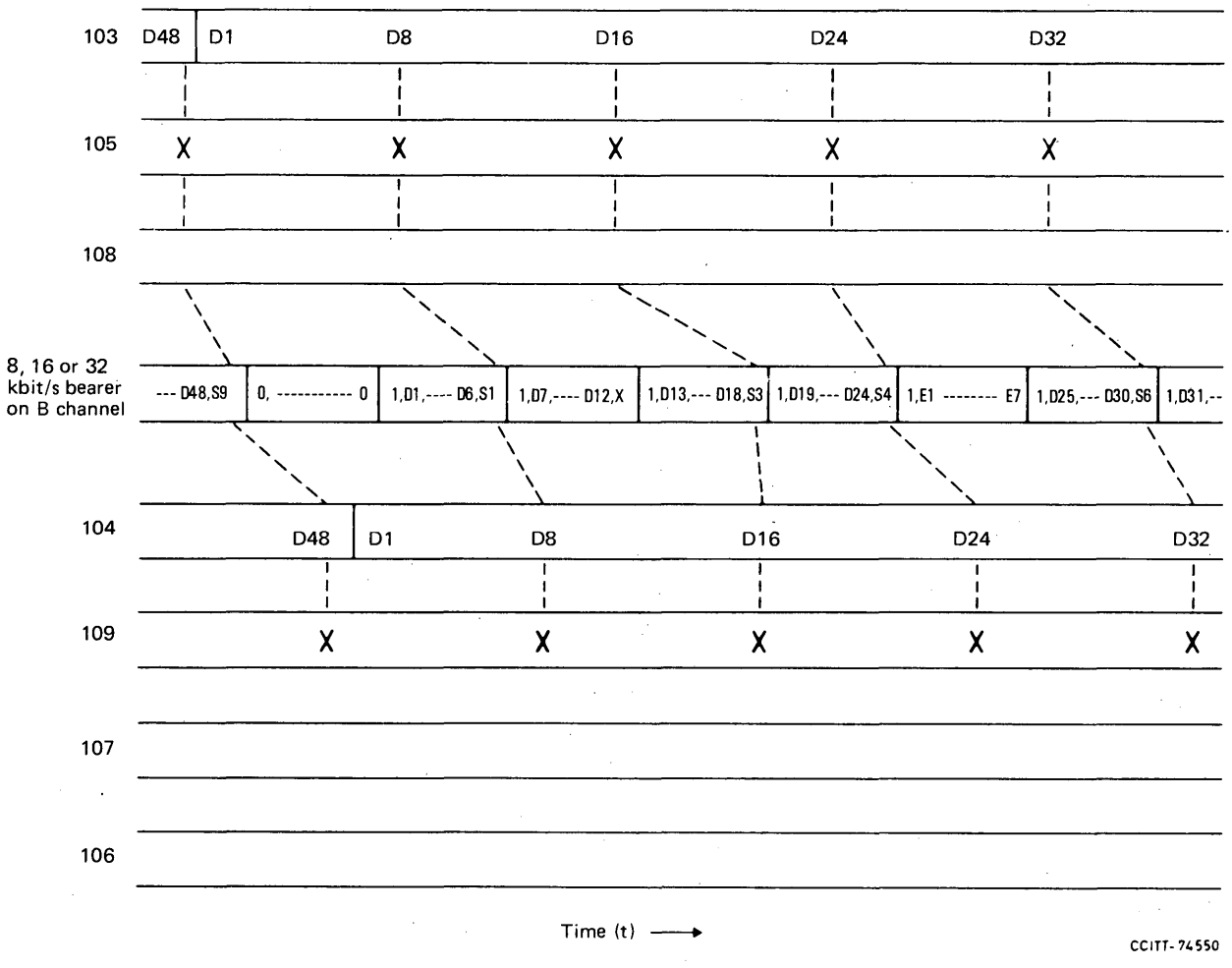
108 ----------	S1, S3, S6, S8 = SA	---------- 107
105 ----------	S4, S9 = SB	---------- 109
Frame synch and 106/IU ----------	X	---------- 106

Control information, conveyed by the S bits, and user data, conveyed by the D bits, should not have different transmission delays. The S bits should therefore transmit control information sampled simultaneously with the D bits in the positions specified in Table 4/V.110 and as presented in Figure 4/V.110.

TABLE 4/V.110

Coordination between S bits and D bits

S bit	D bit	
	Octet No.	Bit No.
S1	2	3 (D8)
S3	3	5 (D16)
S4	4	7 (D24)
S6	7	3 (D32)
S8	8	5 (D40)
S9	9	7 (D48)



Note 1 – In order to maintain conformity with the bit rate adaptation of X.1 user classes of service described in Recommendation X.30 (I.461), the bits S1 and S6, S3 and S8, S4 and S9 are used to convey channel status information associated with the P, Q and R bit groups respectively.

Refer to § 2.1.1.2.3 of Recommendation X.30 (I.461) for detailed information concerning the mapping of the information on circuit C of the X.21 interface to the S bits and to the I bits of the distant interface.

Note 2 — The coordination between S and D bits described in Table 4/V.110 and Figure 4/V.110 is intended to provide for compatibility with Recommendation X.30 (I.461). Whether this coordination is strictly necessary in the context of Recommendation V.110 is for further study.

FIGURE 4/V.110

Coordination between S bits and D bits

2.1.2.4 *User rate identification*

The E bits in conjunction with the intermediate rate (see Table 2/V.110 in § 2.1.2.1) provide the user data signalling rate identification. The coding of these bits shall be as shown in Table 5/V.110.

TABLE 5/V.110

User rate identification
(Note 1)

Intermediate rates			E1	E2	E3	E4	E5	E6	E7
8	16	32	(Note 3)						
600			1	0	0	X [a]	X	X	1 or 0 (Note 2)
1200			0	1	0	X	X	X	X
2400			1	1	0	X	X	X	X
		12 000	0	0	1	X	X	X	X
	7200	14 400	1	0	1	X	X	X	X
4800	9600	19 200	0	1	1	X	X	X	X

[a] "X" indicates spare bits which are reserved for future use and should be set to binary "1".

Note 1 – The data signalling rates of 600, 2400, 4800 and 9600 bit/s are also Recommendation X.1 user classes of service (see also Recommendation X.30/I.461).

Note 2 – In order to maintain compatibility with Recommendation X.30 (I.461), the 600 bit/s user rate E7 is coded to enable the 4 × 80 bit multiframe synchronization. To this end, E7 in the fourth 80 bit frame is set to binary 0 (see § 2.1.2.6 and Table 6a/V.110).

Note 3 – A possible future use for bit E4 is to identify whether the user data is in the synchronous or asynchronous mode (for example: E4 = binary 1 might indicate the synchronous mode whilst E4 = binary 0 might indicate the asynchronous mode). The provision of asynchronous mode operation and the assignment of bit E4 is for further study.

2.1.2.5 *Data bits*

Data are conveyed in D bits, i.e. up to 48 bits per 80 bit frame. In this Recommendation the octet boundaries of the user's data stream are not defined.

2.1.2.6 *Bit assignment*

The adaptation of 600, 1200 and 2400 bit/s rates to the 8 kbit/s intermediate rate are shown in Tables 6a/V.110, 6b/V.110 and 6c/V.110 respectively.

The adaptation of 7200 and 14 400 bit/s rates to the 16 and 32 kbit/s intermediate rate, respectively, use the data bit assignments shown in Table 6d/V.110.

The adaptation of 4800, 9600 and 19 200 bit/s rates to the 8, 16 and 32 kbit/s intermediate rate, respectively, use the data bit assignments shown in Table 6e/V.110.

The adaptation of 1200 bit/s user rate to 32 kbit/s intermediate rate is for further study.

2.1.3 *Frame synchronization and additional signalling capacity*

2.1.3.1 *Search for frame synchronization*

The following 17 bit alignment pattern is used to achieve frame synchronization:

0 0 0 0 0 0 0 0 1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX
1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX

It is assumed that the error rate will be sufficiently low to expect frame synchronization following the detection of one 80 bit frame.

TABLE 6a/V.110

Adaptation of 600 bit/s user rate to 8 kbit/s intermediate rate

0	0	0	0	0	0	0	0
1	D1	D1	D1	D1	D1	D1	S1
1	D1	D1	D2	D2	D2	D2	X
1	D2	D2	D2	D2	D3	D3	S3
1	D3	D3	D3	D3	D3	D3	S4
1	1	0	0	E4	E5	E6	E7 [a]
1	D4	D4	D4	D4	D4	D4	S6
1	D4	D4	D5	D5	D5	D5	X
1	D5	D5	D5	D5	D6	D6	S8
1	D6	D6	D6	D6	D6	D6	S9

[a] See Note 2 to Table 5/V.110.

TABLE 6b/V.110

Adaptation of 1200 bit/s user rate to 8 kbit/s intermediate rate

0	0	0	0	0	0	0	0
1	D1	D1	D1	D1	D2	D2	S1
1	D2	D2	D3	D3	D3	D3	X
1	D4	D4	D4	D4	D5	D5	S3
1	D5	D5	D6	D6	D6	D6	S4
1	0	1	0	E4	E5	E6	E7
1	D7	D7	D7	D7	D8	D8	S6
1	D8	D8	D9	D9	D9	D9	X
1	D10	D10	D10	D10	D11	D11	S8
1	D11	D11	D12	D12	D12	D12	S9

TABLE 6c/V.110

Adaptation of 2400 bit/s user rate to 8 kbit/s intermediate rate

0	0	0	0	0	0	0	0
1	D1	D1	D2	D2	D3	D3	S1
1	D4	D4	D5	D5	D6	D6	X
1	D7	D7	D8	D8	D9	D9	S3
1	D10	D10	D11	D11	D12	D12	S4
1	1	1	0	E4	E5	E6	E7
1	D13	D13	D14	D14	D15	D15	S6
1	D16	D16	D17	D17	D18	D18	X
1	D19	D19	D20	D20	D21	D21	S8
1	D22	D22	D23	D23	D24	D24	S9

TABLE 6d/V.110

Adaptation of N [a] × 3600 bit/s user rate to the intermediate rate

0	0	0	0	0	0	0	0
1	D1	D2	D3	D4	D5	D6	S1
1	D7	D8	D9	D10	F	F	X
1	D11	D12	F	F	D13	D14	S3
1	F	F	D15	D16	D17	D18	S4
1	1	0	1	E4	E5	E6	E7
1	D19	D20	D21	D22	D23	D24	S6
1	D25	D26	D27	D28	F	F	X
1	D29	D30	F	F	D31	D32	S8
1	F	F	D33	D34	D35	D36	S9

F = filling bit

[a] N = 2 or 4 only.

TABLE 6e/V.110

Adaptation of N [a] × 4800 bit/s user rate ti the intermediate rate

0	0	0	0	0	0	0	0
1	D1	D2	D3	D4	D5	D6	S1
1	D7	D8	D9	D10	D11	D12	X
1	D13	D14	D15	D16	D17	D18	S3
1	D19	D20	D21	D22	D23	D24	S4
1	0	1	1	E4	E5	E6	E7
1	D25	D26	D27	D28	D29	D30	S6
1	D31	D32	D33	D34	D35	D36	X
1	D37	D38	D39	D40	D41	D42	S8
1	D43	D44	D45	D46	D47	D48	S9

[a] N = 1, 2 or 4 only.

2.1.3.2 *Frame synchronization monitoring and recovery*

The monitoring of the frame synchronization shall be a continuous process using the same procedures as for initial detection.

Loss of frame synchronization shall not be assumed unless at least three consecutive frames, each with at least one framing bit error, are detected.

Following loss of frame synchronization the TA shall enter a recovery state as discussed in § 4.1.5. If recovery is not successful further maintenance procedures must be used.

Definition of what constitutes an unrecoverable loss of frame synchronization requires further study. Procedures following an unrecoverable loss of frame synchronization requires further study.

2.1.3.3 *Additional signalling capacity (E bits)*

The E bits, in addition to providing the user data signalling rate identification as specified in § 2.1.2.4, provide for additional signalling capacity. The use of this capacity is for future study. The unused E bits should be set to binary 1.

Note – Refer to Note 3 of Table 5/V.110.

2.1.4 *Adaptation of intermediate rates to 64 kbit/s*

Since rate adaptation of a single intermediate rate (e.g. 8, 16, or 32 kbit/s) to the 64 kbit/s B channel rate and the possible multiplexing of several intermediate rate streams[2)] to the 64 kbit/s B channel rate must be compatible to enable interworking, a common approach is needed for the second step rate adaptation and, possibly, for intermediate rate multiplexing. This second step rate adaptation method is described in Recommendation I.460.

2.2 *Rate adaptation of 48 and 56 kbit/s user rates to 64 kbit/s*

The 48 and 56 kbit/s user data signalling rates are adapted to the 64 kbit/s B channel rate in one step as indicated in Tables 7a/V.110 and 7b/V.110 respectively.

TABLE 7a/V.110

Adaptation of 48 kbit/s user rate to 64 kbit/s

Octet number	Bit number							
	1	2	3	4	5	6	7	8
1	1	D1	D2	D3	D4	D5	D6	S1
2	0	D7	D8	D9	D10	D11	D12	X
3	1	D13	D14	D15	D16	D17	D18	S3
4	1	D19	D20	D21	D22	D23	D24	S4

Note 1 – 48 kbit/s is also a Recommendation X.1 user class of service (see also Recommendation X.30/I.461, § 2.2.1).

Note 2 – Refer to § 2.1.2.3 for the use of status bits and bit X; however for international interworking, bit X must be set to binary 1. This bit may be used for other purposes in a national network.

2) Multiplexing of several intermediate rate streams is for further study.

TABLE 7b/V.110

Adaptation of 56 kbit/s user rate to 64 kbit/s

Octet number	Bit number							
	1	2	3	4	5	6	7	8
1	D1	D2	D3	D4	D5	D6	D7	1
2	D8	D9	D10	D11	D12	D13	D14	1
3	D15	D16	D17	D18	D19	D20	D21	1
4	D22	D23	D24	D25	D26	D27	D28	1
5	D29	D30	D31	D32	D33	D34	D35	1
6	D36	D37	D38	D39	D40	D41	D42	1
7	D43	D44	D45	D46	D47	D48	D49	1
8	D50	D51	D52	D53	D54	D55	D56	1

Note – The bits numbered 8 are provisionally set to 1. Further study is required to determine whether or not certain of these bits may be used to indicate end-to-end frame synchronization of entry to and exit from the data transfer for the 56 kbit/s user rate.

3 Interchange circuits

3.1 *Essential and optional interchange circuits*

The essential and optional interchange circuits are listed in Table 8/V.110 below.

3.2 *Timing arrangements*

The TA shall derive ISDN timing from the received bit stream of the ISDN's basic user/network interface (see §§ 5 and 8 of Recommendation I.430). This network timing shall be used by the TA to provide the DTE with transmitter signal element timing on circuit 114 and receiver signal element timing on circuit 115.

3.3 *Circuit 106*

After the start-up and retrain synchronization sequences, the ON state of circuit 106 shall be delayed relative to the ON state of circuit 105 (where implemented) by an interval of at least N bits (a value of N equal to 24 has been proposed, but the value is for further study). ON to OFF state transitions of circuit 106 shall follow ON to OFF state transitions of circuit 105 (when implemented) by less than 2 ms. Where circuit 105 is not implemented, the initial circuit 106 transition to the ON state shall be delayed by an interval greater than or equal to N bits relative to the corresponding transition in the state of circuit 109. Subsequent transitions in the state of circuit 105 should occur solely in accordance with the operating sequences defined in § 4.

3.4 *Circuit 109*

OFF to ON and ON to OFF transitions of circuit 109 should occur solely in accordance with the operating sequence defined in § 4.

TABLE 8/V.110

Interchange circuit		Notes
No.	Description	
102	Signal ground or common return	
102a	DTE common return	2
102b	DCE common return	2
103	Transmitted data	
104	Received data	
105	Request to send	3
106	Ready for sending	
107	Data set ready	
108/1	Connect data set to line	4
108/2	Data terminal ready	4
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	5
112	Data signalling rate selector (DCE source)	5
113	Transmitter signal element timing (DTE source)	6
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
125	Calling indicator	7
140	Loopback/maintenance test	8
141	Local loopback	8
142	Test indicator	8

Note 1 – All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 3.5).

Note 2 – Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 are used at data signalling rates above 20 kbit/s.

Note 3 – Not required for DTEs that operate with DCEs in the continuous carrier mode.

Note 4 – This circuit shall be capable of operations as circuit 108/1 or 108/2 depending on its use.

Note 5 – The use of this circuit is for further study.

Note 6 – The use of circuit 113 is for further study, since its application is restricted by the synchronous nature of ISDN.

Note 7 – This circuit is used with the automatic answering terminal adaptor function.

Note 8 – The use for loopback testing is for further study.

3.5 *Electrical/mechanical characteristics of interchange circuits*

3.5.1 *Basic ISDN user/network interface*

The electrical and mechanical characteristics of the basic ISDN user/network interface are described in §§ 8 and 10 of Recommendation I.430.

3.5.2 *DTE/DCE interface*

3.5.2.1 *Rates less than or equal to 19.2 kbit/s*

Use of electrical characteristics conforming to Recommendation V.28, is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note – Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all-balanced, interface for the V-series application which minimizes the number of interchange circuits.

3.5.2.2 *Rates greater than 19.2 kbit/s*

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended together with the use of the connector and pin assignment plan specified by ISO 4902.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

ii) In the case of circuits 105, 106, 107 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1, or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies, with receivers configured as specified by Recommendation V.10 for category 2.

Alternatively the interface defined in Appendix II to Recommendation V.35 together with connector and pin assignment plan specified by ISO 2593 may be used.

3.6 *Fault condition on interchange circuits*

(See § 7 of Recommendation V.28 for association of the receiver failure detection types).

3.6.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

3.6.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

3.6.3 All other circuits not referred to above may use failure detection types 0 or 1.

4 Operating sequence

4.1 *TA-A duplex operation*

When using the TA-A to provide alternate voice/data service within an ISDN, the call is established in the (end-to-end) digital mode using the procedures applicable to the particular network and/or terminal configuration. Voice coordination is used to determine compatibility issues such as: data signalling rate, duplex vs. half-duplex, etc.

The internal arrangement of the ISDN terminal equipment (TE1) functional grouping, the TA and the DTE (with a V-series type interface) is not within the scope of this Recommendation. It is assumed that some internal means is provided for the TE1 to control the transfer from the voice to the data mode and from the data to the voice mode. For example, it is assumed that the means are provided to control circuits 108/1 (Connect data set to line) or 108/2 (Data terminal ready) internally, that is within the station at the customer premises. However, for the purpose of this Recommendation circuit 108/2, as defined in Recommendation V.24, is assumed.

4.1.1 *Idle (or ready) state*

4.1.1.1 During the idle (or ready) state the TA (DCE) will be receiving the following from the DTE:

Circuit 103 = continuous binary 1
Circuit 105 = (See footnote[3])
Circuit 108/1 = OFF; circuit 108/2 = ON

4.1.1.2 During the idle (or ready) state the TA will transmit continuous binary 1s into the B and D channels (i.e., all bits of Table 2/V.110 = binary 1).

4.1.1.3 During the idle (or ready) state the TA (DCE) will transmit the following toward the DTE:

Circuit 104 = continuous binary 1
Circuit 107 = OFF
Circuit 106 = OFF
Circuit 109 = OFF

[3] In many duplex DTEs circuit 105 is either permanently in the ON condition or it is not present. If not present, the function must be set in an ON condition in the TA. See § 4.1.2.3 for the case where a duplex DTE can operate circuit 105.

4.1.2 *Connect TA to line state*

4.1.2.1 When the station arrangement is switched from the voice to the data mode, circuit 108 if not previously ON, is switched from the OFF to the ON condition.

Note – The manual transfer from voice to data at both ends of the connection must occur at approximately the same time.

Switching to the data mode causes the TA to transmit the following toward the ISDN (refer to Table 2/V.110):

a) frame synchronization pattern, as follows:
   - octet 0 = all binary 0s
   - bit number one of octets 1-9 = binary 1

b) data bits = binary 1

c) status bits S = OFF and X = OFF.

Note 1 – At this time circuit 103 is not connected to the data channel (e.g., the binary 1 condition of the data bits is generated within the TA).

Note 2 – In the following description only the inter-operation between DTE/DCE (TE2/TA) interface and the intermediate rate frames (Tables 6a/V.110 to 6e/V.110) and the 64 kbit/s frame of Table 7a/V.110 are discussed. The second step rate of adaptation and "disadaptation" and the multiplexing and demultiplexing of the ISDN basic user/network interface are discussed in Recommendations I.460 and I.430, respectively.

4.1.2.2 At this time (i.e. switching to data mode) the receiver in the TA will begin to search for the frame synchronization pattern in the received bit stream (see § 2.1.3.1).

4.1.2.3 When the receiver recognizes the frame synchronization pattern, it causes the S and X bits in the transmitted frames to be turned ON (provided that circuit 108 is ON).

4.1.2.4 When the receiver recognizes that the status bits S and X are in the ON condition it will perform the following functions:

a) Turn ON circuit 107 toward the DTE.

   Note – A duplex DTE that implements and is able to operate circuit 105 may be expected to turn this circuit ON at any time. However, if not previously turned ON, it must be turned ON in response to the ON condition on circuit 107.

b) Then, circuit 103 may be connected to the data bits in the frame; however the DTE must maintain a binary 1 condition until circuit 106 is turned ON in the next portion of the sequence.

c) Turn ON circuit 109 and connect the data bits to circuit 104.

   Note – Binary 1 is being received on circuit 104, at this time.

d) After an *N* bit interval (see § 3.3), it will turn ON circuit 106.

e) Circuit 106 transitioning from OFF to ON will cause the transmitted data to transition from binary 1 to the data mode.

4.1.3 *Data transfer state*

4.1.3.1 While in the data transfer state the following circuit conditions exist:

a) circuits 105 (when implemented), 106, 107, 108/1 or 108/2 and 109 are in the ON condition;

b) data is being transmitted on circuit 103 and received on circuit 104.

4.1.4 *Disconnect or return to voice mode*

4.1.4.1 At the completion of the data transfer phase, the local DTE will indicate a *disconnect request* by turning OFF circuit 108. This will cause the following to occur:

a) the status bits S in the frame toward ISDN will turn OFF, status bits X are kept ON;

b) circuit 106 will be turned OFF;

c) the data bits in the frame will transition from data mode to binary 0.

4.1.4.2 If circuit 108 is still ON at the remote TA, this TA will recognize the transition of the status bits from ON to OFF and the data bits from *data* to binary 1 as a disconnect signal and it will turn OFF circuits 107 and 109. This DTE should respond by turning OFF circuit 108 and transferring to the voice mode. If the TE1 is off-hook the connection will be maintained in the voice mode. If the TE1 is on-hook, the TE1 will control the disconnection via the ISDN D channel signalling protocol. At this time, the DTE/DCE interface should be in the *idle* (or *ready*) state.

4.1.4.3 The TA at the station that originated the disconnect request will recognize reception of S = OFF or the loss of framing signals as a *disconnect acknowledgement* and turn OFF circuits 107 and 109 and transfer to the voice mode. If the TE1 is off-hook the connection will be maintained in the voice mode. If the TE1 is on-hook, the TE1 will control the disconnection via the ISDN D channel signalling protocol. At this time, the DTE/DCE interface should be in the *idle* (or *ready*) state.

4.1.5 *Loss of frame synchronization*

4.1.5.1 In the event of loss of frame synchronization by the signals on the B channel, the TA should attempt to resynchronize as follows:

a) Turn OFF circuit 106.

b) Circuit 104 passes from the data mode to binary 1.

c) The DTE should respond to circuit 106 OFF by placing circuit 103 in a binary 1 condition.

d) Turn OFF status bit X and set the data bits to binary 1 in the transmitted frame.

e) The remote TA upon recognition of status bit X OFF and binary 1 on the data bits will turn OFF circuit 106 which will cause the remote DTE to place circuit 103 in a binary 1 condition.

f) The local TA should attempt to resynchronize on the incoming signal.

g) If after an interval of, say, three seconds the local TA cannot attain synchronization, it should send a *disconnect request* by turning OFF all of the status bits for several (say three) frames with data bits set to binary 0 and then disconnect by turning OFF circuit 107 and transferring to the voice mode as discussed in § 4.1.4.2 above.

Note – The values of three seconds and three frames are provisional and should be confirmed or amended after further study.

h) If synchronization is achieved, the TA should turn ON status bit X toward the distant station and, after an *N* bit interval (see § 3.3), turn ON circuit 106 which will cause circuit 103 to change from binary 1 to the data mode.

Note – During a resynchronization attempt circuits 107 and 109 should remain ON.

4.2 *TA-A half-duplex operation*

The alternate voice/data call establishment and voice coordination for the interworking of half-duplex DTEs equipped with V-series type interfaces is the same as discussed in § 4.1 above. The only difference between half-duplex and duplex operation is in the control of the circuits 105, 106 and 109, as follows:

Note – This is a unique application; therefore, TA arranged for half-duplex operation will not be able to interwork with either a V-series or an X-series duplex DTE (TE2).

4.2.1 In a TA arranged to accommodate half-duplex DTEs, circuit 109 will be under the control of the status bits S in the incoming frame, as follows:

a) If at the local interface circuit 109 is OFF and circuit 104 is in the binary 1 state, the DTE may *request to send* by turning ON circuit 105.

b) The TA will then turn ON status bits S in the transmitted frame which will turn ON circuit 109 in the remote interface and connect circuit 104 to the data bit stream of the incoming frame.

c) After an *N* bit interval (see § 3.3) the local TA will turn ON circuit 106, which will allow the local DTE to transmit data on circuit 104.

d) Upon completion of the transmission the local/DTE will turn OFF circuit 105. This will in turn:
   - turn OFF circuit 106 in the local interface and circuit 103 will revert to the binary 1 state,
   - turn OFF status bits S which will in turn at the remote TA turn OFF circuit 109 and place circuit 104 in a binary 1 condition.

e) At this time the remote DTE is able to reverse the sequence by turning ON circuit 105.

4.3 *TA-B*

The mapping of V.25 and/or V.25 *bis* automatic calling and/or automatic answering procedures to the ISDN D channel signalling protocols is for further study.

5 Testing facilities

The provision of maintenance test loops is for further study.

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